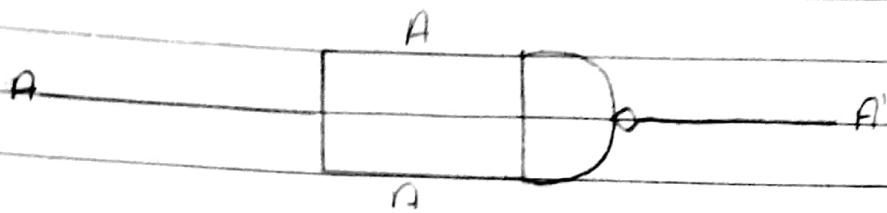


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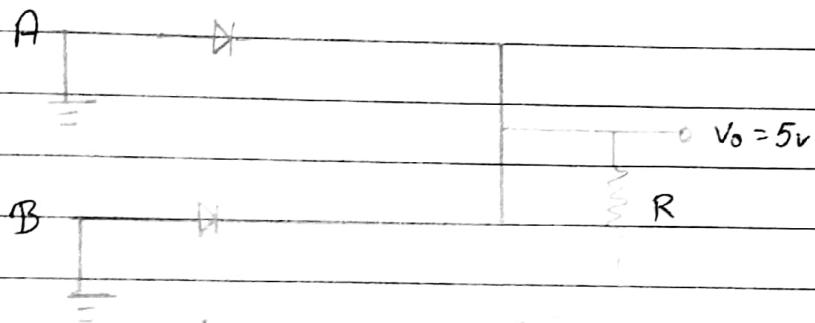
PhysicsDigital logic families :

- * NAND Gate as NOT Gate →



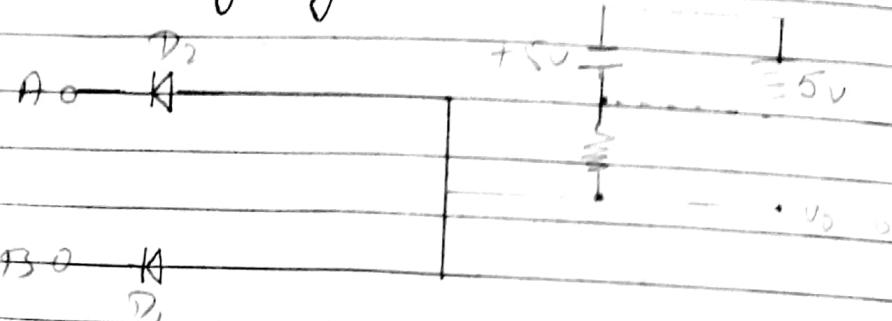
INPUT	OUTPUT	
A	B	y
0	0	1
1	1	0

- * OR Gate using by diode →



$$\begin{array}{lll}
 A=0, B=1 & Y=1 \\
 A=1, B=0 & Y=1 \\
 A=0, B=0 & Y=0 \\
 A=1, B=1 & Y=1
 \end{array}$$

* AND Gate using diode \rightarrow



$$A = 0$$

$$B = 0$$

$$Y = 0$$

$$A = 1$$

$$B = 0$$

$$Y = 0$$

$$A = 0$$

$$B = 1$$

$$Y = 0$$

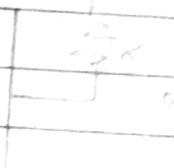
$$A = 1$$

$$B = 1$$

$$Y = 1$$

* NAND Gate by using diode \rightarrow

forwarded
Resistance $\leftarrow D$



$$A = 0$$

$$B = 0$$

$$Y = 0$$

$$\bar{Y} = 1$$

$$A = 1$$

$$B = 0$$

$$Y = 0$$

$$\bar{Y} = 1$$

$$A = 0$$

$$B = 1$$

$$Y = 0$$

$$\bar{Y} = 1$$

$$A = 1$$

$$B = 1$$

$$Y = 1$$

$$\bar{Y} = 0$$

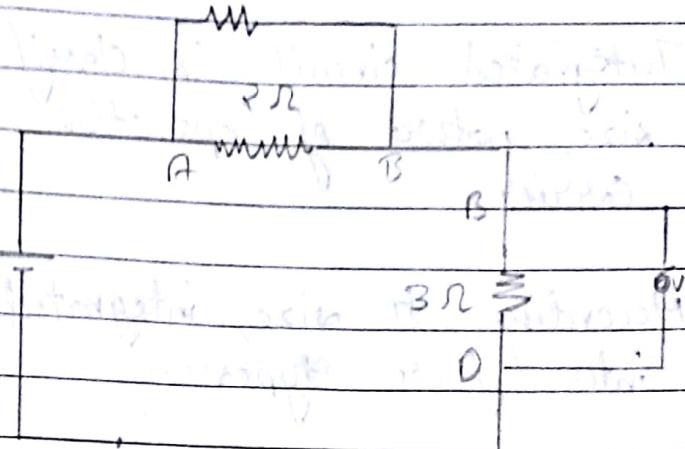
Constant \rightarrow Transistor (NPN)

Battery

Resistance

Diode

* Reference \rightarrow



$$V_A = 10V \quad V_C = 6V$$

$$10V - 2\Omega - 3\Omega$$

$$V_B = 6V \quad V_D = 0V$$

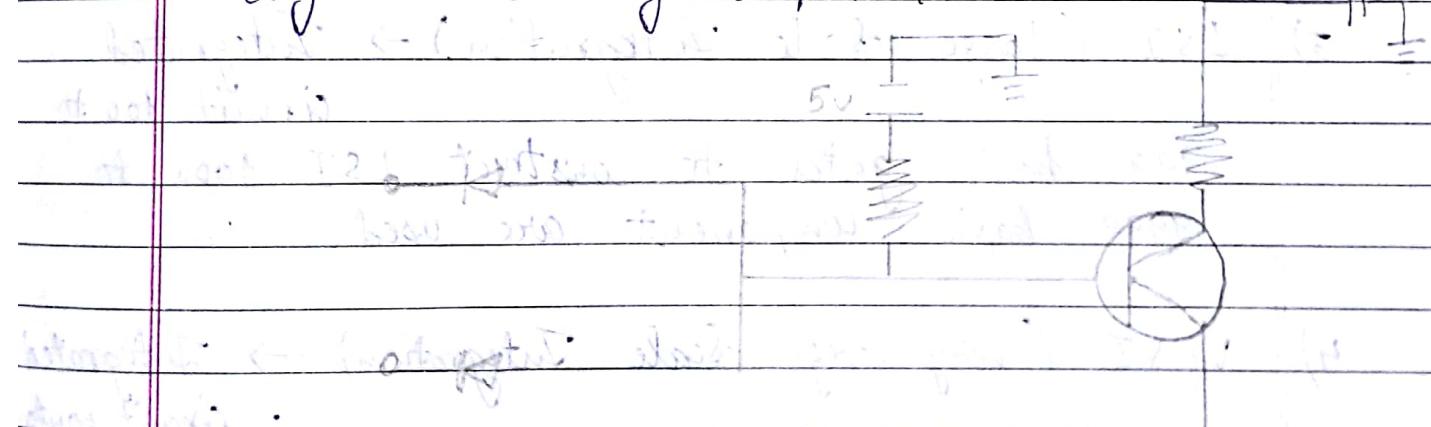
$$10V - 5\Omega$$

$$V_E = 0V$$

$$I = 10/5 = 2A$$

Integrated Circuit \rightarrow Electronics circuit made by resistors, diodes and transistor which is used to realise logic expression is called integrated circuit.

* It may contain multiple complicated circuit with large number of components.



This circuit is used to realise A.B (NAND) gate expression. It contains 2 diodes, 2 resistors, 1 NPN transistor.

* Integrated circuit is classified according to its size, mode of operation and nature of charge carrier.

* According to size, integrated circuit is classified into four types

1) SSI (Small Scale Integration) → This IC may contain less than twelve basic gates. If the number of component (resistor, diodes, transistor) is less than 100 it is small scale integration.

2) MSI (Medium Scale Integration) → Integrated circuit contain twelve or less than equal to 99 (12 to 99) basic gates to construct MSI 100 to 999 basic component are used.

3) LSI (Large Scale Integration) → Integrated circuit 100 to 999 basic gates to construct LSI 1000 to 9999 basic component are used.

4) VLSI (Very Large Scale Integration) → Integrated circuit contain more than equal to 1000 basic gates to construct VLSI 10000 and more than basic component are used.

IC's

SSI	M S I	L S I	V L S I
No. of basic gates ≤ 12	No. of basic gates ≤ 99	No. of basic gates $\geq 100 < 999$	No. of basic gates ≤ 1000
No. of component < 100	No. of component < 999	No. of component ≤ 9999	No. of component ≤ 10000

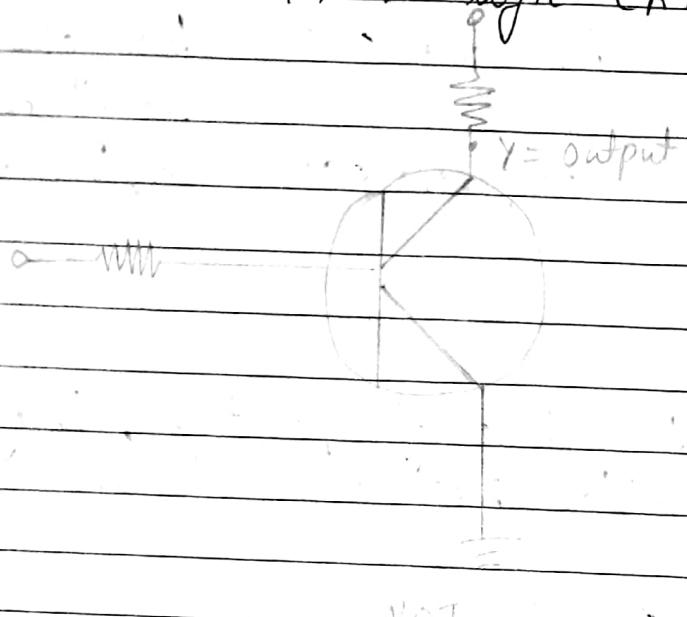
* According to nature of operation, integrated circuit is classified into two - types.

- 1) Saturated Operation IC
- 2) Non-Saturated Operation IC

Physics

i) Saturated Operation IC \rightarrow In saturated logic family following circuits are used :-

ii) Resistor transistor logic (RTL)

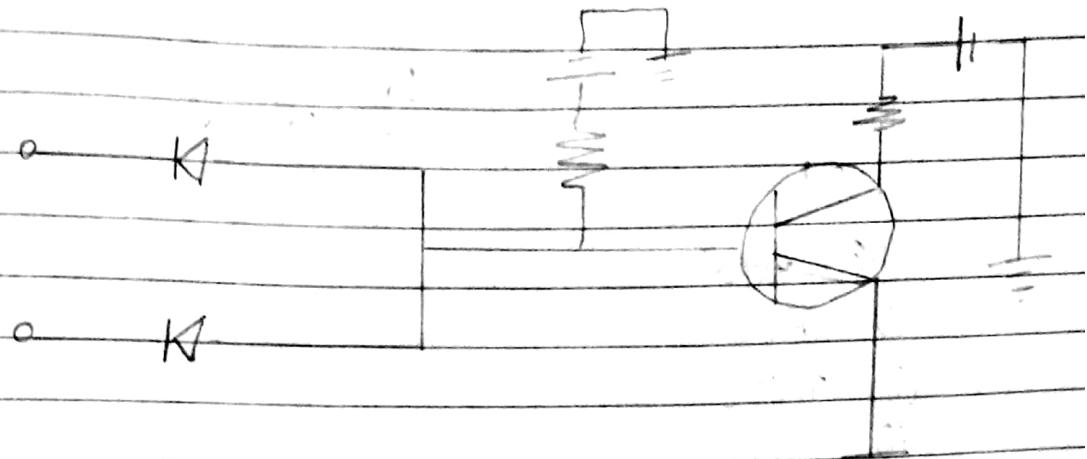


NOT

iii) Direct Coupled transistor logic (DCTL) \rightarrow In these circuit transistor is coupled with resistor.

iv) Integrated Injection logic (I₂L) \rightarrow It is made of transistor and diode.

v) Diode - transistor logic (DTL) \rightarrow It is design by using of diode and transistor.



(v) High Threshold logic (HTL) → These logic family operated at threshold voltage.

(vi) Transistor Transistor logic (TTL) → All above logic family are operated on the saturation mode of diode & transistor.

Non saturated bipolar hole & electron.

2) Non-Saturated Operation IC → bipolar family

There are two types of non-saturated IC

- (i) Schottky TTL
- (ii) Emitter coupled logic (ECL)

Logic family

Unsaturated

- (i) RTL
- (ii) DCTL
- (iii) IIL
- (iv) DTL
- (v) NTL
- (vi) TTL

Semi-saturated

- i) Schottky TTL
- ii) ECL

* Unipolar logic family :- There are three types of unipolar family. These devices are formed by metal oxide semiconductor field effect transistor (MOSFET). It is also known as MOS device.

MOS device

PMOS

(p-channel)
In this channel
p-channel is
employed

NMOS

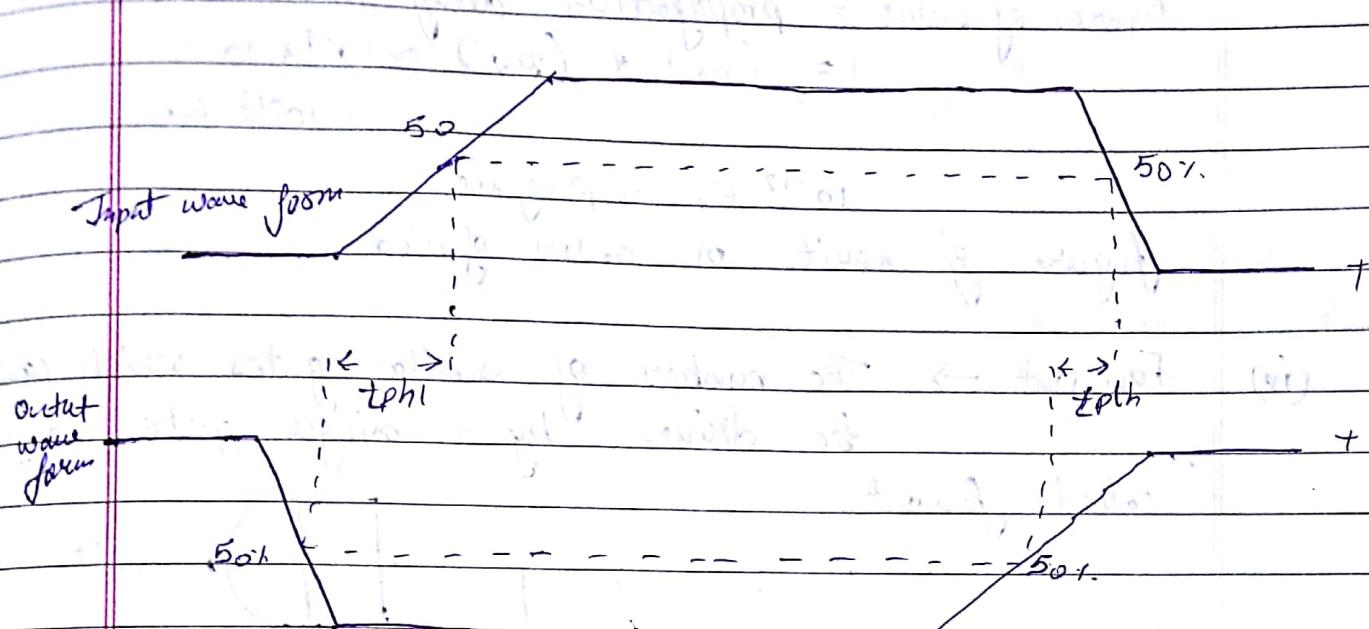
(N-channel)
It is employed
by n-channel
of device

CMOS

(complementary)
This device
employed by
P and N channel
both

* Characteristics of Integrated Circuit →

(i) Speed of operation :- The speed of operation of a digital circuit depend upon propagation delay time. It is measured by delay time b/w 50 percent of voltage level of input and output wave forms.



$$\text{Propagation delay time} = t_{phl} + t_{pH} / 2$$

(ii) Power dissipation \rightarrow The amount of energy dissipate by IC's per unit time is called power dissipation of IC's.

$$P_{diss} = I_{cc} \cdot V_{cc}$$

I_{cc} is the current through IC and V_{cc} is the supplied potential difference to IC. It's order will be milliwatt.

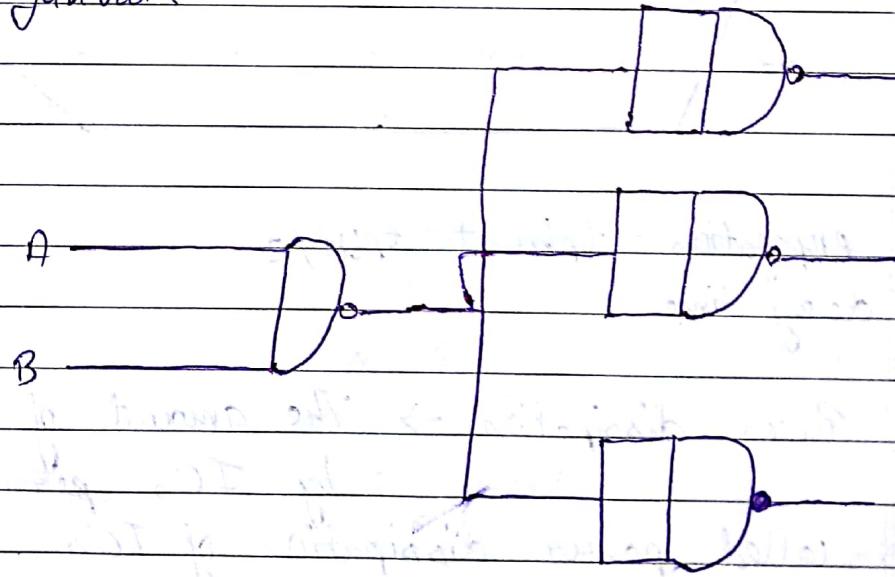
$$1 \text{ mW} = 10^{-3} \text{ W}$$

(iii) Figure of merit \rightarrow Figure of merit IC's depends upon propagation delay time and power dissipation by IC's. It's the product of propagation delay time and power.

$$\begin{aligned}\text{Figure of merit} &= \text{propagation delay time} * \text{power} \\ &= (\text{ns}) * (\text{MW}) = 10^{-9} \times 10^{-3} \\ &= 10^{-12} \text{ Ws}\end{aligned}$$

10^{-12} Ws = picojule
figure of merit or order of pico

(iv) Fan out \rightarrow The number of similar gates which can be driven by a single gate is called fanout.



These figure has fanout = 3

IC should have high fanout. So that it operate more gates.

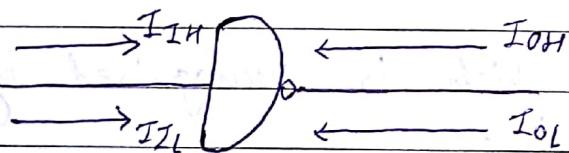
(v) Current and voltage parameter \rightarrow For IC circuit following current and voltage parameter are used.

1. High level input voltage (V_{IH}) \rightarrow This is the minimum input voltage which is recognized by the gate when logic is 1.
2. low level input voltage (V_{IL}) \rightarrow This is the maximum input voltage which is recognised by the gate when logic is 0.
3. High level output voltage (V_{OH}) \rightarrow This is the minimum output voltage which is recognised by the gate when logic is 1.
4. low level output voltage (V_{OL}) \rightarrow This is the maximum output voltage which is recognised by the gate when logic is 0.
5. High level input current (I_{IH}) \rightarrow This is the minimum input current which is recognised by the gate when logic is 1.

6. low level input current (I_{IL}) → This is the maximum input current which is recognised by the gate when logic is 1.

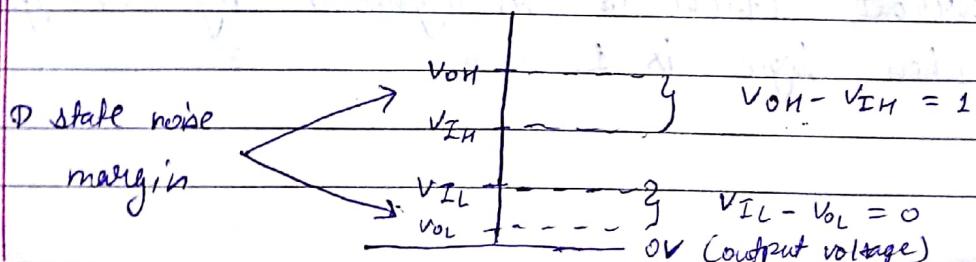
7. High level output current (I_{OH}) → This is the minimum output current which is recognised by the gate when logic is 0.

8. Low level output current (I_{OL}) → This is the maximum output current which is recognised by the gate when logic is 1.



(vi) Noise Immunity → A stray electric & magnetic field may induce unwanted voltages to IC's, that is called noise.

The ability of IC's to tolerate noise is called noise immunity. IC should have high noise immunity.



(vii) Power supply requirement → Amount of power or supply voltage which is required by IC's to operate is called power supply requirement.

(viii) Operating temperature → The temperature range for which IC function properly is known as operating temperature. Generally, the range of operating temperature is 0°C to 70°C Celsius for consumer and the range of temperature for military application will be -55 to 125°C .

(ix) Flexibility available → Various flexibility are available for IC logic families.

(a) the breadth of series → It represent the type of different logic functions available in series.

(b) Popularity of series → It depends upon cost and other parameter function for this cost should be low.

(c) Wired logic capability → without any extra hardware the output of IC's are connected together is called its wired logic capability such type of logic capability perform additional logic without any extra hardware.

(d) Availability of component outputs \Rightarrow This is a property of ICs is used to eliminate the need of additional inverters.

(e) Type of output \rightarrow Passive pullup, active pullup, open collector, drain, tri-state are known as type of output.

* Integrated Injection logic \rightarrow

Integrated injection logic is the specified form of direct coupled transistor logic. It is easier to fabricate with bipolar junction transistor.

It is very small chip area & consume less power & easier to operate at low voltage.

In given figure integrated injection logic is based on inverter property of transistors. It is also refer as Merge Transistor logic (MTL).

V_{in}	T_1	V_{out}
High	ON	0
Low	OFF	1

If input voltage for transistor T_1 is high. The base current b , will have two component one due to V_{in} and the other is due to I_s . Transistor T_1 is on. So Idle V_c , will be 0 due to short circuit b/w collector & emi terminal.

So potential drop at o/p will be 0.

Input

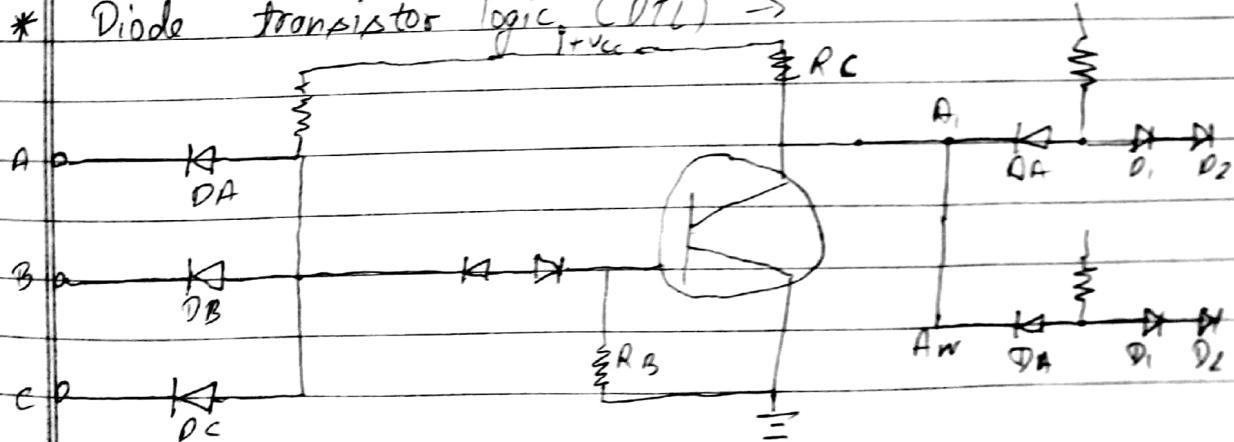
	V_o	T_2	V_o
(low)	0	off	1
(High)	1	on	0

When V_{in} is 0 that is low potential then Transistor T_1 is off and output V_o will be 1.

When V_{in} is 1 that is at high voltage Transistor T_2 is on and V_o output will be 0.

When V_{in} is 0 that is at low voltage Transistor T_2 is off and output V_o will be 1. So this circuit swing b/w 0 and 1 depends upon input voltage of Transistor.

* Diode transistor logic (DTL) \rightarrow



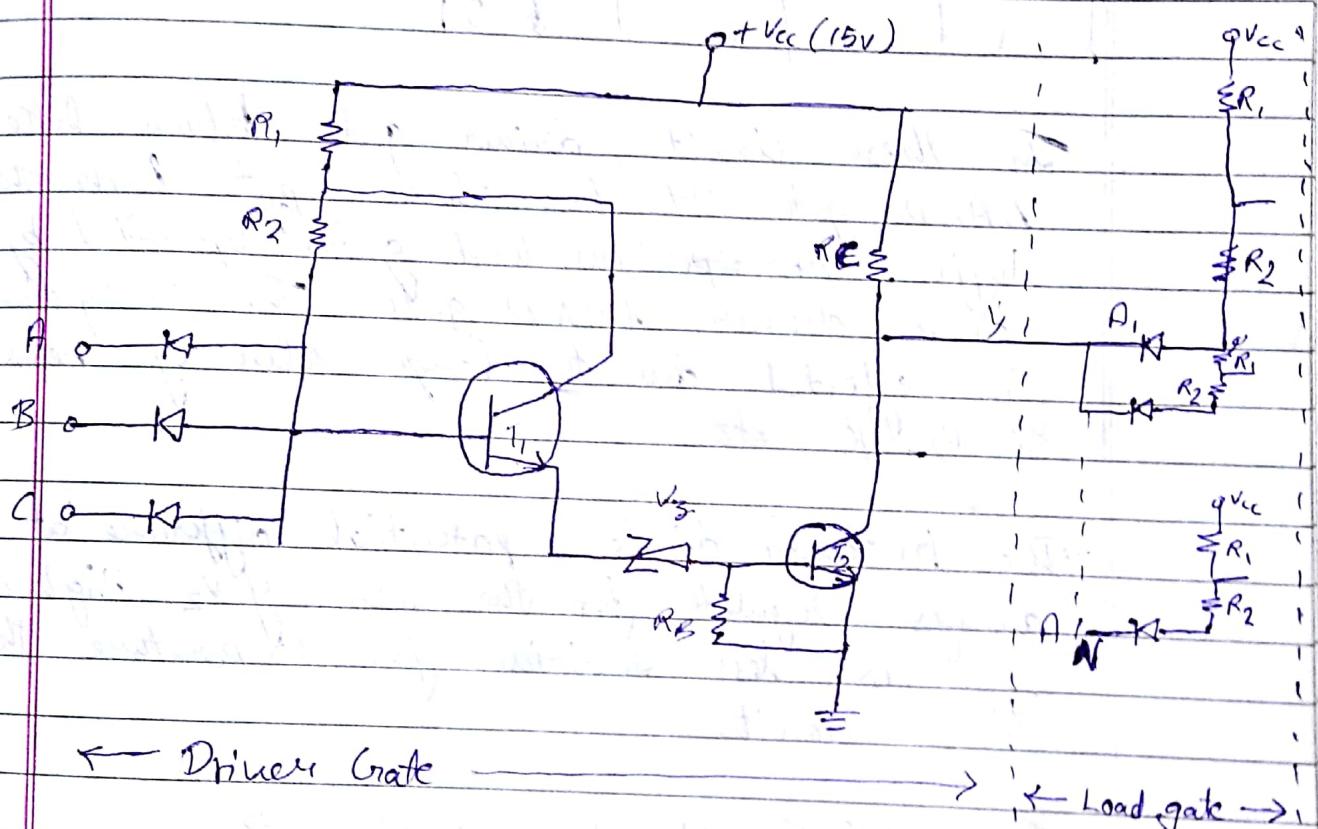
This is three input (A, B, C) Diode Transistor
This circuit is driven by NAND gate. Load
gate are similar to the driven gate. The
input diode D_A, D_B, D_C conduct through
resistance R if corresponding input is low
then output will be high which is inputs
transistor T .

So transistor T will be ON. Then output of
transistor will be 0. Then there will be no
potential drop for load gates. If input
of diode D_A, D_B and D_C is high then output
will be low that is 0. So transistor T will
be off. Then output of transistor X , will be
1. Then load gates are operated by NAND
gate

07/03/18

Physics

High threshold logic (HTL) \rightarrow Due to presence of electric motors on/off control system, high voltage switches the noise level is quite high. In these situations DTL circuit is redesigned with a high supply voltage (upto 15 volt). The diode is replaced by zener diode and resistance is modified by its higher values. Such modified circuit is known as high threshold logic.



Truth Table

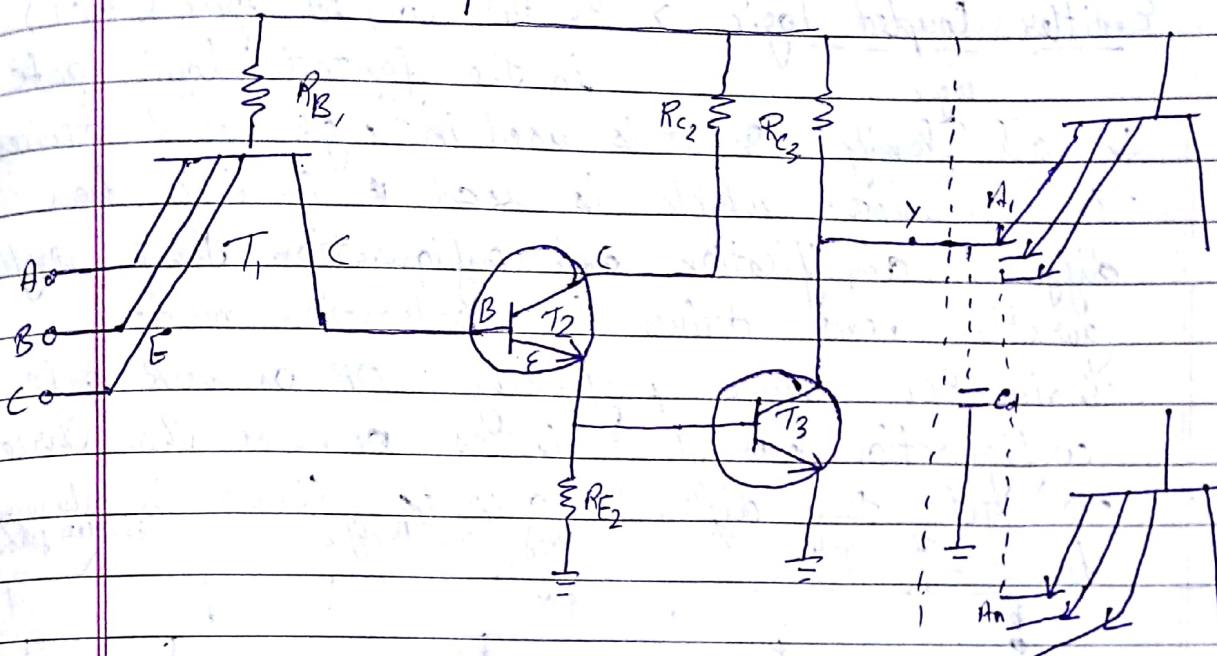
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

In these circuit, driver gate behave like a NAND gate. It has three input high threshold logic. ~~The open~~ An load gates ^{are} operated by these driver NAND gate. The propagation delay is affected due to large value of resistance R_1, R_2, R_c , etc.

Due to zener diode, potential difference at T_2 always regulate for the value of V_Z . High threshold logic is less sensitive for temperature than DTL circuit.

Transistor Transistor logic (TTL) \rightarrow

$+V_{CC}(5V)$



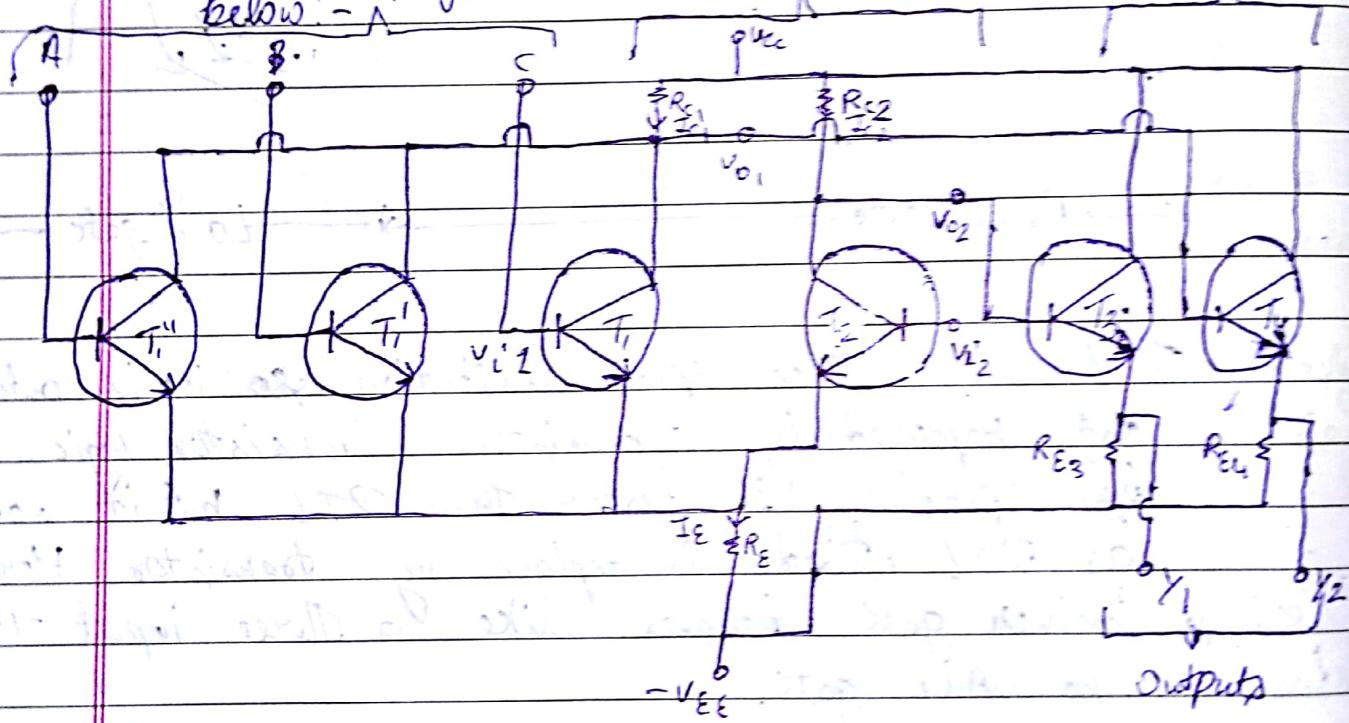
← Driver gate → ← Load gate →

DTL circuit has speed limitation so it is outdated and replaced by Transistor Transistor logic. TTL has operation SP faster than DTL but it works as DTL i.e., Diode is replace by transistor. Here driver gate behaves like a three input TTL or NAND gate.

103/2018

Emitter Coupled logic \rightarrow Emitter Coupled logic (ECL) is the fastest logic gate in all family. So, it is used in high speed devices. The transistor which is used in ECL has different amplification and configuration that configuration never drives in saturation mode.

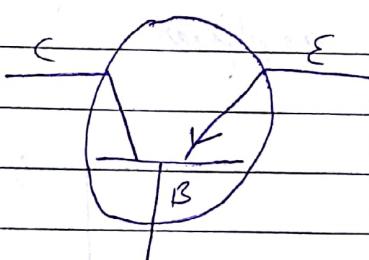
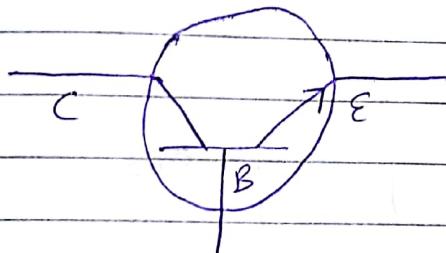
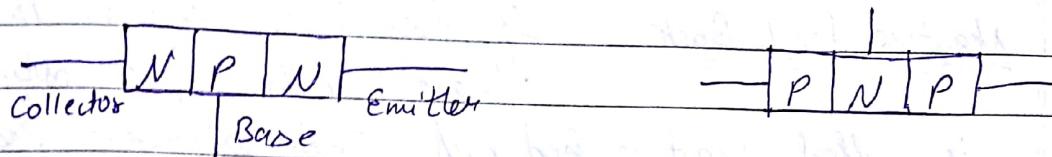
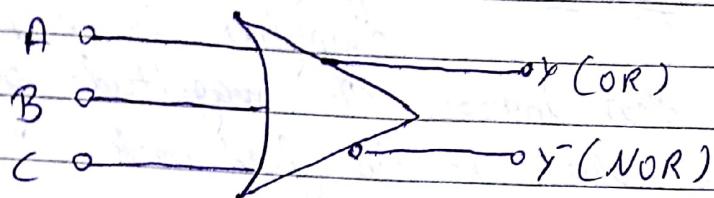
Basic ECL circuit performing OR or NOR gate configuration has three inputs or more than three to get two different outputs. Circuit is shown below:-



In given circuit, three inputs A, B, C is given to base of transistors T_{1''}, T_{1'}, T₁. The collector terminal of input ~~transistor~~ transistors are connected to V_{cc} (High voltage). Emitter terminal of input transistors are connected to -V_{EE} (Low voltage). Differential amplifier is made of transistors T₂ and T₃. The inputs of differential amplifier is V₁ and V_{1''}. Output of differential

amplifier is V_{B1} and V_{B2} . These output are collected with transistor T_3 and T_4 . It works like input for transistor T_3 and T_4 . Combination of T_3 and T_4 known as Emitter follower T_3 's emitter voltage gives output y_1 and y_2

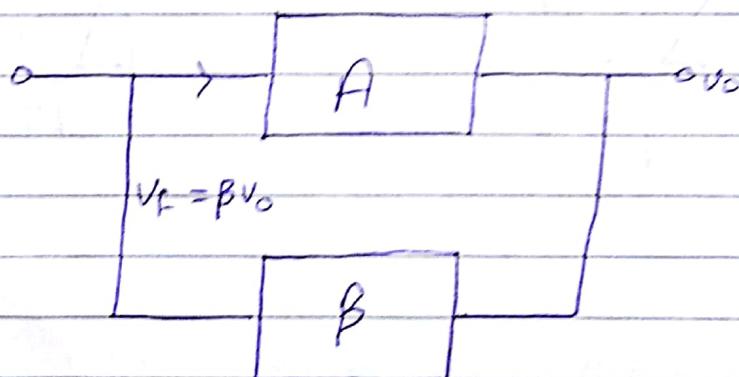
* Simplified circuit of this figure



Feed Back Amplifier

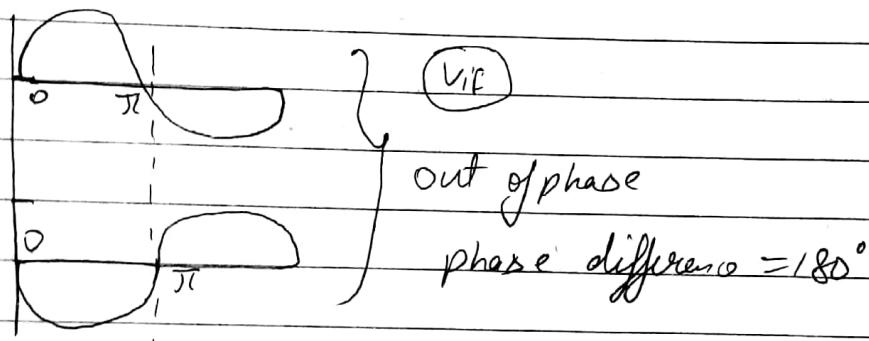
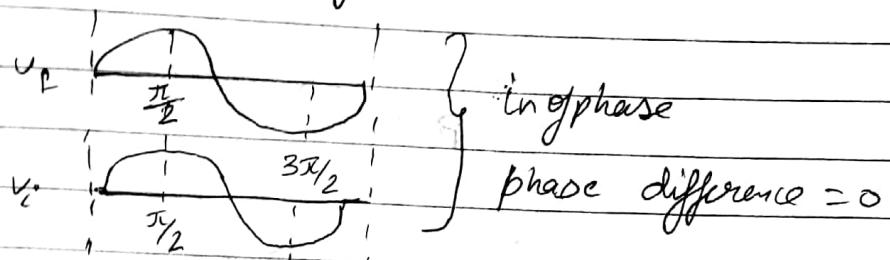
If a part of output energy of an electrical source is transferred to its input that source is called feed back & such amplifiers are known as feed back amplifiers. There are two types of feed back.

- 1) Positive Feed Back → If feedback signal given to an amplifier is in phase with input signal that increase the magnitude of input signal that is called positive feed back.
- 2) Negative Feed Back → If feedback signal is out of phase with input signals that is called Negative feed back. This decrease the gain of amplifier.



In given figure amplifier is represented by box (A) & feed back network is represented by Beta box (B). Feedback Network B fed Up voltage to input within input for amplifier will be V_{if} . For ideal feed back network.

- (1) There should be no change in the ~~given~~ gain of amplifier due to Beta network.
- (2) The input signal voltage must be transmitted by amplifier only.
- (3) The feedback voltage must be transmitted through Beta network only.
- (4) Due to Beta network there should not be any loading on amplifier circuit.



After feed back.

The resultant voltage at input after feedback is

$$v_{if} = v_i - v_f \quad \text{--- (1)}$$

(For negative feed back)

$$v_{if} = v_i + v_f \quad \text{--- (2)}$$

(For positive feed back)

From eq (1) & (2) for negative feed back

$$v_{if} = v_i - \beta v_o \quad (\text{for Negative feed back})$$

$$v_{if} = v_i + \beta v_o \quad (\text{for + feed back})$$

gain of amplifier :-

$$A = \frac{\text{output voltage}}{\text{input voltage}} = \frac{V_o}{V_i}$$

After feed back gaining voltage

$$A = \frac{V_o'}{V_i}$$

$$A = \frac{V_o'}{V_i' - BV_o'} \rightarrow \text{negative feed back}$$

$$(A = \frac{V_o'}{V_i' + BV_o'}) \rightarrow \text{positive feed back}$$

$$\Rightarrow A(V_i + BV_o') = V_o' \quad \text{for +ve}$$

$$A V_i = AB V_o' + V_o'$$

$$\frac{A V_i}{(AB + 1)} = V_o' \quad X$$

$$A V_i = V_o' - AB V_o'$$

$$A V_i = V_o' \quad \frac{1}{(1-AB)}$$

$$\boxed{V_o' = \frac{A V_i}{1+AB}} \rightarrow \text{for negative feed back}$$

let us consider

$$\boxed{\frac{V_o'}{V_i} = AF}$$

$$\frac{A V_i}{(1-AB) V_i} = AF \Rightarrow \boxed{\frac{A}{1-AB} = AF} \quad \text{for +ve}$$

$$\boxed{\frac{V_o - V_o}{1+AB} = AF}$$

here AB is known as loop gain of circuit. For the feed back loop gain is positive & for -ve feed back loop gain is negative.

$|AB|$ is known as return difference. It may be positive, negative or zero.

Case-1

If return difference is greater than one then $|AF| > |A|$. This is the case for negative feedback ($-AB$)

$$|1-AB| > 1$$

$$AF = \frac{A}{1+AB}$$

Case-2

If return difference is less than one then $|AF| < |A|$. This is the case for positive feedback.

$$AF = \frac{A}{1-AB}$$

Case-3

$$|1-AB| = 0$$

$$AF = \infty$$

If return difference is 0 then AF is ∞ that is output voltage can be obtain without any input voltage. This is the condition for an oscillator.

Gain of amplifier with feedback also ^{measured} in decibel (dB)

$$g_0 \log_{10} \left(\frac{A}{AF} \right) = (g_0 \log_{10} (1-AB)) \text{ dB}$$

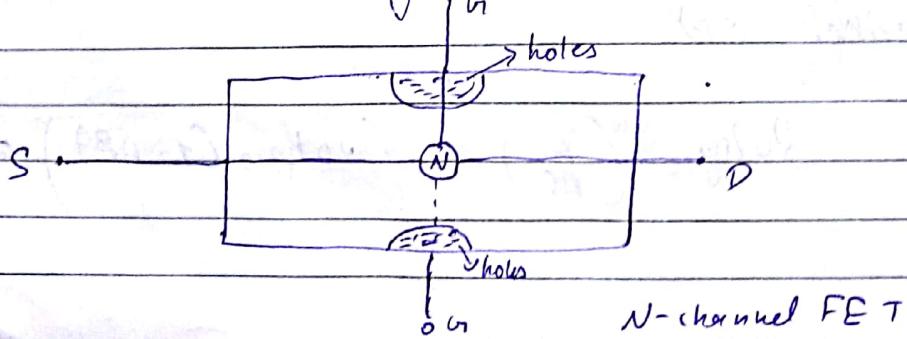
22/03/18

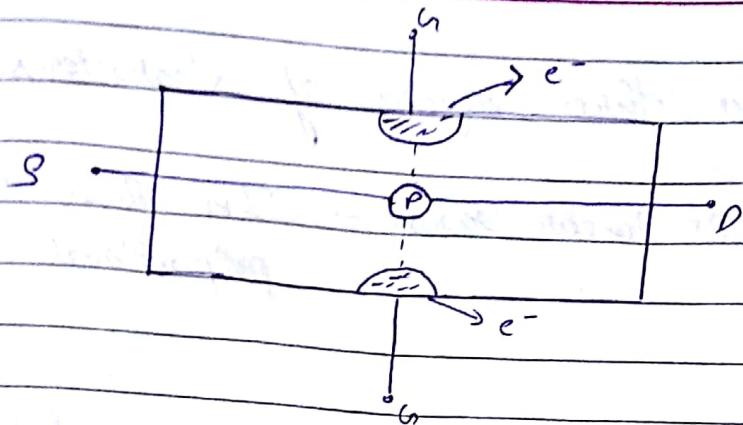
Field effect transistor (FET) It is a semi-conductor device which apply electric potential to control output current. So, it is a voltage control device. It has one type of majority charge carrier that is electron or hole. There are two type of FET

(1) JFET \rightarrow It is junction field effect transistor

(2) MOSFET \rightarrow It is metal oxide semiconductor field effect transistor.

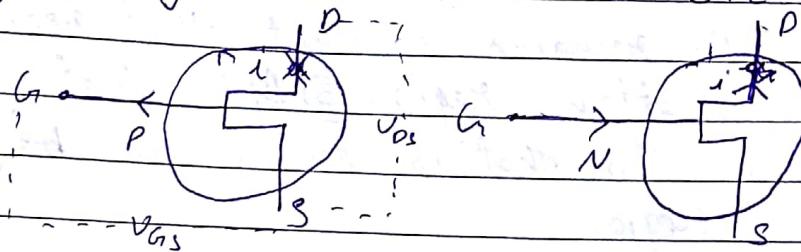
1) JFET \rightarrow It is N-Type or P-Type doped transistor. N-Type as majority carrier electron and P-TYPE as majority carrier hole. N-Type semiconductor is also called as N-channel FET. P-Type semiconductor is also called as P-channel FET. The terminals of FET is called source (S) and Drain (D). Through this ends majority carrier flow. Majority carrier enters from source and leave it from drain. Two opposite faces in perpendicular direction to source-drain line are heavily doped with opposite kind of impurities and known as gate (G).





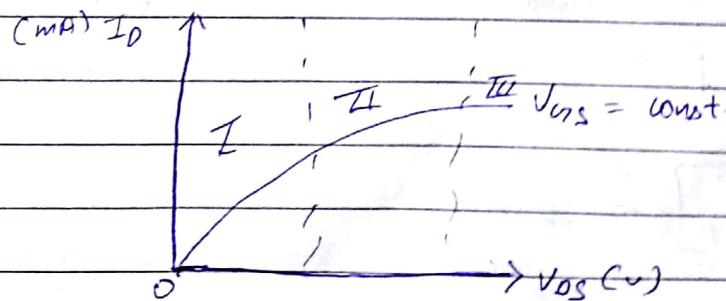
P-channel JFET

Electron symbol for N-BAND P-channel JFET



In source - drain circuit of JFET, The output or of drain - current I_D depends upon drain voltage (V_{DS}) and gate voltage (V_{GS}).

If reverse biased voltage (V_{GS}) of gate remains constant, Then The family of curves showing the dependence of drain current (I_D) with forward drain voltage (V_{DS}). This is known as common source-drain characteristics.



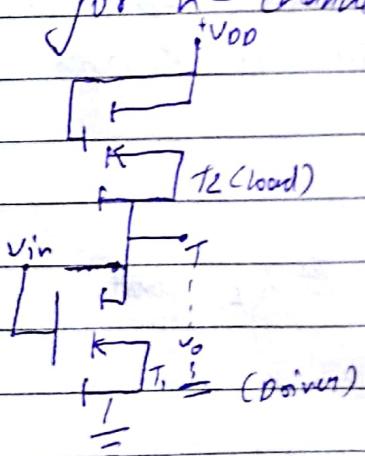
There are three regions of characteristics curve

(1) Resistive or linear region \rightarrow In these regions, I_D is proportional to V_{DS} .

(2) Saturation region \rightarrow At the boundary of linear region or resistive region, for V_{DS} is equal to constant

I_D remains constant. That region is called saturation region (3) After that for constant value of I_D that is known as pinch off voltage region.

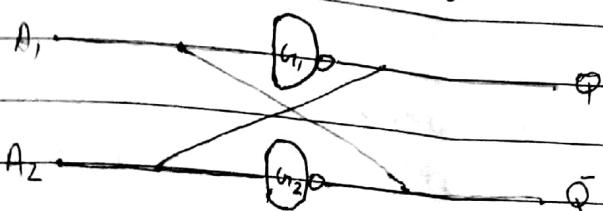
(2) MOSFET \rightarrow (Metal oxide semiconductor field effect transistor) \rightarrow MOSFET circuit is used due to high density fabrication and low power dissipation. Then MOSFET is used in devices circuit has p or n-channel. Circuit with p-channel is known as p-MOS with n-channel known as n-MOS. Charge carrier for p-channel will be hole and charge carrier for n-channel will be electron.



(Rest MOSFET detail is
in last page)

11/04/2018
 Flip flop \rightarrow flip flop is a device which is used to store binary data. Memory elements are formed by flip flop. It is designed by basic logic gates or universal logic gate.

(1) Latch or 1-bit memory cell



In given memory cell, two NAND gates G_1 and G_2 are used to latch information or locked information. G_1 and G_2 works as inverter / NOT gate.

Truth Table

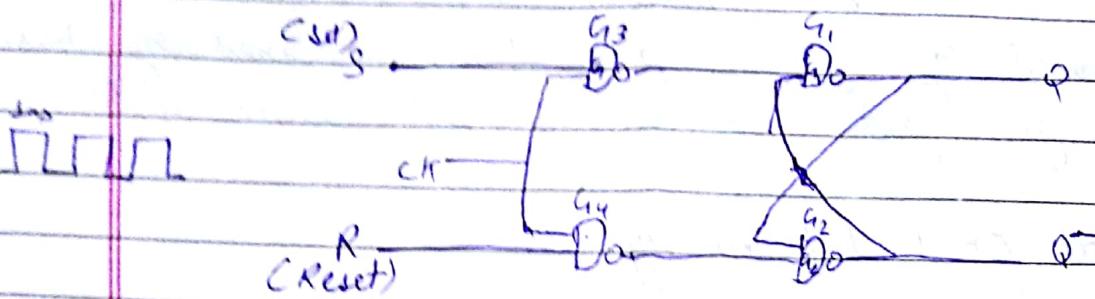
A_1	A_2	Q	\bar{Q}	
1	1	?	?	Uncertain
0	1	1	0	
1	0	0	1	
0	0	?	?	Uncertain

$Q = 1 \Rightarrow$ Set state

$Q = 0 \Rightarrow$ Reset state

Latch is operated for complementary inputs. If both inputs are 0 and 1, result will be uncertain. So this conditional prohibited.

(2) S-R flip flop



In S-R flip flop input is inverted by using NAND (or NOR) gate then supply to latch.

gate

Due to G_3 and G_4 $S=0 \& R=0$ gives output $Q=1$ & $\bar{Q}=0$ for $A_1=0 \& A_2=1$. Now for SR flip flop $0\ 0$ is not possible habitat. But $S=1, R=1$ both outputs try to be 1 which is not allowed. So these condition is prohibited .

S	R	Q_{out}	\bar{Q}	
0	0	Q_n	\bar{Q}_n	
1	0	1	0	
0	1	0	1	
1	1	?	?	Uncertain

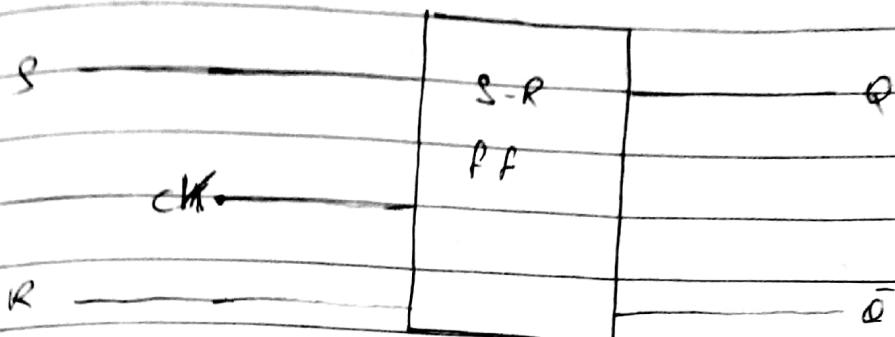
(clock)

(3) clk is used in S-R flip flop to synchronise the input of SR flip flop. $\text{clk}=1$, clock is present. In this case, operation is exactly the same as SR flip flop.

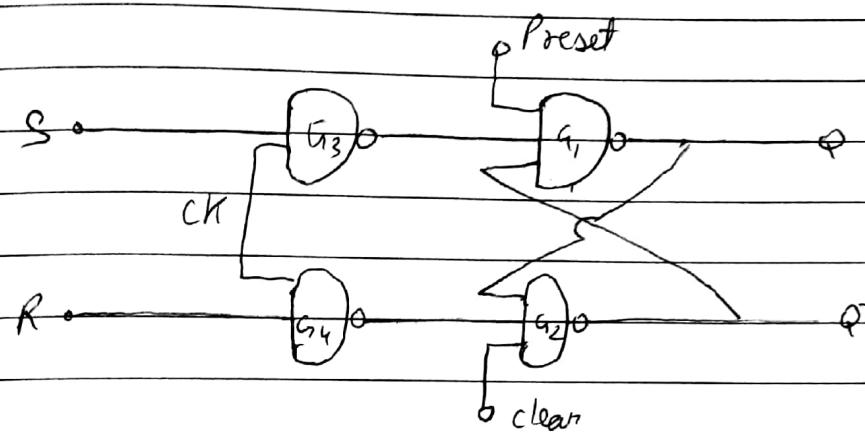
If $\text{clk}=0$, clock is not present, that is $\text{clk}=0$.

In this case, output doesn't depend upon S and R.

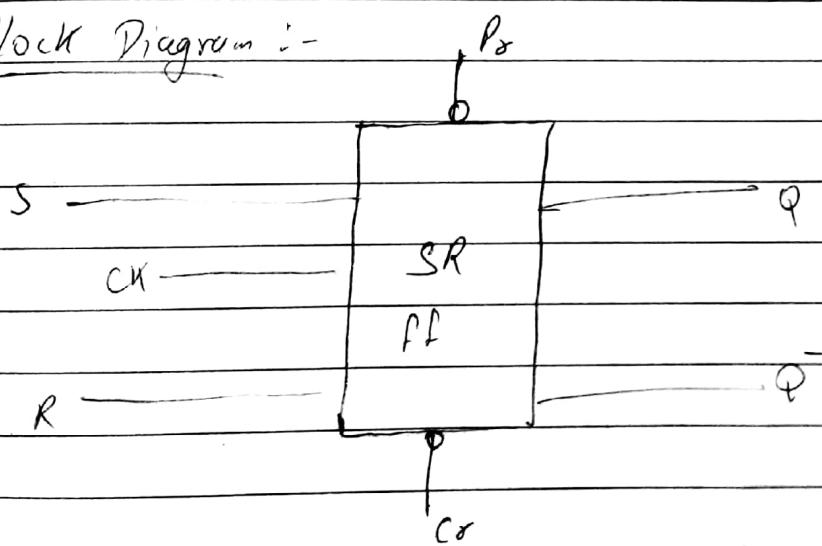
* Block Diagram



SR flip flop with Preset & clear



Block Diagram :-



When preset = Clear = 1, the circuit operate in accordance with SR flip flop

If $PR=0$, $CR=1$, Then $Q = 1$, $\bar{Q} = 0$. It does not depends upon input of SR flip flop. These operation is known as clear.

If $PR=1$, $CR=0$, then $Q = 0$, $\bar{Q} = 1$. These operation is known as preset.

1/20/18

Master slave J-K flip flop

- * Gate G₁, G₂, G₃ and G₄ formed Master flip flop.
The clock for master flip flop will be positive or positive edge triggered.
- * Master flip flop is same as J-K flip flop.
The output will be Q_M and Q̄_M.
- * When CK = 1, master flip flop is enabled and gives output Q_M and Q̄_M
- * G₅, G₆, G₇ and G₈ formed slave flip flop.
When CK = 1, then CK from for slave flip flop CK = 0.
- * This time slave flip flop is disabled.
When CK = 0, master flip flop is disabled and slave flip flop is enabled.
- * Slave flip flop gives output after pulse delay when master flip flop is operated. The input of slave flip flop commanded by output of master flip flop.
- * The final output depends upon clock pulse given to master flip flop
- * Truth Table for master & slave flip flop will be same as J-K flip flop

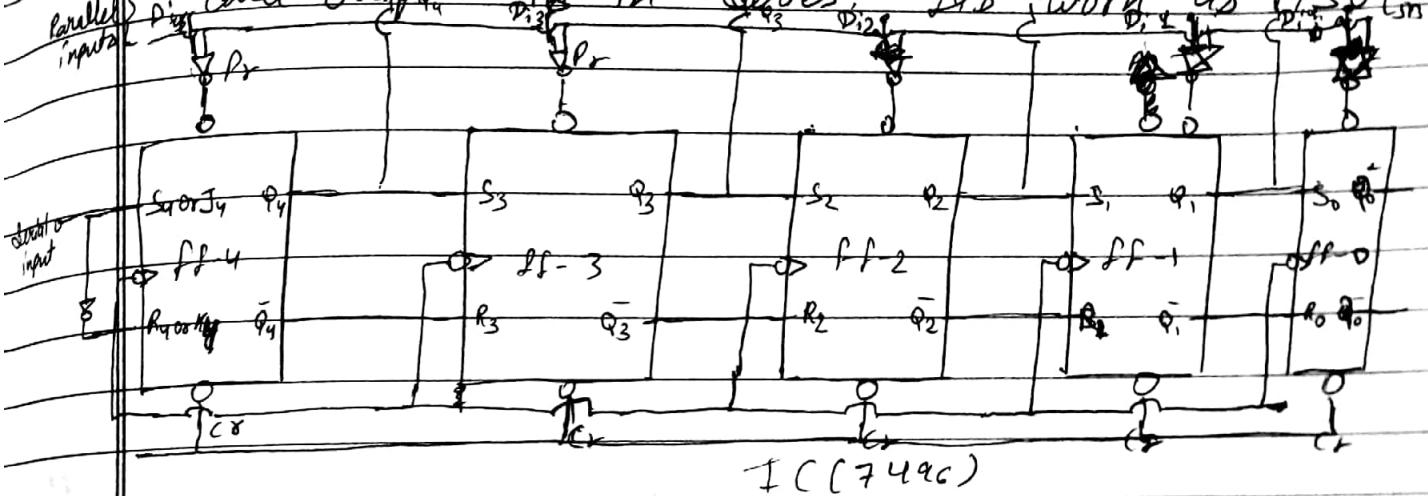
advantage of flip flop

- * Master slave flip flop is designed to overcome race-around difficulty
- * So that the uncertainty in output of J-K flip flop is removed

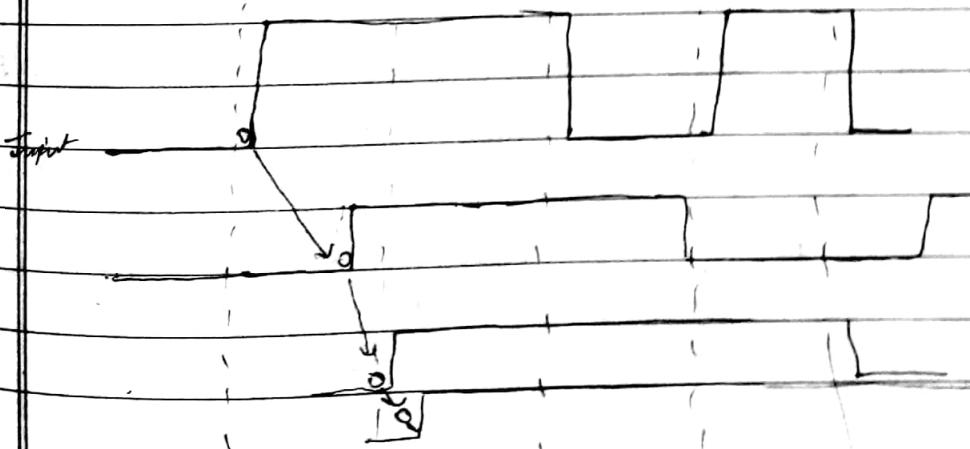
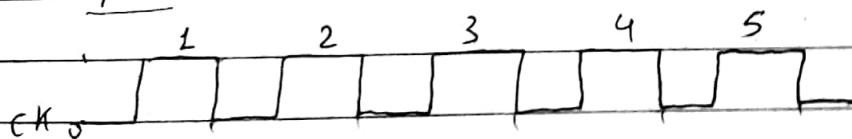
Shift register

A 5-bit

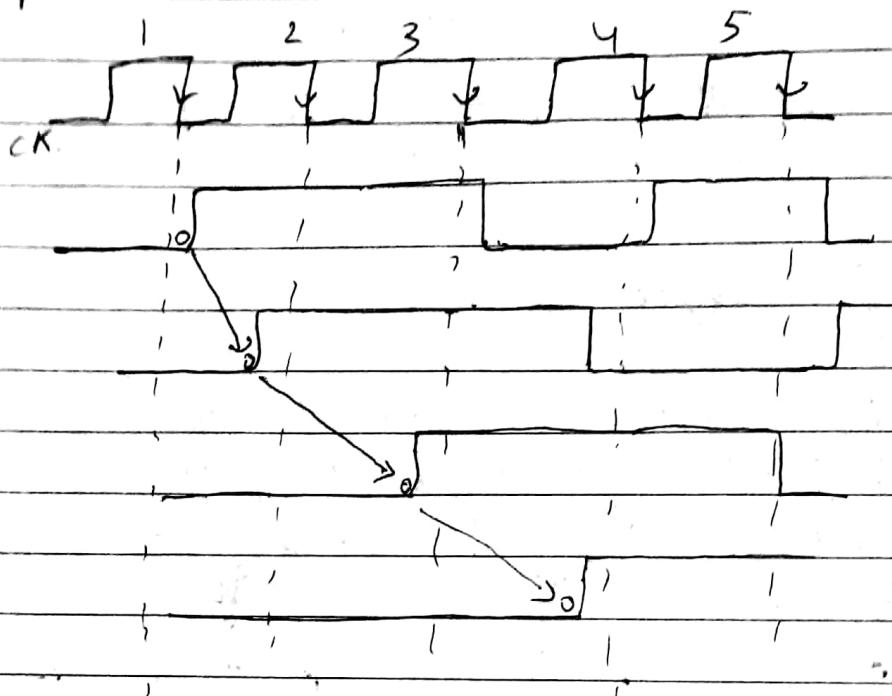
- * Shift register is made of master slave flip flop. For this shift register inputs are parallel and outputs are in series. It's work as $D_5 S_0 C_0$.



Wave form of shift register from serial input



Wave form of serial shift registers from serial input.



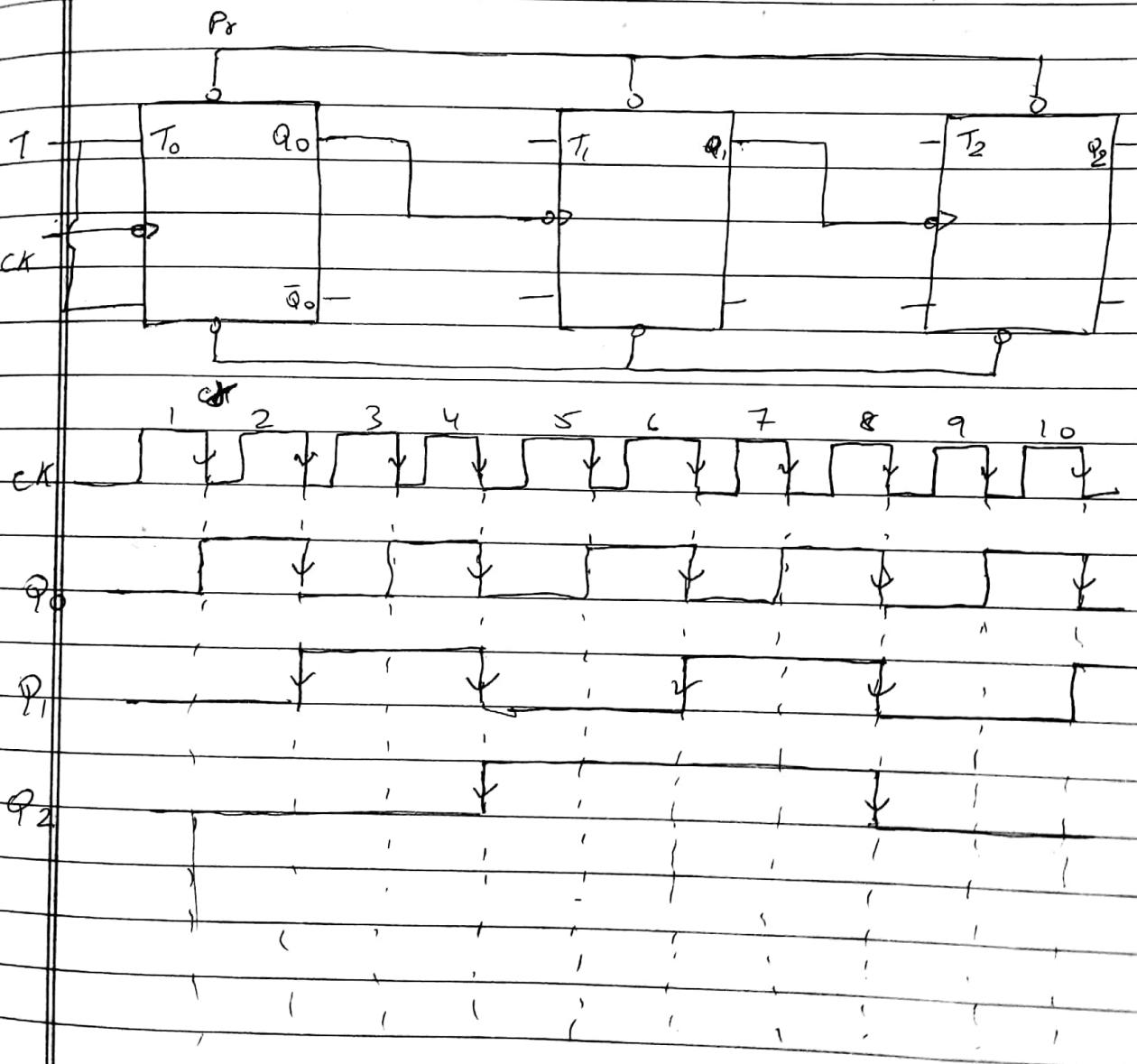
Synchronous and asynchronous counter \Rightarrow If all

flip flop in a counter are not clocked simultaneously. That counter is called ripple counter or asynchronous counter.

* If all flip flop are clocked are simultaneously that counter is called synchronous counter.

* A circuit use for counting the pulse is known as counter

- * If the no. of state in counter is capital N
It is known as modulo N , or divide
by N counter.
- * For ring counter N state is known as N modulo,
but other counter known as two N modulo.
- # A 3-bit binary counter

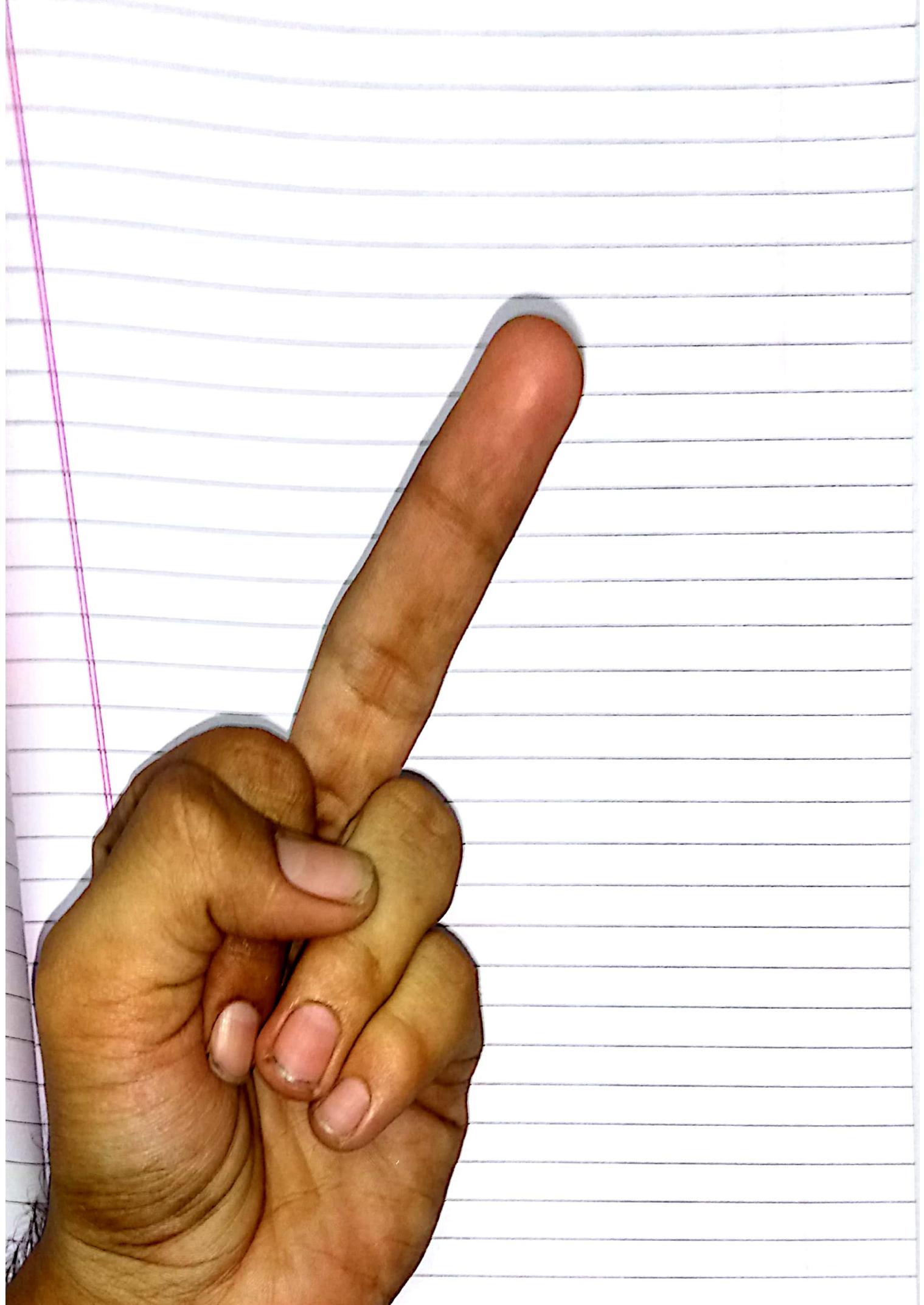


* Up/Down counter \rightarrow If the output of counter increases with successive clock pulse. It is called up counter. It is triggered with negative edge clock. (do above eg. of ^{3-bit binary counter} clock pulse)

If the output of counter decrease with successive clock pulse. It is called down counter. It is triggered with positive edge clock.
(e.g. reverse of eg. of 3-bit binary counter)

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MOSFET → Most logic is used for designed of LSI and VLSI ICs. It is not use forSSI or MSI. Most of the microprocessor memories and peripheral devices formed by MOSFET circuit.



Physics

A logic function is

$$y = (A+B \cdot C) \cdot (B+C \cdot A)$$

(a) Design a circuit using gates to realize the function.

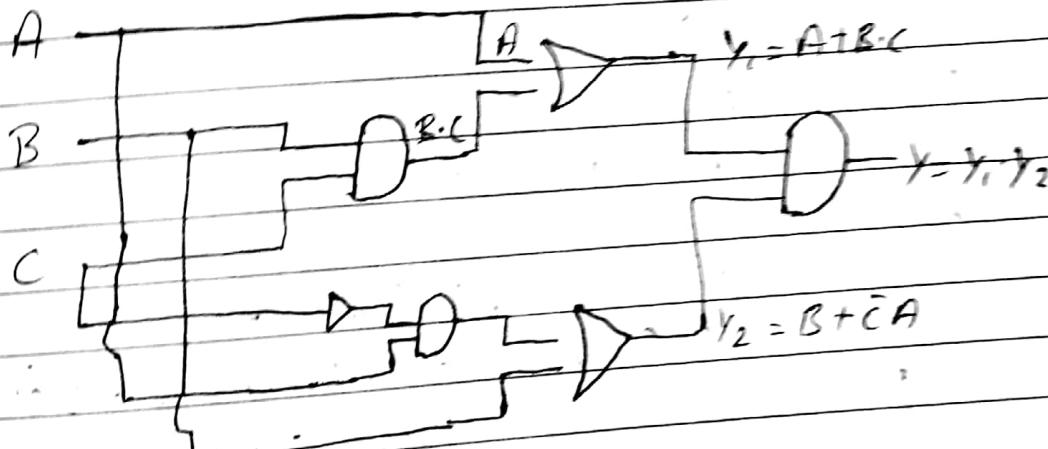
(b) Write down the SOP and POS form

(c) Write down the canonical SOP form and canonical POS form

(d) $y = y_1 \cdot y_2$

$$y_1 = A + B \cdot C$$

$$y_2 = B + \bar{C} \cdot A$$



(b) ii) SOP form \Rightarrow

Simplifying given expression:-

$$\begin{aligned} & \because A(B+C) \\ & = AB + AC \end{aligned}$$

$$y = (A+B \cdot C) \cdot (B+C \cdot A)$$

$$y = (A \cdot B) + (A \cdot \bar{C} \cdot A) + (B \cdot C \cdot B) + (B \cdot C \cdot \bar{A})$$

$$y = A \cdot B + A \cdot \bar{C} + B \cdot C + B \cdot \bar{C} \cdot \bar{A} \quad \therefore \bar{C} = 0 \quad \therefore \bar{B} \bar{B} = B$$

$$\rightarrow [Y = AB + A\bar{C} + BC]$$

called SOP form

Sum of Product form

(ii) POS form \Rightarrow (Product of sum form) \Rightarrow

$$Y = (A+B)(B+\bar{C}A)$$

$$Y = (A+B)(A+C)(B+\bar{C})(C+\bar{A})$$

$$\Rightarrow Y = (A+B)(A+C)(B+\bar{C})$$

$$A+B C$$

$$\therefore \boxed{A+B C = (A+B)(A+C)}$$

$$(A+C)$$

Q2 Qbit

(c)

(i) Canonical SOP form

We have simplified SOP form

$$Y = A \cdot B + A \cdot \bar{C} + B \cdot C$$

Now

$$Y = A B C (\underline{S+C}) + A \bar{C} (B+\bar{B}) + B C (A+\bar{A})$$

$$Y = A \cdot B \cdot C + A \cdot B \cdot \bar{C} + A \cdot \bar{C} \cdot B + A \cdot \bar{C} \cdot \bar{B} + B \cdot C \cdot A + B \cdot C \cdot \bar{B}$$

$$\boxed{Y = A \cdot B \cdot C + A \cdot B \cdot \bar{C} + A \cdot \bar{C} \cdot B + A \cdot \bar{C} \cdot \bar{B} + B \cdot C \cdot A}$$

(ii) Standard (Canonical) POS form

Simplified form

$$Y = (A+B)(A+C)(B+\bar{C})$$

$$Y = (A+B+0)(A+C+0)(B+\bar{C}+0)$$

$$Y = (A+B+(C\bar{C}))(A+C+(B\bar{B}))(B+\bar{C}+A\bar{A})$$

$$Y = (A+B+C) \cdot (A+\bar{B}+\bar{C}) \cdot (\bar{A}+C+\bar{B}) \cdot (\bar{A}+\bar{C}+\bar{B}) \\ (B+\bar{C}+\bar{A}) \cdot (\bar{B}+\bar{C}+\bar{A}) \\ \Rightarrow Y = (A+B+C) \cdot (A+\bar{B}+\bar{C}) \cdot (B+\bar{C}+\bar{A}) \cdot (\bar{A}+B+\bar{C})$$

(d) Realise these standard SOP and POS from using DeMorgan's

2) (e) A, B, C = 3 variables, $2^3 = 8$ rows, column = 4
(0 to 7)

i	$A^{2=4}$	$B^{1=2}$	$C^{0=1}$	Y
0	0	0	0	0 \rightarrow POS $\rightarrow M_0$
1	0	0	1	1 \rightarrow SOP $\rightarrow m_1$
2	0	1	0	1 \rightarrow SOP $\rightarrow m_2$
3	0	1	1	0 \rightarrow POS $\rightarrow M_3$
4	1	0	0	1 \rightarrow SOP $\rightarrow m_4$
5	1	0	1	0 \rightarrow POS $\rightarrow M_5$
6	1	1	0	0 \rightarrow POS $\rightarrow M_6$
7	1	1	1	1 \rightarrow SOP $\rightarrow m_7$

Q.2
Determine the minimum and maximum term by given truth table of 3 variables.

Ans

1. Minimum term or min term \rightarrow

* Denoted by m_i

* $i = \text{no. of rows}$

* If $y=1$ then it will be min term

so here min terms are:-

$$y = m_1 + m_2 + m_4 + m_7$$

$$y = \sum m(1, 2, 4, 7)$$

* This min term will give output in SOP form.

2) Maximum term or max term

* Denoted by M_i

* $i = \text{no. of rows}$

* If $y=0 \Rightarrow$ max terms

so maxterms are

$$Y = M_0 \cdot M_3 \cdot M_5 \cdot M_8$$

$$\Rightarrow Y = \prod M(0, 3, 5, 6)$$

* This Max term will output in POS form

Q.3 Realise a truth table using

$$\text{(i) } Y = \sum m(0, 1, 2, 3, 7, 8, 11, 12, 13)$$

$$\text{(ii) } Y = \prod M(4, 5, 6, 14, 15)$$

Q1 Simplifying the following expressions using K-map for 4 variables A, B, C, D

$$Y = m_0 + m_3 + m_5 + m_7 + m_8 + m_9 + m_{12} \text{ or}$$

$$Y = \sum m (1, 3, 5, 7, 8, 9, 12) \text{ or}$$

$$Y = \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}D + \bar{ABC}D + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D$$

K-map :-

$$n=2 (A, B) \Rightarrow 2^2 = 4$$

$$i \rightarrow 0 \rightarrow 3$$

A B	0	1
0	0	2
1	1	3

$$00 = 2^1 \times 0 + 2^0 \times 0 = 0$$

$$01 = 2^1 \times 0 + 2^0 \times 1 = 1$$

$$11 = 2^1 \times 1 + 2^0 \times 1 = 2 + 1 = 3$$

$$10 = 2^1 \times 1 + 2^0 \times 0 = 2$$

$$n=3 (A, B, C) \quad 2^3 = 8$$

$$i \rightarrow 0 \rightarrow 7$$

A B C	000	011	111	110
0	000 = 0	010 = 2	110 = 6	100 = 4
1	001 = 1	011 = 3	111 = 7	101 = 5

$$n=4 (A, B, C, D) \quad 2^4 = 16$$

A B C D	0000	0111	1111	1010
0	0	4	12	8
1	1	5	13	9
0	3	7	15	11
1	2	6	14	10

Rules :-

1) No shall should remain without grouping as
complete as

2) Binary (Adjacent)

Octal \rightarrow Quad \rightarrow Bits

(8) (4) (1)

3) 3-bit mapping \rightarrow Essential Prime Implicant (EPI)

	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	AB	$\bar{A}\bar{B}\bar{C}$
a)	00	01	11	10	
b)	00	01	11	10	
c)	10	11	01	00	
d)	10	11	01	00	
e)	00	01	11	10	
f)	00	01	11	10	
g)	10	11	01	00	
h)	10	11	01	00	

$$Y = m(1, 5, 7) + m(2, 4) + m(6, 9)$$

$$Y = \bar{A}D + A\bar{C}\bar{D} + A\bar{B}C$$

6.2 Simplifying the following expression using K-map for
4-variable P, Q, R, S

$$Y = m_0 + m_3 + m_5 + m_7 + m_8 + m_9 + m_{10} + m_{11}$$

15

	$\bar{A}B$	$A\bar{B}$	$\bar{A}\bar{B}$	AB	$\bar{A}\bar{B}$
$\bar{C}D$	00	01	11	10	
CD	00	01	11	10	
$\bar{C}D$	11	10	01	00	
CD	11	10	01	00	
$\bar{C}D$	10	01	00	11	
CD	10	01	00	11	
$\bar{C}D$	01	00	11	10	
CD	01	00	11	10	
$\bar{C}D$	00	11	10	01	
CD	00	11	10	01	
$\bar{C}D$	11	01	10	00	
CD	11	01	10	00	
$\bar{C}D$	01	10	00	11	
CD	01	10	00	11	
$\bar{C}D$	00	01	10	00	
CD	00	01	10	00	

$$Y = m(1, 5, 3, 7) + m(12, 8, 13, 9)$$

$$Y = \bar{A}D + A\bar{D}\bar{C}$$

Q.3 Plot the logical Expression

$$Y = ABCD + A\bar{B}\bar{C}D + A\bar{B}\bar{C} + AB$$

on a 4-variable K-map and obtain the simplified expression from K-map

Ans 3) Standard SOP form

$$Y = ABCD + A\bar{B}\bar{C}D + A\bar{B}\bar{C} + AB$$

Now

$$Y = ABCD + A\bar{B}\bar{C}D + A\bar{B}\bar{C}(D + \bar{D}) + AB(C + \bar{C})(D + \bar{D})$$

$$Y = ABCD + A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}\bar{C}\bar{D} + AB(CD + C\bar{D} + \bar{C}\bar{D})$$

$$Y = ABCD + A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}C\bar{D} + AB_{CD} + AB_{C\bar{D}} + AB_{\bar{C}\bar{D}}$$

$$Y = \sum m(8, 10, 11, 12, 13, 14, 15)$$

K-map :-

	0	1	2	3
0	0	1	1	0
1	1	0	1	0
2	0	1	0	1

$$Y = m(12, 13, 15, 14) + m(12, 8, 14, 10) + m(15, 11, 14)$$

$$Y = AB + A\bar{D} + AC$$

Q4

Simplify the expression using K-map

$$Y = \Sigma_m(7, 9, 10, 11, 12, 13, 14, 15)$$

Ans

$$\text{Ans} : - Y = AB + AD + AC + BC\bar{D}$$

Q5

Simplify the expression using K-map

$$Y = \Sigma_m(3, 4, 5, 7, 9, 13, 14, 15)$$

$$\text{Ans} : - Y = \bar{A}CD + ABC + A\bar{C}\bar{D} + \bar{A}BC\bar{D}$$

Q6

Simplify the expression using K-map

$$Y = \Sigma_m(0, 1, 4, 6, 5, 8, 9, 12, 13, 14)$$

$$\text{Ans} : - Y = (\bar{B} + D)$$

Q.3

Obtain

- (a) SOP
 (b) POS

$$F(A, B, C, D) = \sum m(0, 1, 2, 5, 8, 9, 10)$$

	$A\bar{B}$	$A+B$	$A+\bar{B}$	$\bar{A}+\bar{B}$	$\bar{A}+B$		\downarrow	\downarrow
CD	00	00	01	11	10			
00	0	0	0	0	0			
01	1	1	0	1	0			
11	3	+	15	11				
10	2	6	0	0	10			

$$Y = M(0, 4, 12, 8, 1, 5, 13, 9) \cdot M(13, 4, 6, 14)$$

$$Y = C \cdot (\bar{B} + D)$$

09/03/2018

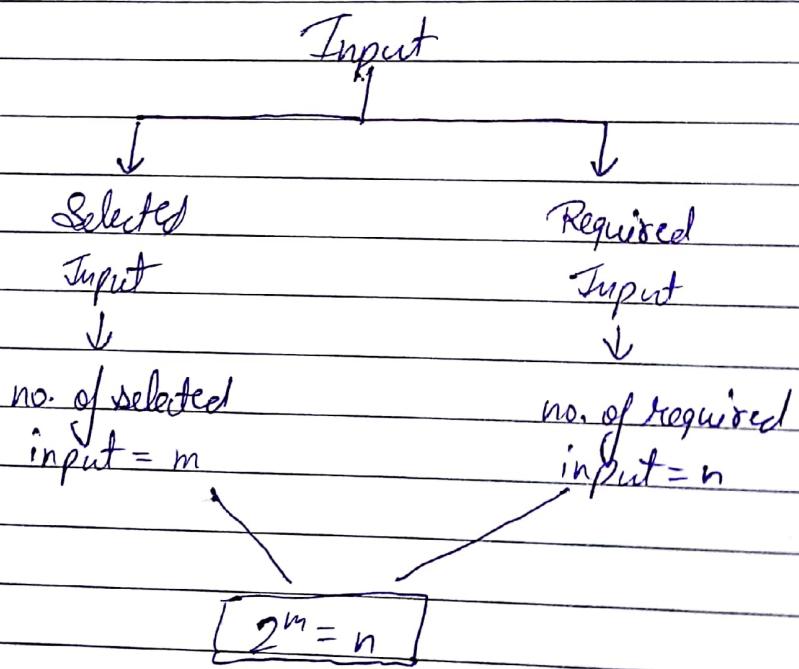
* Combinational Circuits =>

i) Multiplexers

Three types of multiplexer :-

- (i) 4:1
- (ii) 8:1 (74151)
- (iii) 16:1 (74150)

Multiplexer is a digital device which gives you opportunity to choose output among giving inputs By the help of selected inputs



Eg:-

(i) $2:1$ multiplexer

Input Output

$$(2)^2 \quad m = 1$$

$$n = 2$$

$$\text{iv) } 4:1 = 2^2:1$$

$$m = 2$$

$$n = 1$$

$$8:1 = (2)^3:1$$

$$m = 3$$

$$n = 8$$

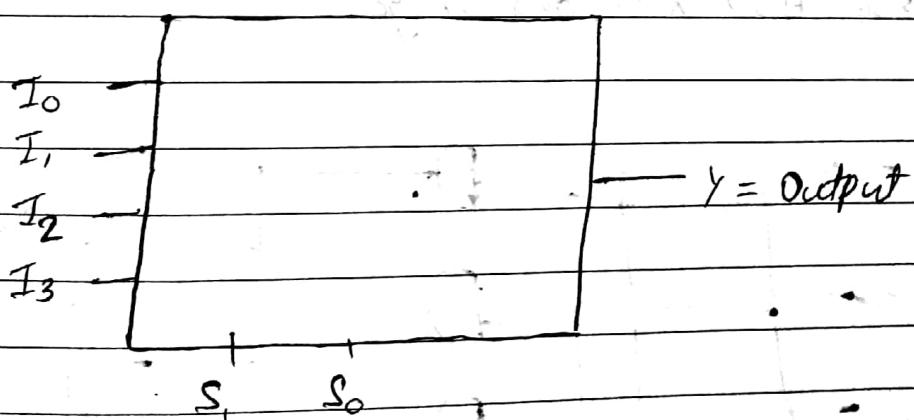
$$16:1 = (2)^4:1$$

$$m = 4$$

$$n = 16$$

(ii) 4:1 multiplexer

* Block diagram



Here required input = $(I_0 \rightarrow I_3) = 4$

selected input = $(S_1, S_0) = 2$

* Truth Table :-

Input		Output
S_1	S_0	y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

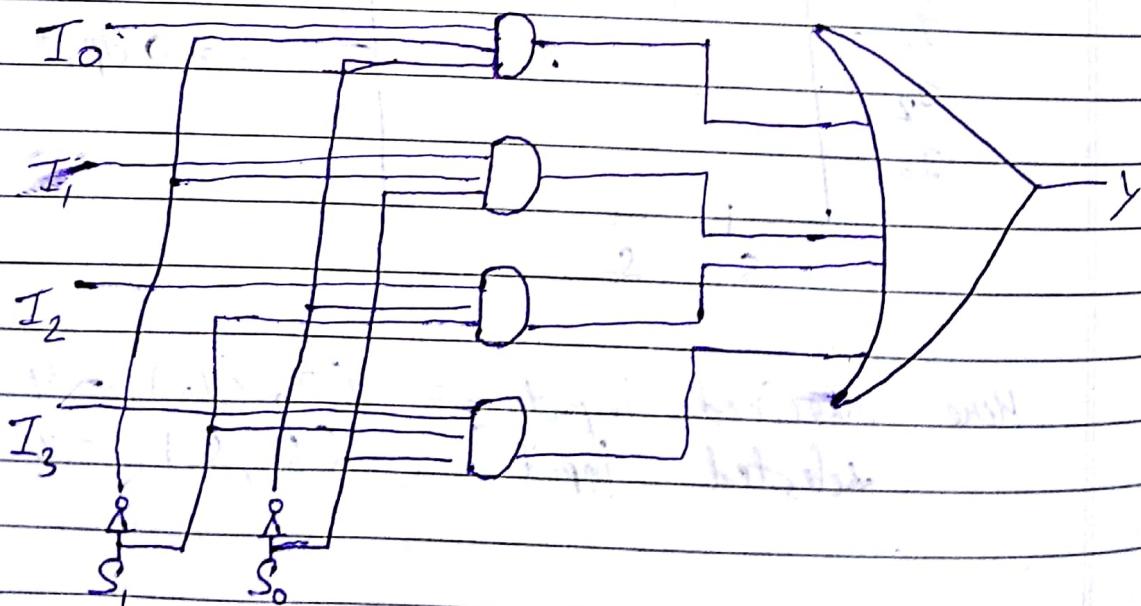
* logic expression

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

* Boolean Diagram \Rightarrow

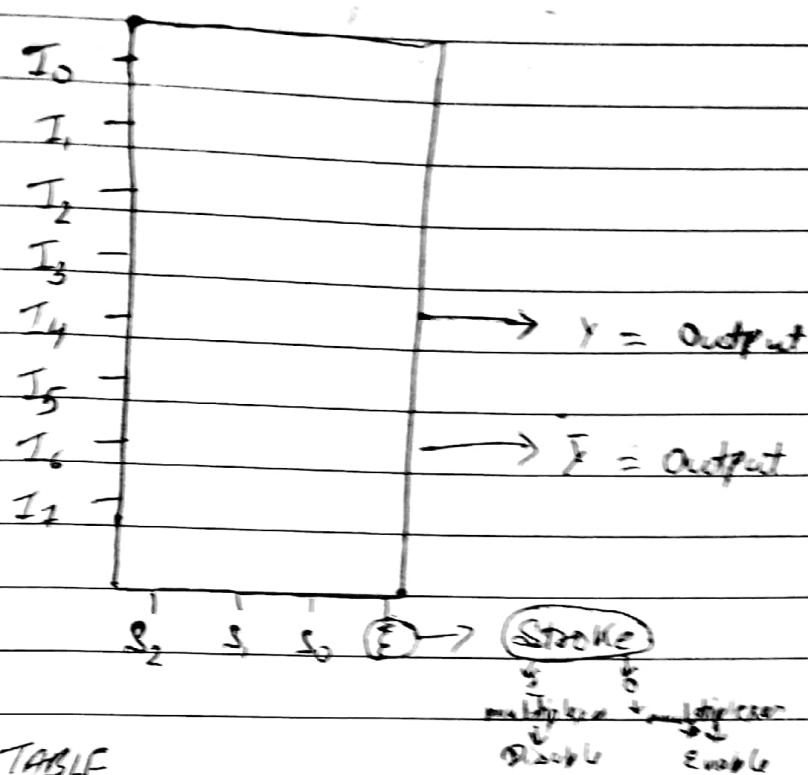
$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

Using AND, NOT and OR gate



(2) 8:1 multiplexer (74151 - IC)

* Block Diagram



* TRUTH TABLE

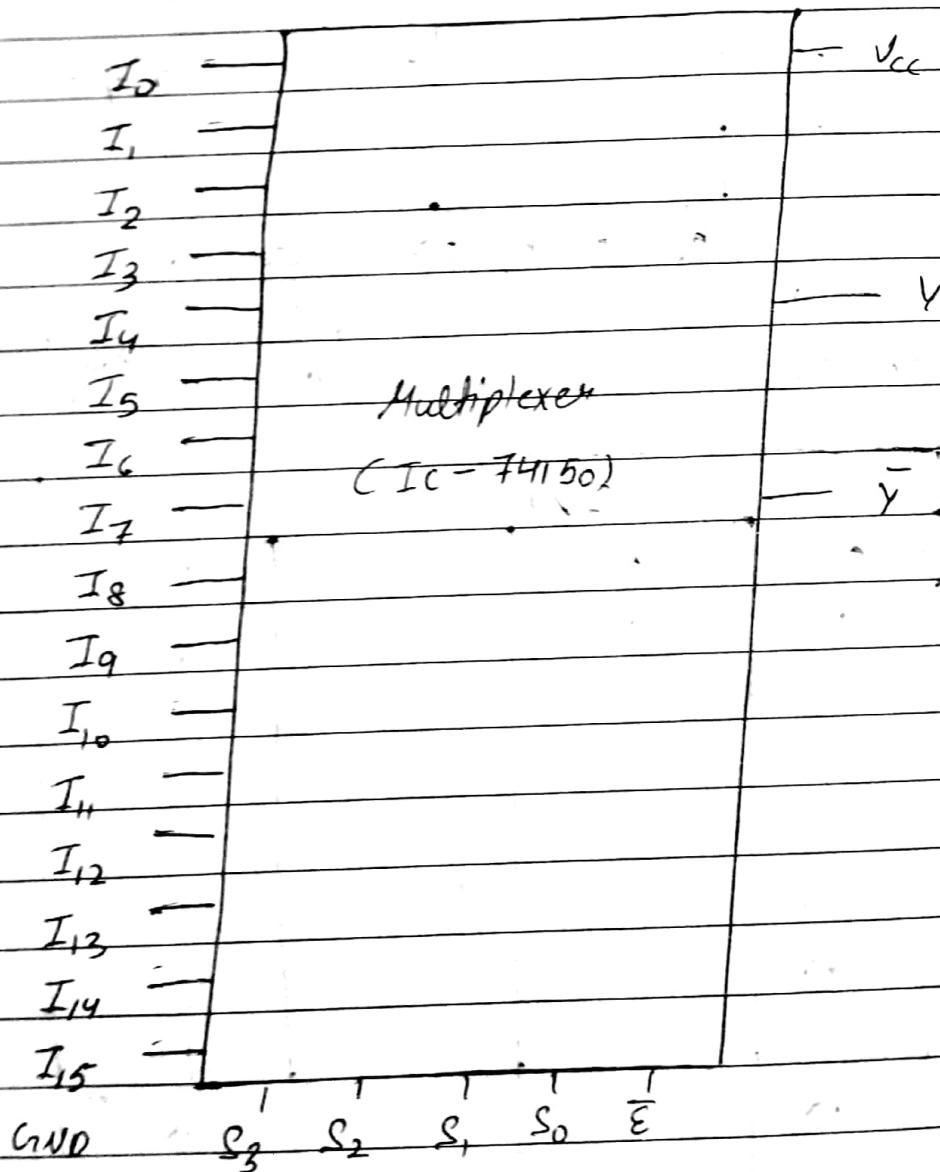
INPUT				OUTPUT	
E	S_2	S_1	S_0	y	\bar{x}
1	X	X	X	1	0
0	0	0	0	I_0	\bar{I}_0
0	0	0	1	I_1	\bar{I}_1
0	0	1	0	I_2	\bar{I}_2
0	0	1	1	I_3	\bar{I}_3
0	1	0	0	I_4	\bar{I}_4
0	1	0	1	I_5	\bar{I}_5
0	1	1	0	I_6	\bar{I}_6
0	1	1	1	I_7	\bar{I}_7

* Boolean Diagram \Rightarrow

$$Y = \bar{E}_0 [\bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \\ \bar{S}_2 S_1 S_0 * I_3 + \bar{S}_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 \bar{S}_0 I_5 + \\ S_2 S_1 \bar{S}_0 I_6 + S_2 \bar{S}_1 S_0 I_7]$$

3) 16:1 multiplexer ($I_C = 74150$)

* Block Diagram



where $I_0 \rightarrow I_{15} = 16$ ~~output~~ inputs

$S_3 \rightarrow S_0 = 4$ select Input
 $\bar{E} = \text{Enable}$

V_{cc} = power supply
 y, \bar{y} = Output

always $\bar{E} = 0$ multiplexer - Enable
 $\bar{E} = 1$ Disable

15

Stroke	Select Input				Output	
	\bar{E}_1	S_3	S_2	S_1	S_0	y
0	0	0	0	0	0	I_0
1	0	0	0	0	1	I_1
2	0	0	0	1	0	I_2
3	0	0	0	1	1	I_3
4	0	0	1	0	0	I_4
5	0	0	1	0	1	I_5
6	0	0	1	1	0	I_6
7	0	0	1	1	1	I_7
8	0	1	0	0	0	I_8
9	0	1	0	0	1	I_9
10	0	1	0	1	0	I_{10}
11	0	1	0	1	1	I_{11}
12	0	1	1	0	0	I_{12}
13	0	1	1	0	1	I_{13}
14	0	1	1	1	0	I_{14}
15	0	1	1	1	1	I_{15}
16	1	x	x	x	x	0

Boolean expression

$$y_0 = \bar{S}_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0$$

$$y_1 = \bar{S}_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 I_1$$

$$y_2 = \bar{S}_3 \bar{S}_2 \bar{S}_1 S_0 I_2$$

$$y_3 = \bar{S}_3 \bar{S}_2 S_1 \bar{S}_0 I_3$$

$$y_4 = \bar{S}_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 I_4$$

$$y_5 = \bar{S}_3 S_2 \bar{S}_1 \bar{S}_0 I_5$$

$$y_6 = \bar{S}_3 S_2 \bar{S}_1 \bar{S}_0 I_6$$

$$y_7 = \bar{S}_3 S_2 \bar{S}_1 S_0 I_7$$

$$y_8 = S_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 I_8$$

$$y_9 = S_3 \bar{S}_2 \bar{S}_1 S_0 I_9$$

$$y_{10} = S_3 \bar{S}_2 S_1 \bar{S}_0 I_{10}$$

$$y_{11} = S_3 \bar{S}_2 S_1 \bar{S}_0 I_{11}$$

$$y_{12} = S_3 \bar{S}_2 \bar{S}_1 \bar{S}_0 I_{12}$$

$$y_{13} = S_3 \bar{S}_2 \bar{S}_1 S_0 I_{13}$$

$$y_{14} = S_3 \bar{S}_2 S_1 \bar{S}_0 I_{14}$$

$$y_{15} = S_3 \bar{S}_2 S_1 S_0 I_{15}$$

logic diagram

AND gate = 16

OR = 1

NOT = 5

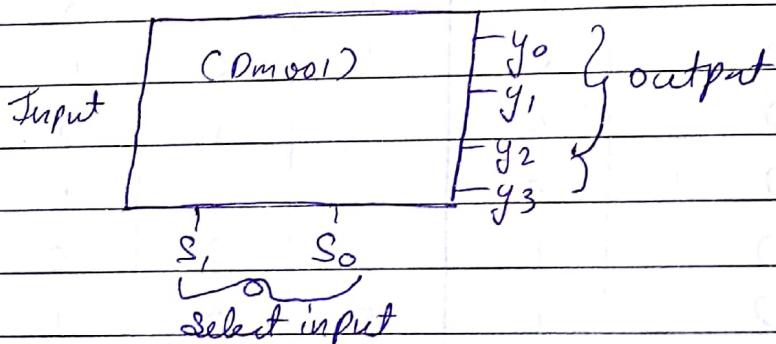
Demultiplexer (DM001)

* Demultiplexer = one into many

* Input = one

* Output = 2^m

* 1:4 Demultiplexer



* Truth Table

input Data	Select input	Output
I	S ₁ 0	y ₃ y ₂ y ₁ y ₀
I	0 0	0 0 0 1
I	1 0	0 1 0 0
I	1 1	1 0 0 0

Logic expression

$$y_0 = \bar{S}_1 \bar{S}_0 I$$

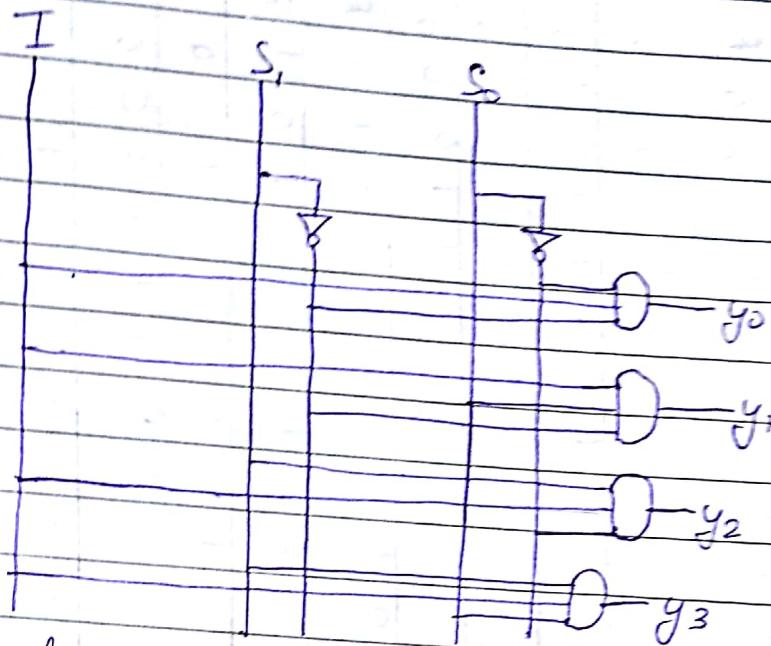
$$y_1 = \bar{S}_1 S_0 I$$

$$y_2 = S_1 \bar{S}_0 I$$

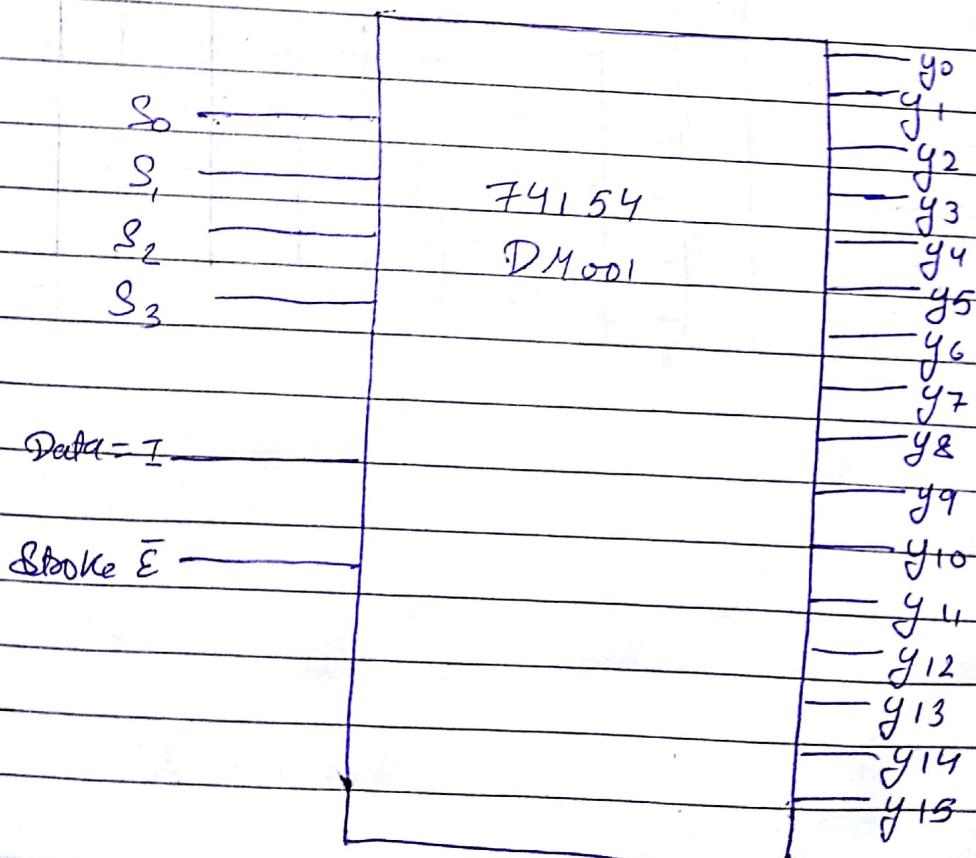
$$y_3 = S_1 S_0 I$$

AND = 4

NOT = 2



② 1:16 demultiplexer ($IC - 74154$)
* Block Diagram



Decoder → Decoder is a type of demultiplexer without data input because here Behaves select input behaves like input.

$$[n : 2^n]$$

To identify Decoder use this formula.

$$n = \text{Data input}$$

$$\text{Output} = 2^n$$

Eg : 3 : 8 decoder

$$n = 3$$

$$\text{Output} = 8 = (2)^3$$

Truth Table

A	B	C	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Boolean Expression for output

$$D_0 = \bar{A} \bar{B} \bar{C}$$

$$D_1 = \bar{A}\bar{B}\bar{C}$$

$$D_2 = \bar{A}\bar{B}C$$

$$D_3 = \bar{A}BC$$

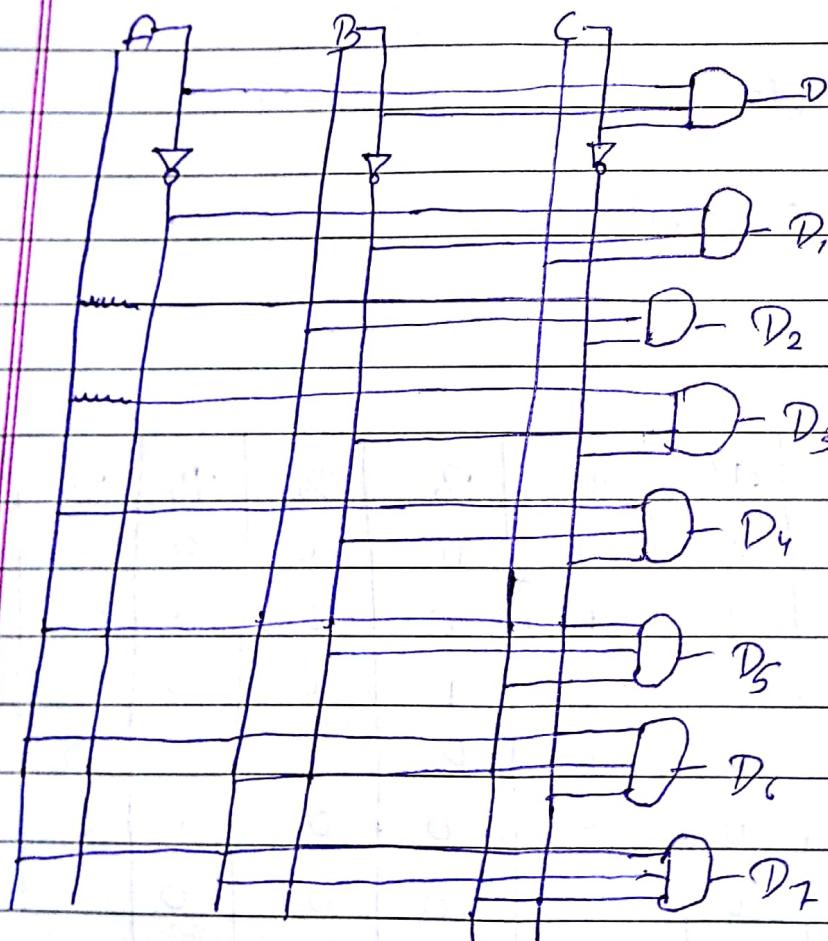
$$D_4 = A\bar{B}\bar{C}$$

$$D_5 = A\bar{B}C$$

$$D_6 = AB\bar{C}$$

$$D_7 = ABC$$

logic Diagram

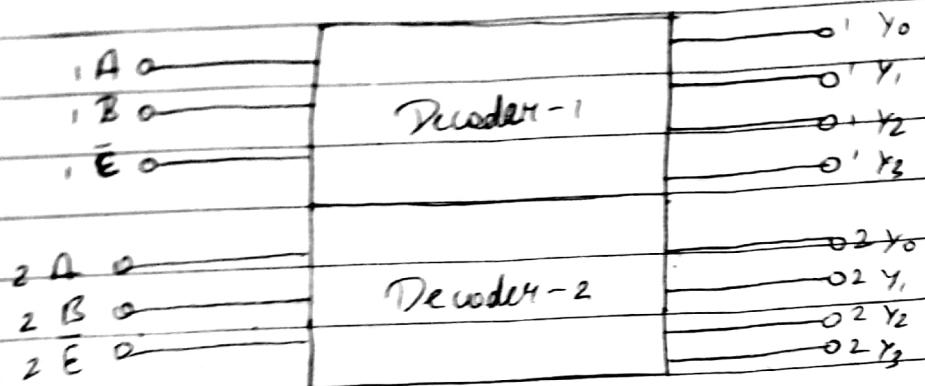


2:4

⇒ Dual Decoder (74139) ⇒

15,

* Block Diagram



* There are two decoders in one packet

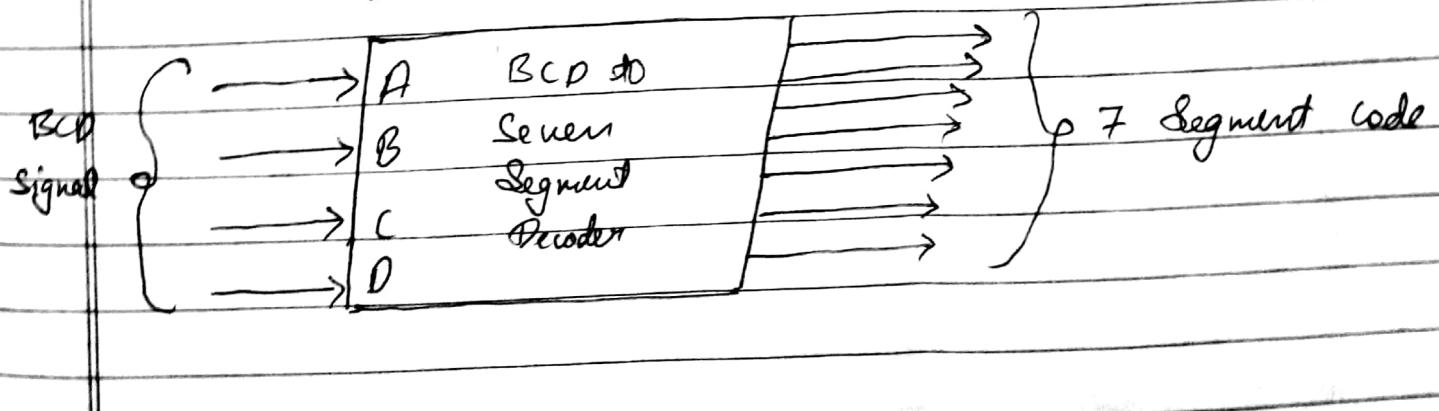
* Input = 2² = 4 for each decoder
Output = $2^2 = 4$

* Here Input are at "active low" signal

* Stroke or enable is also at "active low" signal

BCD (Binary coded decimal) To Seven segment decoder ⇒

* Block Diagram



* Display of decimal digits in 7 segment display

* Truth Table \Rightarrow

BCD Inputs				Seven Segment Outputs						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	0	1	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	0	1	0	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1

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DATE: / /

BCD to

$$\begin{array}{c}
 \begin{array}{c} a \\ | \\ b \end{array} & \begin{array}{c} a \\ | \\ b \end{array} & \begin{array}{c} a \\ | \\ b \end{array} & \begin{array}{c} a \\ | \\ b \end{array} \\
 \begin{array}{c} e \\ | \\ c \\ -d \end{array} & \begin{array}{c} c \\ | \\ d \end{array} & \begin{array}{c} e \\ | \\ c \\ -d \end{array} & \begin{array}{c} e \\ | \\ c \\ -d \end{array}
 \end{array}$$

$$\begin{array}{c}
 \begin{array}{c} a \\ | \\ f \end{array} & \begin{array}{c} a \\ | \\ f \end{array} & \begin{array}{c} a \\ | \\ b \end{array} & \begin{array}{c} d \\ | \\ b \end{array} & \begin{array}{c} a \\ | \\ b \end{array} \\
 \begin{array}{c} g \\ | \\ c \\ -d \end{array} & \begin{array}{c} c \\ | \\ d \end{array} & \begin{array}{c} c \\ | \\ e \\ -d \end{array} & \begin{array}{c} e \\ | \\ c \\ -d \end{array} & \begin{array}{c} e \\ | \\ c \\ -d \end{array}
 \end{array}$$

K-Map for 7-segment decoder

1) For output a

$$a = \sum_m (0, 2, 3, 5, 6, 7, 8, 9) + \sum_d (10, 11, 12, 13, 14, 15)$$

		\bar{AB}	\bar{AB}	\bar{AB}	\bar{AB}	
		CD	00	01	11	10
CD	00	0	4	12	13	11
CD	01	1	5	13	9	14
CD	11	3	7	15	10	12
CD	10	2	6	14	11	15

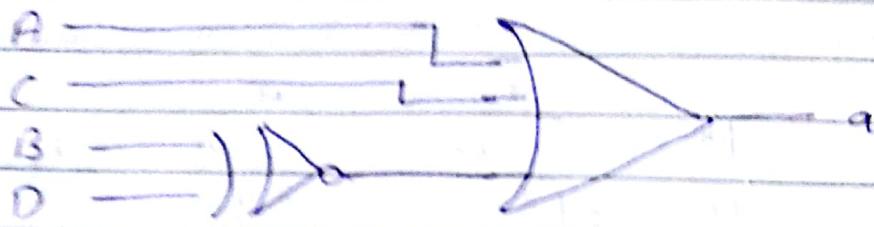
(i) Given Priority to output

(ii) Make sure no. min. term remain without grouping

$$\begin{aligned}
 a = & m(0, 8, 2, 10) + m(5, 13, 7, 15) + m(2, 3, 6, 7, 14, 15) + \\
 & m(8, 9, 10, 11, 12, 13, 14, 15)
 \end{aligned}$$

$$a = \bar{B}\bar{D} + BD + C + A$$

$$\begin{aligned}
 a = & \underbrace{\bar{B}\bar{D}}_{\text{Ex-NOR}} + \underbrace{BC}_{\text{DR}} + A + C
 \end{aligned}$$

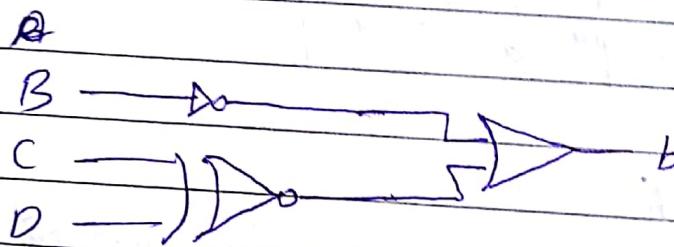
Logic Diagram

2) For output b

$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD	m_0	m_1	m_2	m_3	m_4	m_5	m_6	m_7	m_8	m_9	m_{10}	m_{11}	m_{12}	m_{13}	m_{14}	m_{15}
00	11	11	11	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	
01	10	01	01	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	
11	01	00	00	1	0	0	1	1	0	0	1	1	1	0	1	1	0	1	
10	00	11	11	0	1	0	0	1	1	0	0	1	0	1	0	0	1	1	

$$b = m(0, 4, 12, 8) + m(3, 7, 15, 14) + m(0, 1, 3, 2, 8, 9, 11, 10)$$

$$b = \underbrace{\bar{C}\bar{D}}_{X-NOR} + \underbrace{CD}_{OR} + \bar{B}$$

Logic Diagram

P Realise the following outputs of seven-segment decode using K-map in SOP form and make logic diagram also.

$$3 \quad c = \sum m(0, 1, 3, 4, 5, 6, 7, 8, 9) + \sum d(10, 11, 12, 13, 14, 15)$$

$$4 \quad d = \sum m(0, 2, 3, 5, 6, 8, 9) + \sum d(10, 11, 12, 13, 14, 15)$$

$$5 \quad c = \sum m(0, 2, 6, 8)$$

$$+ \sum d(10, 11, 12, 13, 14, 15)$$

, 15

$$6 \quad f = \sum m(0, 4, 5, 6, 8, 9)$$

$$+ \sum d(10, 11, 12, 13, 14, 15)$$

$$7 \quad g = \sum m(2, 3, 4, 5, 6, 8, 9)$$

$$+ \sum d(10, 11, 12, 13, 14, 15)$$

$$\text{Ans} \quad C = \bar{C} + D + B$$

$$4 \quad d = B\bar{C}D + \bar{B}\bar{D} + \bar{B}C + C\bar{D} + A$$

$$5 \quad e = (\bar{B} + C)\bar{D}$$

$$6 \quad f = A + \bar{C}\bar{D} + B(\bar{C} + \bar{D})$$

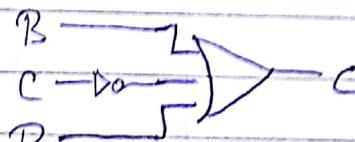
$$7 \quad g = B\bar{C} + \bar{B}C + A + C\bar{D}$$

24/03/16

Ques (2)

	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	AB
$\bar{C}\bar{D}$	00	01	11	10
$\bar{C}D$	01	11	10	01
CD	11	10	01	00
$C\bar{D}$	10	00	00	11

logic diagram



$$C = \sum m(0, 1, 4, 5, 12, 13, 8, 9) + \sum m(1, 3, 5, 7, 13, 15, 9, 11) + \sum m(4, 5, 7, 6, 12, 13, 15, 14)$$

$$C = \bar{C} + D + B$$

Ans (4)

	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	AB
$\bar{C}\bar{D}$	00	01	11	10
$\bar{C}D$	01	11	10	01
CD	11	10	01	00
$C\bar{D}$	10	00	00	11

$$d = \sum m(5, 13) + \sum m(3, 2, 10) + \sum m(2, 6, 14, 10) + \sum m(0, 2, 8, 10) + \sum m(12, 13, 15, 14, 8, 9, 11, 10)$$

$$d = B\bar{C}D + C\bar{A}\bar{B} + C\bar{D} + \bar{B}\bar{D} + A$$

Logic Diagram:

Ques (5)

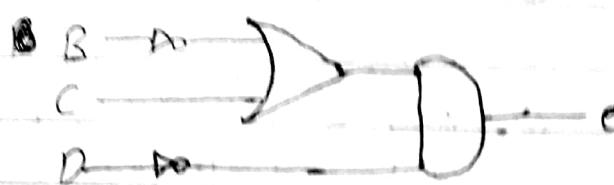
	$\bar{A}\bar{B}$	\bar{AB}	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}\bar{D}$	00	11	10	01	10
$\bar{C}D$	01	11	10	01	11
$C\bar{D}$	11	01	00	10	01
CD	10	00	11	10	00

$$e = m(0, 2, 8, 10) + m(2, 6, 14, 10)$$

$$e = \bar{B}D + \bar{C}D$$

$$e = \bar{D}(\bar{B} + C)$$

logic diagram



Ques (6)

	$\bar{A}\bar{B}$	\bar{AB}	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}\bar{D}$	00	11	10	01	10
$\bar{C}D$	01	11	10	01	11
$C\bar{D}$	11	01	00	10	01
CD	10	00	11	10	00

$$\begin{aligned}
 F &= m(0, 4) + m(4, 12, 6, 14) + m(4, 12, 5, 13) + m(12, 13, 15, \\
 &\quad 14, 8, 9, 11, 10) \\
 &= A\bar{C}\bar{D} + B\bar{D} + B\bar{C} + A \\
 &= A + C\bar{D} + B(\bar{D} + \bar{C})
 \end{aligned}$$

logic Diagram:

A(7)	AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
CD	00	01	10	11	10
$\bar{C}\bar{D}$ 00	1	1	1	0	1
$\bar{C}\bar{D}$ 01	1	1	0	1	1
$\bar{C}D$ 11	0	1	0	1	0
$C\bar{D}$ 10	1	0	1	0	0

$$\begin{aligned}
 g &= m(4, 5, 12, 13) + m(3, 2, 11, 10) + m(2, 6, 14, 10) + \\
 &\quad m(12, 13, 15, 14, 8, 9, 11, 10)
 \end{aligned}$$

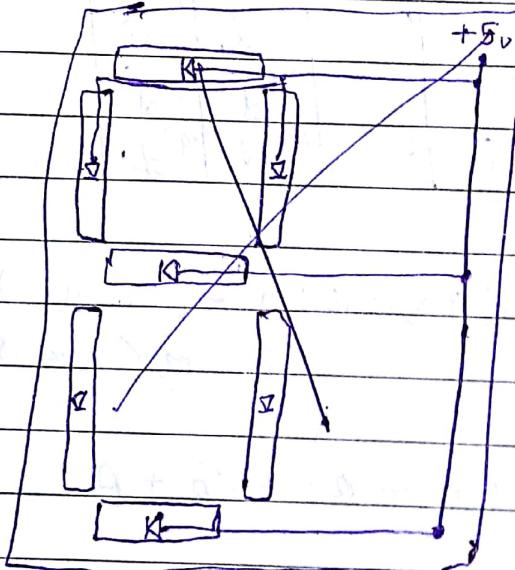
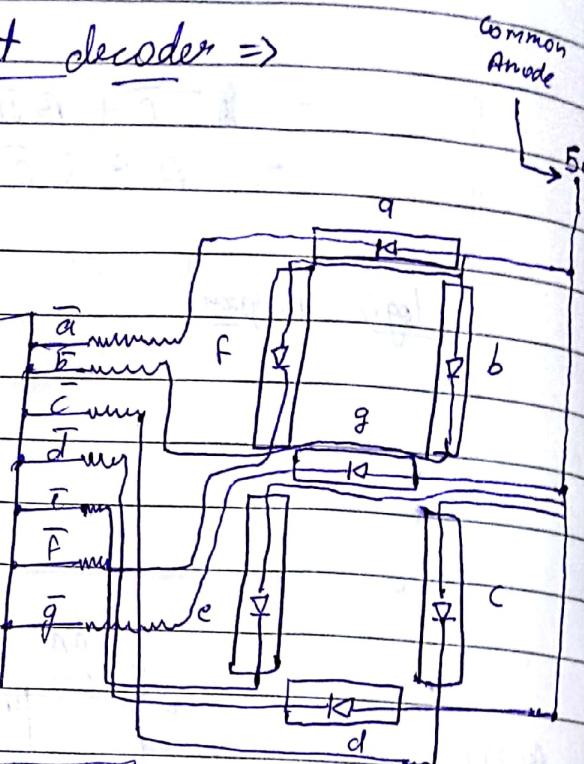
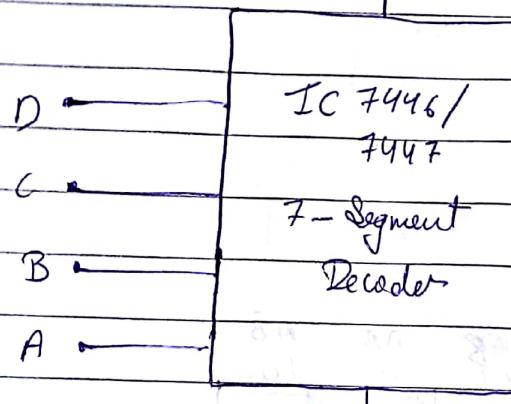
$$g = B\bar{C} + \bar{B}C + C\bar{D} + A$$

$$g = A + C\bar{D} + \bar{B}C + \bar{B}\bar{C}$$

IC 7446/7447 and 7448/7449

BCD to seven segment decoder =>

* Block diagram $+5V$ V_{CC}



Here

$\overline{D^n}$ = Diode

A, B, C, D = BCD Inputs

$\bar{a}, \bar{b}, \dots, \bar{g}$ = Outputs

$\overline{\equiv}$ = Grounded

V_{CC} = Power Supply

$m_m = R_s = \text{current control resistance}$

Imp. facts :-

1. In IC - 7446/7447 7-Segment decoder outputs are active low.
 2. Diodes of all 7-segment display are forward biased
- means p-type S.C. is connected with common anode ($+5_v$)
 → means n-type S.C. is connected with active low signal
3. If we will make block diagram of IC 7448/7449 7-segment display then we have to connect p-type S.C. to common cathode and outputs to active type high signals.

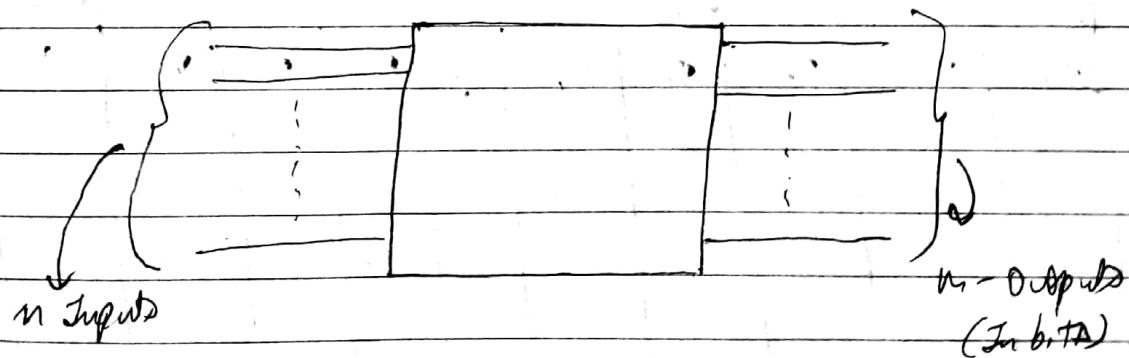
($\bar{g} \rightarrow g$)

⋮

($\bar{g} \rightarrow g$)

Encoder →

* Block diagram

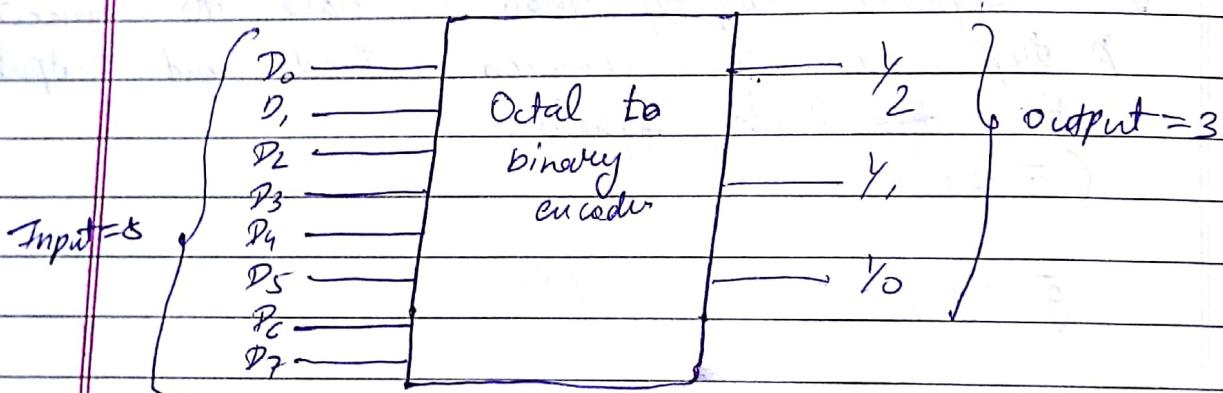


An Encoder is a digital circuits that performs the inverse operation of a decoder. So the process opposite of the decoding is called encoding.

Encoder is a combinational logic circuit that converts an active input signal into a coded output signal.

1 Octal to Binary ~~Encoder~~ \Rightarrow
(e:3) Encoder

* Block diagram



* Truth Table

	Input								Output		
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y_2	Y_1	Y_0
0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	0	0	0	1
3	0	0	0	1	0	0	0	0	0	1	0
4	0	0	0	0	1	0	0	0	1	0	1
5	0	0	0	0	0	1	0	0	0	1	0
6	0	0	0	0	0	0	1	0	1	0	0
7	0	0	0	0	0	0	0	1	1	0	0

5	0	0	0	0	0	1	0	0	1	0	1
6	0	0	0	0	0	0	1	0	1	1	0
7	0	0	0	0	0	0	0	1	1	1	1

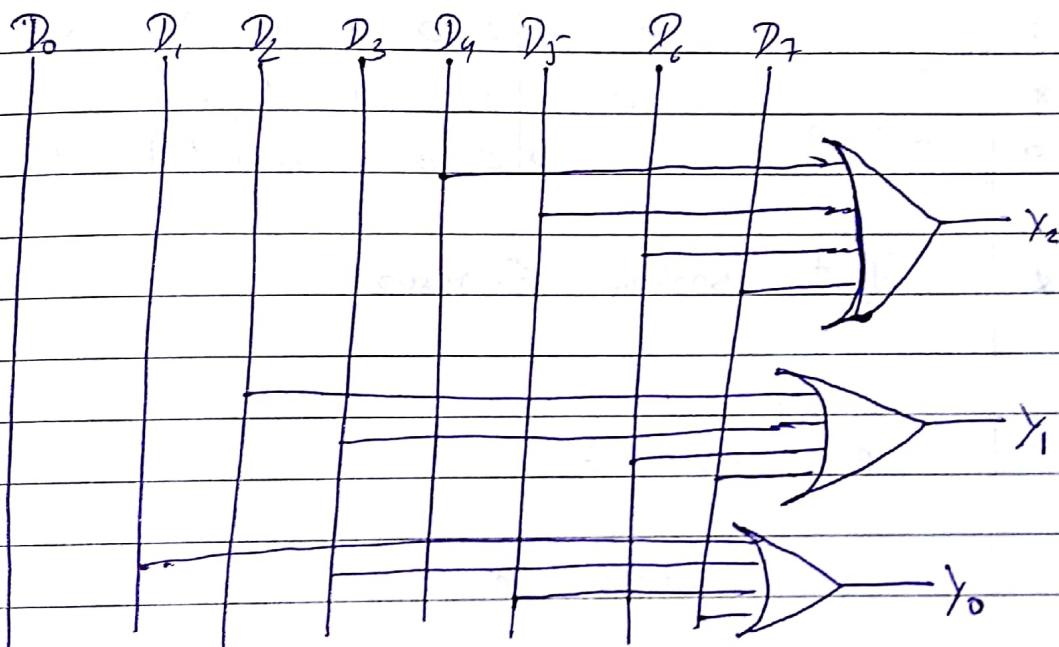
* Logic Expression

$$Y_2 = D_4 + D_5 + D_6 + D_7$$

$$Y_3 = D_2 + D_3 + D_6 + D_7$$

$$Y_0 = D_1 + D_3 + D_5 + D_7$$

* Logic Diagram



Decimal to BCD Encoder \Rightarrow

* Truth Table

Inputs										BCD outputs			
0	1	2	3	4	5	6	7	8	9	A	B	C	D
0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	0	0	0	0	1	0
3	0	0	0	1	0	0	0	0	0	0	0	0	1
4	0	0	0	0	1	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	0	0	0	1	0	1
6	0	0	0	0	0	0	1	0	0	0	1	1	0
7	0	0	0	0	0	0	0	1	0	0	0	1	1
8	0	0	0	0	0	0	0	0	1	0	1	0	0
9	0	0	0	0	0	0	0	0	1	1	0	0	1

* Output Boolean Expression

$$A = 8 + 9$$

$$B = 4 + 5 + C + 7$$

$$C = 2 + 3 + 6 + 7$$

$$D = 1 + 3 + 5 + 7 + 9$$

Priority Encoder \Rightarrow It is a type of encoder which priority function is included

- If the operation two or more inputs are equal to 1 at the same time, that input having highest priority will take precedence

Truth Table

D_0	Inputs			Outputs			V
	D_1	D_2	D_3	y_2	y_1	y_0	
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0
x	1	0	0	0	0	0	1
x	x	1	0	0	1	0	1
x	x	x	1	1	1	1	1

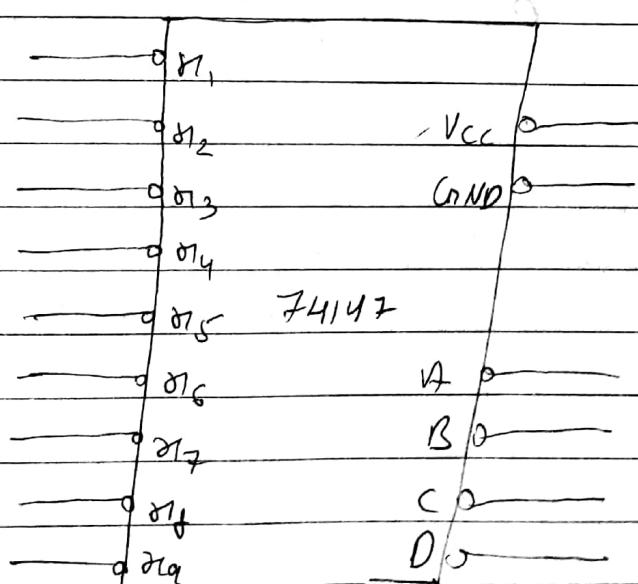
Here V is valid output indicator

If $d_0/d_1/d_2/d_3 = 1 \Rightarrow V=1$

If there is no 1 in input $\Rightarrow V=0$

Priority

Decimal $8 \rightarrow 3$ BCD Encoder (IC 74147)

Logic Symbol

* Truth Table \Rightarrow

	Input									Output			
	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	A	B	C	D
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	x	x	x	x	x	x	x	x	0	0	1	1	0
2	x	x	x	x	x	x	x	0	1	0	1	1	1
3	x	x	x	x	x	x	0	1	1	1	0	0	0
4	x	x	x	x	x	0	1	1	1	1	0	0	1
5	x	x	x	x	0	1	1	1	1	1	0	1	1
6	x	x	x	0	1	1	1	1	1	1	1	0	0
7	x	x	0	1	1	1	1	1	1	1	1	1	0
8	0	1	1	1	1	1	1	1	1	1	1	1	0
9	0	1	1	1	1	1	1	1	1	1	1	1	0

$x_1 \text{ to } x_9 = \text{Input}$

$A, B, C, D = BCD \text{ output}$

GND = Grounded

$V_{cc} = \text{Power supply}$

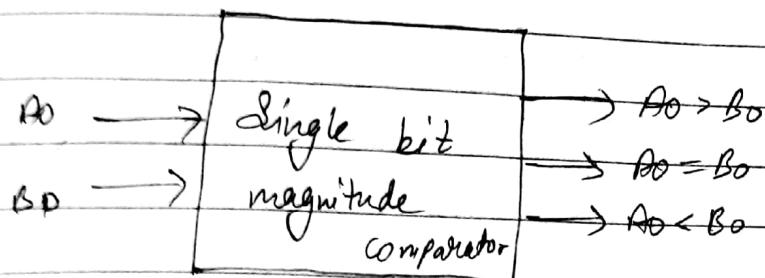
0 = Using 1 at the place of 0 and
Opposite

Q If in ^{given} _{active} truth table x_3, x_5, x_7 inputs are low then what will be BCD output

B $x_7 = 1000$

11. Magnitude comparator \Rightarrow Magnitude comparator is a combinational circuit that compares the magnitude of two no's (A and B) and generates one of the following outputs.

* Block diagram



- 1 $A = B$ } outputs
- 2 $A > B$
- 3 $A < B$

* Here we are using two gates for these operations

1. ~~so~~ AND gate for

$$(a) A > B \quad \begin{array}{c} A_0 \\ B_1 \end{array} \rightarrow D \quad y = A_0 > B_0$$

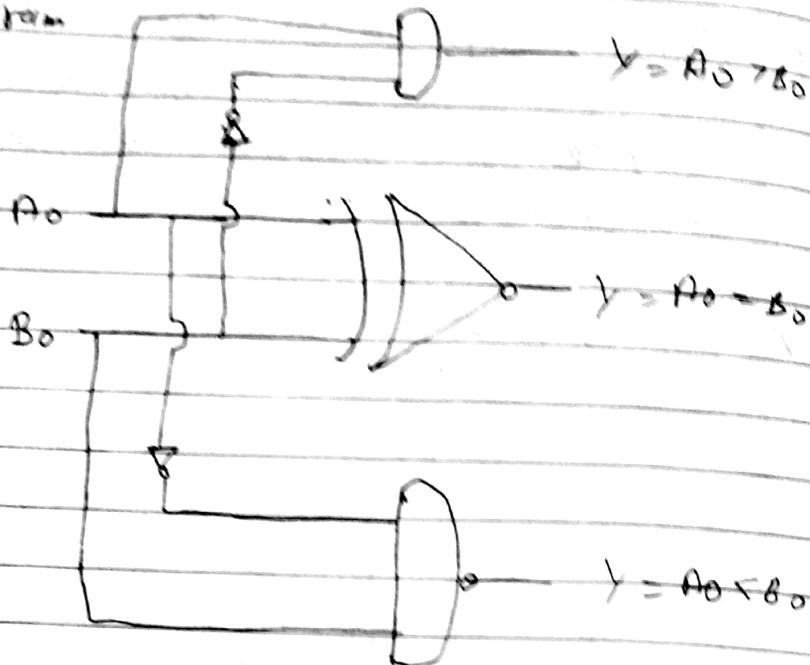
$$(b) A < B \quad \begin{array}{c} A_0 \\ B_1 \end{array} \rightarrow D \quad y = A_0 < B_0$$

~~1 0 1 0~~ $y =$

2. Ex-NOR gate for
 $A = B$

$$A_0 \rightarrow \text{Ex-NOR gate} \rightarrow y = \overline{A_0 B_0} + \overline{A_0 B_0}$$

* logic Diagram

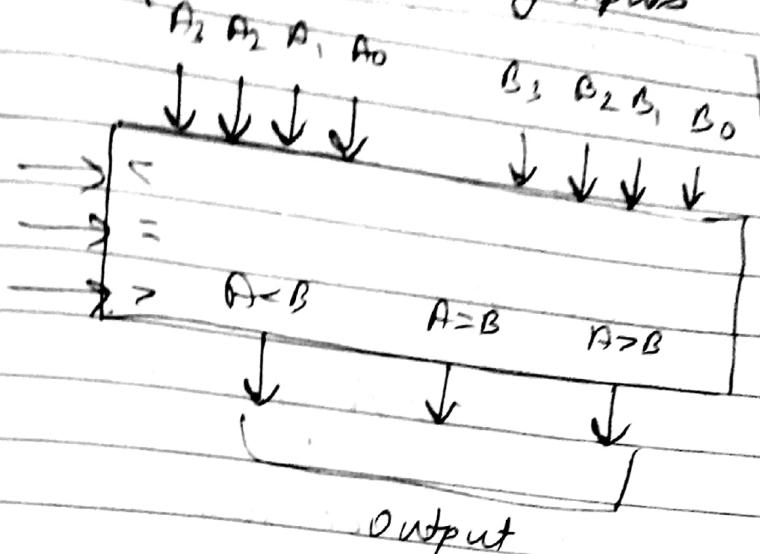


IC - 7485 4-bit Magnitude comparator =>

* Truth Table

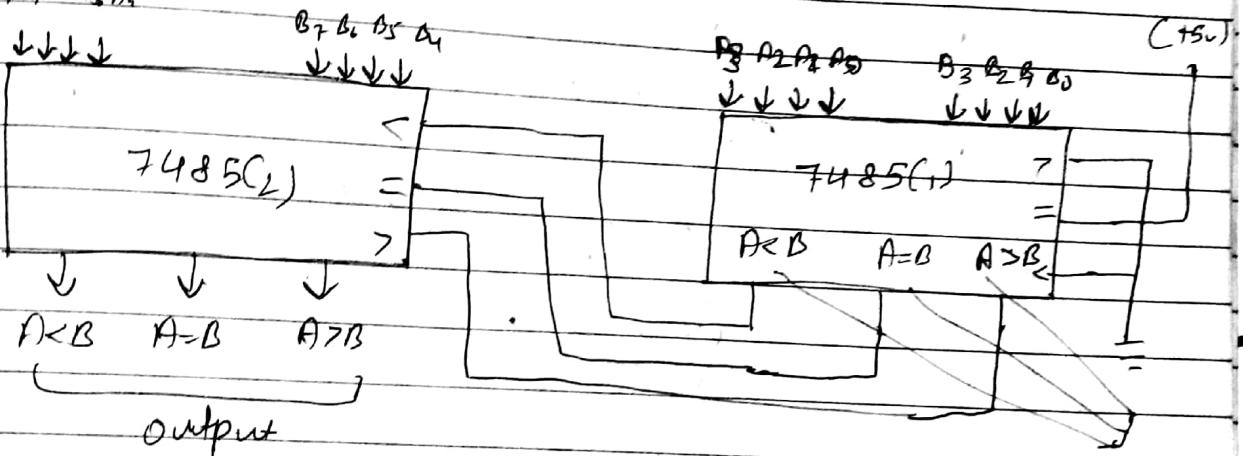
Comparing input				Cascading input			Output		
$A_3 B_3$	$A_2 B_2$	$A_1 B_1$	$A_0 B_0$	$A > B$	$A < B$	$A = B$	$A > B$	$A \leq B$	$A = B$
$A_3 > B_3$	X	X	X	X	X	X	1	0	0
$A_3 < B_3$	X	X	X	X	X	X	0	1	0
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	1	0	0
"	$A_2 < B_2$	X	X	X	X	X	0	1	0
"	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	1	0	0
"	"	$A_1 < B_1$	X	X	X	X	0	1	0
"	"	$A_1 = B_1$, $A_0 > B_0$	X	X	X	X	1	0	0
"	"	"	$A_0 < B_0$	X	X	X	0	1	0
$A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$, $A_0 = B_0$	X	X	X	1	0	0	0	1	0
"	"	"	"	0	1	0	0	0	1
"	"	"	"	0	0	1	1	0	1

Logic symbol Selecting inputs



ascending of Ic-7485

$A_7 A_6 A_5 \alpha$



* Parity generator; Parity Checker.

Parity Checker \rightarrow It's a combinational circuit which is used to check the parity of any binary number

② Here we have two types of poverty:-

(a) Even parity (b) odd parity

③ Exhibit a binary number

$$\begin{array}{r} 1001 \\ \text{MSB} = 1 \end{array}$$

So parity is equals to odd

(ii) Let's another binary no.

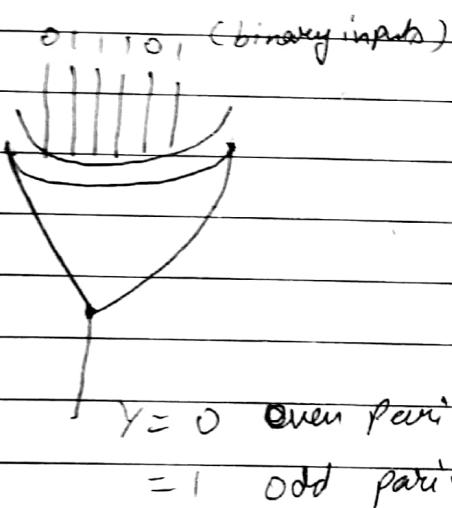
$$01110$$

MSB = 0 \Rightarrow Parity = even

④ Here Ex-OR gate will be used to check the parity -

(a) If output of Ex-OR = 1 \Rightarrow Odd parity

(b) If output of Ex-OR = 0 \Rightarrow Even parity



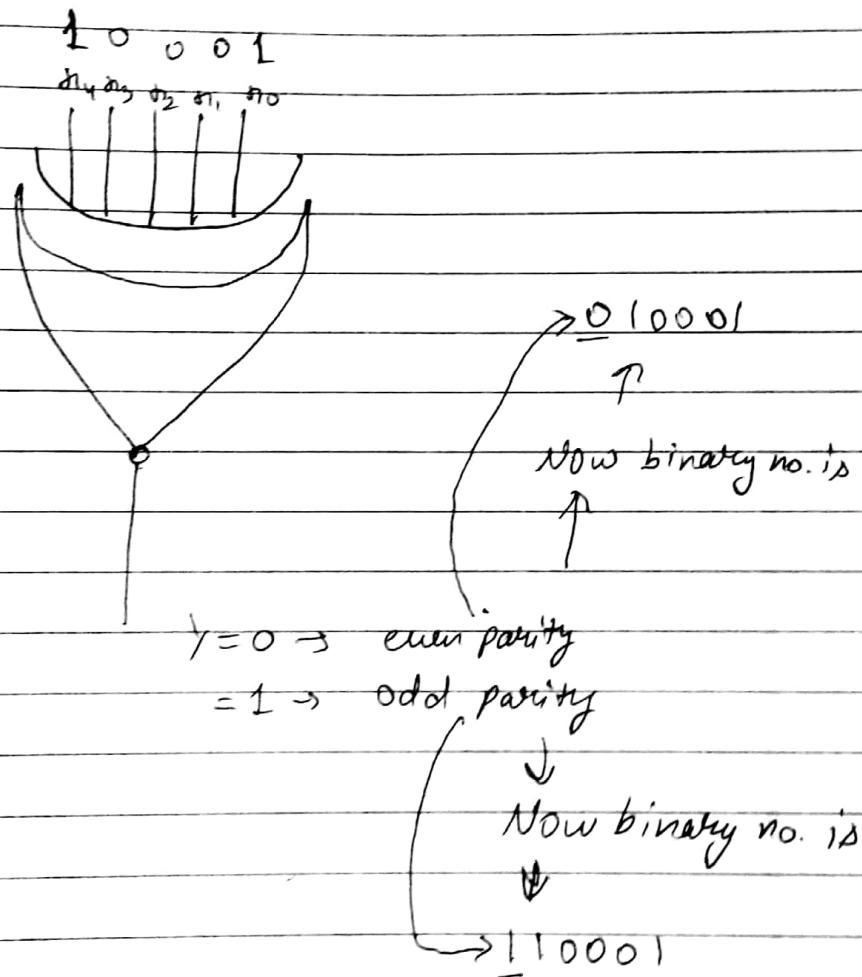
Parity Generation

* A combinational circuit which is useful to generate parity for any binary number

This is called parity generator.

Here we will use EX-NOR gate to generate parity. -

- If output of EX-NOR = 0 then generated parity is equal to even.
- If output = 1, generated parity = odd.



~~Exist~~