

# DIGITAL PHYSICS

The Universe Is a Programmed System



## Chapter

# 4

# Logic Families

### 4.1 INTRODUCTION

Logic gates and memory devices are fabricated as *integrated circuits* (ICs) because the components used such as resistors, diodes, bipolar junction transistors and the insulated gate or metal-oxide semiconductor field-effect transistors are the integral parts of the chip. The various components are interconnected within the chip to form an electronic circuit during assembly. The ICs result in an increase in reliability and a reduction in weight and size.

Small Scale Integration (SSI) refers to ICs with fewer than 10 gates on the same chip. Medium Scale Integration (MSI) includes 12 to 100 gates per chip. Large Scale Integration (LSI) refers to more than 100 upto 5000 gates per chip. Very Large Scale Integration (VLSI) devices contain several thousand gates per chip.

Integrated circuits are classified into two general categories: (i) *Linear* and (ii) *Digital*. Linear integrated circuits operate with continuous signals and are used to construct electronic circuits such as amplifiers, voltage comparators, etc. Digital integrated circuits operate with binary signals and are invariably constructed with integrated circuits.

### 4.2 DIGITAL INTEGRATED CIRCUITS

The various logic families can be placed into two broad categories according to the IC fabrication process: (i) Bipolar and (ii) Metal-oxide semiconductor (MOS).

ICs come in the following types of packages:

- (i) Dual-in-Line Package (DIP)
- (ii) Leadless Chip Carrier (LCC)
- (iii) Plastic Leaded Chip Carrier (PLCC)
- (iv) Plastic Quad Flat Pack (PQFP) and
- (v) Pin Grid Array (PGA)

#### 4.2.1 Bipolar Logic Families

The important elements of a bipolar IC are resistors, transistors and diodes (varactor diodes used as capacitors). Based on the two main operations of bipolar ICs, i.e., saturated and non-saturated, bipolar families are classified into

- (i) saturated logic and
- (ii) non-saturated logic.

The following are the saturated bipolar logic families:

- ✓ 1. Resistor-Transistor Logic (RTL)
- 2. Direct-coupled Transistor Logic (DCTL)
- ✓ 3. Diode-Transistor Logic (DTL)
- 4. High Threshold Logic (HTL)
- ✓ 5. Transistor-Transistor Logic (TTL)
- 6. Integrated-injection Logic ( $I^2L$ )

The following are the non-saturated logic families:

- ✓ 1. Schottky TTL
- ✓ 2. Emitter-coupled Logic (ECL)

### 4.2.2 MOS Families

The MOS families include

- 1. PMOS  $p$ -channel MOSFETs
- 2. NMOS  $n$ -channel MOSFETs
- 3. CMOS Complementary MOSFETs

### 4.3 CHARACTERISTICS OF DIGITAL ICs

Some of the important parameters or properties of various logic families are listed as follows:

- 1. Speed of operation (Propagation delays)
- 2. Power dissipation
- 3. Fan-in
- 4. Fan-out
- 5. Noise immunity
- 6. Operating temperature
- 7. Power supply requirements

The comparison of performance of digital ICs may be made with reference to the above properties.

#### 4.3.1 Speed of Operation

The speed of operation of an IC is expressed in terms of propagation delay. *Propagation delay* is defined as the time taken for the output of a gate to change after the inputs have changed.

A logic signal always experiences a delay in going through a circuit. The two propagation delay times shown in Fig. 4.1 are defined as follows:

$t_{PLH}$ : It is the propagation delay time in going from logical LOW (0 state) to logical HIGH (1 state).

It is the average transition delay time for the signal to propagate from input to output when the signals change in values i.e.

$t_{PHL}$ : It is the propagation delay time in going from logical HIGH (1 state) to logical LOW (0 state).

It is evident that  $t_{PHL}$  is the delay in the output response as it goes from LOW state to a HIGH state, and vice versa for  $t_{PLH}$ . The delay times are measured between the 50% voltage levels of the input and output waveforms. In general, the two delays  $t_{PHL}$  and  $t_{PLH}$  are not necessarily equal and will vary depending on load conditions. The values of propagation times are a measure of the relative speed of logic circuits. The average of the above two propagation delays  $(t_{PLH} + t_{PHL})/2$  is called the average propagation delay and is used to rate the circuit. It is a function of the switching time of the individual transistors or MOSFETs in the circuit.

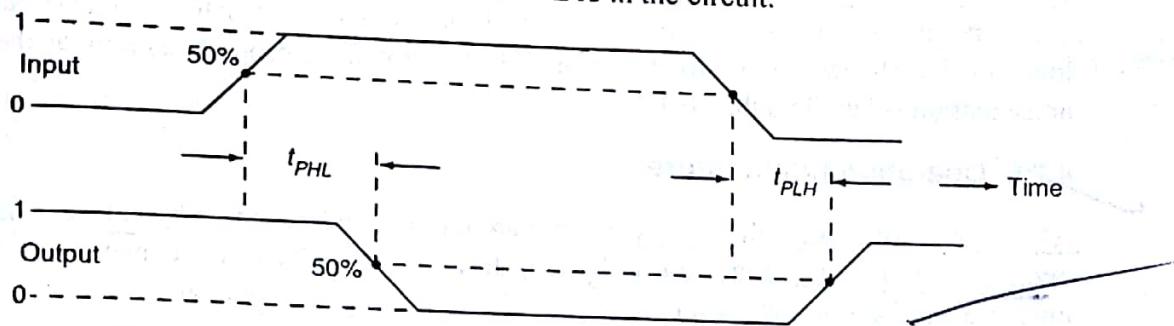


Fig. 4.1 Propagation delays

#### 4.3.2 Power Dissipation

V ~~x~~ (mean I)

DC Volt.

Power dissipation is a measure of the power consumed by the logic gate when fully driven by all its inputs, and it is expressed in milliwatts or nanowatts. The d.c. or average power dissipation is the product of d.c. supply voltage and the mean current taken from that supply. It is a measure of power consumed.

#### 4.3.3 Fan-in by the gate when fully driven by all inputs

The fan-in of a gate is the number of inputs connected to the gate without any degradation in the voltage levels. For example, an eight-input gate requires one Unit Load (UL) per input. Its fan-in is 8. This parameter determines the functional capabilities of a logic circuit.

The no of inputs connected to the gate

#### 4.3.4 Fan-out without any degradation in the voltage level

Fan-out is the maximum number of similar logic gates that a gate can drive without any degradation in voltage levels. Very often a gate will drive several other gates. Each driven gate requires a certain current which must be supplied by the driving gate. The driving gate must be capable of supplying this current while maintaining the required voltage level. In part, this is a function of the output impedance of the driving gate and the input impedance of the driven gates. Usually, in a given logic family, gates drive others of the same type. If their output impedance is low while their input impedance is high, then one gate can often drive many others.

It specifies the no. of standard loads that the output of the gate can drive without impairment of its normal operation

Maximum noise voltage added to an input signal of a digital circuit that don't cause an undesirable change in a circuit output expressed in  $\text{volts}$ .

### 4.3.5 Noise Immunity or Noise Margin

The term noise denotes an unwanted signal voltage, e.g., hum, transients and glitches.

Noise can sometimes cause the input voltage of a logic gate to drop below  $V_{\text{H}}^{\text{(min)}}$  or rise above  $V_{\text{L}}^{\text{(max)}}$ , which leads to unreliable operation. *Noise immunity* is the maximum noise voltage that may appear at the input of a logic gate without changing the logical state of its output. A quantitative measure of noise immunity is called *noise margin*.

The difference between the operating input-logic voltage level and the threshold voltage is called the *noise margin of the circuit*. The manufacturer usually quotes the noise margin, which refers to the amplitude of the noise voltage that may cause the logic level to change. In the worst case, a TTL gate functions properly as long as the noise margin is kept less than 0.4V.

### 4.3.6 Operating Temperature

All IC gates are semiconductor devices that are temperature-sensitive by nature. The operating temperature ranges for an IC vary from  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for consumer and industrial applications and from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for military applications.

### 4.3.7 Power Supply Requirements

The amount of power and supply voltage required by an IC are the main parameters to be taken into consideration while choosing a proper power supply.

### 4.3.8 Current and Voltage Parameters

The following currents and voltages are very important in designing digital systems. The values given below are for TTL gates only.

**High-level input voltage ( $V_{\text{H}}$ ) [ $V_{\text{in}(1)}$ ]** It is the minimum voltage level required for a logical 1 at an input. Its minimum value is 2V.

**Low-level input voltage ( $V_{\text{L}}$ ) [ $V_{\text{in}(0)}$ ]** It is the maximum input voltage required for a logical 0 (LOW) at an input. Its maximum value is 0.8V.

**High-level output voltage ( $V_{\text{OH}}$ ) [ $V_{\text{out}(1)}$ ]** It is the minimum voltage required for a logical 1 state at the output. Its minimum value is 2.4V.

**Low-level output voltage ( $V_{\text{OL}}$ ) [ $V_{\text{out}(0)}$ ]** It is the maximum voltage available at the circuit's output corresponding to the logical 0 state. Its maximum value is 0.4V.

**High-level input current ( $I_{\text{H}}$ ) [ $I_{\text{in}(1)}$ ]** The current that flows through an input when a specified high-level voltage is applied to that input.

**Low-level input current ( $I_{\text{L}}$ ) [ $I_{\text{in}(0)}$ ]** The current that flows through an input when a specified low-level voltage is applied to that input.

**High-level output current ( $I_{\text{OH}}$ ) [ $I_{\text{out}(1)}$ ]** The current that flows from an output in the logical 1 state under specified load conditions.

**Low-level output current ( $I_{\text{OL}}$ ) [ $I_{\text{out}(0)}$ ]** The current that flows from an output in the logical 0 state under specified load conditions.

#### 4.4 CURRENT-SOURCING AND CURRENT-SINKING LOGIC

Logic families can be categorised depending upon the flow of current from the output of one logic circuit to the input of another. Current-sourcing and current-sinking logic gates are illustrated in Fig. 4.2(a) and (b) respectively.

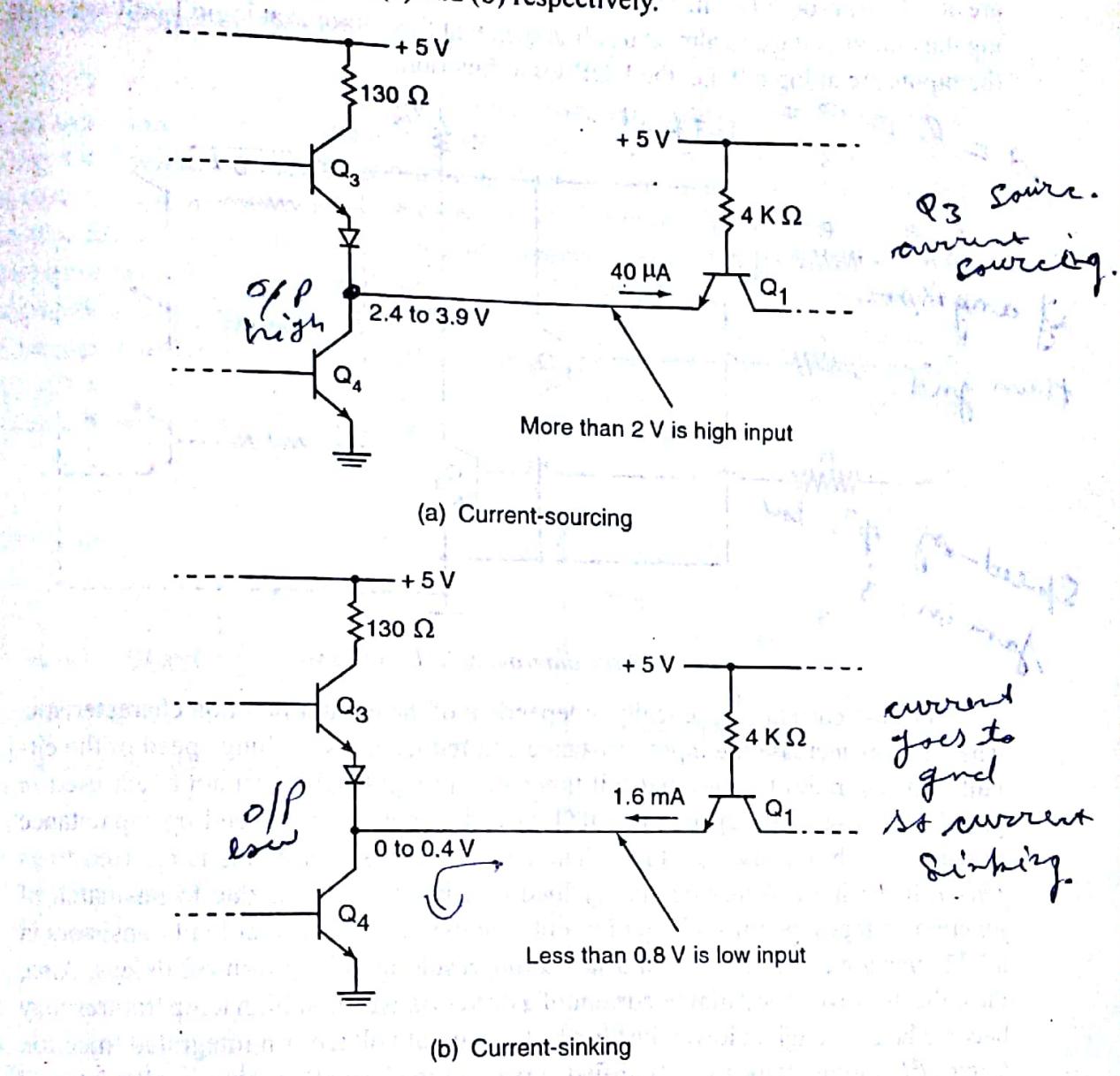


Fig. 4.2

When a standard TTL gate output is HIGH as shown in Fig. 4.2(a), a reverse emitter current of 40 mA flows from transistor Q<sub>3</sub> of driver gate to the emitter of transistor Q<sub>1</sub> of load gate, and hence Q<sub>3</sub> acts as a *current source*.

When a standard TTL gate output is LOW as shown in Fig. 4.2(b), an emitter current of 1.6 mA flows from the emitter of transistor Q<sub>1</sub> of load gate to the collector of transistor Q<sub>4</sub> of driver gate. As Q<sub>4</sub> is saturated, current flows through it to the ground, and hence Q<sub>4</sub> acts as a *current sink*.

#### 4.5 RESISTOR-TRANSISTOR LOGIC (RTL)

The basic diagram of an RTL NOR gate consisting of resistors and transistors is shown in Fig. 4.3. When the inputs  $A$ ,  $B$  and  $C$  are at 0V (or logic 0), the transistors are turned OFF. Hence the output goes to  $+V_{cc}$ , i.e., logic 1. If either one or all input terminals are at  $+V_{cc}$  (or logic 1), one transistor or all would be fully turned ON, thereby reducing the output voltage to almost 0V. It is seen that the output is at logic 1 only when all the inputs are at logic 0, i.e. the NOR logic function.

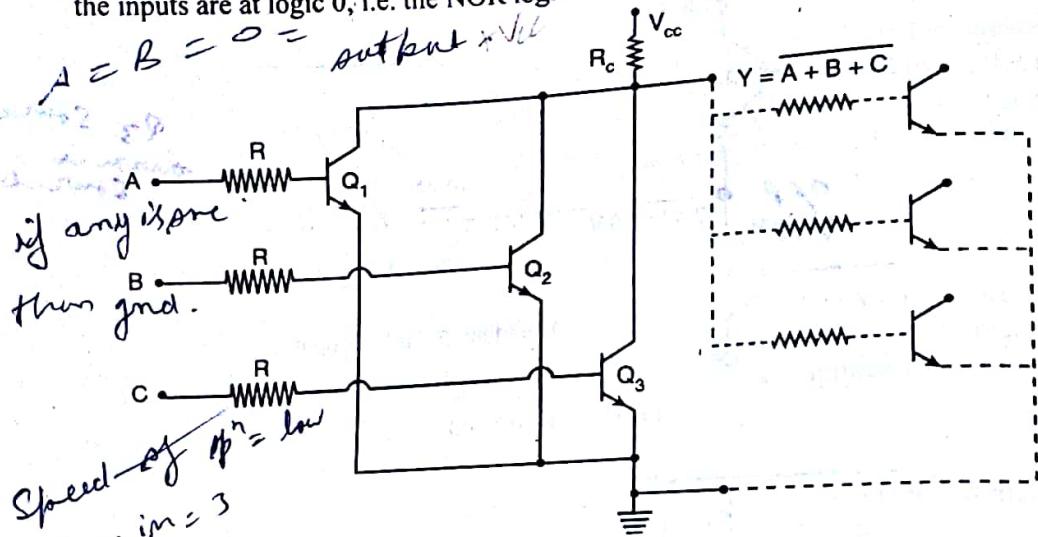


Fig. 4.3 Basic diagram of RTL NOR gate

The base current is practically independent of the emitter junction characteristic. The resistors increase the input resistance and reduce the switching speed of the circuit. This degrades the rise and fall times of any input pulse. An approach used in practice to increase the speed of an RTL circuit is to connect a speed-up capacitance in parallel with the base resistance. The number of input terminals is referred to as *fan-in*. Reducing current-hogging by load transistors, which is due to mismatch of junction voltages, permits a larger fan-out. Another problem is that load transistors in a RTL gate are driven heavily into saturation, resulting in long turn-off delays. Also, the collector reverse saturation current of a driver transistor at high temperatures may become large enough to lower the already low output voltage. An Integrated Injection Logic (*I<sup>2</sup>L*) circuit, which is a modified version of the basic RTL circuit, alleviates all these problems.

The following are the characteristics of the RTL family.

- Speed of operation is low, i.e., the propagation delay is of the order of 500 ns; it cannot operate at speeds above 4 MHz.
- Fan-out is 4 or 5 with a switching delay of 50 ns, and fan-in is 4.
- Poor noise immunity.
- High average power dissipation. Elimination of base resistors in RTL will reduce the power dissipation which results in Direct-coupled Transistor Logic (DCTL).

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- (e) The noise margin from zero to the threshold voltage is about 0.5V, and from one to the threshold voltage is only 0.2V.
- (f) Sensitive to temperature.

The RTL family of ICs includes NOR gates with two, three or four inputs, flip-flops and four-bit shift registers.

## 4.6 RESISTOR-CAPACITOR-TRANSISTOR LOGIC (RCTL)

The RCTL circuit employs a capacitor in parallel with an input resistor to increase the speed and to improve noise immunity. The basic circuit of a RCTL NOR gate is shown in Fig. 4.4. During the transient, the capacitor bypasses the resistor, with the result that the base currents grow and the input capacitance discharges more quickly. The use of the capacitor also allows higher values of resistance, making possible lower power dissipation per gate. In comparison with the RTL family, the RCTL circuits have low propagation delay time  $t_{pd}$ , ranging from 10 to 15 ns, although having the same values of fan-out and fan-in. In RCTL circuit, manufacturing of PN junction capacitor is difficult and also occupies larger area. The RCTL circuit is not ideal for fabrication because it includes a high proportion of resistors and capacitors.

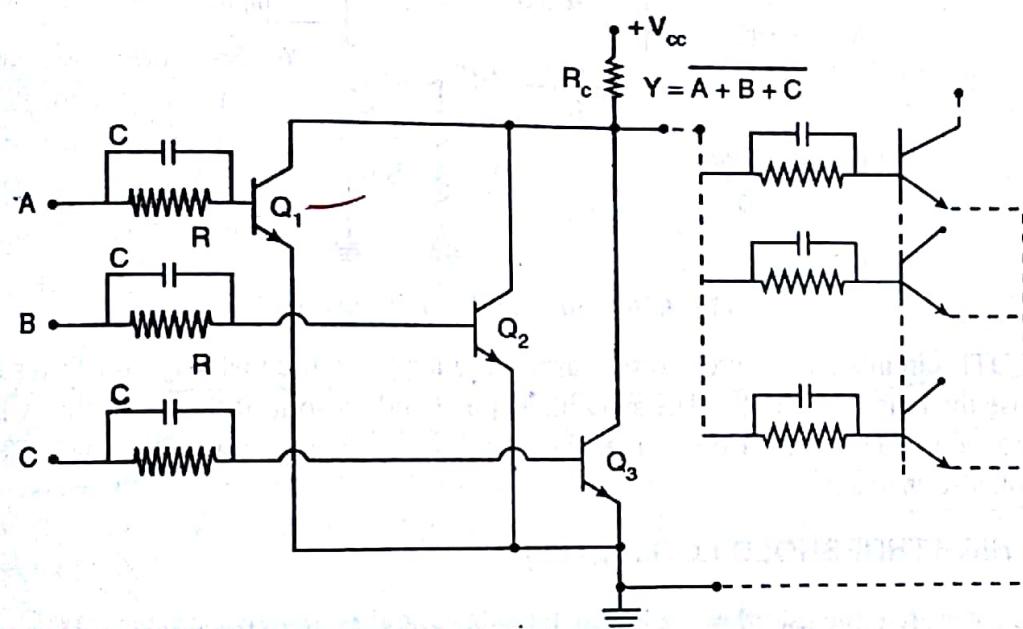


Fig. 4.4 Basic circuit of RCTL NOR gate

## 4.7 DIODE-TRANSISTOR LOGIC (DTL)

The DTL family eliminates the problem of decreasing output voltage with increasing load. The basic circuit of a DTL NAND gate is shown in Fig. 4.5(a). Two diodes in this circuit,  $D_A$  and  $D_B$ , perform the logic AND operation followed by a transistor which results in a NAND gate. When both the inputs are at logic HIGH level, diodes  $D_1$  and  $D_2$  are reverse-biased. Diodes  $D_1$  and  $D_2$  and transistor are the diodes  $D_A$  and  $D_B$  are reverse-biased. Diodes  $D_1$  and  $D_2$  and transistor are switched ON and hence the output is LOW. The additional diode  $D_2$  increases the noise margin. If any of the inputs drops to ground potential (logic 0), the correspond-

ing input diode will conduct, and current will flow through the diode and  $R_D$ , causing a voltage drop at the input of the diode  $D_1$ . The base voltage becomes low and the transistor remains cut off and hence the output is HIGH.

The DTL family has the following characteristics.

**Propagation delay** The turn-off delay is considerably larger than the turn-on delay, often by a factor of 2 or 3. The propagation delay of DTL is 25 ns.

**Fan-out** A fan-out as high as 8 is possible with the DTL family because of the high input impedance of the subsequent gates in the logic 1 state.

**Fan-in** It has a fan-in of 8.

**Noise immunity** The noise margin is high due to the additional diode ( $D_2$ ) connected in series with  $D_1$ . The noise margin of the DTL NAND gate circuit shown in Fig. 4.5(a) is 0.8V when the output is low and 3.4V when the output is high.

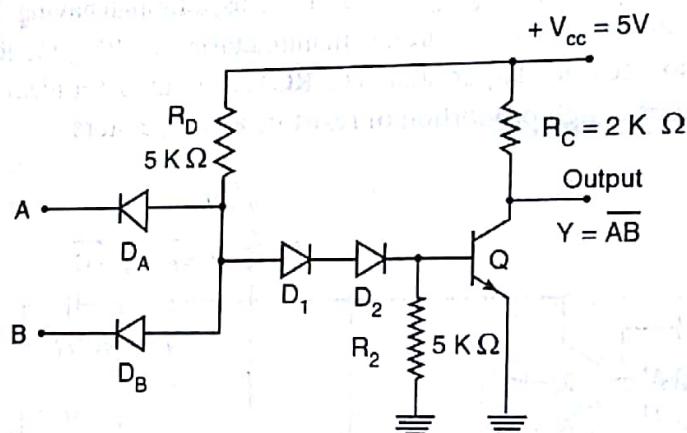


Fig. 4.5(a) Basic DTL NAND gate

DTL circuits have better noise margin, higher fan-out capability and faster response than the RTL family. The switching speed and fan-out of the DTL family are improved in TTL family. However, as the switching speed increases, the power dissipation also increases.

#### 4.8 HIGH THRESHOLD LOGIC (HTL)

HTL gates are quite useful in the industrial environment where the noise level is usually high due to the presence of motors, high voltage switches, etc. A HTL NAND gate can be derived from an ordinary DTL NAND gate by replacing diode  $D_2$  by a 6.9V Zener diode and using a higher supply voltage (+15V instead of 5V) as shown in Fig. 4.5(b). The resistor values are also increased so that the same currents are obtained in both ordinary DTL and HTL NAND gates. Because of the use of 6.9V Zener diode, the noise margin of this circuit is increased to 7V.

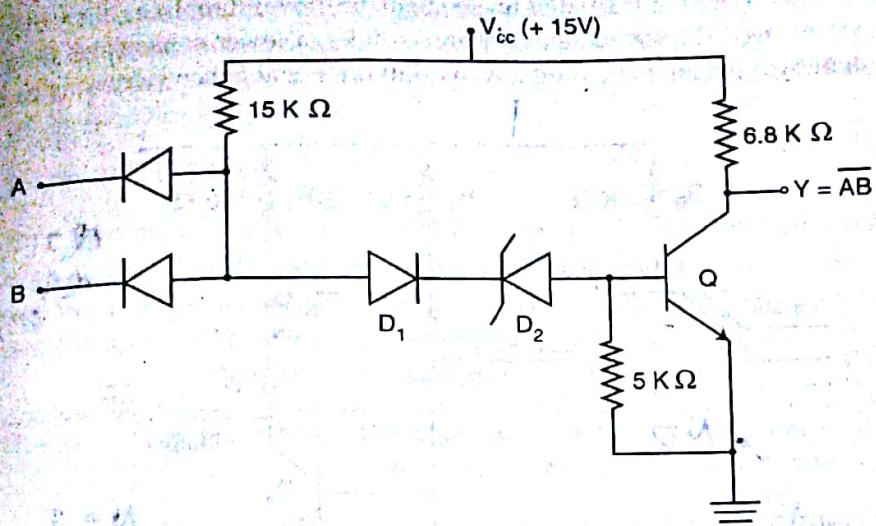


Fig. 4.5(b) Basic TTL NAND gate

#### 4.9 TRANSISTOR-TRANSISTOR LOGIC (TTL or T<sup>2</sup>L)

The most commonly used saturating logic family called the Transistor-Transistor Logic, (TTL or T<sup>2</sup>L), has the fastest switching speed when compared to other logic families that utilize saturated transistors. The series 54/74 TTL family has grown and evolved into five major divisions:

- (i) standard (SN 54/74)
- (ii) high-speed (SN54H/74H)
- (iii) low-power (SN54L/74L)
- (iv) schottky-diode-clamped (SN54S/74S)
- (v) low power schottky. (SN54LS/74LS)

Although the high-speed and low-power series were designed for specific applications, all four families are compatible and are capable of interfacing directly with one another.

They have the following typical characteristics in common:

- (i) Supply voltage : 5.0V
- (ii) Logical 0 output voltage : 0V to 0.4V
- (iii) Logical 1 output voltage : 2.4V to 5V
- (iv) Logical 0 input voltage : 0V to 0.8V
- (v) Logical 1 input voltage : 2V to 5V
- (vi) Noise immunity : 0.4V

##### 4.9.1 TTL NAND Gate

The basic circuit for the TTL logic family is the NAND gate. The TTL circuit uses a special single multi-emitter transistor that is fabricated with several emitters at its input. The number of emitters used depends on the desired fan-in of the circuit. Since

a multi-emitter transistor is smaller in area than the diodes it replaces, the yield from a wafer is increased. Moreover, smaller area results in lower capacitance to the substrate, thereby reducing the circuit rise and fall times and hence increasing its speed.

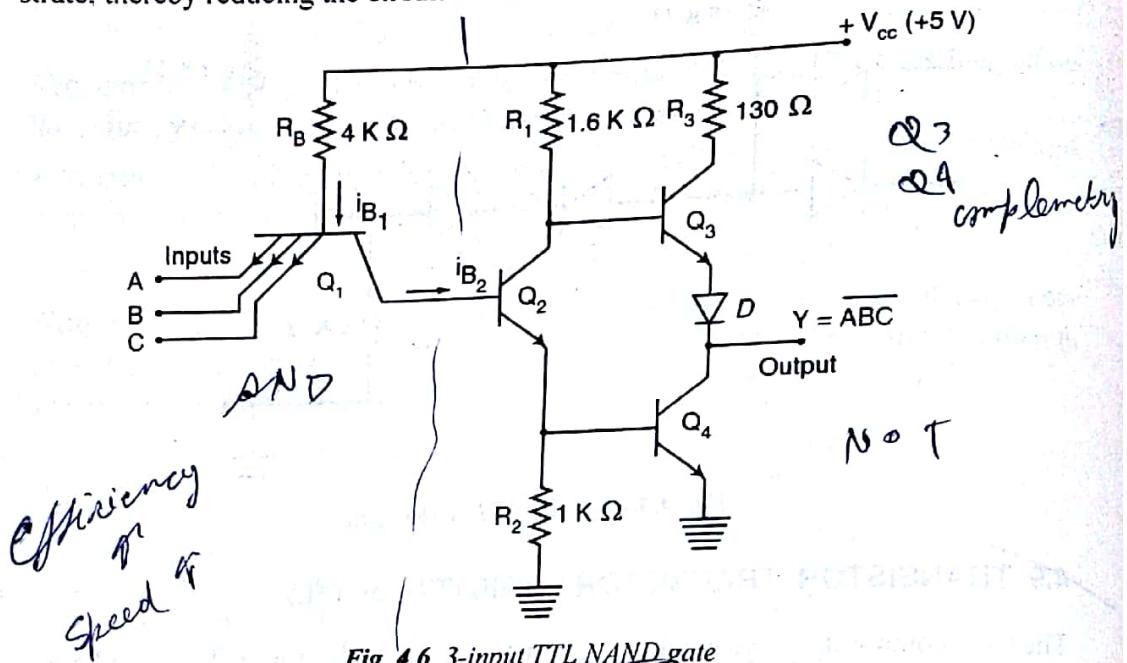


Fig. 4.6 3-input TTL NAND gate

**Circuit operation** The basic circuit of the TTL NAND gate is shown in Fig. 4.6. The output is taken from the collector of transistor  $Q_4$ . Each emitter of  $Q_1$  acts like a diode. Therefore, transistor  $Q_1$  and the  $4\text{k}\Omega$  resistor act like a 3-input AND gate and the rest of the circuit inverts the signal. Hence, the overall circuit acts like a 3-input NAND gate.

When either or all inputs ( $A$ ,  $B$  and  $C$ ) are at  $0\text{V}$  (logic 0), the corresponding emitter-base junction of  $Q_1$  becomes forward-biased. The value of  $R_B$  is selected so as to ensure that  $Q_1$  is turned ON. However, the value of current  $i_{B_2}$  flowing through the base of  $Q_2$  reduces the potential at the base of  $Q_2$ , and hence transistors  $Q_2$  and  $Q_4$  are cutoff so that the output voltage is at  $V_{cc}$  (logic 1).

If all the inputs are high (logic 1), the emitter-base junction of  $Q_1$  is reverse-biased so that it has no base current. Hence,  $Q_1$  is OFF. However, its collector-base junction is forward-biased supplying base current  $i_{B_2}$  to  $Q_2$ . The current  $i_{B_2}$  will be sufficiently large to saturate  $Q_2$ . As a result, transistor  $Q_2$  is turned ON and the drop across  $R_2$  is sufficient to forward bias the base-emitter junction of  $Q_4$ , thereby turning  $Q_4$  ON. Hence, the output at its collector is low (logic 0). The function of diode  $D$  is to prevent both  $Q_3$  and  $Q_4$  from being ON simultaneously.

In the absence of diode  $D$ , the transistor  $Q_3$  will conduct slightly when the output is LOW. In order to prevent this, the diode is connected between the emitter of  $Q_3$  and the collector of  $Q_4$ . The voltage drop across the diode keeps the base-emitter junction of  $Q_3$  reverse-biased. In this way, transistor  $Q_4$  only conducts when the output is LOW, which confirms the conditions for NAND operation.

As TTL input circuits require higher drive currents than DTL, they are designed to have high power output stages. The open collector gates are used in three major applications: driving a lamp and relay, performing a wired logic and for the construction of common bus system.

#### 4.9.2 Other TTL Series

The TTL gate has a number of circuits in its series. They have been developed to provide a wider choice of speed and power-dissipation characteristics. There are five series in the TTL family which are listed in Table 4.1 together with their respective propagation delay and power dissipation characteristics.

Table 4.1 Characteristics of 5 TTL versions

Version	Abbreviation	Propagation delay (ns)	Power dissipation (mW)	Maximum clock rate (MHz)	Fan-out
Standard	TTL	10	10	35	10
Low power	LTTL	33	1	3	10
High speed	HTTL	6	22	50	10
Schottky	STTL	3	19	125	10
Low power Schottky	LSTTL	9.5	2	45	10

**Standard series 54/7400 TTL** The Standard TTL gate was the first version of the TTL family. The basic standard gate circuit shown in Fig. 4.6 features a multiple-emitter input and an active pull-up output configuration. The use of multiple emitters is a major contribution to derive fast-switching speeds of TTL. Low output impedance is attained with totem-pole output stage consisting of transistors  $Q_3$  and  $Q_4$ , which also results in improved noise immunity and faster switching.

Standard series 54/74 line includes shift registers, counters, decoders, memories, data selectors and arithmetic elements in addition to SSI devices.

**Low power TTL, 54/74L00 series** Low power TTL circuits designated as the 74L00 series have essentially the same basic circuit as the standard 7400 series except that all the resistor values are increased.

Since an increase in resistance results in the reduction of power dissipation, the power requirements of low power gates are less than one-tenth of those of standard ICs. Series 54L/74L devices have a power dissipation of only 1 mW per gate and an average propagation delay of 33 ns. Low frequency, battery-operated circuits, such as calculators, are well suited for this version of the TTL series.

**High-speed TTL, 54H/74H00 series** The basic circuitry for this series is essentially the same as the standard 7400 series except that smaller resistor values are used and the emitter-follower transistor  $Q_3$  is replaced by a Darlington pair. Hence, the output section consists of a Darlington transistor pair  $Q_3$  and  $Q_4$  as shown in Fig. 4.7. This arrangement provides slightly higher speed (6 ns per gate) than the standard gate. The smaller resistances, however, increase power dissipation to about 22 mW.

Series 54H/74H master-slave flip-flops and edge-triggered flip-flops are capable of operating with clock input frequencies as high as 50 MHz.

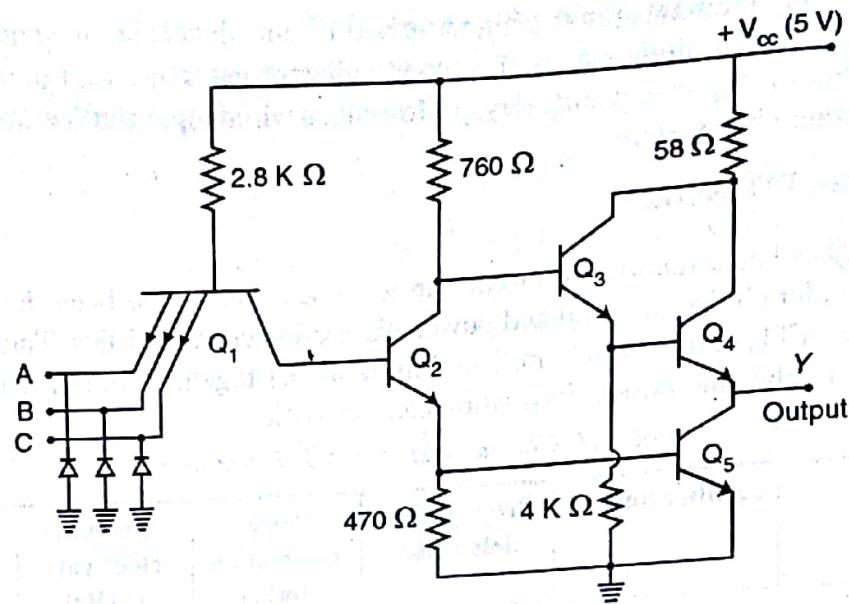
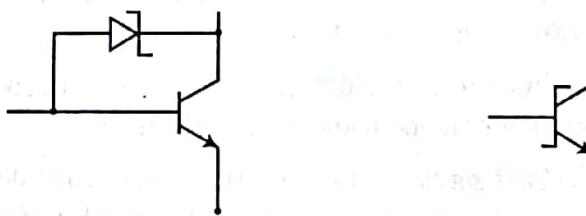


Fig. 4.7 High speed TTL gates, SN 54H/74H

**Schottky TTL, 54S/74S00 series** TTL 54S/74S series have the *highest speed* among TTL gates. This is achieved by using a Schottky-barrier diode (SBD) as a clamp from base to collector of each circuit transistor as shown in Fig. 4.8(a). The symbol for a transistor with a Schottky-barrier diode clamp is shown in Fig. 4.8(b). The characteristics of the SBD that make it useful as a clamp are its low forward voltage drop (0.25V) and its fast switching speed. When used as a clamp, the SBD diverts most of the excess base current and prevents the transistor from reaching saturation. This reduces the average propagation delay to 3 ns for a typical NAND gate.



(a) Transistor and Schottky-barrier diode clamp

(b) Symbol for transistor with Schottky-barrier diode clamp

Fig. 4.8

Schottky TTL devices are very fast, and are capable of operating at 100 MHz. The 74S00 series has a propagation delay of 3 ns and an average power dissipation of about 20 mW per gate.

**Low power Schottky TTL, 74LS00 series** By increasing internal resistance as well as using Schottky diodes, manufacturers have come up with a compromise between low power and high speed: low power Schottky TTL. It compares favourably with the standard TTL in speed and requires considerably less power.

These devices are numbered 74LS00, 74LS01, 74LS02, etc. A low power Schottky gate has a power dissipation of around 2 mW and a propagation delay of 9.5 ns.

### 4.9.3 TTL Circuit Output Connections

A number of output connections are provided using TTL logic gates. Each of the five TTL versions comes in one of three output circuit configurations commonly referred to as:

1. Totem-pole output
2. Open-collector output
3. Tri-state output.

$Q_3, Q_4$  common ✓

**Totem-pole output** The circuit of Fig. 4.6 shows a TTL NAND gate with totem-pole output. The totem-pole output is the standard output of a TTL gate and is specifically designed to reduce the propagation delay in the circuit and to provide sufficient output power for a high fan-out. The output in circuit of Fig. 4.6 is obtained as a high voltage level when  $Q_1$  is ON or a low voltage level when  $Q_4$  is ON. The circuit is designed in such a way that both  $Q_3$  and  $Q_4$  can never be ON at the same time. When either  $Q_4$  or  $Q_3$  conducts, the output impedance is low and hence the totem-pole output of a standard TTL circuit cannot be connected to any other output without causing a serious loading problem. This loading problem can be eliminated by a modified TTL circuit, called a Tri-state TTL circuit.

$O/P$  impedance  $\downarrow 1\Omega$

The totem-pole output configuration has the advantage of low output impedance in both logical states. When  $Q_3$  is conducting, the output impedance is around 70 ohms; when  $Q_4$  is saturated, the output impedance is only 12 ohms. Because of such low output impedance, any stray output capacitance is rapidly charged and discharged, thereby changing the output voltage quickly from one state to the other. This lower output impedance is also responsible for the capability of the gate to drive high capacitive loads, for low-noise susceptibility and high-speed performance characteristics of Series 54/74. Totem-pole outputs cannot be connected together to form an AND function as in open-collector outputs.

Speed  
gr

**Open-collector output** The open-collector TTL gate needs an external resistor that must be connected between the collector of a pull-down transistor and the supply voltage for proper operation. The TTL NAND gate with open-collector output is obtained by removing the following components: transistor  $Q_3$ , diode  $D$  and resistor  $R_3$  of Fig. 4.6. The resulting open collector TTL NAND gate is shown in Fig. 4.9(a). As the collector of  $Q_4$  is open, this open collector gate will not work properly unless an external pull-up resistor is connected as shown in Fig. 4.9(b). The output is taken at the collector of transistor  $Q_4$ . A high voltage level will appear at the output in the HIGH state.

Open-collector gates provide the versatility of wire AND operation or OR operation with a large number of logic variables. For instance, Fig. 4.10 shows three TTL devices connected to the common pull-up resistor. This has the advantage of combining the output of the three devices without using a final OR gate (or AND gate). This combining is done by a direct connection of the three outputs to the lower end of the common pull-up resistor. This is very useful when many devices are wire-ORed together. For instance, in some systems, the outputs of 16 open-collector devices are connected to a pull-up resistor.

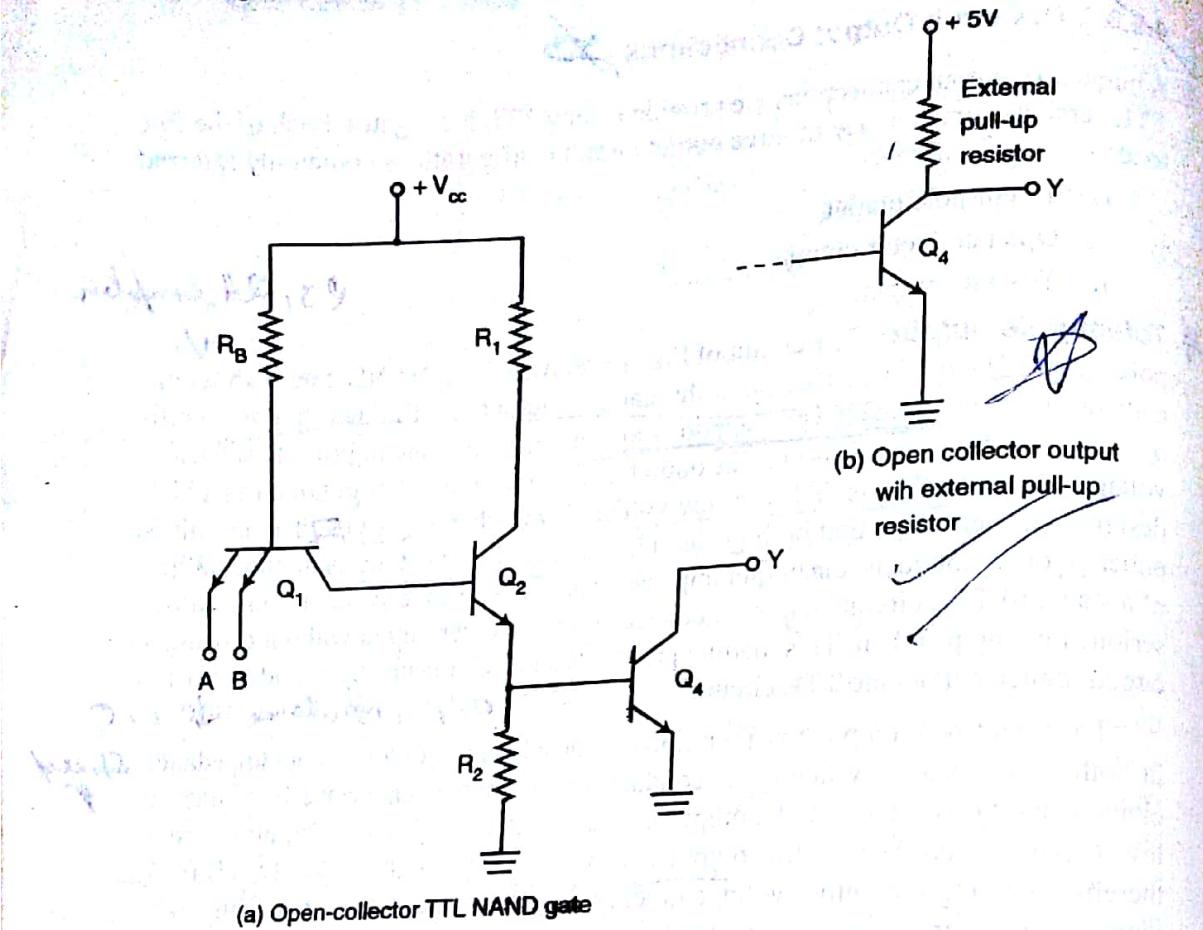


Fig. 4.9

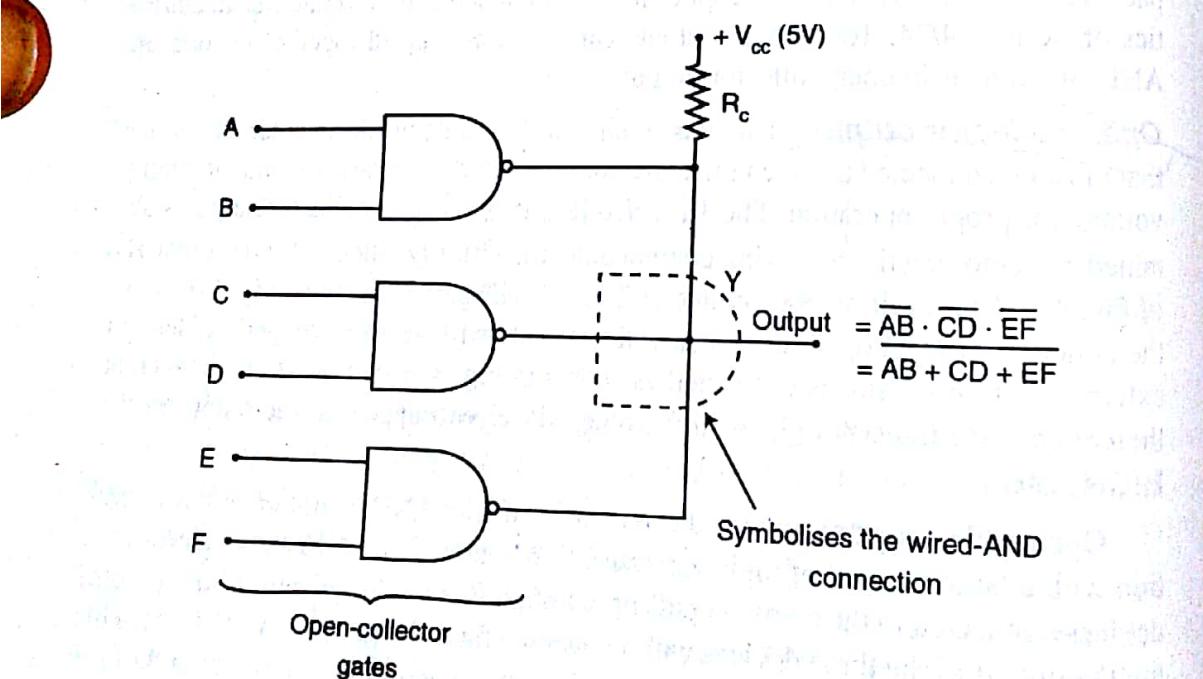


Fig. 4.10 Wired-AND operation using open-collector gates

The main disadvantage of open-collector gates is that switching time delay is increased because the pull-up resistance is few KΩ, which results in a relatively long

time constant when it is multiplied by the stray output capacitance. The slow switching speed of open-collector TTL devices becomes worse when the output goes from low to high. When the output transistor  $Q_4$  in the circuit of Fig. 4.9 goes into cutoff, then any capacitance across the output has to charge through the pull-up resistor. This charging produces a relatively slow exponential rise between the low and high state. Also, the circuit is more sensitive to noise at the output.

**Tri-state output** A very popular output connection that incorporates the benefits of totem-pole and open-collector in the single circuit is the tri-state output connection.

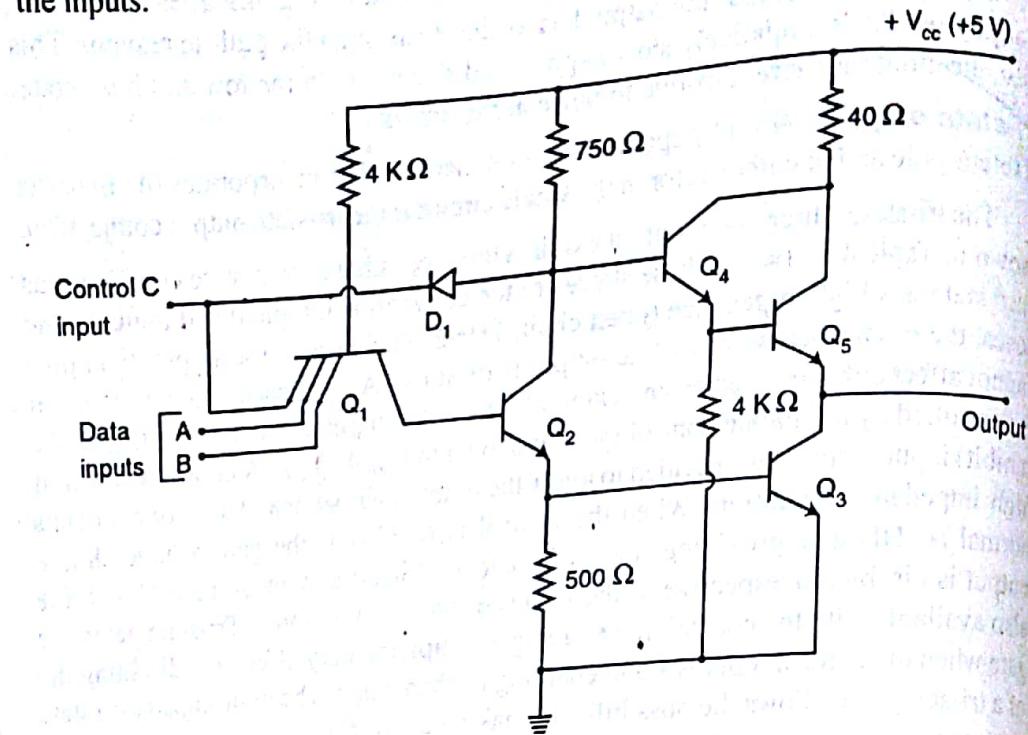
The tri-state (three state) output exhibits three possible output-state conditions as shown in Table 4.2. Two of these states are the conventional logic 0 and logic 1. The third state is a high impedance (open circuit) state. This means, for all practical purposes, the circuit behaves as if the output is disabled. As a consequence, the output cannot affect or be affected by any external signal at its input terminals. The third state is controlled by a separate control input as shown in Fig. 4.11(b). A control (Select or Inhibit) input terminal is provided to allow the output to be switched into (or out of) its high impedance condition. When the control input  $C$  is 1, the gate behaves like a normal NAND gate providing states of 0 and 1. When the control input  $C$  is 0, the output is disabled irrespective of the values of the normal inputs. Tri-state gates are also available with the control input having a complementary effect, i.e. disabling the gate when the control input is 1 and enabling it when it is 0. The high-impedance state of a tri-state gate allows the possibility of making a direct wire connection from many outputs to a common bus line, in which only one output line will be enabled while all other outputs are disabled by their respective control inputs.

Table 4.2 Truth table for tri-state TTL NAND gate

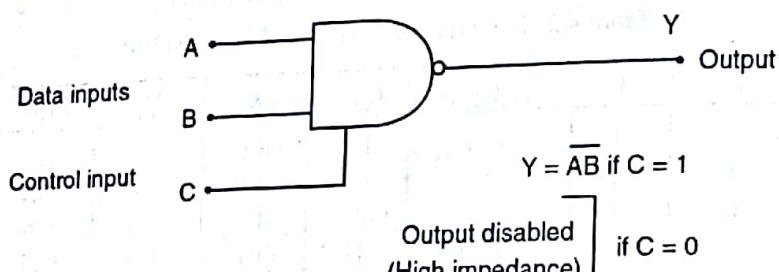
A	B	C	$Q_1$	$Q_2$	$Q_3$	$Q_4$	$Q_5$	Y
0	0	1	ON	OFF	OFF	ON	ON	1
0	1	1	ON	OFF	OFF	ON	ON	1
1	0	1	ON	OFF	OFF	ON	ON	1
1	1	1	OFF	ON	ON	OFF	OFF	0
X	X	0	ON	OFF	OFF	OFF	OFF	Open-circuit

**Operation of tri-state TTL NAND gate** Table 4.2 shows the truth table summarizing the operation of the tri-state NAND circuit of Fig. 4.11(a). When the control input  $C$  is HIGH (1) and any input  $A$  or  $B$  is LOW,  $Q_1$  is ON and both  $Q_2$  and  $Q_3$  are OFF. Hence,  $Q_4$  and  $Q_5$  will be turned ON and the output will be at the HIGH level (nearly +3.6V). When the control input  $C$  is HIGH and both inputs  $A$  and  $B$  are HIGH, transistor  $Q_1$  becomes OFF, and thereby drives both the transistors,  $Q_2$  and  $Q_3$ , ON. Hence,  $Q_4$  and  $Q_5$  are OFF and the output is LOW(0). Thus, when the control input  $C$  is HIGH, the circuit operates like a totem-pole output circuit. When the control input is in LOW state, then diode  $D_1$  conducts and therefore the voltage at the base of transistor  $Q_4$  is 0.7V which is not enough to make both the transistors,  $Q_4$  and  $Q_5$ , to switch to the ON state. Also, since  $Q_1$  is conducting, the transistor  $Q_2$  is in a cutoff state and therefore  $Q_3$  is also OFF. So, neither the output transistor  $Q_5$  nor  $Q_4$  is ON and the

output is open circuited or in HIGH impedance state. Therefore, it is concluded that there are three states of the output—LOW, HIGH and Open circuit as determined by the inputs.



(a) Basic circuit of TTL NAND gate with tri-state (3-state) output



(b) Symbol for tri-state NAND gate

Fig. 4.11

#### 4.9.4 TTL Parameters

Series 54/7400 devices work reliably over a temperature range of 0 to 70°C and over a supply range of 4.75 to 5.25V.

**Floating inputs** When a TTL input voltage is HIGH (ideally +5V) as shown in Fig. 4.12(a), the emitter current is zero. When a TTL input is unconnected (floating) as shown in Fig. 4.12(b), there is no flow of emitter current because of the open circuit. Hence, a floating TTL input is equivalent to a high input.

Also, when an input terminal is left open, it acts like a small antenna and picks up stray electromagnetic noise voltages leading to malfunctioning or erroneous operation of the gate. Therefore, it is a must to connect the unused TTL inputs either to the

ground or to the  $V_{CC}$ , depending upon the gate. For example, in AND and NAND gates, the unused input must be connected to  $V_{CC}$ , while in OR and NOR gates the unused inputs should be connected to ground.

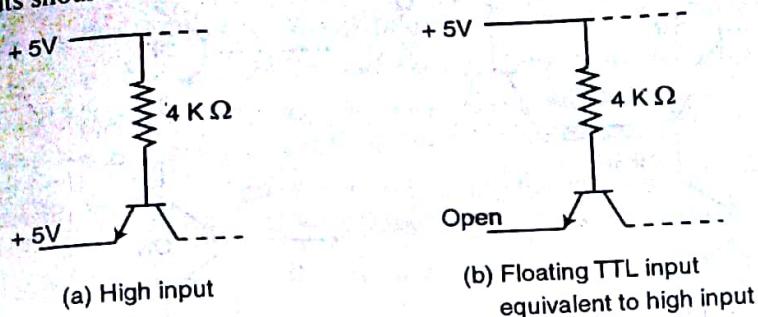


Fig. 4.12

**Current sourcing and current sinking** When the output of a gate is HIGH, thereby providing current to the input of the gate being driven, the output is said to act as a *current source*. For a TTL circuit, the maximum current drawn by an input from a high output is  $40\mu A$ .

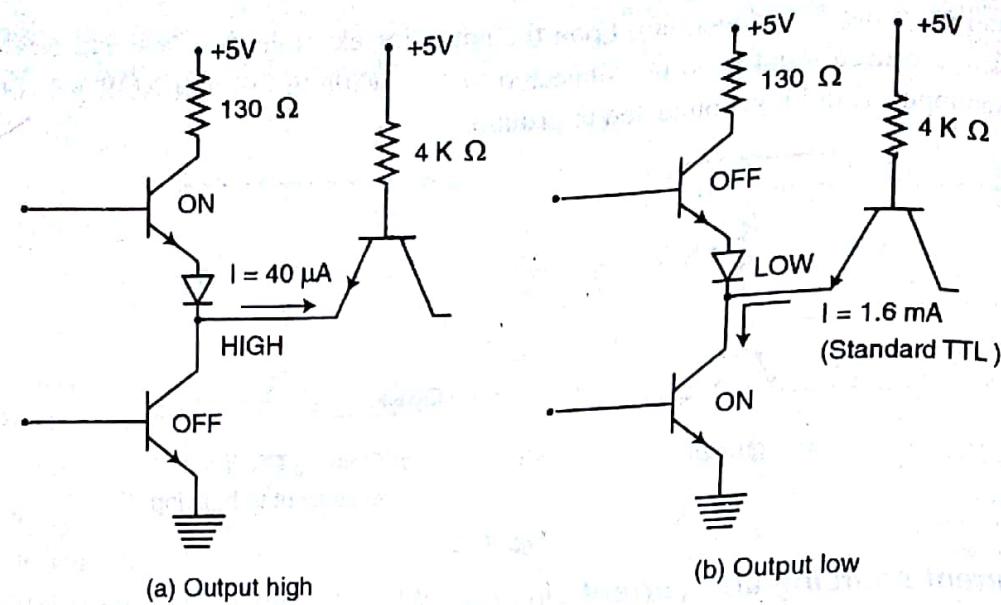
When the output of a TTL gate goes LOW, it must be capable of sinking current drawn from gate inputs which are driven LOW. The driver then operates as a *current sink*. In a standard TTL gate, when one of its inputs is low, a current of  $1.6mA$  flows out of the device. Thus,

$$I_{IL}(\text{max}) = -1.6mA \quad \text{and} \quad I_{IH}(\text{max}) = +40\mu A.$$

Here, the negative sign indicates that the current flows out of the device. [Refer to Fig. 4.12(a) and (b).]

**Standard loading** A TTL device can source (high output) or sink current (low output). Specification sheets of standard TTL devices show that any 54/7400 series can sink upto  $16mA$  and is denoted by  $I_{OL}(\text{max}) = 16mA$  and can source up to  $400\mu A$ , denoted by  $I_{OH}(\text{max}) = -400\mu A$ . The negative sign indicates that the conventional current is out of the device. Since the maximum output currents, i.e.  $I_{OL}(\text{max})$  and  $I_{OH}(\text{max})$ , are 10 times larger than the input currents, i.e.  $I_{IL}(\text{max})$  and  $I_{IH}(\text{max})$ , we can connect upto 10 TTL emitters to any TTL output.

**Fan-out** The maximum number of TTL loads that can be driven by a TTL driver is called fan-out. As discussed in the previous section, 10 TTL inputs can be connected to the output of a standard TTL. Thus, the fan-out of standard TTL is 10. When the totem-pole output of a TTL gate goes HIGH, it reverse-biases another gate input with the resulting current ( $40mA$ , maximum) as shown in Fig. 4.13(a). The TTL output going low must sink a current from the gate being driven, as shown in Fig. 4.13(b). The current from one standard TTL load is  $1.6mA$ , while from an LS circuit the load current is only  $0.36mA$ . Using the standard unit as reference, one unit load is then the same as a current of  $1.6mA$  into a low output. Since a standard output drive is capable of sinking the current of  $16mA$ , it can drive upto 10 loads.



*Fig. 4.13 Fan-out operation*

For LOW power TTL,

$$I_{II}(\max) = -0.18 \text{ mA}; \quad I_{IH}(\max) = 10 \text{ : A}$$

$$I_{OL}(\text{max}) = 3.6 \text{ mA}; I_{OH}(\text{max}) = -200 \text{ nA}$$

Considering HIGH output state :  $\frac{I_{OH\ max}}{I_{IH\ max}} = \frac{200\ mA}{10\ mA} = 20$

Considering LOW output state :  $\frac{I_{OL \text{ max}}}{I_{IL \text{ max}}} = \frac{3.6 \text{ mA}}{0.18 \text{ mA}} = 20$

Therefore, twenty LOW power TTL gate inputs can be connected to the output of another LOW power TTL gate.

For LOW power Schottky TTL,

$$I_{H\parallel}(\text{max}) = -0.36 \text{ mA}; I_{H\perp}(\text{max}) = 20 \text{ mA}$$

$$I_{OL}(\text{max}) = 8 \text{ mA}; I_{OH}(\text{max}) = -400 \text{ mA}$$

Therefore, for lowpower Schottky TTL,

$$\text{Fan - out} = \frac{8 \text{ mA}}{0.36 \text{ mA}} = 22 \text{ (or)} \quad \frac{400 : A}{20 : A} = 20, \text{ whichever is less.}$$

Also, a particular type of TTL gate can be connected with other types of TTL. For example, if a standard TTL is connected with a HTTL, the fan-out is 8; if it is connected with a LTTL, the fan-out is 40; if it is connected to a STTL, the fan-out is 8 and with a LS series, the fan-out is 20. The above data is summarised in Table 4.3.

**Table 4.3** Fan-outs

TTL Driver	TTL load				
	74	74 H	74 L	74 S	74 LS
74	10	.8	40	8	20
74 H	12	10	50	10	25
74 L	2	1	20	1	10
74 S	12	10	100	10	50
74 LS	5	4	40	4	20

**Switching speed** The TTL circuit has the fastest switching speed of any saturated logic. Two switching parameters are tested on TI 54/74 TTL gates: propagation delay time  $t_{PHL}$  from a logical 1 to a logical 0 level at the output and propagation delay time  $t_{PLH}$  from a logical 0 to a logical 1 level at the output. These switching tests are performed at the following nominal conditions:  $V_{CC} = 5V, T_A = 25^\circ C$  and  $N = 10$ . Acceptable devices have  $t_{PHL} \leq 15\text{ns}$  and  $t_{PLH} \leq 22\text{ns}$ . Note that  $t_{PHL}$  decreases with increasing temperature, and  $t_{PLH}$  is independent of temperature. The propagation delay time of a standard TTL gate is approximately 10ns.

**Supply current characteristics** Power supply current requirements for all series 54/74 circuits are specified as maximum current drains with maximum permissible power-supply voltage,  $V_{CC}$ . Maximum  $I_{CCL}[I_{CC}(0)]$  per gate is specified as 5.5 mA and maximum  $I_{CCH}[I_{CC}(1)]$  per gate is specified as 2.0 mA. At the nominal supply voltage of 5V, typical  $I_{CCL}$  per gate is 3mA and typical  $I_{CCH}$  is 1 mA. Thus,  $I_{CCL}$  is about 3 times larger than  $I_{CCH}$ .

**Worst case input and output voltages** Theoretically, logic LOW state is 0V and a logic HIGH state is 5V. But, practically for TTL gates, there is a window or a range of low voltages which is still recognised as LOW state and a range of high voltages which is still recognised as HIGH state. Also, this range of LOW and HIGH state voltages is different at inputs and outputs of a TTL gate.

For a TTL gate, the worst case input voltages are:

$V_{IL, \text{max}} = 0.8\text{ V}$  (It means a voltage from 0 to 0.8V without changing the output is recognized as LOW state.)

$V_{IH, \text{min}} = 2\text{ V}$  (It means a voltage from 5V down to 2V without changing the output is recognized as HIGH state.)

A LOW voltage greater than 0.8V and a HIGH voltage lower than 2V lead to unpredictable input state. Similarly, the worst case output voltages are:

$V_{OL, \text{max}} = 0.4\text{ V}$  (It means a LOW state output having any value from 0 to 0.4V.)

$V_{OH, \text{min}} = 2.4\text{ V}$  (It means a HIGH state output having any value from 5 to 2.4V.)

Thus, as far as TTL output is concerned, a LOW voltage greater than 0.4V and a HIGH voltage less than 2.4V leads to unpredictable output state.

**Noise immunity** It is the maximum induced noise voltage a TTL device can withstand without a false change in the output state. The rating of the circuit depends upon the smallest noise voltage that will perturb it. TTL gate has less noise immunity. From the above section, the worst case LOW voltages are:

$$V_{OL(\text{max})} = 0.4\text{ V}$$

$$V_{IL(\text{max})} = 0.8\text{ V}$$

and the worst case HIGH voltages are :

$$V_{OH(\text{min})} = 2.4\text{ V}$$

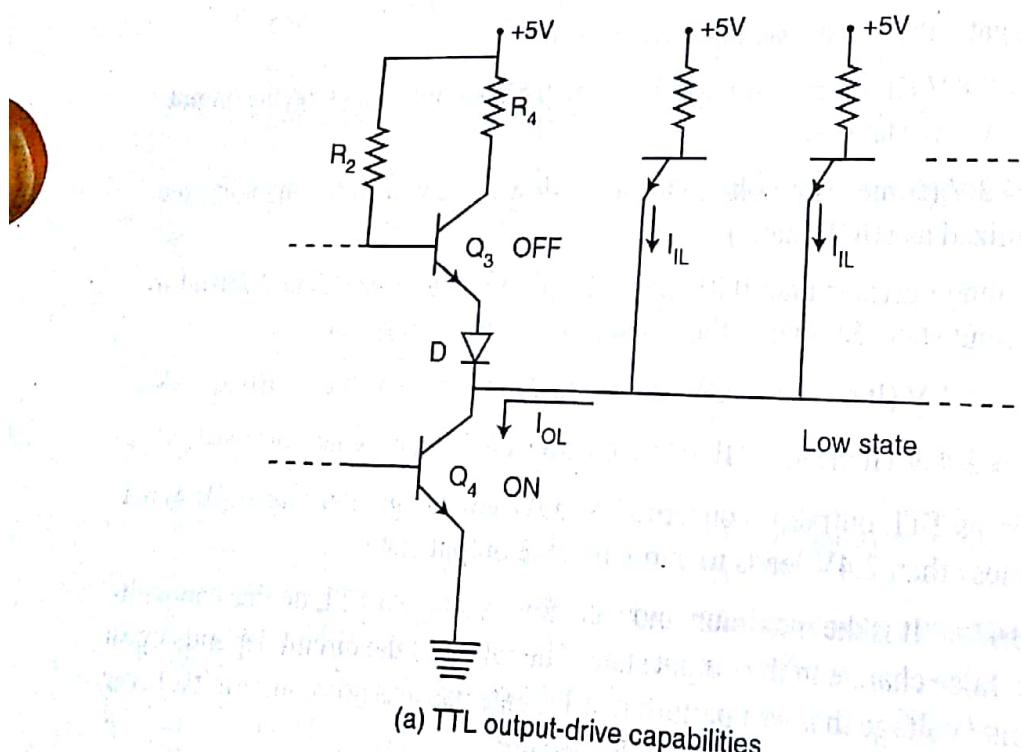
$$V_{IH(\text{min})} = 2\text{ V}$$

One can observe that there is a difference of 0.4V in both cases. This difference between maximum input LOW voltage and maximum output LOW voltage is called noise immunity. The smallest magnitude of noise voltage that would perturb the input signal is 0.4V.

**Power dissipation** A standard TTL gate is operated with a power supply of 5 volts, which draws an average supply current of 2mA, resulting in a power dissipation of  $2\text{mA} \times 5\text{V} = 10\text{mW}$ .

**Loading rules** A single TTL output in the LOW state connected to several TTL inputs is shown in Fig. 4.14(a). Transistor  $Q_4$  is ON and is acting as a current sink for all the currents ( $I_{IL}$ ) coming back from each input. Although  $Q_4$  is saturated, its ON state resistance is some value other than zero, so the current  $I_{OL}$  produces an output voltage drop  $V_{OL}$ . The value of  $V_{OL}$  must not exceed 0.4V for TTL, and this limits the value of  $I_{OL}$  and thus the number of loads that can be driven.

Fig. 4.14(b) shows the HIGH-state situation. The transistor  $Q_3$  is acting as an emitter-follower and is sourcing current to each TTL input. If too many loads are driven, however, the total output current  $I_{OH}$  can become too large, causing larger drops across  $R_2$ ,  $Q_3$  and  $D$ , thereby lowering  $V_{OH}$  below the minimum allowable voltage 2.4V.



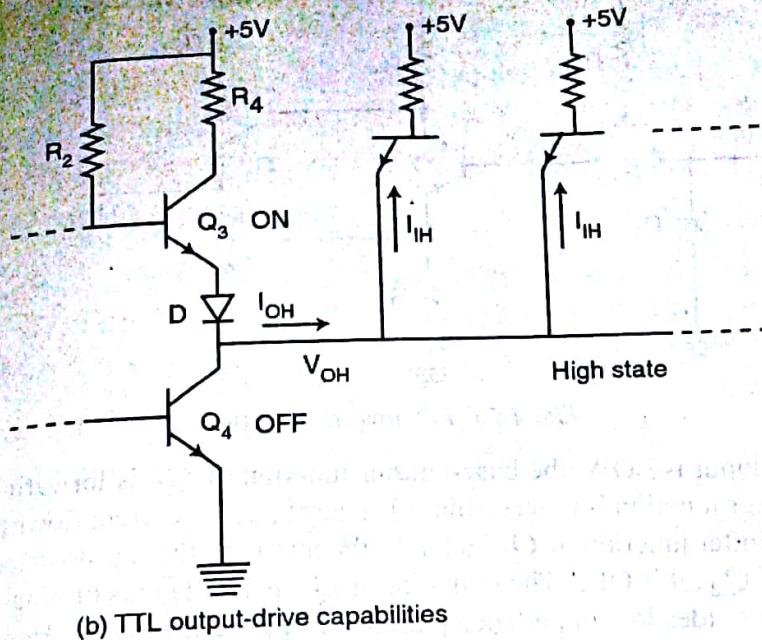


Fig. 4.14

**Protective (clamping) diodes.** The input signals for the TTL circuit are always positive. If negative signals were to be inadvertently applied, excess input current could result which might damage the circuit. In a general circuit, the load inductance coupled with stray capacitance can result in damped sinusoidal transients. Such signals might result in values  $V_A$ ,  $V_B$  or  $V_C$  which are negative for short periods of time.

To prevent these transient negative voltages (swings) from becoming substantial, diodes are usually connected from each input to ground as shown in Fig. 4.15. These diodes do not affect positive signals. The protective diodes limit negative excursions to about  $-0.7V$ .

#### 4.9.5 TTL Inverter

The circuit diagram of a TTL inverter is shown in Fig. 4.16. The transistor  $Q_1$  is the input coupling transistor and  $D_1$  is the protective diode. Transistor  $Q_2$  is called a phase splitter, and the combination of transistors  $Q_3$  and  $Q_4$  forms the totem-pole output circuit.

**Operation** When a HIGH ( $+5V$ ) voltage is applied at the input ( $A$ ), the base-emitter junction of  $Q_1$  becomes reverse-biased and the base-collector junction is reverse-biased. The current then flows through  $R_1$  and base-collector junction of  $Q_1$  into the base of  $Q_2$ . Therefore, the transistor  $Q_2$  drives into saturation and a voltage drop across  $R_2$  turns ON the transistor  $Q_4$ . So, the output is nearer to LOW potential.

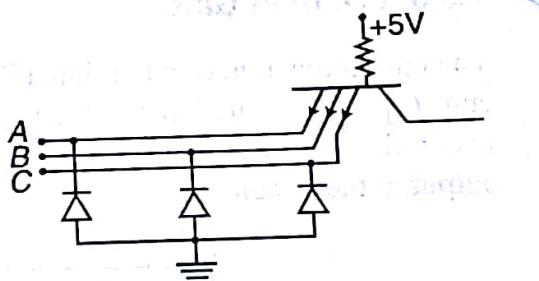


Fig. 4.15 A protected TTL input circuit

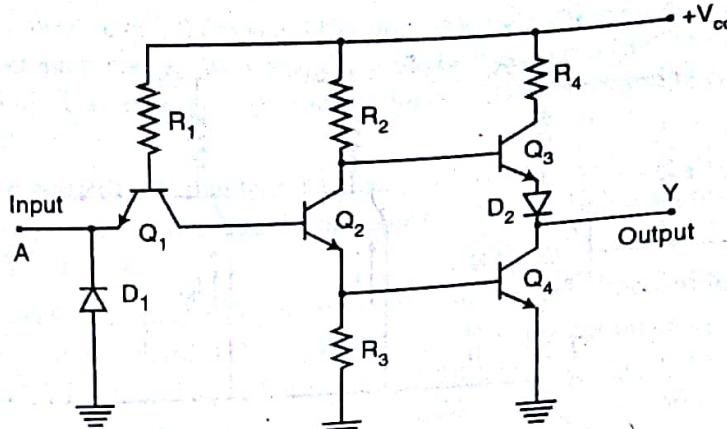


Fig. 4.16 TTL inverter circuit

When the input is LOW, the base-emitter junction of  $Q_1$  is forward-biased and the base-collector junction is reverse-biased. Therefore, the current flows through  $R_1$  and the base-emitter junction of  $Q_1$  to the LOW input. As there is no current flowing into the base of  $Q_2$ , it is OFF. The collector of  $Q_2$  is HIGH thus turning  $Q_3$  ON. A saturated  $Q_3$  provides low impedance path from  $V_{CC}$  to the output. Hence, the output is HIGH.

#### 4.9.6 TTL NOR Gate

The circuit diagram of a two-input TTL NOR gate is shown in Fig. 4.17. In this circuit,  $Q_1$  and  $Q_2$  are input transistors, and transistors  $Q_3$  and  $Q_4$  that are connected in parallel act as a phase splitter. The combination of  $Q_5$  and  $Q_6$  forms a totem-pole output in the circuit.

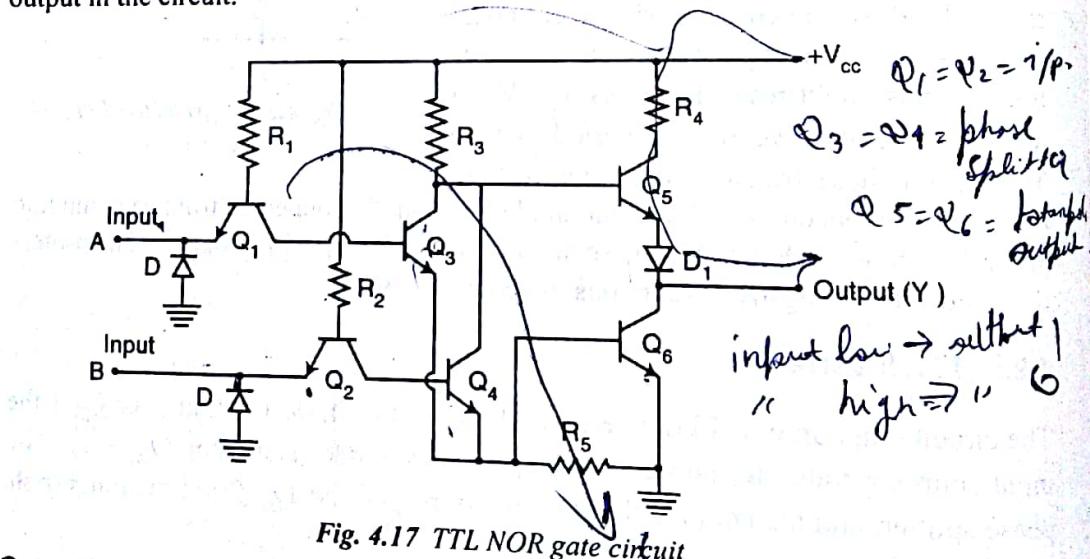


Fig. 4.17 TTL NOR gate circuit

**Operation** When the inputs are LOW, the base-emitter junctions of  $Q_1$  and  $Q_2$  are forward-biased and pull current away from transistors  $Q_3$  and  $Q_4$ , keeping them OFF. As a result,  $Q_5$  is ON and  $Q_6$  is OFF, producing a HIGH output.

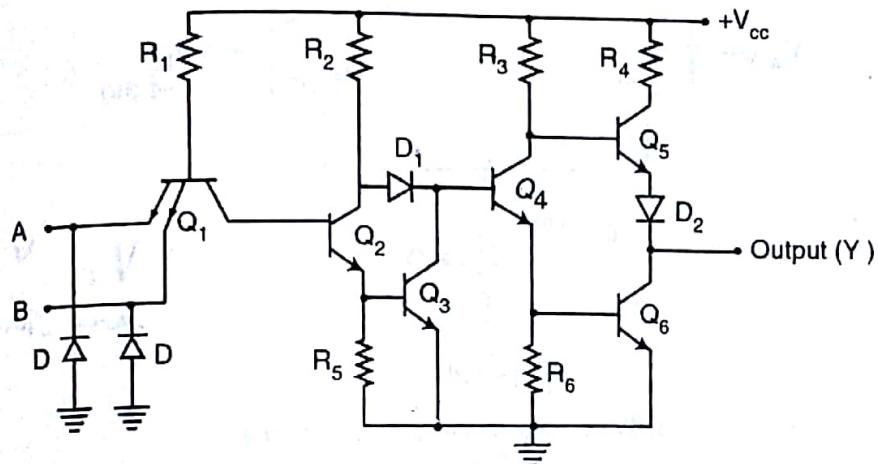
When input  $A$  is LOW and input  $B$  is HIGH,  $Q_3$  is OFF and  $Q_4$  is ON. The transistor  $Q_4$  turns ON  $Q_6$  and turns OFF  $Q_5$ , producing a LOW output.

When input A is HIGH and input B is LOW,  $Q_3$  is ON and  $Q_4$  is OFF. The transistor  $Q_3$  turns ON  $Q_6$  and turns OFF  $Q_5$ , producing a LOW output.

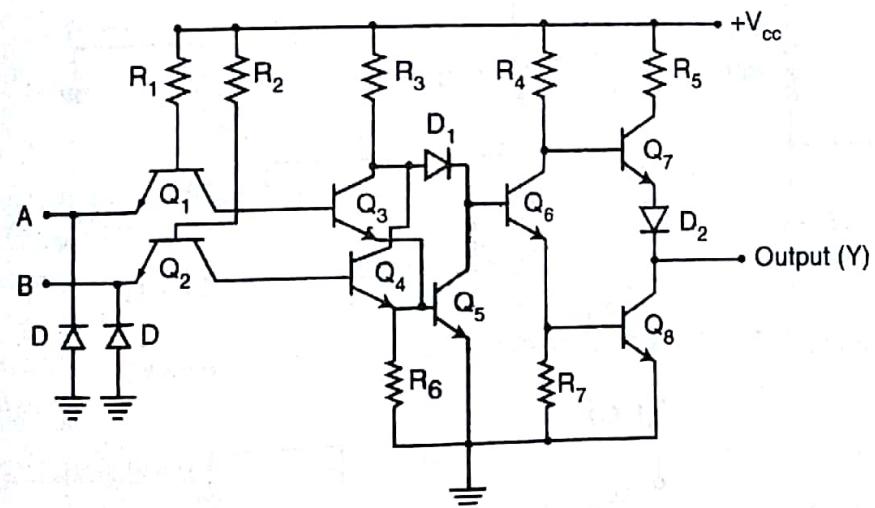
When both inputs A and B are HIGH, transistors  $Q_3$  and  $Q_4$  are ON. This has the same effect as either one being ON, turning  $Q_6$  ON and  $Q_5$  OFF. The result is a LOW output. Thus, this circuit functions as a NOR gate.

#### 4.9.7 TTL AND and OR Gate

The circuits of a TTL two-input AND gate and a two-input OR gate are shown in Fig. 4.18(a) and (b) respectively. In each diagram, the arrangement of transistors provides an inversion. That is, a NAND becomes an AND and a NOR gate becomes an OR.



(a) TTL AND gate



(b) TTL OR gate

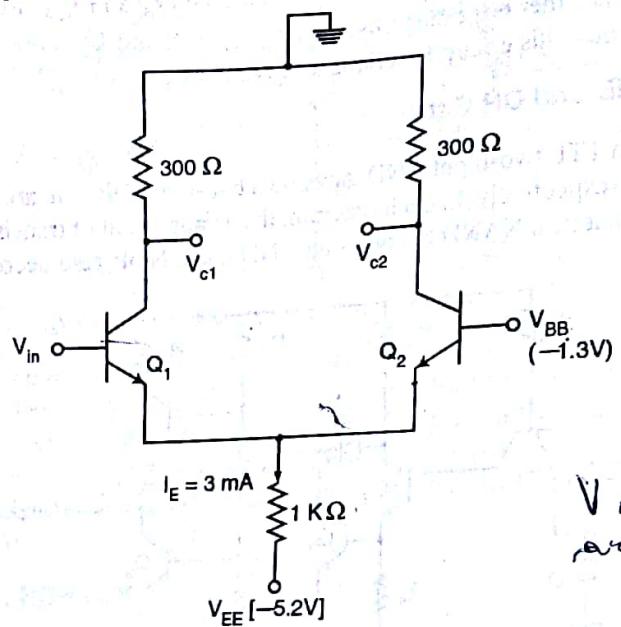
Fig. 4.18

#### 4.10 Emitter-Coupled Logic (ECL) NON-SATURATING LOGIC

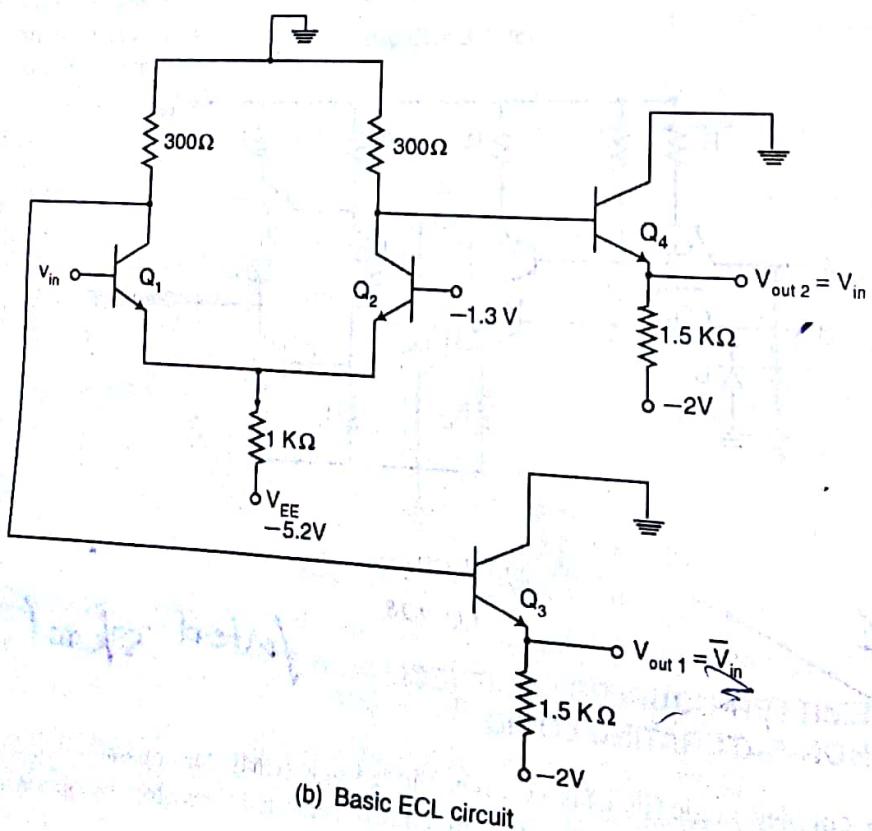
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Emitter-coupled Logic (ECL) is a Current-Mode Logic (CML) or non-saturated digital logic family, which eliminates the turn-off delay of saturated transistors by operating in

the active mode. At present, the ECL family has the fastest switching speed among the commercially available digital ICs. The propagation delay time of a typical ECL gate is 1ns. Also, it requires a relatively large silicon area and dissipates high power.



(a) Differential amplifier of ECL circuit



(b) Basic ECL circuit

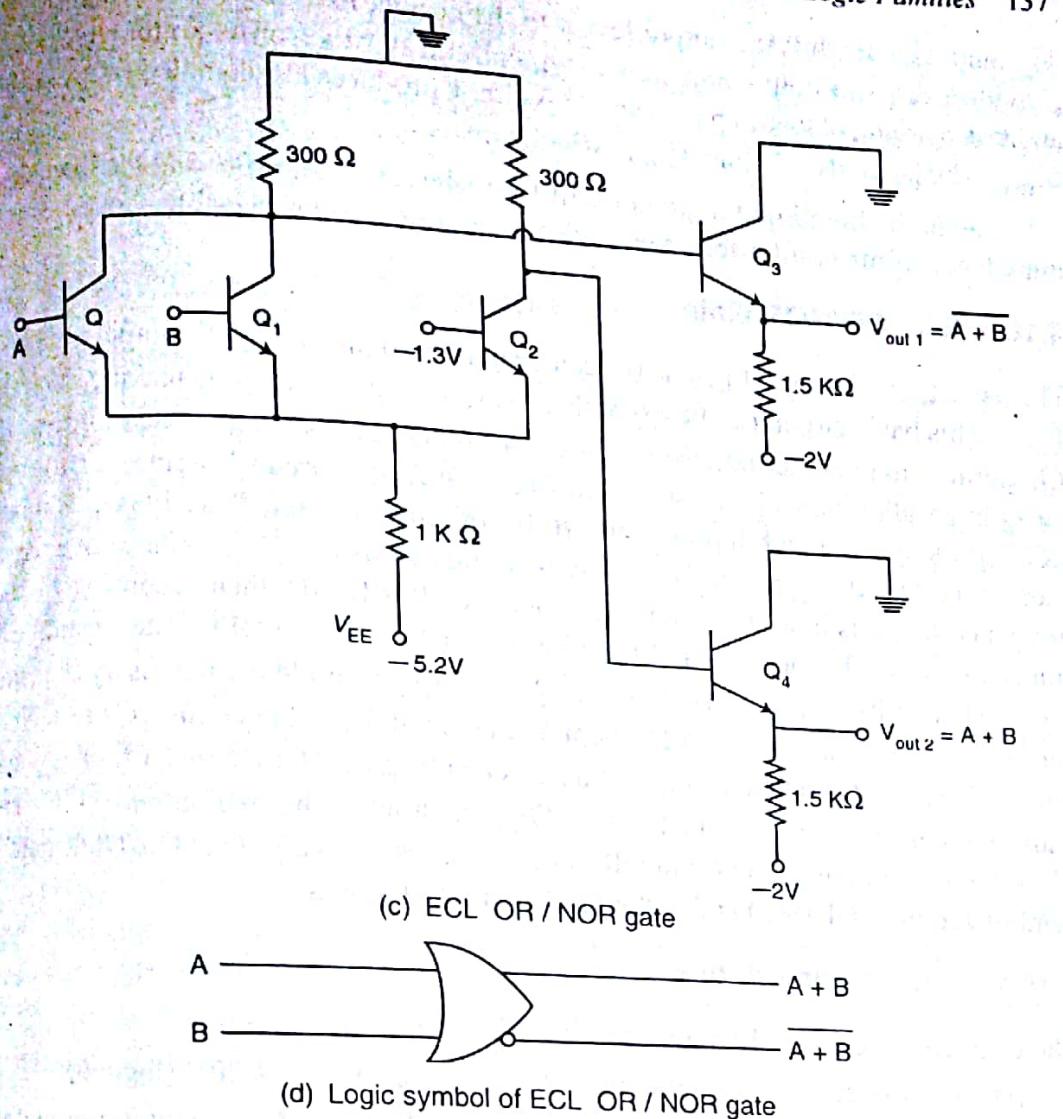


Fig. 4.19

The basic circuit of emitter-coupled logic is a differential amplifier as shown in Fig.4.19(a). As a constant current is drawn by the differential amplifier even during transition from one state to another, the power supply line can be free of noise and spikes. Because of the active mode of operation of the differential amplifier, there is no storage delay in switching between ON and OFF states of the transistors in the differential pair.

The  $V_{EE}$  supply produces a fixed current  $I_E$ , which remains around 3mA during normal operation. This current is allowed to flow through  $Q_1$  or  $Q_2$ , depending on the voltage level at  $V_m$ . In other words, this current switches between the collectors of  $Q_1$  and  $Q_2$  as  $V_m$  switches between its two logic levels of -1.7V (logical 0 for ECL) and -0.8V (logical 1 for ECL).  $V_{e1}$  and  $V_{e2}$  are the complements of each other, and the output voltage levels are not the same as the input logic levels.

The output voltage levels are made equal to the input logic level by connecting  $V_{e1}$  and  $V_{e2}$  to emitter-follower stages ( $Q_3$  and  $Q_4$ ), as shown in Fig.4.19 (b). The emitter followers perform two functions: (i) they subtract approximately 0.8V from

$V_{C1}$  and  $V_{C2}$  to shift the output levels to the correct ECL logic levels, and (ii) they provide a very low output impedance (typically  $7\ \Omega$ ), which provides for large fan-out and fast charging of load capacitance. This circuit produces low complementary outputs:  $V_{out1}$ , which equals  $\bar{V}_m$  and  $V_{out2}$ , which equals  $V_m$ .

Due to the high input impedance of the differential amplifier and the low output impedance of the emitter follower, high fan-out operation is possible.

#### 4.10.1 ECL OR/NOR Gate

The basic ECL circuit of Fig.4.19(b) can be used as an inverter if the output is taken at  $V_{out1}$ . This basic circuit can be expanded to more than one input by making transistor  $Q_1$  parallel to the other transistors for other inputs. By connecting one more transistor  $Q$  in parallel with  $Q_1$ , as shown in Fig.4.19(c), the circuit becomes a two-input ECL OR/NOR gate with inputs  $A$  and  $B$ . If both inputs  $A$  and  $B$  are LOW, then both transistors,  $Q$  and  $Q_1$ , are in the OFF state while transistor  $Q_2$  is in the active region and its collector is in a LOW state. If either  $A$  or  $B$  is HIGH, then accordingly either transistor  $Q$  or  $Q_1$  conducts and the transistor  $Q_2$  is in the OFF state, resulting in HIGH state at its collector. Transistors  $Q_3$  and  $Q_4$  provide the necessary d.c. shift for voltage correction. Thus, if the output is taken at  $V_{out1}$  the circuit acts as a NOR gate; if the output is taken at  $V_{out2}$ , it acts as an OR gate. Here, either  $Q_1$  or  $Q_2$  can cause the current to be switched out of  $Q_2$ , resulting in the two outputs,  $V_{out1}$  and  $V_{out2}$  being the logical NOR and OR operations, respectively. This OR/NOR gate is symbolized in Fig.4.19(d) and is the fundamental ECL gate.

#### 4.10.2 ECL Characteristics

The characteristics of an ECL circuit are as follows:

- (i) The logic levels are nominally  $-0.8\text{V}$  (logic 1) and  $-1.70\text{V}$  (logic 0).
- (ii) The transistors never saturate, i.e. storage delay in ECL circuit is eliminated, and hence switching speed is very high. Typical propagation delay time is  $1\text{ns}$ , which makes ECL faster than advanced Schottky TTL (74AS series).
- (iii) Because of the low noise margin, 250 milli-volt, ECL circuits are not reliable in heavy industrial environments.
- (iv) An ECL logic block usually produces an output and its complement. This eliminates the need for inverters.
- (v) Fan-outs are typically around 25, owing to the low-impedance emitter-follower outputs. Such a small fan-out is a limitation compared with the saturating logic families or the MOS logic families.
- (vi) Typical power dissipation for a basic ECL gate is  $40\text{ mW}$ , somewhat higher than the 74AS series. This is true because all the transistors are in the active mode.
- (vii) The total current flow in an ECL circuit remains relatively constant regardless of its logic state. This helps to maintain an unvarying current drain on the circuit power supply even during switching transitions. Thus, no noise spikes will be internally generated like those produced by TTL totem-pole circuits.

The ECL family is not as widely used as the TTL and MOS families except in very high frequency applications, where its speed is superior. Its relatively low noise margins and high power drain are disadvantages when compared with other logic families. Another drawback is its negative supply voltage and logic levels, which are not compatible with the other logic families; this makes ECL difficult to use in conjunction with TTL and MOS circuits.

#### 4.11 INTEGRATED-INJECTION LOGIC ( $I^2L$ )

Integrated-Injection Logic, IIL or  $I^2L$ , is a new LSI technique also called Merged Transistor Logic (MTL) that uses both *n-p-n* and *p-n-p* bipolar junction transistors to form a large number of IC gates on a chip. It reduces the number of metal inter-connections. When operated at low speeds,  $I^2L$  dissipates less power (5mW) than any logic family including CMOS. At high speeds (5ns), it only dissipates 5mW per gate. Because of its high speed and less power dissipation, it is used in large computers.

**Operation** The basic  $I^2L$  inverter circuit is shown in Fig. 4.20(a). Due to the absence of resistors, the  $I^2L$  inverter occupies much smaller area than a  $T^2L$  inverter. The base of  $Q_1$  and emitter of  $Q_2$  are internally merged; the collector of  $Q_1$  and the base of  $Q_2$  are merged, and hence only four separate regions are required to form the two transistors. Thus, the entire  $I^2L$  gate takes only the space of a single TTL multiple-emitter transistor.

The *p-n-p* transistor  $Q_1$  acts as a current source and active pull-up, and the multiple-collector *n-p-n* transistor  $Q_2$  operates as an inverter. Most of the current leaving from the emitter of  $Q_1$  is injected directly into the base of  $Q_2$ , and hence the emitter of  $Q_1$  is known as the *injector*, and the integrated gate structure is called the Integrated Injection Logic.

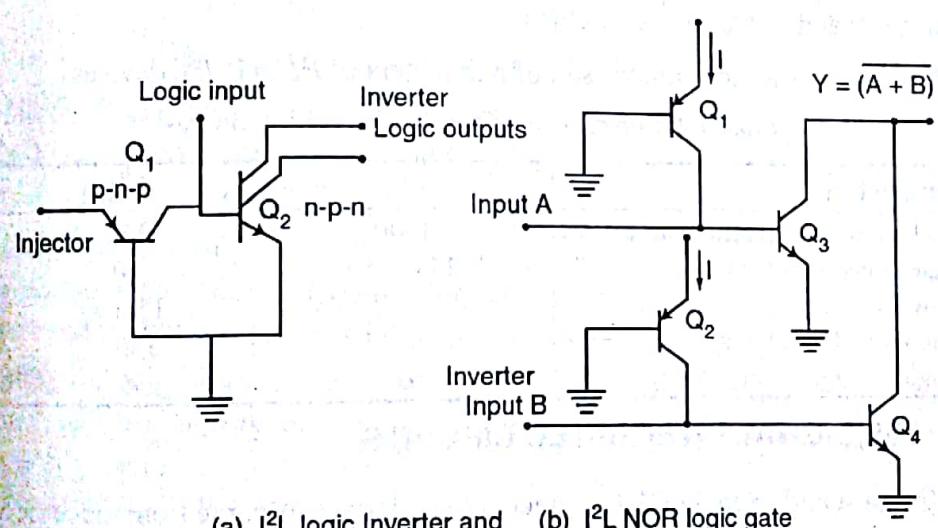


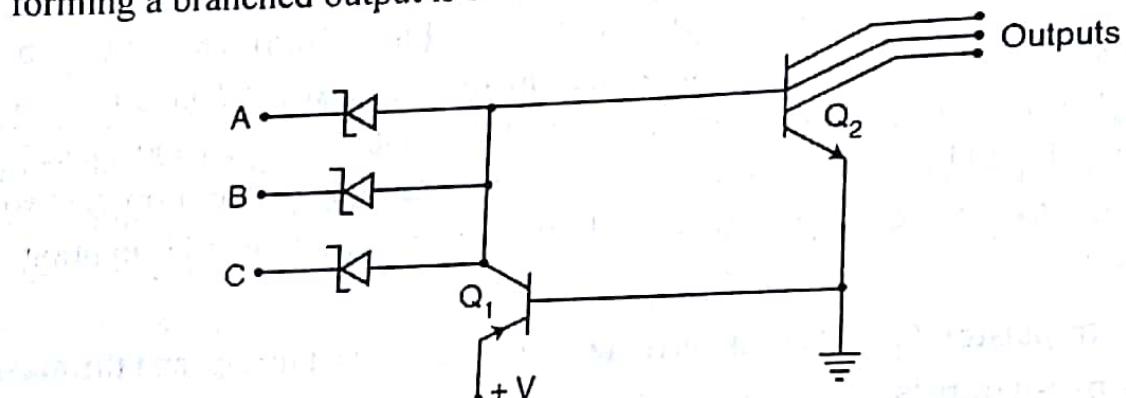
Fig. 4.20

The base of  $Q_1$  and emitter of  $Q_2$  are internally merged and the collector of  $Q_1$  and base of  $Q_2$  are merged, the entire  $I^2L$  gate takes only the space of a single TTL multiple-emitter transistor.

A low input voltage of 0.1V, the saturation voltage of the preceding multi-collector transistor, pulls injector current out of the input of the *n-p-n* transistor  $Q_2$ . Then this injector current flows through the driving transistor  $Q_1$ . With no base current, the inverter transistor  $Q_2$  turns OFF and its output goes HIGH. A high input voltage of 0.8V or more to the logic input terminal allows the injector current to hold the inverter transistor ON, and hence its output goes LOW.

Fig. 4.20(b) shows the circuit of *P<sup>L</sup>* NOR gate with two inputs *A* and *B* and output *Y*. If either or both of the inputs are HIGH, one or both *n-p-n* transistors ( $Q_3$  and  $Q_4$ ) are ON, and hence the output goes LOW. If both the inputs are LOW, then both  $Q_3$  and  $Q_4$  are turned OFF, and hence the output is HIGH. Thus, the circuit acts as a NOR gate.

The *P<sup>L</sup>* circuit resembles the DCTL circuit. The *P<sup>L</sup>* gate with three Schottky diodes in the base region that realise the AND function and with three collector leads forming a branched output is shown in Fig. 4.21.



*Fig. 4.21 Schottky  $I^2L$  gate*

In summary, the *P<sup>L</sup>* family is one of the more promising of the bipolar families. It has already found application in video games, watches, television tuning and control and memory and microprocessor chips.

Table 4.4 shows the comparison of parameters of *P<sup>L</sup>* and *T<sup>2</sup>L* devices.

*Table 4.4 Comparison of typical  $P^L$  and  $T^2L$  devices*

### 4.12.1 MOSFET

In MOSFET, the channel can be of *p* or *n* type, depending on whether the majority carriers are either holes or electrons. The mode of operation can be *enhancement* or *depletion*, depending on the state of the channel region at zero gate voltage. If the channel is initially doped lightly with *p*-type impurity, a conducting channel exists at zero gate voltage and the device is said to operate in the *depletion mode*. In this mode, current flows unless the channel is depleted by an applied gate field. If the region beneath the gate is left initially uncharged, a channel must be induced by the gate field before current can flow. Thus, the channel current is enhanced by the gate voltage and such a device is said to operate in the *enhancement mode*.

The schematic symbols for the *n*-channel and *p*-channel enhancement MOSFETs are shown in Fig. 4.22. The direction of the arrow indicates the type of channel *p* or *n*. The symbols show a broken line between the *source*, *substrate* and *drain* to indicate that there is *normally* no conducting channel among these electrodes. The symbol also shows a separation between the *gate* and the other terminals to indicate the very high resistance ( $>10,000\text{ M}\Omega$ ) between the *gate* and *channel*.

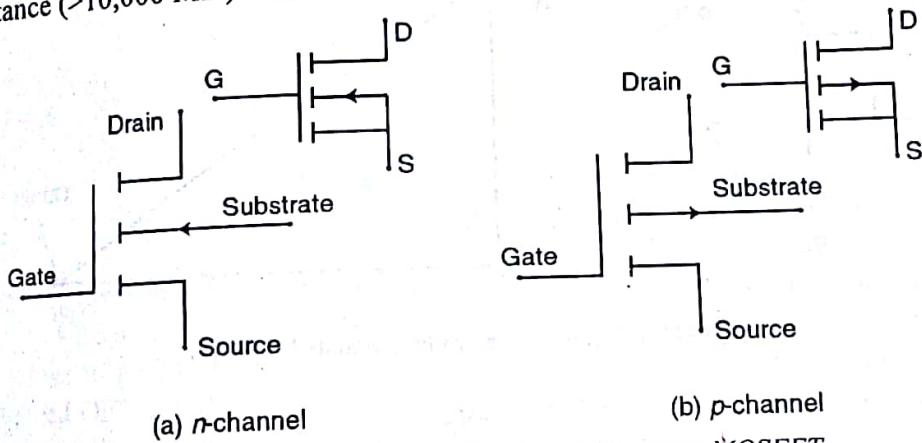


Fig. 4.22 Schematic symbols for the enhancement MOSFETs

**PMOS** It uses only *p*-channel enhancement MOSFET. A resistor at the output of a PMOS circuit could be used to drop the high level voltage to one suitable for CMOS circuit. *Holes* are the current carriers for PMOS.

**NMOS** It uses only *n*-channel enhancement MOSFET. NMOS has a greater packing density than PMOS. *Free electrons* are the current carriers in NMOS. These circuits require voltage typically ranging from 5V to 12V.

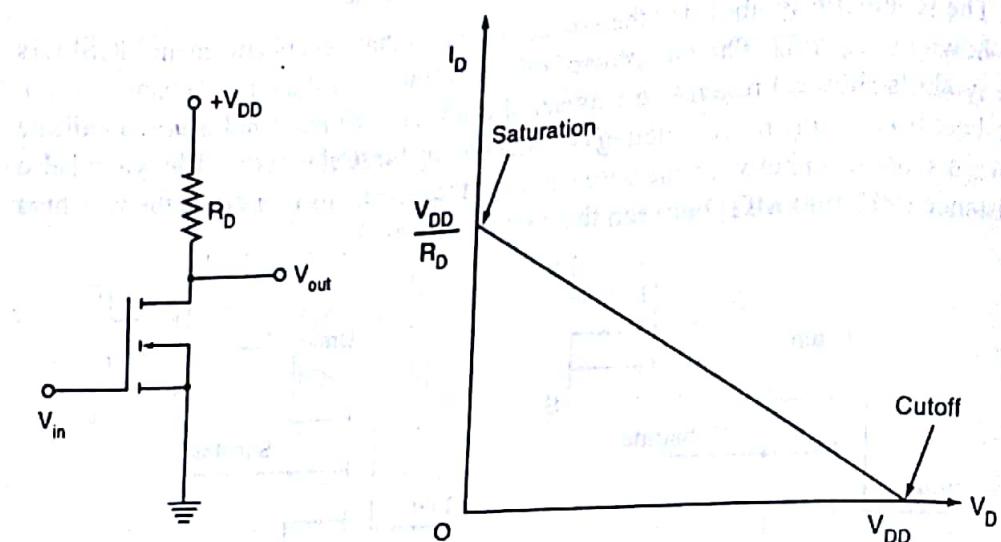
**CMOS** It uses both *p*-and *n*-channel devices. It has the greatest complexity and lowest packing density among the MOS families. It possesses the important advantages of much lower power dissipation, very high input impedance and high noise immunity. The CMOS logic gates are used in battery-operated portable equipment. Its main disadvantage is its low speed due to high input impedance.

PMOS and NMOS digital ICs have a greater packing density and are therefore more economical than CMOS. NMOS is also about twice as fast as PMOS. PMOS and NMOS find their widest applications in LSI (microprocessors, memories, ROMs, etc.) while CMOS is widely used in MSI applications.

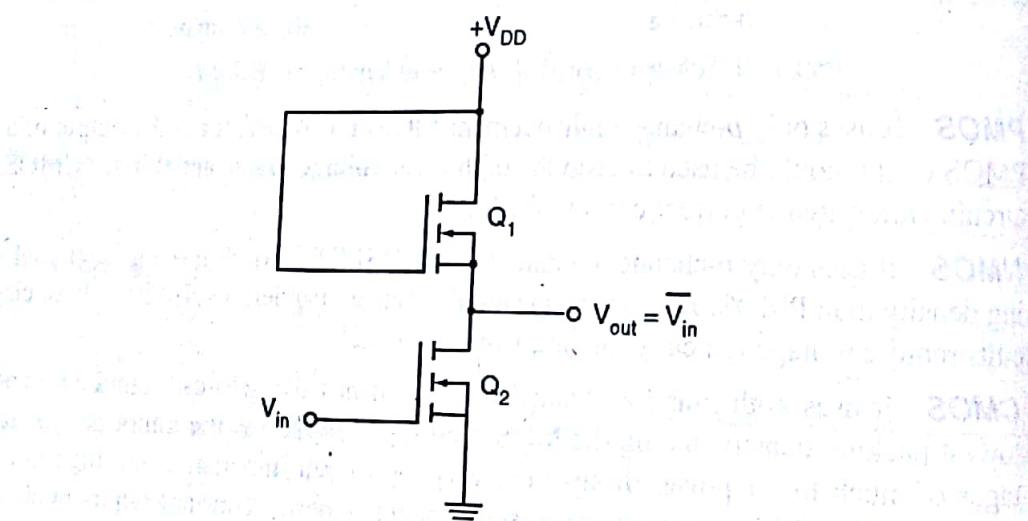
### 4.12.2 MOSFET Logic Circuits

For an *n*-channel MOS, supply voltage is of about +5V. The two voltage levels are a function of the threshold voltage  $V_T$ . The low level ranges anywhere from zero to  $V_T$ , and the high level ranges from  $V_T$  to  $V_{DD}$ . The *n*-channel gates usually employs positive logic.

Fig. 4.23 shows a MOSFET driver with a passive load resistor ( $R_D$ ). MOSFET acts as a switch depending on  $V_{in}$ , either low or high. It switches between saturation and cutoff. When  $V_{in}$  is low, MOSFET is cutoff and hence  $V_{out}$  is high. When  $V_{in}$  is high, MOSFET is saturated and hence  $V_{out}$  is low.



(a) MOSFET driver with passive load and its load line



(b) MOSFET driver with active load

Fig. 4.23

In MOS technology, MOSFET fabrication is easier than resistors. For this reason, the resistor  $R_D$  in Fig. 4.23(a) is replaced by an *n*-channel MOSFET as shown in

Fig. 4.23(b). The gate of the upper MOSFET is connected to the drain; this MOSFET always conducts and behaves like the resistor,  $R_D$ . The upper MOSFET has a resistance ten times greater than that of the lower MOSFET. When the input voltage is low (below  $V_T$ ),  $Q_2$  turns OFF. Since  $Q_1$  is always ON, the output voltage is at about  $V_{DD}$ . When the input voltage is high (above  $V_T$ ),  $Q_2$  turns ON. Current flows from  $V_{DD}$  through the active load resistor,  $Q_1$ , and into  $Q_2$ . Thus, the circuit behaves as an inverter. The geometry of the two MOS devices must be such that the resistance of  $Q_2$  when conducting is much less than the resistance of  $Q_1$  to maintain the output  $Y$  at a voltage below  $V_T$ .

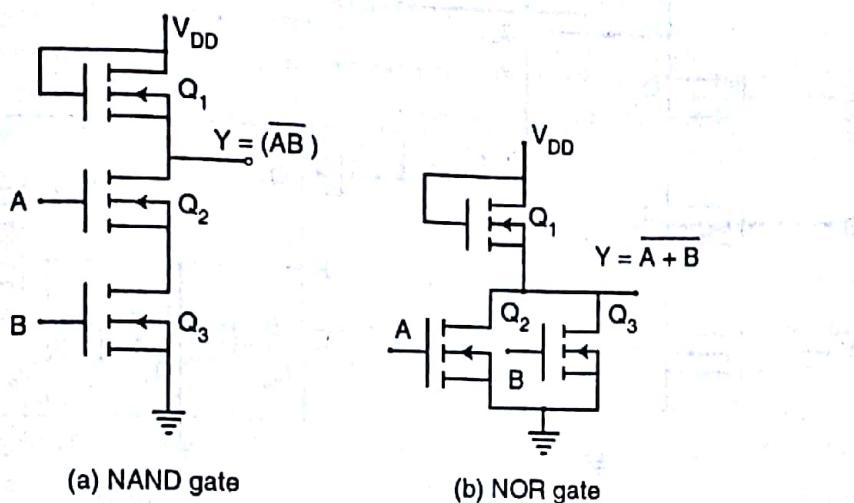


Fig. 4.24 n-channel MOS logic circuits

The circuit of NMOS NAND gate that uses three transistors in series is shown in Fig. 4.24(a). Inputs  $A$  and  $B$  must be high for all transistors to conduct and cause the output to go LOW. If either of the inputs is LOW, the corresponding transistor is turned OFF and the output is HIGH. Again, the series resistance formed by the two active MOS devices must be much less than the resistance of the load of MOSFET.

The NOR gate that uses two NMOS transistors in parallel is shown in Fig. 4.24(b). If either of the inputs is HIGH, the corresponding MOS transistor conducts and the output is LOW. If the inputs are LOW, both MOSFETs are OFF, and hence the output is HIGH.

Fig. 4.25(a) illustrates a 3-input NMOS AND gate with an additional output inverter. The transistors  $Q_1$  and  $Q_2$  serve as loads. If any one input is at 0V, then the corresponding input transistor is in OFF state, resulting in conduction of  $Q_6$ . This leads to 0V at the output. If all inputs are at a high voltage, the MOSFETs  $Q_3$ ,  $Q_4$  and  $Q_5$  will be ON and they offer a low resistance compared to the resistance of the load transistor  $Q_1$ , then the transistor  $Q_6$  goes OFF. The output is now at a high level. Hence, the circuit acts as an AND gate.

A 3-input n-channel MOS OR gate with an output inverter is shown in Fig. 4.25(b). A 3-input NMOS OR gate with an output inverter is shown in Fig. 4.25(b). Transistors  $Q_1$ ,  $Q_4$ ,  $Q_5$  and  $Q_6$  form a NOR gate, and transistors  $Q_2$  and  $Q_3$  form an inverter. Transistors  $Q_1$  and  $Q_2$  act as loads. If the voltage is equal to  $V_{DD}$  at one of the inputs, the corresponding transistor is ON and allows the current to flow. The voltage at point K then drops close to zero, the transistor  $Q_3$  switches OFF, and

the output voltage approaches the level  $V_{DD}$ . If all the inputs are LOW (at 0V), the transistors  $Q_4$ ,  $Q_5$  and  $Q_6$  turn OFF, and the voltage at point K comes close to  $V_{DD}$ . The transistor  $Q_3$  then switches ON and the output drops to zero. Hence, this circuit performs the OR function.

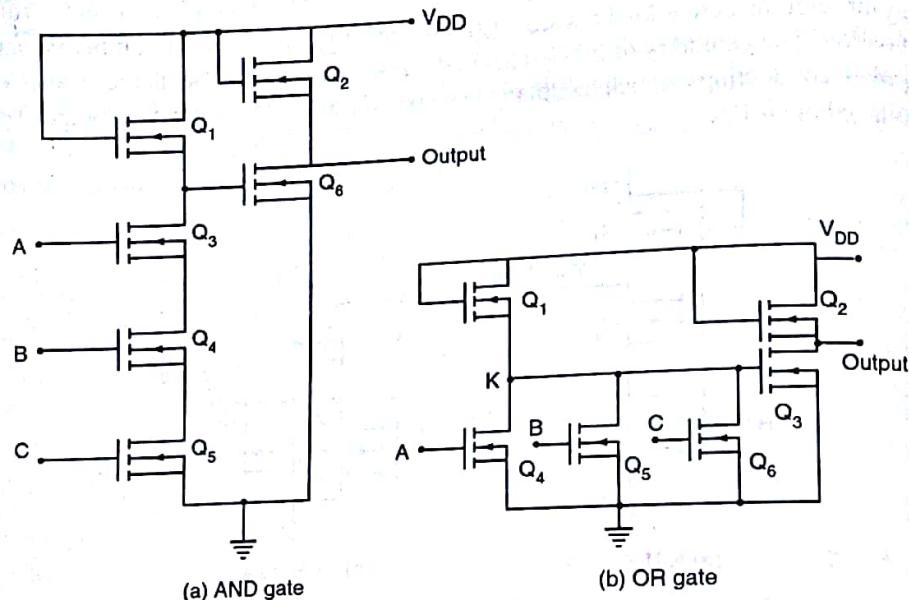


Fig. 4.25 n-channel MOS logic circuits

#### 4.12.3 Characteristics of MOS Logic

MOS logic families are slower in operating speed, require much less power, have a better noise margin and a higher fan-out.

**Operating speed** A typical NMOS NAND gate has a propagation delay of 50ns. The combination of large  $R_{out}$  and large  $C_{load}$  serves to increase switching time.

**Noise margin** Typically NMOS noise margins are around 1V.

**Fan-out** The fan-out capabilities of MOS logic would be virtually unlimited because of the extremely high input resistance at each MOSFET input. MOS logic can easily operate at a fan-out value of 50.

**Power drain** MOS logic circuits draw small amount of power because of the relatively large resistance being used.

**Process complexity** MOS logic is the simplest logic family when it comes to fabrication since it uses only one basic element, an NMOS (or PMOS) transistor. It does not require resistors, diodes, etc. This characteristic together with its lower power dissipation ( $P_D$ ) makes it ideally suited for LSI, and this is where MOS logic has made its greatest impact in the digital field.

#### 4.13 C

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### 4.13 COMPLEMENTARY MOS LOGIC

Complementary Symmetry Metal-oxide Semiconductors, COSMOS or CMOS, are logic gates made using both PMOS and NMOS transistors. The basic gates employ both *p*-and *n*-channels enhancement mode complementary symmetry MOSFETs. The power consumption of CMOS under static conditions is extremely low. CMOS logic circuits excel PMOS and NMOS logic elements in a number of features like extremely small d.c. power dissipation, enhanced noise immunity, high fan-out capability and ease of interfacing (compatibility with other logic circuits). CMOS circuits are used both in logic circuits and memory devices. The source terminal of the *p*-channel device is at  $V_{DD}$ , and the source terminal of the *n*-channel device is at ground. The systems employing CMOS transistors require only one power supply source of a wide range of voltages, from +3 to +15V. The CMOS fabrication process is simpler than TTL and has a greater packing density, therefore, permitting more circuitry in a given area and reducing the cost per function.

#### 4.13.1 CMOS Inverter

Just as in the case of ordinary MOS gate, the inverter is basic to the CMOS gate. A basic inverter connection is shown in Fig. 4.26. The driver is transistor  $Q_2$  which is the *n*-channel, and  $Q_1$  (the *p*-channel device) acts as the load. Notice that drains are connected together to provide the output and that the source and substrate are connected together. The source of *p*-channel device is connected to  $+V_{DD}$  and the source of *n*-channel is connected to ground. The gates of the two devices are connected together as a common input. It is important to note that the output voltage is equal to the supply voltage and the current flows through the circuit only during switching of the input voltage from one level to the other.

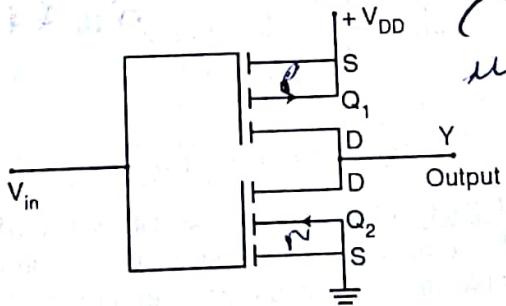


Fig. 4.26 CMOS inverter

CMOS  
used in logic dev.  
& memory dev.

**Operation** When  $V_{in}$  is LOW,  $Q_2$  is OFF but  $Q_1$  is ON. This means the output voltage is HIGH. On the other hand, when  $V_{in}$  is HIGH,  $Q_2$  is ON and  $Q_1$  is OFF. In this case, the output voltage is LOW. Since the output voltage is always opposite in phase to the input voltage, the circuit acts as an inverter.

The operation of CMOS transistors can be described by the following rules:

*n*-channel MOSFETs are turned ON by a positive gate voltage.

*p*-channel MOSFETs are turned ON by a negative gate voltage.

$V_{in} \text{ low} \rightarrow Q_2 \text{ OFF}, Q_1 \text{ ON}$   
 $V_{in} \text{ high} \rightarrow Q_2 \text{ ON}, Q_1 \text{ OFF}$

The CMOS inverter can be modified to build other CMOS logic circuits. A CMOS circuit is ideal in a number of ways. First, it needs extremely low power to operate the circuit. Since either one of the MOS devices is OFF when the input is in LOW or HIGH state, only the leakage current in the order of nanoamperes flows through the circuit and the power dissipation of the CMOS devices is typically in the range of nanowatts. This low power consumption is the reason for the popularity of CMOS devices in pocket calculators, digital wristwatches, and portable microcomputers.

Fan-out for CMOS circuits is ideally infinite since no loading occurs when it is connected to the gate of enhancement MOSFET. Practical values of fan-out greater than 50 are typical.

Propagation delay of a CMOS gate is typically about 25 to 100 ns, depending on the particular device. It increases with greater load capacitance.

#### 4.13.2 CMOS NAND Gate (74C00)

A two-input NAND gate which consists of two *p*-type units in parallel and two *n*-type units in series is shown in Fig. 4.27. Notice that  $Q_1$  and  $Q_2$  form one complementary connection;  $Q_3$  and  $Q_4$  form another.

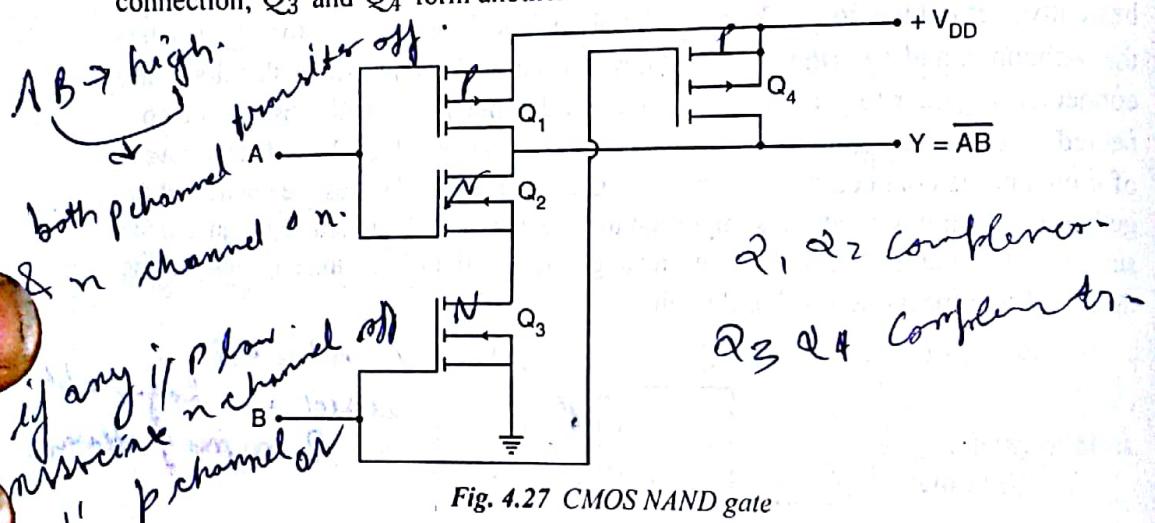


Fig. 4.27 CMOS NAND gate

If both inputs are HIGH, both *p*-channel transistors turn OFF and both *n*-channel transistors turn ON. The output has a low impedance to ground and produces a LOW state. If any input is LOW, the associated *n*-channel transistor is turned OFF and the associated *p*-channel transistor is turned ON. The output is coupled to  $V_{DD}$  and goes to the HIGH state. This functions as a logic NAND gate. The 74C00 is a quad 2-input NAND gate.

To produce the positive AND function, the output of the CMOS NAND gate can be connected to a CMOS inverter.

#### 4.13.3 CMOS NOR Gate

A two-input CMOS NOR gate using a pair of PMOS transistors ( $Q_1$  and  $Q_2$ ) and NMOS transistors ( $Q_3$  and  $Q_4$ ) is shown in Fig. 4.28. Of the two inputs,  $A$  and  $B$ , either of the inputs can turn ON the PMOS or NMOS device connected to it.

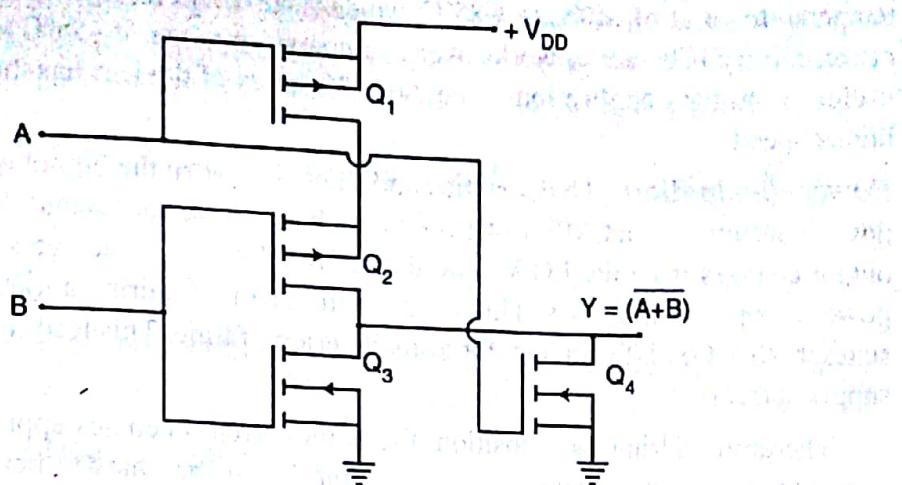


Fig. 4.28 CMOS NOR gate

When both inputs are LOW, both PMOS devices are driven ON and both NMOS devices OFF. The output is coupled to  $V_{DD}$  and goes to the HIGH state. If any input is HIGH, the associated  $p$ -channel transistor is turned OFF and the associated  $n$ -channel transistor turns ON. This connects the output to the ground causing a LOW output. Thus this circuit functions as a NOR gate. A CMOS OR gate can be formed by combining the output of the CMOS NOR gate with a CMOS inverter.

#### 4.13.4 CMOS Series

There are several series of the CMOS digital logic family. The original design of CMOS ICs is recognised from the 4000 number designation. The 74C series are pin-and-function compatible with TTL devices having the same number. The performance characteristics of the 74C series are about the same as the 4000 series. CMOS IC type 74C04 has six inverters with the same pin configuration as TTL type 7404. The 74HC series operates at higher speeds than the 74C series. The 74HCT series is electrically compatible with TTL ICs. This means that the circuit in this series can be connected to inputs and outputs of TTL ICs without the need of additional interfacing circuits. The commercially available CMOS series are listed in Table 4.5.

Table 4.5 Various series of the CMOS logic family

CMOS series	Prefix	Example
Original CMOS	40	4009
Pin compatible with TTL	74 C	74 C04
High-speed and pin compatible with TTL	74 HC	74 HC04
High-speed and electrically compatible with TTL	74 HCT	74 HCT04

#### 4.14 CHARACTERISTICS OF CMOS

The first CMOS logic series was produced by RCA and is known as the 4000 series, which was later developed by other manufacturers. At present, several manufacturers have developed a CMOS series which is pin-for-pin compatible with TTL. This is the 74C00 series and it contains devices that have the same pin assignments and logic operations as their TTL counterparts. Any device in the 74C00 series works over a

temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , which is sufficient for most commercial applications. The 54C00 series works over a temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and is useful for military applications. The 74HC00 series of devices has the advantage of higher speed.

**Power dissipation** Under static conditions (i.e. when the output is constant), the power consumed by a CMOS gate is extremely small (in nanowatts). When a CMOS output changes from the LOW state to the HIGH state (or vice versa), the average power dissipation increases. This is due to the fact that, during a transition between states, both MOSFETs conduct for a small period of time. This leads to a spike in the supply current.

Therefore, during the transition, the drain current becomes appreciable. Moreover, any stray capacitance across the output has to be charged before the output voltage can change. This capacitive charging draws additional current from the supply, thereby increasing the instantaneous power dissipation.

The average power dissipation of a CMOS device whose output is continuously changing is called the *active power dissipation*. This power dissipation per gate increases with frequency and supply voltage. The power consumption of a CMOS gate is around 10mW in the MHz region. Thus, CMOS loses its advantages at higher frequencies.

**Propagation delay time** The propagation delay of a standard CMOS gate ranges from 25 to 150ns, with the exact value depending on the power supply voltage and other factors. A CMOS NAND gate typically has a propagation delay time of about 25ns when  $V_{DD} = 10\text{V}$ , and 50ns when  $V_{DD} = 5\text{V}$ .

**Voltage levels** CMOS can be operated over a supply voltage range of 3 to 15V. A supply voltage of 9 to 12V can be used to obtain the overall best performance of a CMOS gate in respect of high speed and noise immunity. When CMOS is being used with TTL, the  $V_{DD}$  supply voltage is made 5V so that the voltage levels of the two families are the same.

**Noise margin** In CMOS series, the noise margin is typically about 45% of the supply voltage  $V_{DD}$ . They have the same noise margin in both HIGH and LOW states. A  $V_{DD}$  of 5V guarantees a 2.25V noise margin.

**Floating inputs** A floating TTL input is equivalent to a high input. If a CMOS input is floated, a possible noise problem is set up and there is excessive power dissipation. Therefore, it is necessary to connect all the input pins of the CMOS devices to some voltage level, preferably to ground or  $V_{DD}$ .

**Sourcing and sinking** When a standard CMOS driver output is LOW, the current from the CMOS load to the driver is only  $1\ \mu\text{A}$ . This indicates that the CMOS driver has to sink only  $1\ \mu\text{A}$ . Similarly, when the CMOS driver output is HIGH, the CMOS devices are:

$$\begin{aligned} I_{IL(\max)} &= -1\ \mu\text{A}; & I_{IH(\max)} &= 1\ \mu\text{A} \\ I_{OL(\max)} &= 10\ \mu\text{A}; & I_{OH(\max)} &= 10\ \mu\text{A} \end{aligned}$$

**Fan-out** The fan-out of CMOS gates depends on the type of load being connected. If a standard CMOS drives another standard CMOS, the fan-out can be calculated from the input and output currents of the standard CMOS gate given above.

$$\text{Considering low output state: } \frac{I_{OL,\max}}{I_{IL,\max}} = \frac{10\text{ A}}{1\text{ A}} = 10$$

$$\text{Considering high output state: } \frac{I_{OH,\max}}{I_{IH,\max}} = \frac{10\text{ A}}{1\text{ A}} = 10$$

Therefore, 10 standard CMOS gates can be connected to the output of another standard CMOS gate. Thus, the fan-out of standard CMOS gate is 10.

#### 4.15 BiCMOS LOGIC CIRCUITS

BiCMOS logic circuits employ the recent development of digital technology in the silicon fabrication process that combines the speed and driving capability of bipolar junction transistors with the density and low power dissipation of CMOS devices. BiCMOS technology has been used to develop low voltage analog circuits, VLSI circuits and ASICS (Application Specific Integrated Circuits). BiCMOS circuits have little degradation in density. Because of the low output impedance and increased charging and discharging currents of BJTs, the propagation delay of the BiCMOS gate does not increase much as in the CMOS gates. Also, it has good compatibility of the technology with ECL and TTL levels with ready interfacing and little loss of switching speed. With high current capability and faster response, BiCMOS circuits can be used in place of CMOS buffers. They are widely used in ASICS and high density gate arrays. In terms of cost, power and density, BiCMOS technology can be compared with ECL.

**Basic BiCMOS inverter** The circuit of a basic BiCMOS inverter is shown in Fig. 4.29. The complementary pair of PMOSFET ( $Q_1$ ) and NMOSFET ( $Q_2$ ) form the inverter, and the pair of matching NPN transistors  $T_1$  and  $T_2$  form the active pull-up / pull-down driver stage. The circuit operation is analysed for a capacitive load as explained below.

When the logic input is LOW, the PMOS ( $Q_1$ ) is turned ON and NMOS ( $Q_2$ ) is in cut-off. As no channel is formed in  $Q_2$ , the base current for  $T_2$  is zero and hence  $T_2$  is OFF. At the same time, a low resistance conducting channel is formed in  $Q_1$  which provides base current for  $T_1$ . Thus,  $T_1$  operates in the active mode and it supplies  $(\beta + 1)$  times the base current at the emitter to charge the load capacitance. Hence the output voltage is less than the supply voltage  $V_{DD}$  by the base emitter junction voltage  $V_{BE}$  of  $T_1$ . Therefore,  $V_{OH} = V_{DD} - V_{BE}$ . Thus, for a LOW input, the output  $V_0$  is in HIGH state.

When the logic input is HIGH,  $Q_2$  is turned ON while  $Q_1$  is turned OFF. Hence, a low resistance conducting channel is formed in  $Q_2$  that supplies base current to

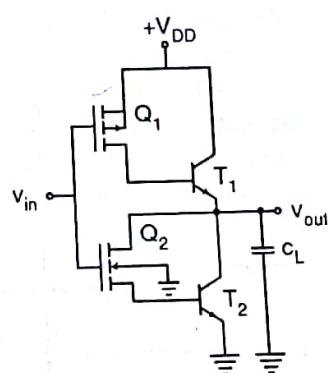


Fig. 4.29 Basic BiCMOS inverter

switch ON the transistor  $T_2$ .  $T_2$  causes a large discharge current from the capacitor. Thus, the high-to-low transition occurs rapidly. When the output voltage reaches the base-emitter cut-in voltage of  $T_2$ , i.e.  $V_{OL} \approx V_{BE}$ , no further discharge takes place. Thus, for a HIGH input, the output  $V_{out}$  is in LOW state and acts as an inverter.

**BiCMOS NAND and NOR gates** The transfer characteristics and switching speed of the basic inverter can be improved by providing paths for discharging the excess carriers from the bases of  $T_1$  and  $T_2$  with additional NMOS devices, resulting in each BJT OFF while the other is ON. The circuit of the conventional BiCMOS inverter is shown in Fig. 4.30. This circuit can be modified to implement BiCMOS NAND and NOR gates as shown in Fig. 4.31(a) and (b) respectively.

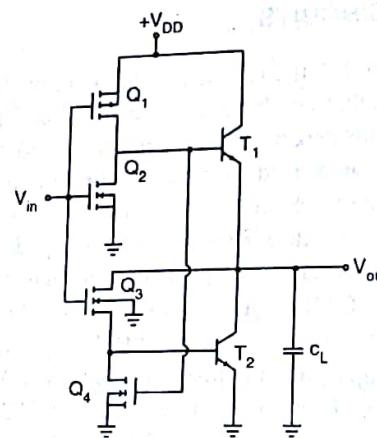
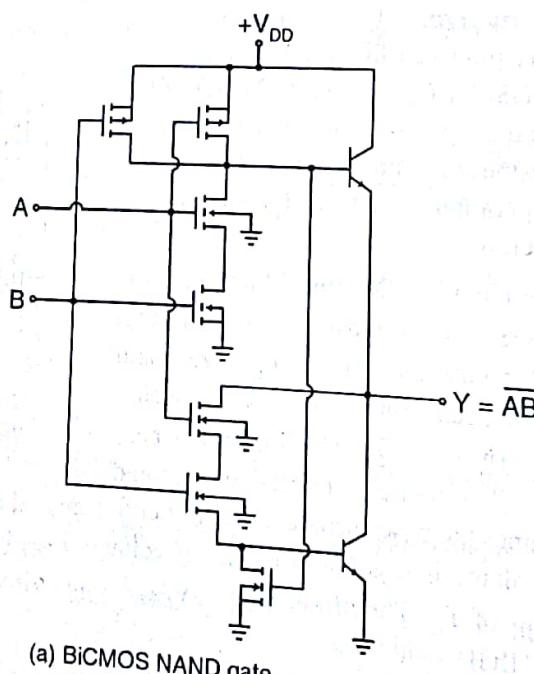


Fig. 4.30 Conventional BiCMOS inverter



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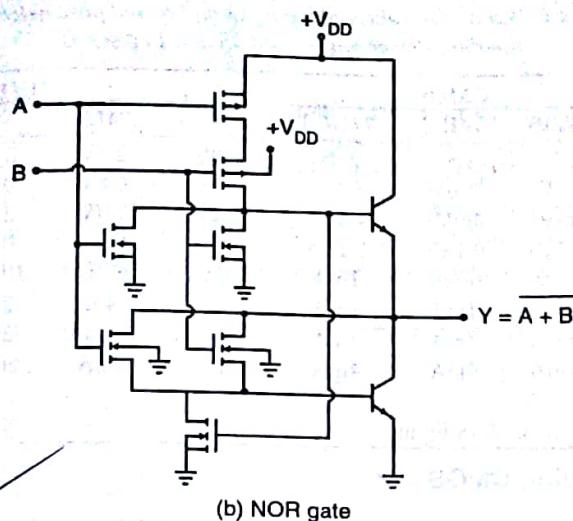


Fig. 4.31

#### 4.16 COMPATIBILITY OR INTERFACING

The output(s) of a circuit or a system should match the input(s) of another circuit or system that has different electrical characteristics. This is referred to as *compatibility*. Interfacing between different logic families is important for compatibility. An interface circuit is one that is connected between the driver and the load; its function is to take the driver output signal and condition it so that it is compatible with the requirements of the load.

The circuit designer must take care in matching the current and voltage characteristics of the two circuits of different logic families connected together. For example, when one circuit using only negative voltage ( $-V$ ) for logic 1 and another using positive voltage ( $+V$ ) for logic 1 are to be inter-connected, they need interface circuit. An interface or buffer circuit between two different logic families is used to match the output characteristics of the driver with the input characteristics of the load. Also, interfacing may be needed between a low speed family and a high speed family. Examples are (i) the serial output of a TTL shift register may need to be interfaced with an ECL gate for high speed processing and (ii) an ECL counter may need to be interfaced with a standard TTL circuit that drives a display.

Table 4.6 contains the worst case values of the input and output parameters for standard devices in the CMOS and TTL series.

##### 4.16.1 Interfacing CMOS with TTL

The method of connecting a driving device to a loading device is known as *interface*. We know that TTL devices need a supply voltage of 5V and CMOS devices need a supply voltage that ranges from 3 to 15V. As the supply requirements are different, several interfacing schemes may be used.

**Table 4.6** Worst case values of the input and output parameters for standard devices in the CMOS and TTL series

Parameter	CMOS			TTL			
	4000B	74HC	74HCT	74	74LS	74AS	74ALS
$V_{IH}$ (min)	3.5V	3.5V	2.0V	2.0V	2.0V	2.0V	2.0V
$V_{IL}$ (max)	1.5V	1.0V	0.8V	0.8V	0.8V	0.8V	0.8V
$V_{OH}$ (min)	4.95V+	4.9V+	4.9V+	2.4V	2.7V	2.7V	2.7V
$V_{OL}$ (max)	0.05V+	0.1V+	0.1V+	0.4V	0.5V	0.5V	0.4V
$I_{IH}$ (min)	1mA	1mA	1mA	40mA	20mA	200mA	20mA
$I_{IL}$ (max)	1mA	1mA	1mA	1.6mA	0.4mA	2mA	100mA
$I_{OH}$ (min)	0.4mA	4mA	4mA	0.4mA	0.4mA	2mA	100mA
$I_{OL}$ (max)	0.4mA	4mA	4mA	16mA	8mA	20mA	8mA

Supply voltages = 5V  
+ CMOS driving only CMOS inputs.

#### 4.16.2 TTL Driving CMOS

**Supply voltage at 5V** One approach to TTL/CMOS interfacing is to use +5V as the supply voltage for both the TTL driver and the CMOS load. When a TTL gate output drives a CMOS input, there is no problem in the LOW state since  $V_{OL(\text{max})} = 0.4\text{V}$  for the TTL output and the CMOS input will accept voltage anywhere up to 1.5V for a LOW state. Thus, the CMOS load always interprets the TTL low-state drive as a LOW state. In the HIGH state, a problem can occur because the minimum TTL output voltage is 2.4V [i.e.  $V_{OH,\text{min}} = 2.4\text{V}$ ]. This 2.4V results in indeterminate action at the CMOS input because it requires a minimum of 3.5V for a HIGH state [i.e.  $V_{IH,\text{min}} = 3.5\text{V}$ ]. Therefore, it is recommended that an *external* pull-up resistor  $R_p$  can be used as shown in Fig. 4.32. The effect of  $R_p$  is to raise  $V_{OH}$  from the TTL circuit to approximately +5V. For instance, when the TTL output is LOW, the lower end of  $R_p = 3.3\text{ K}\Omega$  is grounded. Therefore, the TTL driver sinks a current of roughly 1.5mA.

$$I = \frac{5\text{V}}{3.3\text{K}\Omega} = 1.52\text{mA}$$

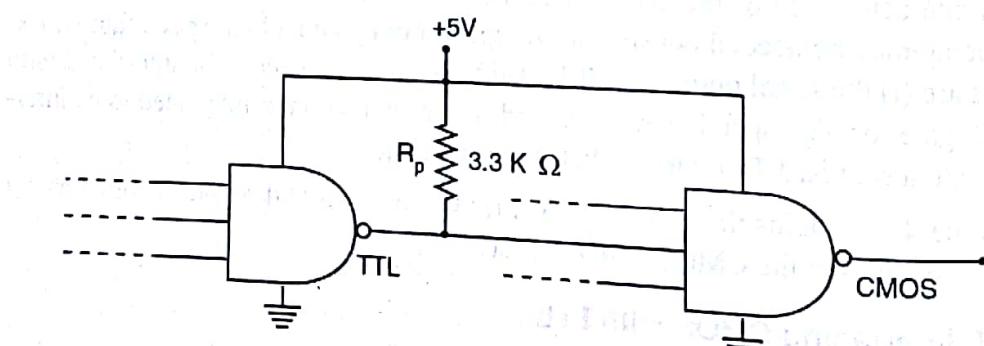


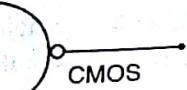
Fig. 4.32 TTL driver and CMOS load

The gate capacitance of the CMOS load has to be charged through the pull-up resistor,  $R_p$ . This slows down the switching speed. In order to increase the speed of is then determined by the maximum sink current of the TTL device, i.e.,  $I_{OL,\text{max}} = 16\text{ mA}$  and the maximum supply voltage ( $V_{cc}$ ) is 5.25V. Then,

parameters for  
series

TTL		
LS	74AS	74ALS
V <sub>DD</sub>	2.0V	2.0V
V <sub>AV</sub>	0.8V	0.8V
V <sub>UV</sub>	2.7V	2.7V
V <sub>UV</sub>	0.5V	0.4V
I <sub>DD</sub>	200mA	20mA
I <sub>AV</sub>	2mA	100mA
I <sub>UV</sub>	2mA	100mA
I <sub>A</sub>	20mA	8mA

Interfacing is to use +5V as load. When a TTL gate is in the LOW state since it will accept voltage anyways interprets the TTL can occur because the [ ]. This 2.4V results in minimum of 3.5V for a need that an external pull-up of  $R_p$  is to raise  $V_{OH}$  when the TTL output is the TTL driver sinks a



through the pull-up increase the speed of minimum resistance TTL device, i.e., 25V. Then,

$$R_{\min} = \frac{5.25V}{16mA} = 328\Omega \approx 330\Omega$$

**Different supply voltages** The performance of CMOS gates deteriorate at lower voltages. This is due to the increase in propagation delay time and decrease in noise immunity. Therefore, a supply voltage that ranges from 9 to 12V can be applied to CMOS devices for better performance. One way of using higher supply voltage is with an open-collector TTL driver, as shown in Fig. 4.33. The open-collector is connected to a supply voltage of +12V through a pull-up resistance of 6.8 KΩ.

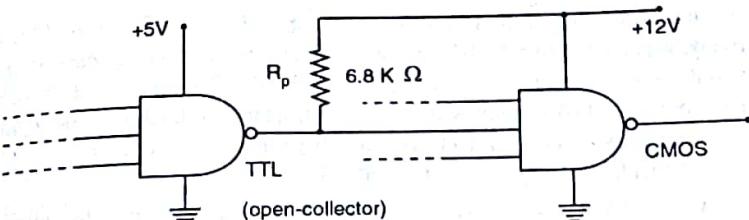


Fig. 4.33 Open-collector TTL driver allows higher CMOS supply voltage

When the TTL output is LOW, the lower end of  $R_p$  is approximately at 0V. The TTL device then has to sink a current approximately equal to 1.76mA.

$$I_{\text{sink}} = \frac{12V}{6.8K\Omega} = 1.76mA$$

When the TTL output is HIGH, the open-collector output increases passively to +12V. In conclusion, TTL outputs are compatible with CMOS input states.

#### 4.16.3 CMOS Driving TTL

To interface a CMOS gate with a TTL gate, the low state output voltage of the CMOS gate must be less than 0.8V, the maximum allowable low state input voltage of the TTL gate. Similarly, the high state output of the CMOS gate must be higher than 2V, the minimum allowable high state input voltage of the TTL gate.

Consider a CMOS driving a low power Schottky TTL gate, shown in Fig. 4.34. When CMOS output is HIGH, there is no problem since  $V_{OH} \approx V_{DD} = +5V$ , which is an acceptable HIGH input for the TTL gate. When the CMOS output is LOW, a problem occurs because of  $I_{IL}$  of the Schottky TTL gate. The worst case output currents for a CMOS gate are:

$$I_{OL,\max} = 360\mu A; I_{OH,\max} = -360\mu A$$

A low power Schottky device has the following worst-case input currents:

$$I_{IL,\max} = -360\mu A; I_{IH,\max} = 20\mu A$$

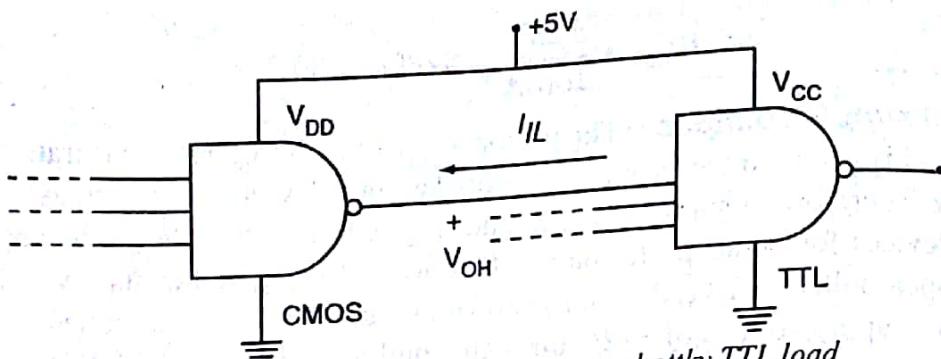


Fig. 4.34 CMOS driver and low power schottky TTL load

From the above output and input currents of CMOS and Schottky TTL gates respectively, it is clear that a CMOS driver can sink  $360\mu\text{A}$  current which is exactly the low state input current for the low power Schottky TTL gate. But, the CMOS driver can source  $360\mu\text{A}$  current which is much higher than the high state input current for the low power Schottky TTL. Hence, only one low power Schottky TTL can be connected to a CMOS driver (i.e. fan-out = 1).

However, a CMOS can not drive a standard TTL. The worst-case low state input current (i.e.,  $I_{IL}$ ) of a standard TTL gate is  $-1.6\text{mA}$ . But, a CMOS driver with low output can sink only  $360\mu\text{A}$  current. Hence, a standard TTL can not be connected to the output of a CMOS gate.

The above problems can be eliminated by connecting a CMOS buffer, a chip with larger output currents, directly to the CMOS driver output. For example, if a CMOS buffer IC 74C902 is connected at the output of the CMOS driver, then two standard TTL gates can be connected. This is due to the following worst-case output currents of CMOS buffer:

$$I_{OL,\max} = 3.6\text{ mA}, \quad I_{OH,\max} = -800\mu\text{A}$$

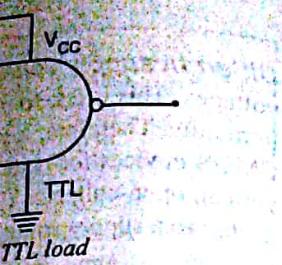
Since  $I_{IL,\max} = -1.6\text{mA}$  for a standard TTL gate, two standard TTL gates can be connected.

#### 4.17 COMPARISON OF LOGIC GATES

Each logic family projects different characteristics in terms of static and dynamic performance, size and cost. Table 4.7 provides a brief comparison of typical performance characteristics of the more commonly used families. Note that some of the values differ because the table contains only average values.

Table 4.7 Comparison of logic families

Characteristics	RTL	DTL	TTL	STTL (Active (High pull-up) speed)	ECL	$I^2L$	MOS	CMOS
	NOR	NAND (NOR)	NAND	NAND	NOR- OR	NAND	NAND- NOR	NAND- NOR
Basic gate(s)								
Logic swing with 5V power supply(V)	2.5	4.7	3.8	3.8	3.6	3.6	3.8	5
Fan-out	5	8	12	12	16	12	12	12
Power dissipation(mW)	20	9	10	2	25	0.1 to 100	0.1	0.002
Propagation delay(ns)	12	12	10	3	2	0.7 to 20	1	1
Noise immunity(V)	0.3	0.3	0.4	0.5	0.4	0.5	2.5	2.5



and Schottky TTL gates current which is exactly L gate. But, the CMOS the high state input cur- power Schottky TTL can

orst-case low state input  
CMOS driver with low  
can not be connected to

MOS buffer, a chip with  
for example, if a CMOS  
buffer, then two standard  
first-case output currents

Standard TTL gates can be

of static and dynamic  
comparison of typical perfor-  
Note that some of the

<sup>2</sup>L MOS CMOS

ND	NAND- NOR	NAND- NOR
6	3.8	5
2	12	12
100	0.1	0.002
20	1	1
4	2.5	2.5

**Example 4.1** For the DTL NAND gate shown in Fig. E4.1,  $V_{BE(sat)} = 0.8V$ ,  $V_y = 0.5V$ ,  $V_{CE(sat)} = 0.2V$ , the drop across the conducting diode is  $0.7V$  and  $V_y$  (diode) =  $0.6V$ . The inputs of this switch are obtained from the outputs of similar gates.

- (a) Verify that the circuit functions as a positive NAND and calculate  $h_{FE} \text{ (min)}$ .

(b) Will the circuit operate properly if  $D_2$  is not used?

(c) Calculate the noise margin if all the inputs are HIGH.

(d) Calculate the noise margin if at least one input is LOW.

Assume for the moment that  $Q$  is not loaded by a following stage.

(e) Calculate fan-out.

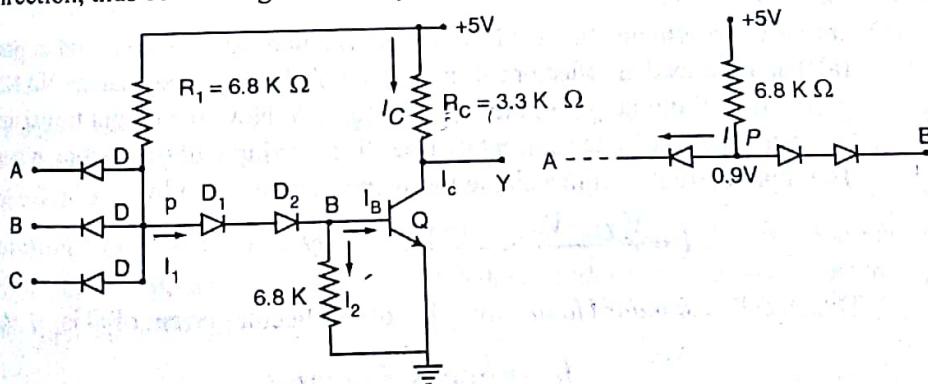
(f) Obtain average power.

**Solution (a)** The logic levels are  $V_{CE(sat)} = 0.2\text{ V}$  for the logic 0 state and  $V_{OC} = 5\text{ V}$  for the logic 1 state. If at least one input is in the 0 state, then the corresponding diode  $D$  conducts and  $V_P = 0.2 + 0.7 = 0.9\text{ V}$ . For the diodes  $D_1$  and  $D_2$  to conduct, a voltage of  $(2)(0.7) = 1.4\text{ V}$  is required. Hence, these diodes are cut-off and  $V_{BE} = 0$ . Therefore,  $Q$  is OFF and the output voltage is  $5\text{ V}$ , i.e.  $Y = 1$ . This confirms the first three rows of the NAND truth table.

If all inputs are HIGH, then all input diodes are OFF. Hence, both  $D_1$  and  $D_2$  conduct, and  $O$  is turned ON. The voltage at  $P$  is

$$V_P = V_{D1} + V_{D2} + V_{BE(\text{sat})}$$

Then, the voltage across each input diode is  $5V - 2.2V = 2.8V$  in the opposite direction, thus confirming that the input diode  $D$  is OFF.



*Fig. E4.1*

To find  $h_{FE(\min)}$ ,

$$I_1 = \frac{V_{CC} - V_P}{R_L} = \frac{5 - 2.2}{6.8 \times 10^3} = 0.412 \text{ mA}$$

$$I_2 = \frac{V_{BE(sat)}}{R_2} = \frac{0.8}{6.8 \times 10^3} = 0.112 \text{ mA}$$