DEBUG LOGIC

Additional debug logic is added in the block to assist post silicon debug. As per the block diagram complete RMS block is divided into various sub blocks. First stage has a pipelined multiplier, Second stage has an Adder block, third stage has a divider block and the last stage has Square root block. Output of each of these stages is then passed onto a 4X1 72 bit Multiplexer. Debug Multiplexer has two bit select lines to select the output of each stage. Each input is 72 bits. Output of this multiplexer is then captured in a debug register. Debug register is 72bits. Output of this register is then sent out serially.

Due to addition of this debug logic we have additional 3 ports at the top level.2 bit select line ports and one output port. We need one clock cycle to register the multiplexer output into the debug register. Data from the debug register is then sent out serially. By doing so we have reduced the port count at the top level. To debug the output of each stage we need to assert the correct values at the select line of the multiplexer and then capture this value in the debug register. We can then pass the serial output of the debug register onto debug analyzer to check the correctness of the result.

