**Name: Praveen Waliitagi**

**SJSU ID: 010059257**

**Exam Seat no: 59**

**Email ID :** [**praveen.waliitagi@sjsu.edu**](mailto:praveen.waliitagi@sjsu.edu)

This Readme File gives the details about my project folder organization and steps to run simulation and synthesis.

**Project** folder is organized as below

It has a top folder by name **s8sp**.

Inside **s8sp** folder I have various sub folders

1. **s8sp\_top** : which contains top file of the design (**s8sp.v**) and **filelist** of the design
2. **Ctrl\_block** : which contains the controller design file (**sys\_controller.v**)
3. **Data\_block** : which contains 3 sub folders
4. **Data\_block\_top (data\_block.v)**
5. **Alu\_block (alu\_block.v CLA8bit.v CLA\_N\_bit.v)**
6. **Reg\_blocks (addr\_reg.v data\_reg.v flag\_reg.v gen\_reg.v local\_ir\_reg.v program\_cnt\_reg.v)**
7. **S8sp\_tb** : which contains the testbench of the design **(tb\_s8sp.v)**
8. **Implementation** folder which contains various subfolder used for simulation and synthesis
9. **dc\_synth :** folder used to run synthesis
10. **ncsim :** folder used to run simulations using cadence ncsim tool
11. **rtl\_vcs :** folder used to run RTL simulations using vcs
12. **netlist\_vcs :** folder used to run netlist simulation using vcs

Steps for RTL simulations

1. Use the following command to simulate the design using NCSIM

***ncverilog +gui*** *Project/s8sp/data\_block/reg\_blocks/addr\_reg.v Project/s8sp/data\_block/reg\_blocks/data\_reg.v Project/s8sp/data\_block/reg\_blocks/flag\_reg.v Project/s8sp/data\_block/reg\_blocks/gen\_reg.v Project/s8sp/data\_block/reg\_blocks/local\_ir\_reg.v Project/s8sp/data\_block/reg\_blocks/program\_cnt\_reg.v Project/s8sp/data\_block/alu\_block/alu\_block.v Project/s8sp/data\_block/alu\_block/CLA8bit.v Project/s8sp/data\_block/alu\_block/CLA\_N\_bit.v Project/s8sp/data\_block/data\_block\_top/data\_block.v Project/s8sp/ctrl\_block/sys\_controller.v Project/s8sp/s8sp\_top/s8sp.v Project/s8sp/s8sp\_tb/tb\_s8sp.v*

1. Use the following command to run simulation using VCS

***vcs -RPP*** *Project/s8sp/data\_block/reg\_blocks/addr\_reg.v Project/s8sp/data\_block/reg\_blocks/data\_reg.v Project/s8sp/data\_block/reg\_blocks/flag\_reg.v Project/s8sp/data\_block/reg\_blocks/gen\_reg.v Project/s8sp/data\_block/reg\_blocks/local\_ir\_reg.v Project/s8sp/data\_block/reg\_blocks/program\_cnt\_reg.v Project/s8sp/data\_block/alu\_block/alu\_block.v Project/s8sp/data\_block/alu\_block/CLA8bit.v Project/s8sp/data\_block/alu\_block/CLA\_N\_bit.v Project/s8sp/data\_block/data\_block\_top/data\_block.v Project/s8sp/ctrl\_block/sys\_controller.v Project/s8sp/s8sp\_top/s8sp.v Project/s8sp/s8sp\_tb/tb\_s8sp.v*

**simv** file will be generated. Source this simv file on the terminal to run simulations.

Steps to run DC synthesis (Once inside **dc\_synth** folder)

1. ***dc\_shell -xg -f synthesis.script***

Synthesis.script file is in the dc\_synth folder which contains all the DC setup and constraint setting for the run.

Steps to run Netlist simulations using VCS

1. ***vcs -R -gui -y /apps/toshiba/sjsu/verilog/tc240c +libext+.tsbvlibp -f s8sp\_filelist***

Contents of s8sp\_file list is as below

s8sp\_netlist.v

tb\_s8sp.v