Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date: 3/4/2021

Name: B.Pravena	SRN: PES2UG19CS076	Section: B

Week#____9_____ Program Number: ____1__

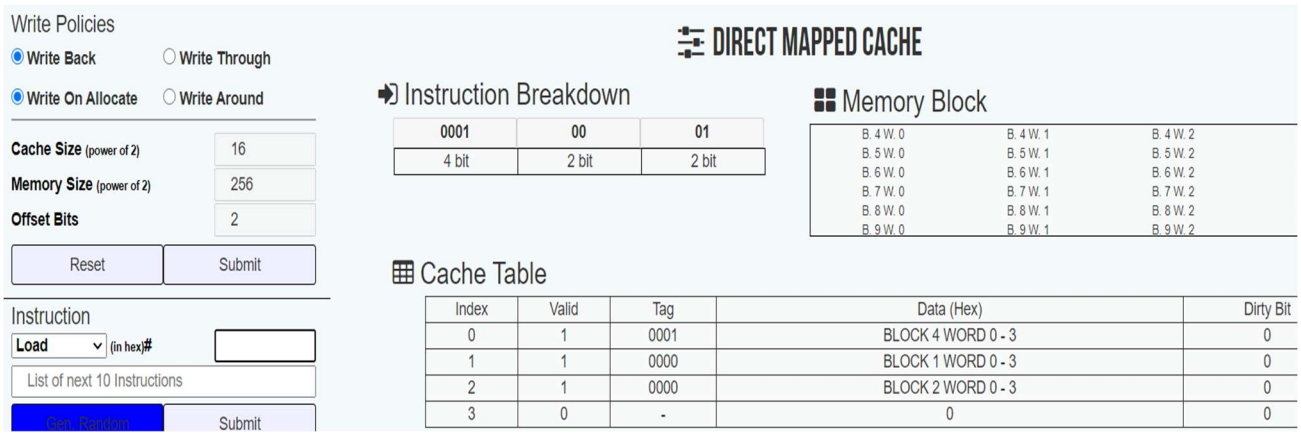
Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes. Find Number of bits in tag, index and offset. The processor generates requests as follows

1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

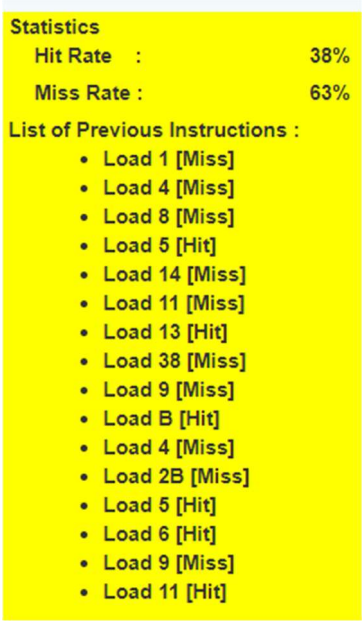
Find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

b) Screenshot showing the Cache Table



c) Screenshot showing hit and miss rates



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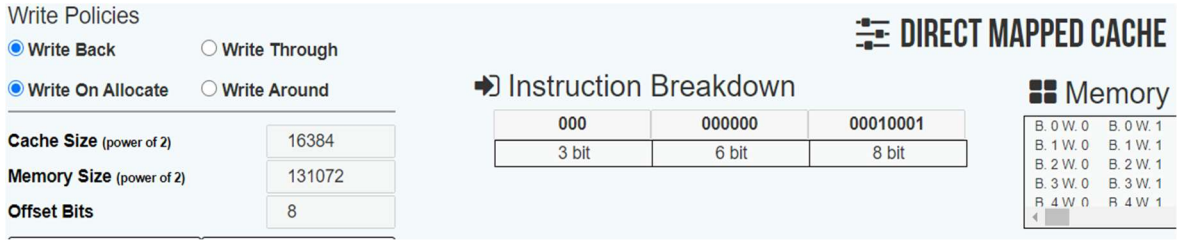
Name: B.Pravena	SRN: PES2UG19CS076	Section: B

Week#____9_____ Program Number: ____2__

Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Generate 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11 and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

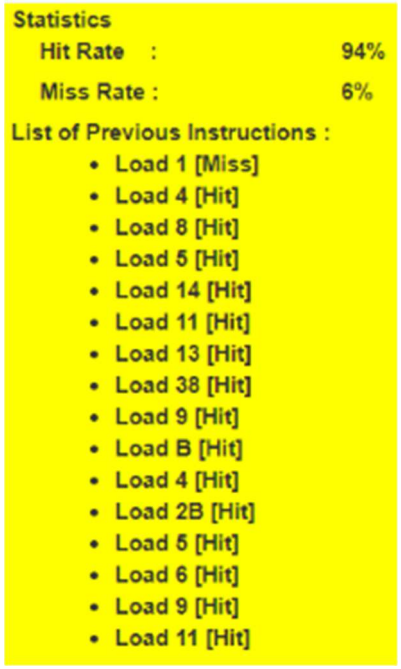


b) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty B
0	1	000	BLOCK 0 WORD 0 - 255	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0
32	0	-	0	0
33	0	-	0	0
34	0	-	0	0
35	0	-	0	0
36	0	-	0	0
37	0	-	0	0
38	0	-	0	0
39	0	-	0	0
40	0	-	0	0
41	0	-	0	0
42	0	-	0	0
43	0	-	0	0
44	0	-	0	0
45	0	-	0	0
46	0	-	0	0
47	0	-	0	0
48	0	-	0	0
49	0	-	0	0
50	0	-	0	0
51	0	-	0	0
52	0	-	0	0
53	0	-	0	0
54	0	-	0	0
55	0	-	0	0
56	0	-	0	0
57	0	-	0	0
58	0	-	0	0
59	0	-	0	0
60	0	-	0	0
61	0	-	0	0
62	0	-	0	0
63	0	-	0	0

c) Screenshot showing hit and miss rates



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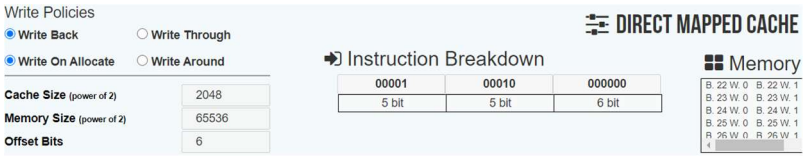
Name: B.Pravena	SRN: PES2UG19CS076	Section: B

Week#____9_____ Program Number: ____3__

A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.
(b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176
All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

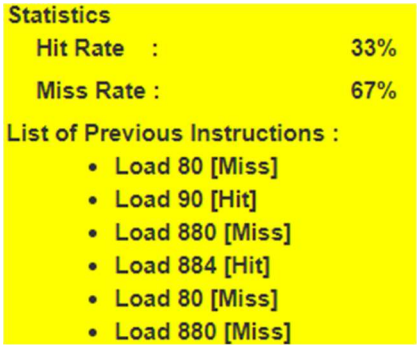


b) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	00001	BLOCK 22 WORD 0 - 63	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates



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4th Semester, Academic Year 2020-21

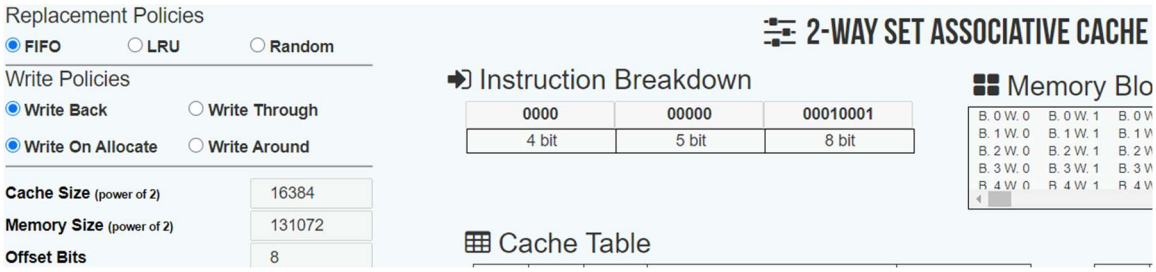
Date: 3/4/2021

Name: B.Pravena	SRN: PES2UG19CS076	Section: B

Week#____9_____ Program Number: ___4__

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Generate 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11 and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor



b) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 255	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates

Statistics

Hit Rate : 94%

Miss Rate : 6%

List of Previous Instructions :

- **Load 1 [Miss]**
- **Load 4 [Hit]**
- **Load 8 [Hit]**
- **Load 5 [Hit]**
- **Load 14 [Hit]**
- **Load 11 [Hit]**
- **Load 13 [Hit]**
- **Load 38 [Hit]**
- **Load 9 [Hit]**
- **Load B [Hit]**
- **Load 4 [Hit]**
- **Load 2B [Hit]**
- **Load 5 [Hit]**
- **Load 6 [Hit]**
- **Load 9 [Hit]**
- **Load 11 [Hit]**

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Date: 3/4/2021

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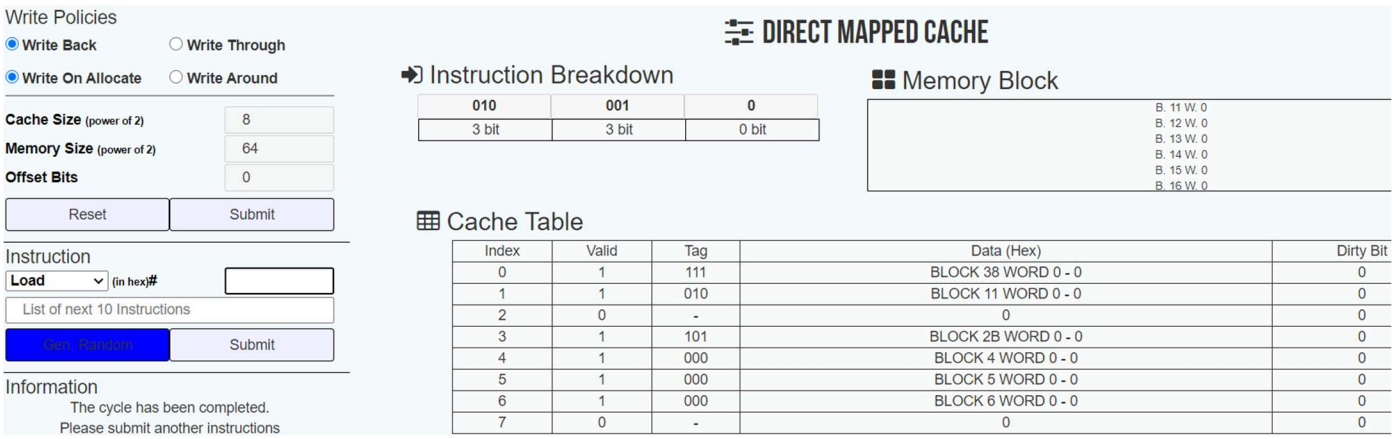
Week#____9_____ Program Number: ___5__

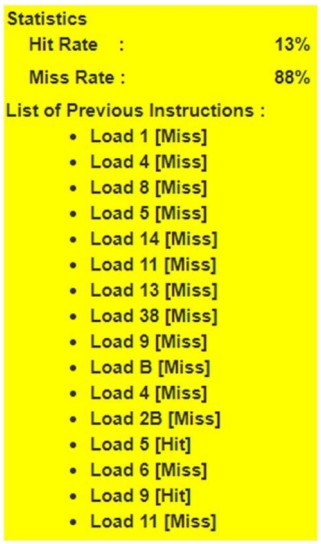
Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty. The addresses 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11 are generated by the CPU. All values in hexadecimal. Clearly label data that is replaced in cache lines and show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used.
The cache is mapped as

a) Direct Mapped
   I. Cache Address Table showing the splitup of the address fields for the requests generated by the processor
   II. Screenshot showing the Cache Table



Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	111	BLOCK 38 WORD 0 - 0	0
1	1	010	BLOCK 11 WORD 0 - 0	0
2	0	-	0	0
3	1	101	BLOCK 2B WORD 0 - 0	0
4	1	000	BLOCK 4 WORD 0 - 0	0
5	1	000	BLOCK 5 WORD 0 - 0	0
6	1	000	BLOCK 6 WORD 0 - 0	0
7	0	-	0	0

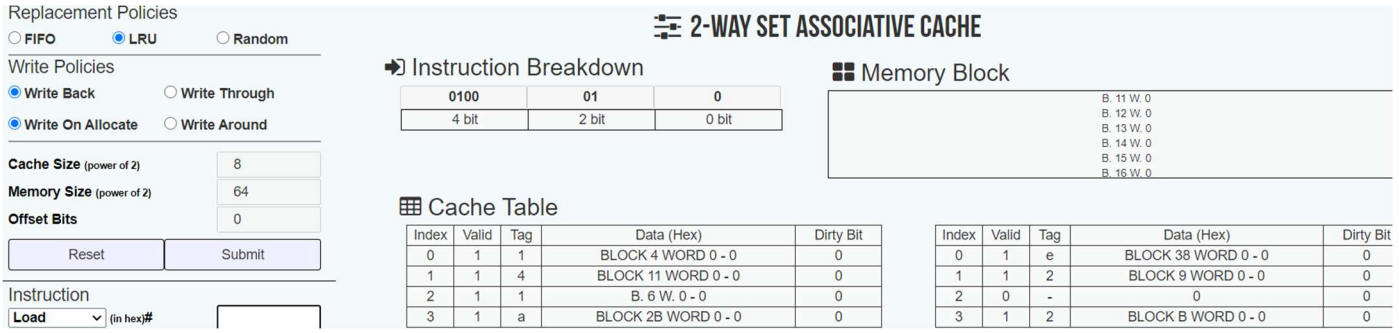
III. Screenshot showing hit and miss rates



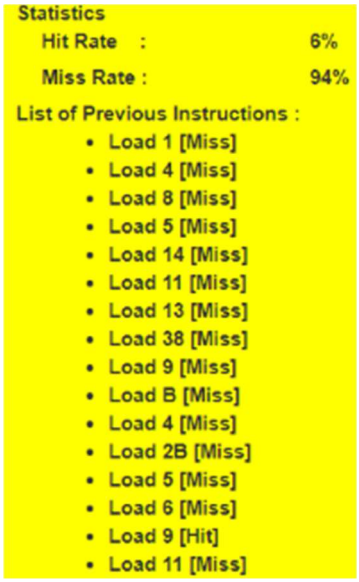
b) Two way set Associative

I. Cache Address Table showing the splitup of the address fields for the requests generated by the processor

II. Screenshot showing the Cache Table



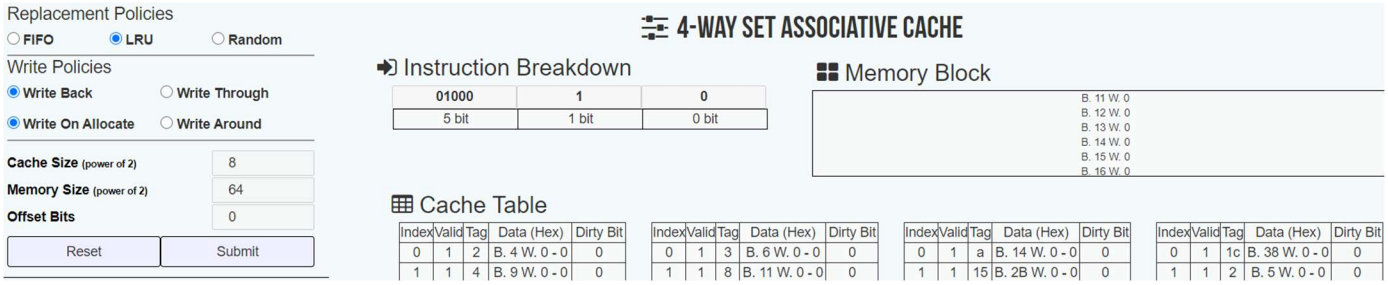
III. Screenshot showing hit and miss rates



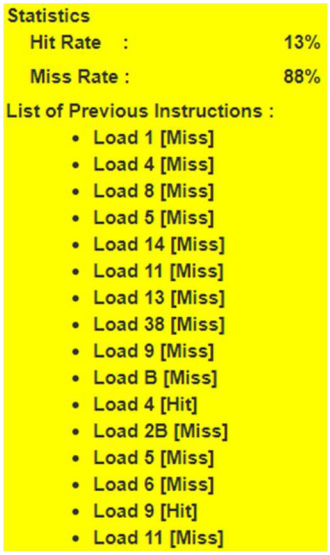
c) Four Way Set associative

I. Cache Address Table showing the splitup of the address fields for the requests generated by the processor

II. Screenshot showing the Cache Table



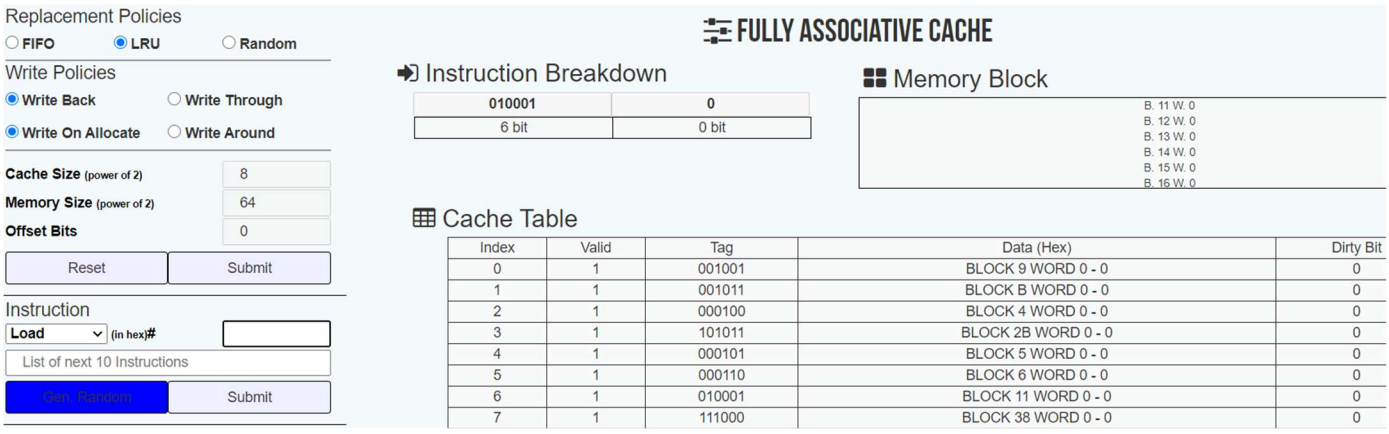
III. Screenshot showing hit and miss rates



d) Fully Associative

I. Cache Address Table showing the splitup of the address fields for the requests generated by the processor

II. Screenshot showing the Cache Table



III. Screenshot showing hit and miss rates