

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date: 3/4/2021

Name: B.Pravena	SRN: PES2UG19CS076	Section: B
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Week# ____9____

Program Number: ____1____

Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes. Find Number of bits in tag, index and offset. The processor generates requests as follows

1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

Find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

b) Screenshot showing the Cache Table

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 16

Memory Size (power of 2): 256

Offset Bits: 2

Reset Submit

Instruction

Load (in hex)#

List of next 10 Instructions

Generate Random Submit

DIRECT MAPPED CACHE

Instruction Breakdown

0001	00	01
4 bit	2 bit	2 bit

Memory Block

B. 4 W. 0	B. 4 W. 1	B. 4 W. 2
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2
B. 6 W. 0	B. 6 W. 1	B. 6 W. 2
B. 7 W. 0	B. 7 W. 1	B. 7 W. 2
B. 8 W. 0	B. 8 W. 1	B. 8 W. 2
B. 9 W. 0	B. 9 W. 1	B. 9 W. 2

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0001	BLOCK 4 WORD 0 - 3	0
1	1	0000	BLOCK 1 WORD 0 - 3	0
2	1	0000	BLOCK 2 WORD 0 - 3	0
3	0	-	0	0

c) Screenshot showing hit and miss rates

Statistics	
Hit Rate :	38%
Miss Rate :	63%
List of Previous Instructions :	
<ul style="list-style-type: none">• Load 1 [Miss]• Load 4 [Miss]• Load 8 [Miss]• Load 5 [Hit]• Load 14 [Miss]• Load 11 [Miss]• Load 13 [Hit]• Load 38 [Miss]• Load 9 [Miss]• Load B [Hit]• Load 4 [Miss]• Load 2B [Miss]• Load 5 [Hit]• Load 6 [Hit]• Load 9 [Miss]• Load 11 [Hit]	

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Week# 9 Program Number: 2

Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Generate 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11 and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

DIRECT MAPPED CACHE

➔ Instruction Breakdown

000	000000	00010001
3 bit	6 bit	8 bit

Memory

B. 0 W. 0	B. 0 W. 1
B. 1 W. 0	B. 1 W. 1
B. 2 W. 0	B. 2 W. 1
B. 3 W. 0	B. 3 W. 1
R. 4 W. 0	R. 4 W. 1

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

16384

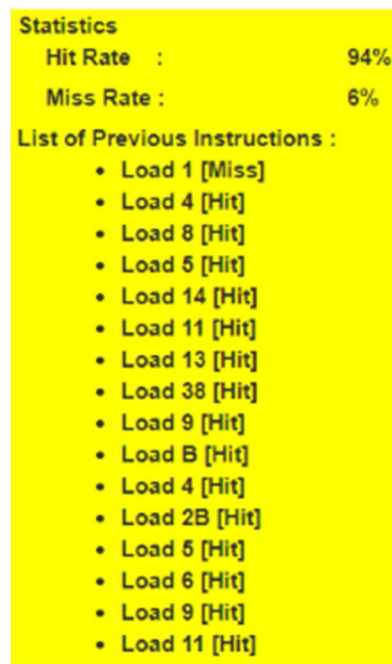
131072

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b) Screenshot showing the Cache Table

Index	Valid	Tag	Data (Hex)	Dirty
0	1	000	BLOCK 0 WORD 0 - 255	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0
32	0	-	0	0
33	0	-	0	0
34	0	-	0	0
35	0	-	0	0
36	0	-	0	0
37	0	-	0	0
38	0	-	0	0
39	0	-	0	0
40	0	-	0	0
41	0	-	0	0
42	0	-	0	0
43	0	-	0	0
44	0	-	0	0
45	0	-	0	0
46	0	-	0	0
47	0	-	0	0
48	0	-	0	0
49	0	-	0	0
50	0	-	0	0
51	0	-	0	0
52	0	-	0	0
53	0	-	0	0
54	0	-	0	0
55	0	-	0	0
56	0	-	0	0
57	0	-	0	0
58	0	-	0	0
59	0	-	0	0
60	0	-	0	0
61	0	-	0	0
62	0	-	0	0
63	0	-	0	0

c) Screenshot showing hit and miss rates



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Week# 9

Program Number: 3

A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

(b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

DIRECT MAPPED CACHE

Instruction Breakdown

00001	00010	000000
5 bit	5 bit	6 bit

Memory

B. 22	W. 0	B. 22	W. 1
B. 23	W. 0	B. 23	W. 1
B. 24	W. 0	B. 24	W. 1
B. 25	W. 0	B. 25	W. 1
R. 26	W. 0	R. 26	W. 1

b) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	00001	BLOCK 22 WORD 0 - 63	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates

Statistics	
Hit Rate :	33%
Miss Rate :	67%
List of Previous Instructions :	
<ul style="list-style-type: none"> • Load 80 [Miss] • Load 90 [Hit] • Load 880 [Miss] • Load 884 [Hit] • Load 80 [Miss] • Load 880 [Miss] 	

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Week# 9 Program Number: 4

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Generate 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11 and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Replacement Policies

☒ FIFO ☐ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

2-WAY SET ASSOCIATIVE CACHE

➔ Instruction Breakdown

0000	00000	00010001
4 bit	5 bit	8 bit

➔ Memory Blo

B.0W.0	B.0W.1	B.0W.
B.1W.0	B.1W.1	B.1W.
B.2W.0	B.2W.1	B.2W.
B.3W.0	B.3W.1	B.3W.
R.4W.0	R.4W.1	R.4W.

Cache Table

b) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 255	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates

Statistics		
Hit Rate :		94%
Miss Rate :		6%
List of Previous Instructions :		
• Load 1 [Miss]		
• Load 4 [Hit]		
• Load 8 [Hit]		
• Load 5 [Hit]		
• Load 14 [Hit]		
• Load 11 [Hit]		
• Load 13 [Hit]		
• Load 38 [Hit]		
• Load 9 [Hit]		
• Load B [Hit]		
• Load 4 [Hit]		
• Load 2B [Hit]		
• Load 5 [Hit]		
• Load 6 [Hit]		
• Load 9 [Hit]		
• Load 11 [Hit]		

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Week# 9 Program Number: 5

Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty. The addresses 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11 are generated by the CPU. All values in hexadecimal. Clearly label data that is replaced in cache lines and show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used. The cache is mapped as

a) Direct Mapped

- Cache Address Table showing the splitup of the address fields for the requests generated by the processor
- Screenshot showing the Cache Table

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Instruction

(in hex)#

List of next 10 Instructions

Information

The cycle has been completed.
Please submit another instructions

DIRECT MAPPED CACHE

➔ Instruction Breakdown

010	001	0
3 bit	3 bit	0 bit

☐ Memory Block

B. 11 W. 0
B. 12 W. 0
B. 13 W. 0
B. 14 W. 0
B. 15 W. 0
B. 16 W. 0

☐ Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	111	BLOCK 38 WORD 0 - 0	0
1	1	010	BLOCK 11 WORD 0 - 0	0
2	0	-	0	0
3	1	101	BLOCK 2B WORD 0 - 0	0
4	1	000	BLOCK 4 WORD 0 - 0	0
5	1	000	BLOCK 5 WORD 0 - 0	0
6	1	000	BLOCK 6 WORD 0 - 0	0
7	0	-	0	0

III. Screenshot showing hit and miss rates

Statistics	
Hit Rate :	13%
Miss Rate :	88%
List of Previous Instructions :	
<ul style="list-style-type: none">• Load 1 [Miss]• Load 4 [Miss]• Load 8 [Miss]• Load 5 [Miss]• Load 14 [Miss]• Load 11 [Miss]• Load 13 [Miss]• Load 38 [Miss]• Load 9 [Miss]• Load B [Miss]• Load 4 [Miss]• Load 2B [Miss]• Load 5 [Hit]• Load 6 [Miss]• Load 9 [Hit]• Load 11 [Miss]	

b) Two way set Associative

I. Cache Address Table showing the splitup of the address fields for the requests generated by the processor

II. Screenshot showing the Cache Table

Replacement Policies

☐ FIFO ☒ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Instruction

Load (in hex)#

2-WAY SET ASSOCIATIVE CACHE

➔ Instruction Breakdown

0100	01	0
4 bit	2 bit	0 bit

☐ Memory Block

B. 11 W. 0
B. 12 W. 0
B. 13 W. 0
B. 14 W. 0
B. 15 W. 0
B. 16 W. 0

☐ Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	BLOCK 4 WORD 0 - 0	0
1	1	4	BLOCK 11 WORD 0 - 0	0
2	1	1	B. 6 W. 0 - 0	0
3	1	a	BLOCK 2B WORD 0 - 0	0

☐ Memory Block

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	e	BLOCK 38 WORD 0 - 0	0
1	1	2	BLOCK 9 WORD 0 - 0	0
2	0	-	0	0
3	1	2	BLOCK B WORD 0 - 0	0

III. Screenshot showing hit and miss rates

Statistics	
Hit Rate :	6%
Miss Rate :	94%
List of Previous Instructions :	
<ul style="list-style-type: none">• Load 1 [Miss]• Load 4 [Miss]• Load 8 [Miss]• Load 5 [Miss]• Load 14 [Miss]• Load 11 [Miss]• Load 13 [Miss]• Load 38 [Miss]• Load 9 [Miss]• Load B [Miss]• Load 4 [Miss]• Load 2B [Miss]• Load 5 [Miss]• Load 6 [Miss]• Load 9 [Hit]• Load 11 [Miss]	

c) Four Way Set associative

- I. Cache Address Table showing the splitup of the address fields for the requests generated by the processor
- II. Screenshot showing the Cache Table

Replacement Policies
☐ FIFO ☒ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)
 Memory Size (power of 2)
 Offset Bits

Reset Submit

4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

01000	1	0
5 bit	1 bit	0 bit

Memory Block

B. 11 W. 0
B. 12 W. 0
B. 13 W. 0
B. 14 W. 0
B. 15 W. 0
B. 16 W. 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B. 4 W. 0 - 0	0
1	1	4	B. 9 W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	3	B. 6 W. 0 - 0	0
1	1	8	B. 11 W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	a	B. 14 W. 0 - 0	0
1	1	15	B. 2B W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1c	B. 38 W. 0 - 0	0
1	1	2	B. 5 W. 0 - 0	0

III. Screenshot showing hit and miss rates

Statistics	
Hit Rate :	13%
Miss Rate :	88%
List of Previous Instructions :	
<ul style="list-style-type: none">• Load 1 [Miss]• Load 4 [Miss]• Load 8 [Miss]• Load 5 [Miss]• Load 14 [Miss]• Load 11 [Miss]• Load 13 [Miss]• Load 38 [Miss]• Load 9 [Miss]• Load B [Miss]• Load 4 [Hit]• Load 2B [Miss]• Load 5 [Miss]• Load 6 [Miss]• Load 9 [Hit]• Load 11 [Miss]	

d) Fully Associative

- I. Cache Address Table showing the splitup of the address fields for the requests generated by the processor
- II. Screenshot showing the Cache Table

Replacement Policies
☐ FIFO ☒ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)
 Memory Size (power of 2)
 Offset Bits

Reset Submit

FULLY ASSOCIATIVE CACHE

Instruction Breakdown

010001	0
6 bit	0 bit

Memory Block

B. 11 W. 0
B. 12 W. 0
B. 13 W. 0
B. 14 W. 0
B. 15 W. 0
B. 16 W. 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	001001	BLOCK 9 WORD 0 - 0	0
1	1	001011	BLOCK B WORD 0 - 0	0
2	1	000100	BLOCK 4 WORD 0 - 0	0
3	1	101011	BLOCK 2B WORD 0 - 0	0
4	1	000101	BLOCK 5 WORD 0 - 0	0
5	1	000110	BLOCK 6 WORD 0 - 0	0
6	1	010001	BLOCK 11 WORD 0 - 0	0
7	1	111000	BLOCK 38 WORD 0 - 0	0

III. Screenshot showing hit and miss rates

Statistics	
Hit Rate :	6%
Miss Rate :	94%
List of Previous Instructions :	
<ul style="list-style-type: none">• Load 1 [Miss]• Load 4 [Miss]• Load 8 [Miss]• Load 5 [Miss]• Load 14 [Miss]• Load 11 [Miss]• Load 13 [Miss]• Load 38 [Miss]• Load 9 [Miss]• Load B [Miss]• Load 4 [Miss]• Load 2B [Miss]• Load 5 [Miss]• Load 6 [Miss]• Load 9 [Hit]• Load 11 [Miss]	
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