Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date: 11/04/2021

Name: B.Pravena	SRN: PES2UG19CS076	Section: B

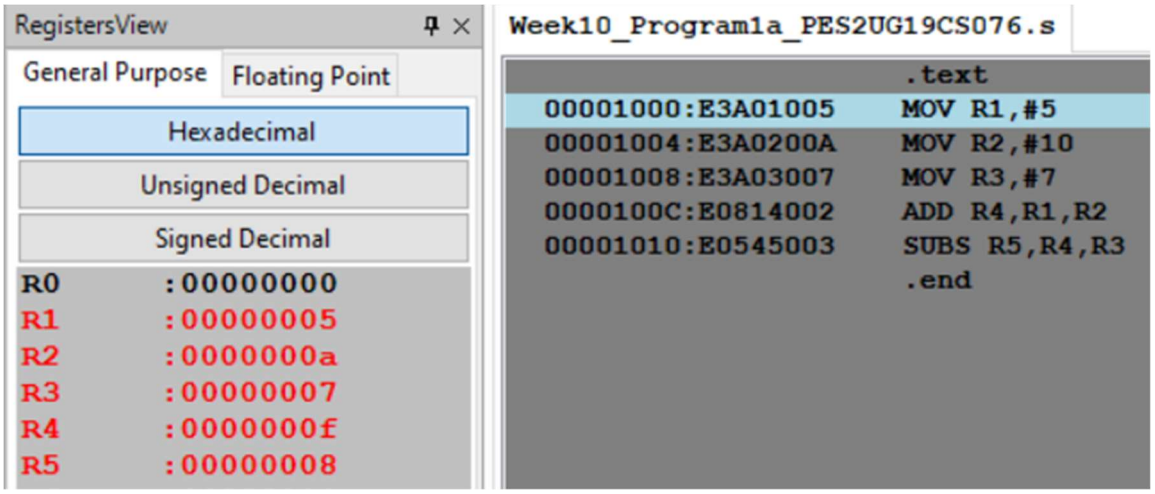
Week#____10_____ Program Number: ____1__

Given a C- Code convert it in its equivalent ARM Code.
These programs need to be executed on ARMSIM Simulator

1) x = (a + b) - c;

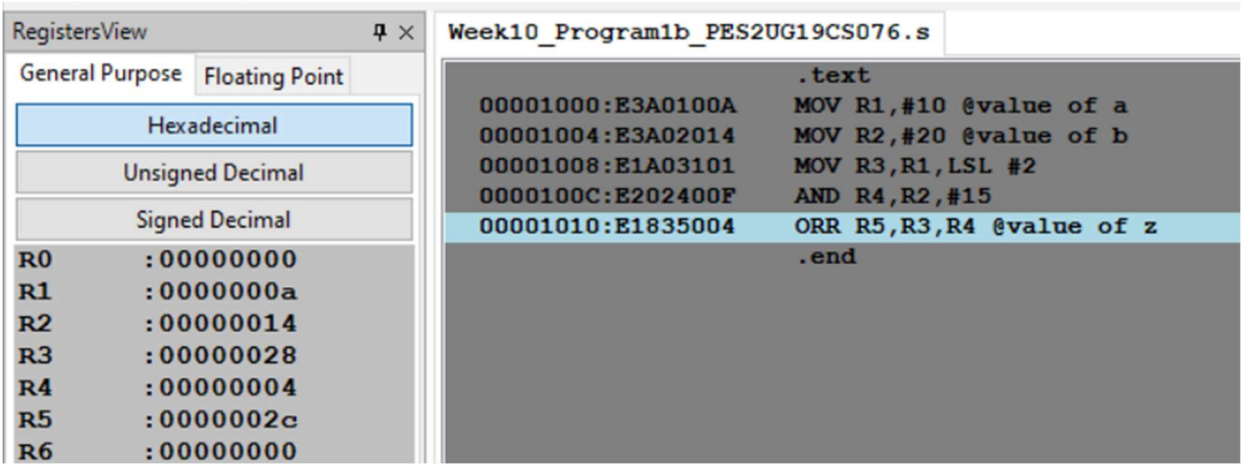
ARM Assembly Language Code

Screenshot showing the value of x, a, b, c in the register window.



2) z = (a << 2) | (b & 15);

ARM Assembly Language Code
Screenshot showing the value of a, b, z in the register window.



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Week#____10_____ Program Number: ____2__

1) Consider the following instructions. Execute these instructions using simulator of 5 stage pipeline of MIPS architecture.

ADD R1, R2, R3
SUB R4, R1, R5.

Observe the following and note down the results.

a) Check whether there is data dependency for the second instruction?

YES. Register R1.

Potential Hazards:

```
RAW: Instructions 0 and 1.  Register R1.
```

b) If yes, then, how many stall states have been introduced?

2 stall states have been introduced.

Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1

INT_Subtract | R1 | R1 | R1 | Insert Instruction

Data Forwarding | Remove Instruction

Help | Reset Application

		CPU Cycles									
Instruction		**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
0	int_add (R1, R2, R3)	IF	ID	+|- (i)	MEM	WB					
1	int_sub (R4, R1, R5)		IF	ID	S	S	+|- (i)	MEM	WB		

Step | Execute All Instructions

Potential Hazards:

```
RAW: Instructions 0 and 1.  Register R1.
```

c) If data forwarding is applied how many stall states have been reduced?

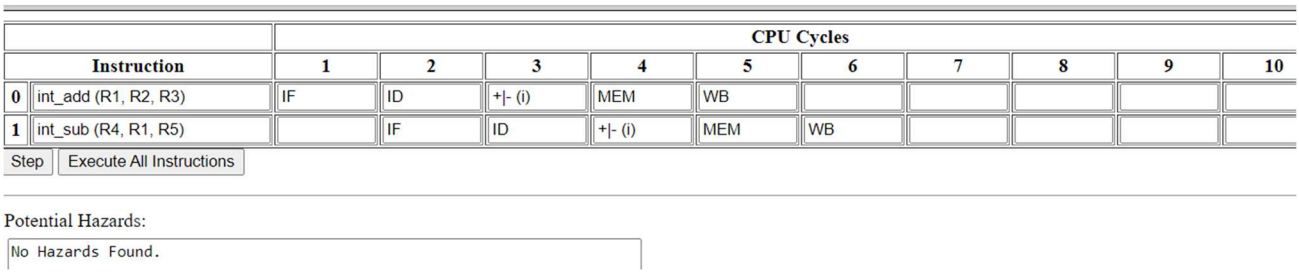
Both stall states get reduced.

Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1

INT_Subtract | R1 | R1 | R1 | Insert Instruction

Data Forwarding | Remove Instruction

Help | Reset Application



		CPU Cycles									
Instruction		1	2	3	4	5	6	7	8	9	10
0	int_add (R1, R2, R3)	IF	ID	+|- (i)	MEM	WB					
1	int_sub (R4, R1, R5)		IF	ID	+|- (i)	MEM	WB				

Step | Execute All Instructions

Potential Hazards:

No Hazards Found.

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Week#____10_____ Program Number: ____3__

Consider the following code segment in C.

A = B + E;
C = B + F;

a) Write the code using MIPS 5 STAGE pipeline architecture.

ARM Assembly Language Code

Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1

INT_Add R1 R1 R1 Insert Instruction

Data Forwarding Remove Instruction

Help Reset Application

		CPU Cycles									
Instruction		1	2	3	4	5	6	7	8	9	10
0	int_add (R3, R1, R2)	IF	ID	+|- (i)	MEM	WB					
1	int_add (R5, R1, R4)		IF	ID	+|- (i)	MEM	WB				

Step Execute All Instructions

b) Find the hazards;

Potential Hazards:

No Hazards Found.

c) Reorder the instructions to avoid pipeline stalls.

If A = B + E;

C = A + F;

There will be stall.

Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1

INT_Add R1 R1 R1 Insert Instruction

Data Forwarding Remove Instruction

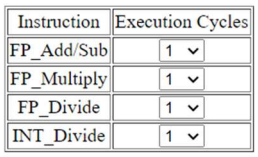
Help Reset Application

		CPU Cycles									
Instruction		1	2	3	4	5	6	7	8	9	10
0	int_add (R3, R1, R2)	IF	ID	+|- (i)	MEM	WB					
1	int_add (R5, R3, R4)		IF	ID	S	S	+|- (i)	MEM	WB		

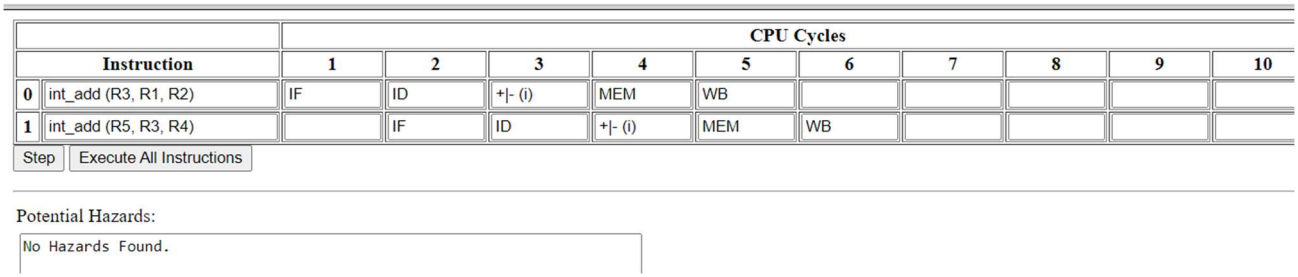
Step Execute All Instructions

Potential Hazards:

RAW: Instructions 0 and 1. Register R3.



Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1



	Instruction	CPU Cycles 1	2	3	4	5	6	7	8	9	10
0	int_add (R3, R1, R2)	IF	ID	+|- (i)	MEM	WB					
1	int_add (R5, R3, R4)		IF	ID	+|- (i)	MEM	WB				

Step | Execute All Instructions

Potential Hazards:

No Hazards Found.

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Week#____10_____ Program Number: ___4__

Using MIPS 5 stage pipeline architecture, execute the following instructions and avoid stall states if any.

```
LW   $10, 20($1)
SUB  $11, $2, $3
ADD  $12, $3, $4
LW   $13, 24($1)
ADD  $14, $5, $6
```

a)Related Screenshot with stalls
b) Related Screenshot without stalls

ARM code -:

LDR R7, [R1], #20
SUB R8, R2, R3
ADD R9, R3, R4
LDR R10, [R1], #24
ADD R11, R5, R6

Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1

INT_Add | R1 | R1 | R1 | Insert Instruction

Data Forwarding | Remove Instruction

Help | Reset Application

	Instruction	1	2	3	4	5	6	7	8	9	10
0	int_ld (R7, Offset, R1)	IF	ID	EX	MEM	WB					
1	int_sub (R8, R2, R3)		IF	ID	+|- (i)	MEM	WB				
2	int_add (R9, R3, R4)			IF	ID	+|- (i)	MEM	WB			
3	int_ld (R10, Offset, R1)				IF	ID	EX	MEM	WB		
4	int_add (R11, R5, R6)					IF	ID	+|- (i)	MEM	WB	

Step | Execute All Instructions

Potential Hazards:

No Hazards Found.

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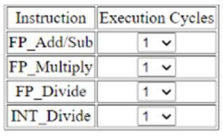
Week#____10_____ Program Number: ___5__

This exercise is to understand the relationship between delay slots, control hazards and branch execution in a 5 stage MIPS pipelined processor.

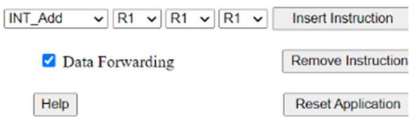
```
Label 1:    LW    $1, 40($6)
            BEQ   $2, $3, Label2    : branch taken
            ADD   $1, $6, $4
Label2:     BEQ   $1, $2, Label1    : branch not taken
            SW    $2, 20($4)
            ADD   $1, $1, $4
```

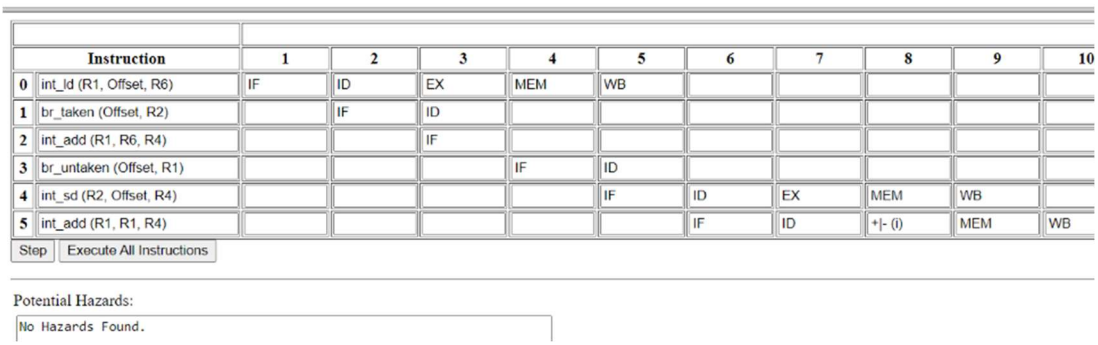
Assume full data forwarding and predict- taken branch prediction.

Note the observations.



Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1





	Instruction	1	2	3	4	5	6	7	8	9	10
0	int_ld (R1, Offset, R6)	IF	ID	EX	MEM	WB					
1	br_taken (Offset, R2)		IF	ID							
2	int_add (R1, R6, R4)			IF							
3	br_untaken (Offset, R1)				IF	ID					
4	int_sd (R2, Offset, R4)					IF	ID	EX	MEM	WB	
5	int_add (R1, R1, R4)						IF	ID	+|- (i)	MEM	WB

Step | Execute All Instructions

Potential Hazards:

No Hazards Found.