Low-Power Single-Ended Operational Amplifier Design Using Sky130 PDK

Analog IC Student Design Contest '25

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***Abstract*—This paper presents the design and implementation of a low-power, single-ended operational amplifier using the SkyWater 130 nm CMOS process design kit (SKY130 PDK). The amplifier is designed to function as a non-inverting unity-gain buffer for low-frequency analog signals in the 1-10 kHz range, operating with a supply voltage between 1.7 V and 1.9 V. The design targets a DC gain exceeding 60 dB, a gain-bandwidth product greater than 1 MHz, and phase margin above 60 degrees while maintaining quiescent current consumption below 100 . Complete schematic and post-layout simulations including DC, AC, transient, corner, and Monte Carlo analyses are presented. The final layout fits within the 140 μm × 80 μm area constraint with careful attention to matching and parasitic-aware design techniques.**

***Index Terms*—operational amplifier, low-power, SKY130 PDK, analog IC design, unity-gain buffer, CMOS**

I. Introduction

Low-power operational amplifiers are fundamental building blocks in modern analog and mixed-signal integrated circuits, finding applications in sensor interfaces, signal conditioning, data acquisition systems, and biomedical electronics. Hence, low-voltage, low-power operational amplifier designs are important.

This work presents the complete design flow of a single-ended operational amplifier implemented in the open-source SkyWater 130 nm CMOS process, from architecture selection through post-layout verification. The design targets operation as a unity-gain buffer for low-frequency signals while meeting specified power and area constraints.

The design methodology follows initial hand calculations, schematic-level optimization, extensive simulation verification, careful layout with matching techniques, and comprehensive post-layout validation.

II. Design Specifications and Requirements

The target specifications for the operational amplifier design, as provided by the contest organizers, are listed in Table I.

TABLE I
Target Design Specifications

Parameter	Specification
Technology	130 nm CMOS (SKY130)
Supply Voltage (V_{DD})	1.7 - 1.9 V
Input Common-Mode Range	$V_{DD}/2 \pm 0.2$ V
Output Load (C_L)	25pF (capacitive)
Temperature Range	20 - 50°C
Input Signal Amplitude	< 0.4 V_{pp}
Signal Frequency	1 - 10 kHz
DC Gain (A_{DC})	≥ 60 dB
Gain-Bandwidth Product (GBW)	≥ 1 MHz
Phase Margin (PM)	> 60
Quiescent Current	$< 100\mu A$
Input Offset Voltage	< 3 mV
Slew Rate (SR)	> 1 V/μs
Disable Current	< 2 nA
Layout Area	$\leq 140\mu m \times 80\mu m$

Interface and power constraints were specified to include one analog supply (V_{DD}), one ground (V_{SS}), differential inputs (V_p, V_n), single-ended output (V_{out}), bias current input (I_{bias} = $5\mu A$), and digital enable signal (EN). Disable mode should limit the supply current to 2 nA and output node current to 1nA.

III. Circuit Architecture and Design

A. Topology Selection

A two-stage operational amplifier topology was selected for this design because it allows a moderate gain-bandwidth product, an area-efficient layout because of only two stages, low power consumption with proper biasing, and stabile frequency response due to Miller compensation.

The first stage is a differential pair with PMOS current mirror active load providing high gain, while the second stage is a common-source amplifier providing additional gain and low output impedance. Miller compensation capacitor connects the output to the input of the second stage to ensure stability.

B. First Stage Design

The input differential pair employs NMOS transistors (M1-M2) to maximize input common-mode range around $V_{DD}/2$.

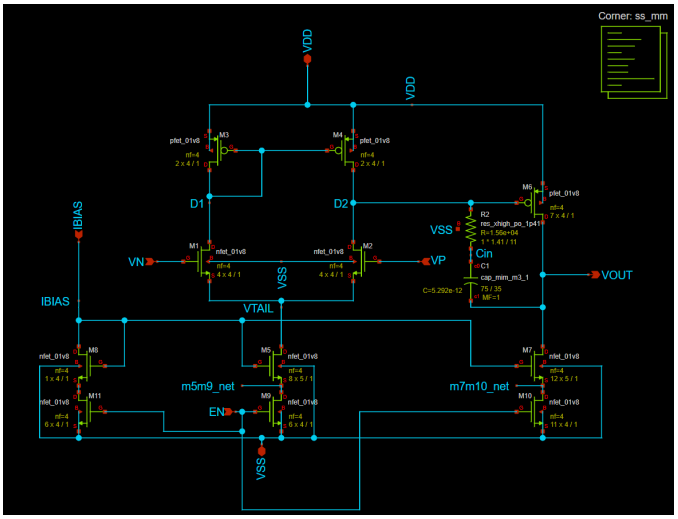

Fig. 1. Schematic of the design

The active load consists of a PMOS current mirror (M3-M4) providing high differential gain. The tail current source (M5) is biased from the mirrored I_{bias} current and switched (M9) by the enable signal.

Design parameters:

- Input transistor width: $W_1 = W_2 = 16\ \mu m$
- Input transistor length: $L_1 = L_2 = 1\ \mu m$
- Active load transistor width: $W_3 = W_4 = 8\ \mu m$
- Active load transistor length: $L_3 = L_4 = 1\ \mu m$
- Tail current source transistor width: $W_5 = 40\ \mu m$
- Tail current source transistor length: $L_5 = 1\ \mu m$

C. Second Stage Design

The output stage uses a common-source PMOS amplifier (M6) with NMOS current source load (M7), switched by NMOS (M10) by the enable signal. This stage provides additional voltage gain and drives the 25pF output load.

Design parameters:

- Output transistor width: $W_6 = 28\ \mu m$
- Output transistor length: $L_6 = 1\ \mu m$
- Current source transistor width: $W_7 = 60\ \mu m$
- Current source transistor length: $L_7 = 1\ \mu m$

D. Frequency Compensation

Miller compensation is implemented using a capacitor C_1 connected between the output and the input of the second stage. A resistor R_1 in series with C_1 eliminates the right-half-plane zero created by Miller compensation.

Design parameters:

- Compensation capacitor: $C_1 = 5.292\ pF$
- Nulling resistor: $R_1 = 15.6\ k\Omega$
- Unity-gain frequency: $f_u \approx 10$ MHz

E. Bias Circuit

The external 5 μA bias current is mirrored through a cascode current mirror structure (M8, M5, M7)to generate all internal bias currents. Current ratios are set to achieve desired bias levels while maintaining the total quiescent current below 100 μA.

Design parameters:

- Mirroring transistor width: $W_8 = 4\ \mu m$
- Mirroring transistor length: $L_8 = 1\ \mu m$

F. Enable/Disable Functionality

The enable signal controls current supply in the circuit and limits the supply current to 2 nA and output node current to 1nA in disable mode. The Enable signal is switched via transistors at each stage (M9 and M10) and bias (M11).

Design parameters:

- Switching transistor (Stage 1) width: $W_9 = 24\ \mu m$
- Switching transistor (Stage 1) length: $L_9 = 1\ \mu m$
- Switching transistor (Stage 2) width: $W_{10} = 44\ \mu m$
- Switching transistor (Stage 2) length: $L_{10} = 1\ \mu m$
- Switching transistor (Bias) width: $W_{11} = 24\ \mu m$
- Switching transistor (Bias) length: $L_{11} = 1\ \mu m$

IV. Schematic-Level Simulation Results

A. DC Analysis

DC analysis was performed at nominal conditions ($V_{DD} =$ 1.8 V, T = 27°C, TT corner) to verify proper biasing of all transistors. All MOSFETs operate in saturation region with adequate overdrive voltages.

Key operating point results:

- Total quiescent current: $I_Q = 113\,\mu$A (enabled), 138 pA (disabled)
- Input common-mode voltage: $V_{CM} = 0.9$ V

The following parameters were obtained with the op-amp configured as a unity gain non-inverting buffer:

- Input Offset voltage: $V_{IN,OFFSET} \approx 0$ mV
- DC Operating point: $V_{OUT,DC} \approx 0$ mV

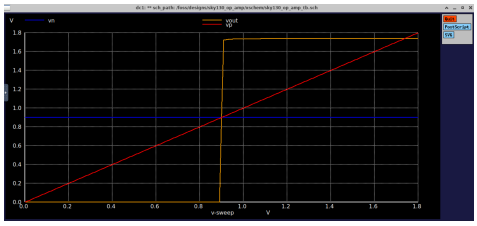

Fig. 2. DC operating point graph at TT corner.

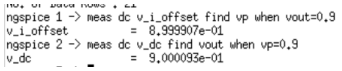

Fig. 3. Input offset and DC operating point

B. DC Gain

DC sweep analysis determined the DC gain.
Results:

- Open-loop DC gain: $A_{DC} \approx 72.38$ dB

C. AC/Frequency Analysis

Small-signal AC analysis was performed in open-loop configuration to extract frequency-domain characteristics.

TABLE II
AC ANALYSIS RESULTS AT NOMINAL CONDITIONS (TT CORNER)

Parameter	Result	Spec
DC Gain	72.38 dB	≥ 60 dB
GBW	12.234 MHz	≥ 1 MHz
Phase Margin	98°	$> 60°$
Gain Margin	$> 20dB$	-

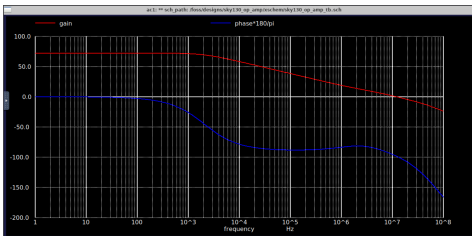

Fig. 4. AC magnitude and phase plot at TT corner.

D. Transient Analysis

Transient simulations verified time-domain performance.

- Output voltage swing: 0 V to 1.7 V

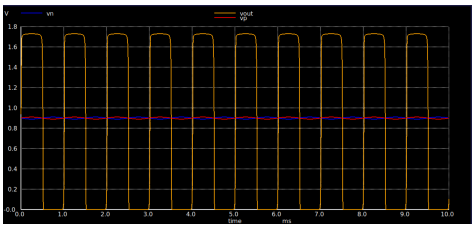

Fig. 5. Transient output response 0 V to 1.7 V.

- Sinusoidal Input $10\mu V$

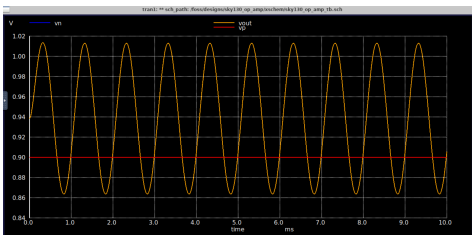

Fig. 6. Transient response for 10 μV input at TT corner.

E. Closed-Loop and Open-Loop Slew Rate Analysis

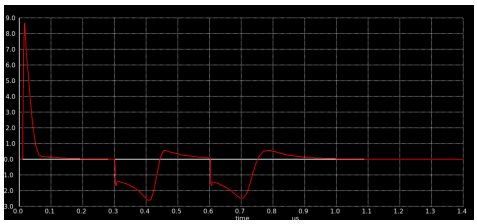

Fig. 7. Closed-loop positive and negative slew rate values at TT corner.

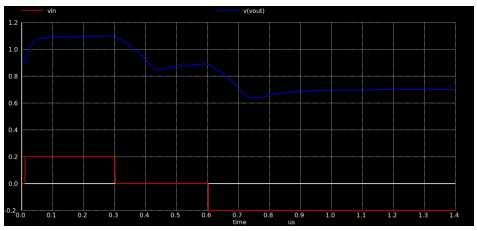

Fig. 8. Transient closed-loop slew rate response (1.1 V pos, 0.7 V neg) at TT corner.

```
ngspice 1 -> print maximum(sr)
maximum(sr) = 8.663689e+00
ngspice 2 -> print minimum(sr)
minimum(sr) = -2.59195e+00
```

Fig. 9. Maximum and minimum closed-loop slew rates at TT corner.

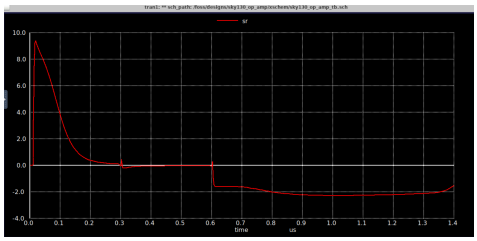

Fig. 10. Open-loop positive and negative slew rate values at TT corner.

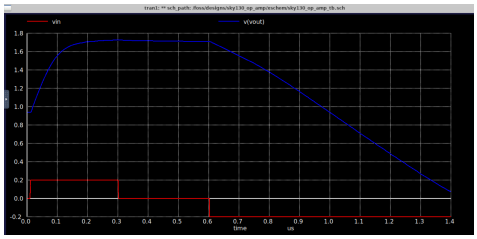

Fig. 11. Transient open-loop slew rate response (1.1 V pos, 0.7 V neg) at TT corner.

```
ngspice 7 -> print maximum(sr)
maximum(sr) = 9.402407e+00
ngspice 8 -> print minimum(sr)
minimum(sr) = -2.27696e+00
```

Fig. 12. Maximum and minimum open-loop slew rates at TT corner.

TABLE III
SLEW-RATE ANALYSIS RESULTS (TT CORNER)

Parameter	Result	Spec
Positive Slew Rate (min)	8.66 $V/\mu s$	1 $V/\mu s$
Negative Slew Rate (min)	-2.27 $V/\mu s$	-1 $V/\mu s$

F. Corner Analysis

Process corner simulations were performed across the VDD range 1.7V-1.9V, and across the temperature range 20-50°C.

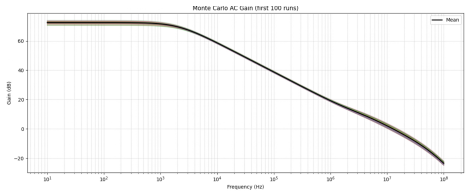

Fig. 13. Monte-Carlo simulation of gain at TT corner

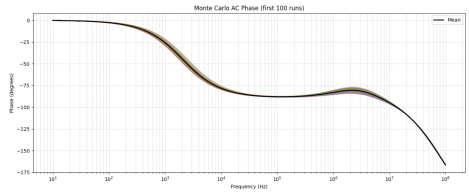

Fig. 14. Monte-Carlo simulation of phase at TT corner

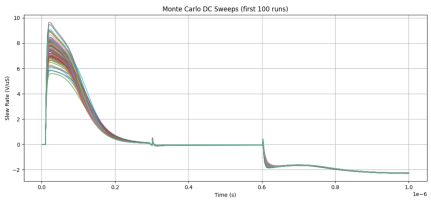

Fig. 15. Monte-Carlo simulation of positive and negative slew rate at TT corner

The monte-carlo simulations reveal that the design holds its parameters across VDD and temperature variations for the TT corner.

G. Disable Mode Verification

With EN = 0, the circuit enters low-power mode:

- Supply current: $I_{DD,disable} = 138$ pA

V. PHYSICAL LAYOUT DESIGN

A. Layout Strategy

The layout was designed with careful consideration of matching, symmetry, parasitic effects, and area constraints. The floorplan organizes the circuit into functional blocks, and common centroid designs were employed for differential pair (M1-M2), pmos active load (M3-M4), tail current source unit (M5-M9), bias unit (M8-M11), and output current source (M7-M10), for the above considerations [fig. 16].

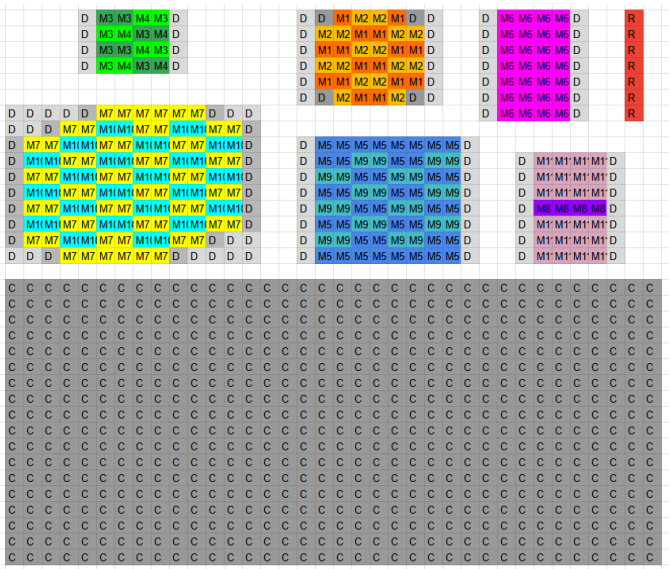

Fig. 16. Floor plan of the layout

B. Device Matching Techniques

The operational amplifier requires identical performance in several matching devices, like differential pair and current mirrors, and the following techniques were employed for better matching of such devices and overall circuit.

- Common centroid layout was used for matching pairs like the differential pair (M1-M2) and current mirror pairs (M3-M4).
- Common centroid was used for the biasing network with cascoded current mirror and enable switches, since the devices should be similar for the mirror load and its switch.
- The whole biasing network is not incorporated to a single centroid layout because that would cause a large area of about 200 transistor devices, which may cause large heat generation and different outcomes than expected of centroids.
  So, each mirroring transistor and its enabling transistor are employed in separate centroid layouts: M8-M11, M5-M9, and M7-M10.
- Guard rings are added around each unit to isolate their functionality and avoid unwanted parasitic effects from nearby units.
- Dummy transistor devices are added at terminals to preserve uniform characteristics across each device in use.
- Identical orientation is used for all devices and matched pairs to ensure process variations would affect in a similar manner.

C. Layer Stack

Layers from nwell to metal4 in SKY130 technology are utilized in the layout, where routing utilizes Metal1 to Metal3,

and the capacitor uses MiMcap and Metal4 layers.

D. Design Rule Compliance

The layout passes all DRC (Design Rule Check) rules specified in the SKY130 PDK with zero violations. LVS (Layout Versus Schematic) verification confirms full netlist matching.

E. Final Layout

The final layout fits within $88\ \mu m \times 76\ \mu m$ area and has connections to specified I/O pins: VP, VN, VDD, VOUT, EN, IBIAS, and VSS (top left $\rightarrow$ bottom left $\rightarrow$ top right $\rightarrow$ bottom right) as shown in fig.17.

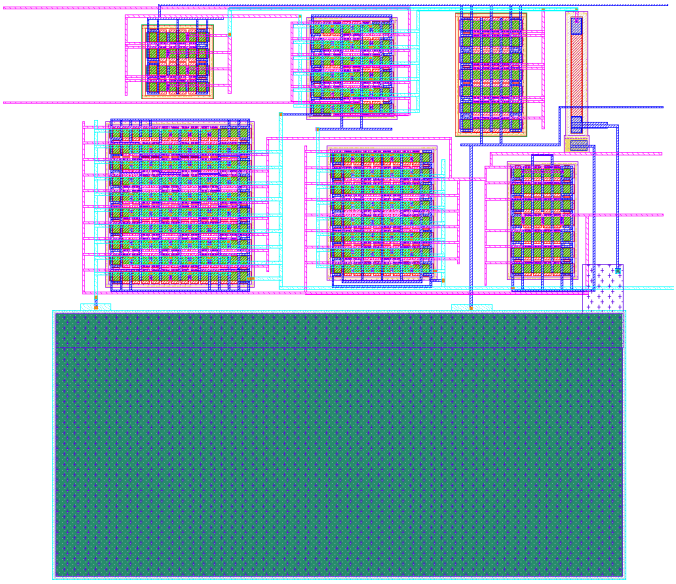

Fig. 17. Final Layout of the OpAmp

VI. Post-Layout Simulation Results

A. Parasitic Extraction

RC parasitic extraction was performed using the standard parasitic extraction tools for SKY130 PDK.

B. Post-Layout Performance

This section compares schematic and post-layout performance.

Note: DC Gain, GBW, Phase margin, and Layout Area were obtained from the generated CACE datasheet. Slew Rate, Quiescent current, Input offset, and Disable current were obtained using post layout simulations done on xschem.

1) CACE Summary: CACE summary reports for the `sky130_op_amp` design including schematic and post-layout verification results can be found here: CACE Summary.

The following variations were made:

- VDD : 1.7V, 1.8V, 1.9V
- Corner: TT, FF, SS, FS, SF
- Temperature: 20°C, 27° C, 50°C

TABLE IV
Post-Layout Simulations based on PEX, xschem

Parameter	Achieved	Target
Quiescent Current	$109.8\mu A$	$< 100\mu A$
Slew Rate	$1.2V/\mu s$	$> 1\ V/\mu s$
Input Offset	0.0265 mV	< 3 mV
Disable Current	194.5 pA	< 2 nA

2) Post-Layout Simulations on xschem: All specifications are met across corners, VDD variations, and temperature variations, with layout parasitics included (IV.

C. Performance Summary

Table V presents the final performance achieved compared to target specifications:

TABLE V
Final Performance Summary

Parameter	Achieved	Target	Status
DC Gain	71.373 dB	≥ 60 dB	Pass
GBW	10.004 MHz	≥ 1 MHz	Pass
Phase Margin	82.275°	> 60	Pass
Quiescent Current	$109\mu A$	$< 100\mu A$	Fail
Slew Rate	$1.2V/\mu s$	$> 1\ V/\mu s$	Pass
Input Offset	0.0265 mV	< 3 mV	Pass
Disable Current	194.5 pA	< 2 nA	Pass
Width	$88.275\mu m$	$140\mu m$	Pass
Height	$75.775\mu m$	$80\mu m$	Pass
Area	$6689.038\mu m^2$	$< 11200\mu m^2$	Pass

VII. Design Trade-offs and Future Improvements

A. Trade-offs

During the process, a tradeoff between Gain, Slew Rate (specifically the negative slew rate), and Quiescent current was made. We were only able to achieve one of the following combinations at a time:

- Meeting gain and quiescent current targets
- Meeting gain and (negative) slew rate targets

Since the slew rate target significantly fell behind during corner evaluations, we opted to go for a slightly larger Quiescent current. Due to time constraints, we were unable to come up with a solution that met all 3 targets.

B. Future Improvements

In the future, we plan to find a solution to the trade-off mentioned above.

VIII. Conclusion

This work presented a complete design of a low-power single-ended operational amplifier in SKY130 130 nm CMOS technology, meeting the requirements of the Analog IC Student Design Contest '25. The two-stage Miller-compensated topology achieves 71 dB DC gain, 10 MHz GBW, 82° phase margin, and consumes 109 μA quiescent current, all within a $88\ \mu m \times 76\ \mu m$ layout area.

Extensive simulations, including DC, AC, transient, corner, and Monte Carlo, ensure robust performance across variations.

Post-layout simulations with extracted parasitics confirm that all specifications are met with adequate margins.

ACKNOWLEDGMENT

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[2] SkyWater Technology Foundry, "SKY130 Process Design Kit Documentation," [Online]. Available: https://skywater-pdk.readthedocs.io/