Low-Power Single-Ended Operational Amplifier Design Using Sky130 PDK

Analog IC Student Design Contest '25

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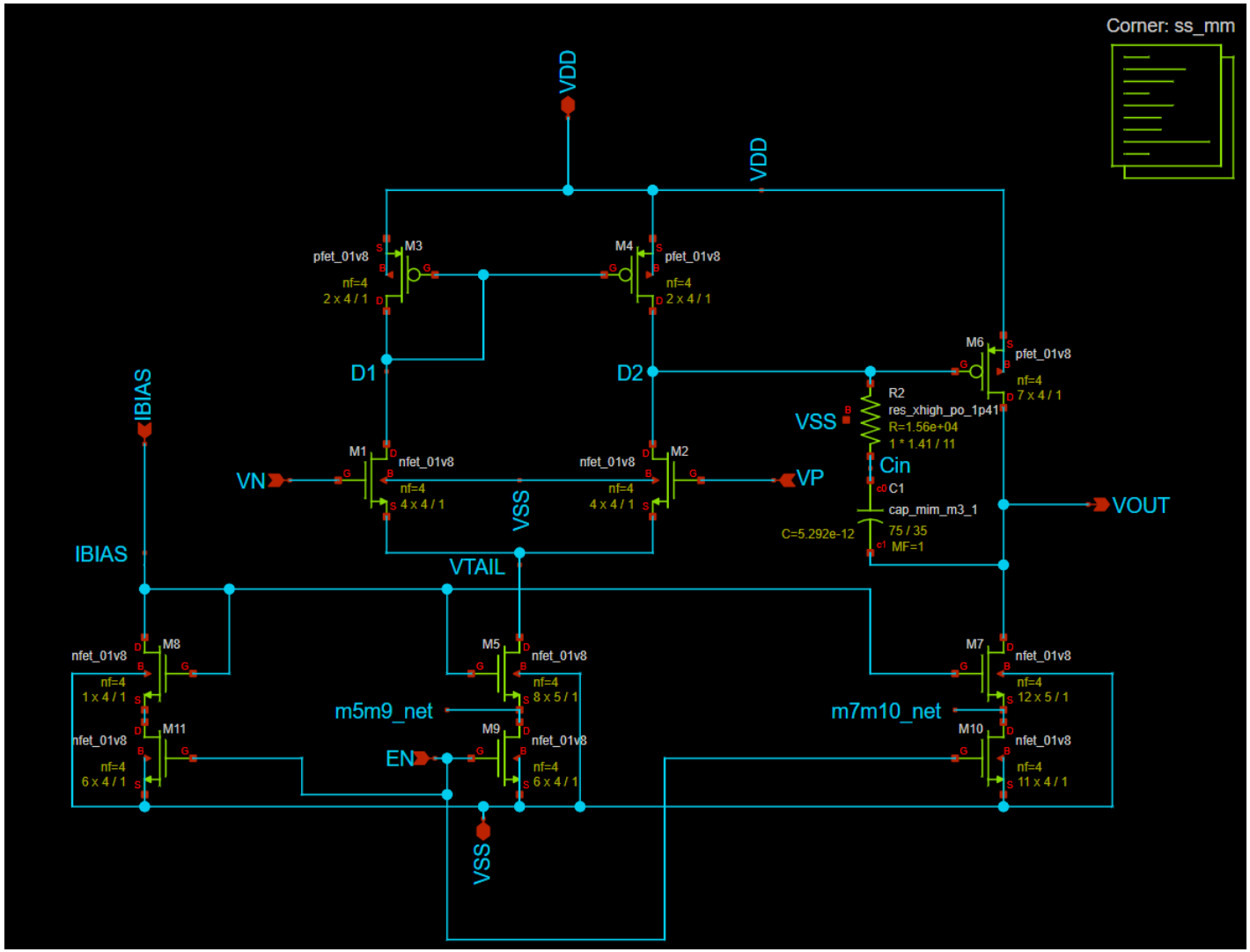
Design Specifications

Parameter	**Specification**
Technology	SKY130 130 nm CMOS
Supply Voltage	1.7 - 1.9 V
Input CM Range	$V_{DD}/2 \pm 0.2$ V
Output Load	25 pF (Capacitive)
Temperature Range	20 - 50 °C
Input Signal Amplitude	$\leq$ 0.4 Vpp
DC Gain	$\geq$ 60 dB
GBW	$\geq$ 1 MHz
Phase Margin	$> 60^\circ$
Quiescent Current	$< 100\mu A$
Input Offset	$< 3\ mV$
Slew Rate	$>$ 1 V / μs
Disable Current	$< 2\ nA$ Supply, $< 1\ nA$ Output
Bias Current	5 μA
Layout Area	$\leq 140\mu m \times 80\mu m$

Circuit Architecture

- Two-stage opamp topology:
  - Stage 1: NMOS differential pair with PMOS active load
  - Stage 2: PMOS common-source amplifier
- Miller compensation for stability
- Enable/Disable functionality reduces current to nA range

Schematic


Corner: ss_mm
VDD
VDD
M3
pfet_01v8
nf=4
2 x 4 / 1
M4
pfet_01v8
nf=4
2 x 4 / 1
D1
D2
IBIAS
M6
pfet_01v8
nf=4
7 x 4 / 1
R2
res_xhigh_po_1p41
R=1.56e+04
1 * 1.41 / 11
VSS
Cin
C1
cap_mim_m3_1
C=5.292e-12
75 / 35
MF=1
VOUT
M1
nfet_01v8
nf=4
4 x 4 / 1
VN
M2
nfet_01v8
nf=4
4 x 4 / 1
VP
VSS
IBIAS
VTAIL
M8
nfet_01v8
nf=4
1 x 4 / 1
M11
nfet_01v8
nf=4
6 x 4 / 1
M5
nfet_01v8
nf=4
8 x 5 / 1
m5m9_net
M9
nfet_01v8
nf=4
6 x 4 / 1
EN
M7
nfet_01v8
nf=4
12 x 5 / 1
m7m10_net
M10
nfet_01v8
nf=4
11 x 4 / 1
VSS

Schematic Highlights

- Input differential pair for high gain
- PMOS active load for first stage
- Common-source output stage drives 25 pF load
- Miller compensation: $C_1 = 5.292$ pF, $R_1 = 15.6$ kΩ
- Bias circuit provides stable currents

Schematic Level Simulation Results (Operating Point)

- Total quiescent current: $I_Q = 113\,\mu$A (enabled), 138 pA (disabled)
- Input common-mode voltage: $V_{CM} = 0.9$ V
- Input Offset voltage: $V_{IN,OFFSET} \approx 0$ mV
- DC Operating point: $V_{OUT,DC} \approx 0$ mV

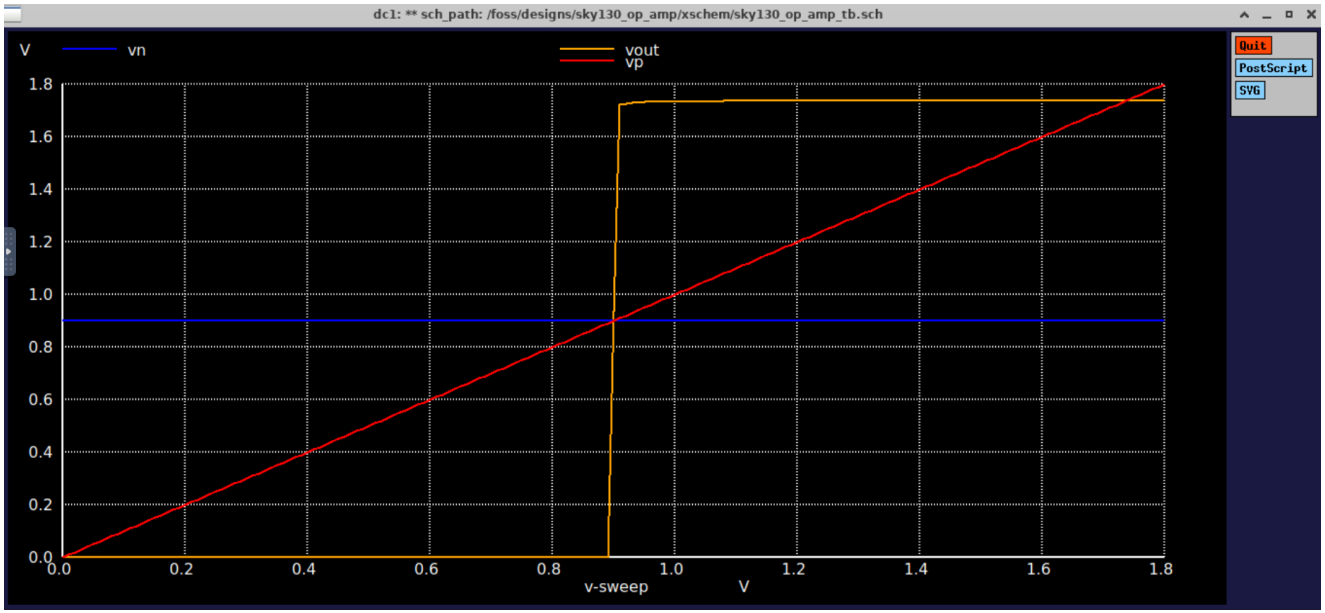


Figure: DC operating point graph at TT corner.

Schematic Level Simulation Results (Frequency)

Parameter	Achieved	Spec
DC Gain	72.38 dB	≥ 60 dB
GBW	12.234 MHz	≥ 1 MHz
Phase Margin	98°	> 60
Slew Rate	8.66 / -2.27 V/μs	$> 1/-1$ V/μs

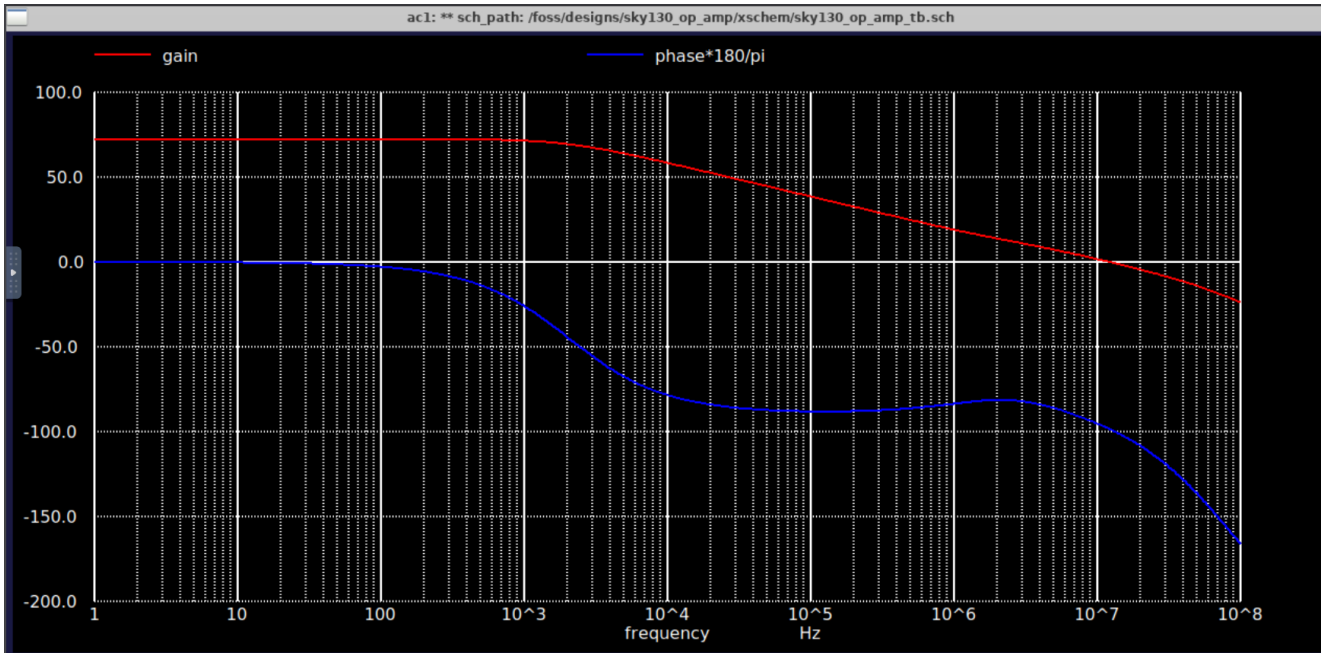
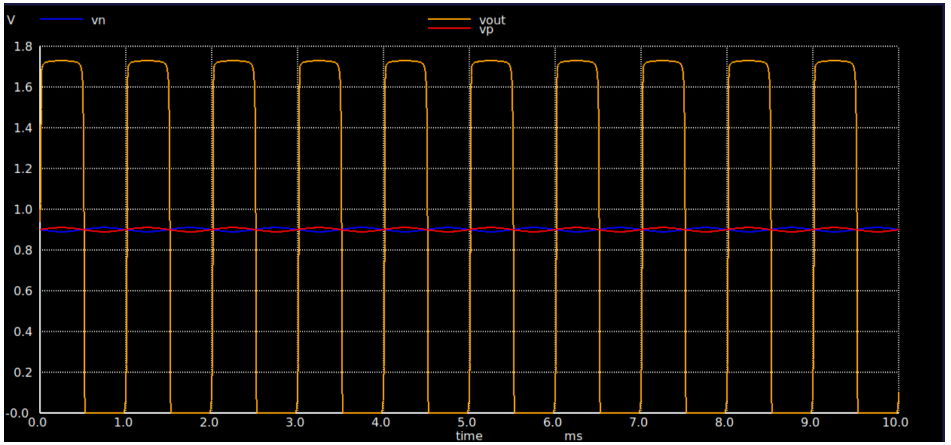
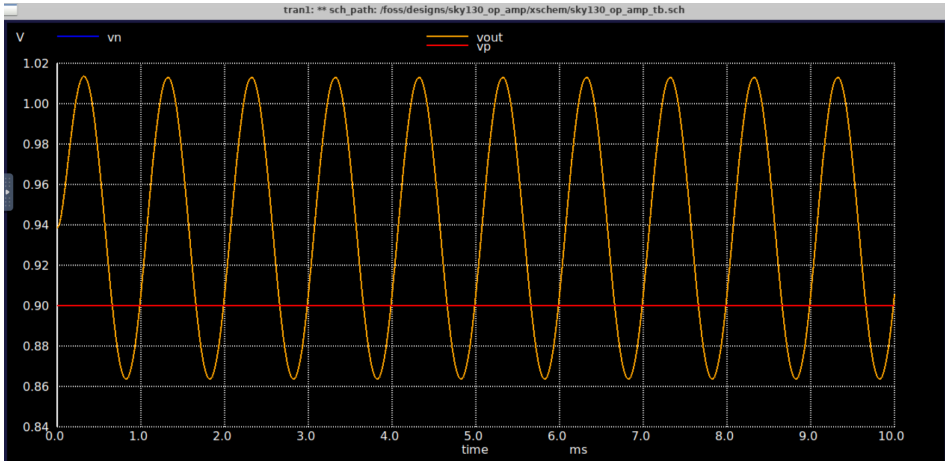


Figure: Phase and Gain

Schematic Level Simulation Results (Transient Response)

- Output swing: 0 - 1.7 V
- Sinusoidal response verified for low-level inputs (10 μV)





Schematic Level Simulation Results

Slew Rate

Table: Slew-Rate Analysis Results (TT corner)

Parameter	**Result**	**Spec**
Positive Slew Rate (min)	8.66 $V/\mu s$	1 $V/\mu s$
Negative Slew Rate (min)	-2.27 $V/\mu s$	-1 $V/\mu s$

Disable Mode

With EN = 0, the circuit enters low-power mode:

- Supply current: $I_{DD,disable} = 138$ pA

Process Corners - Monte Carlo Analysis

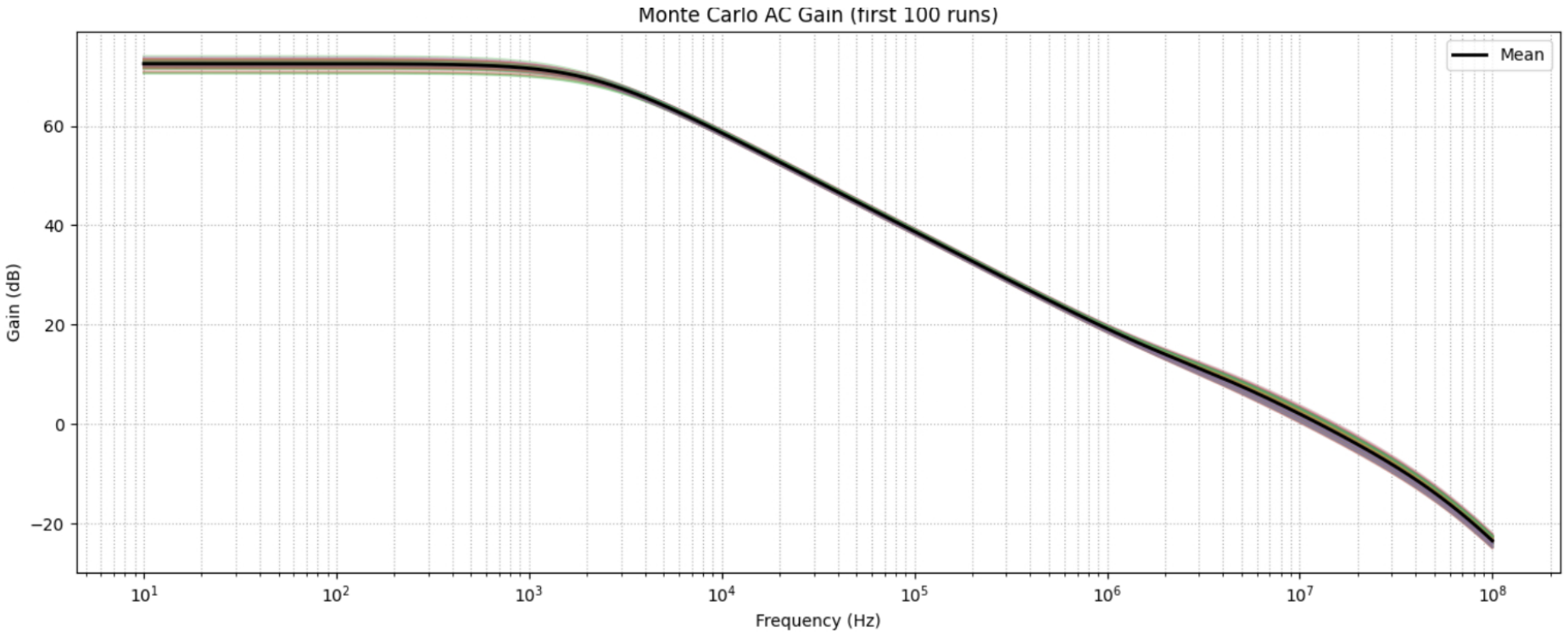


Figure: Monte-Carlo simulation of gain at TT corner

Process Corners - Monte Carlo Analysis

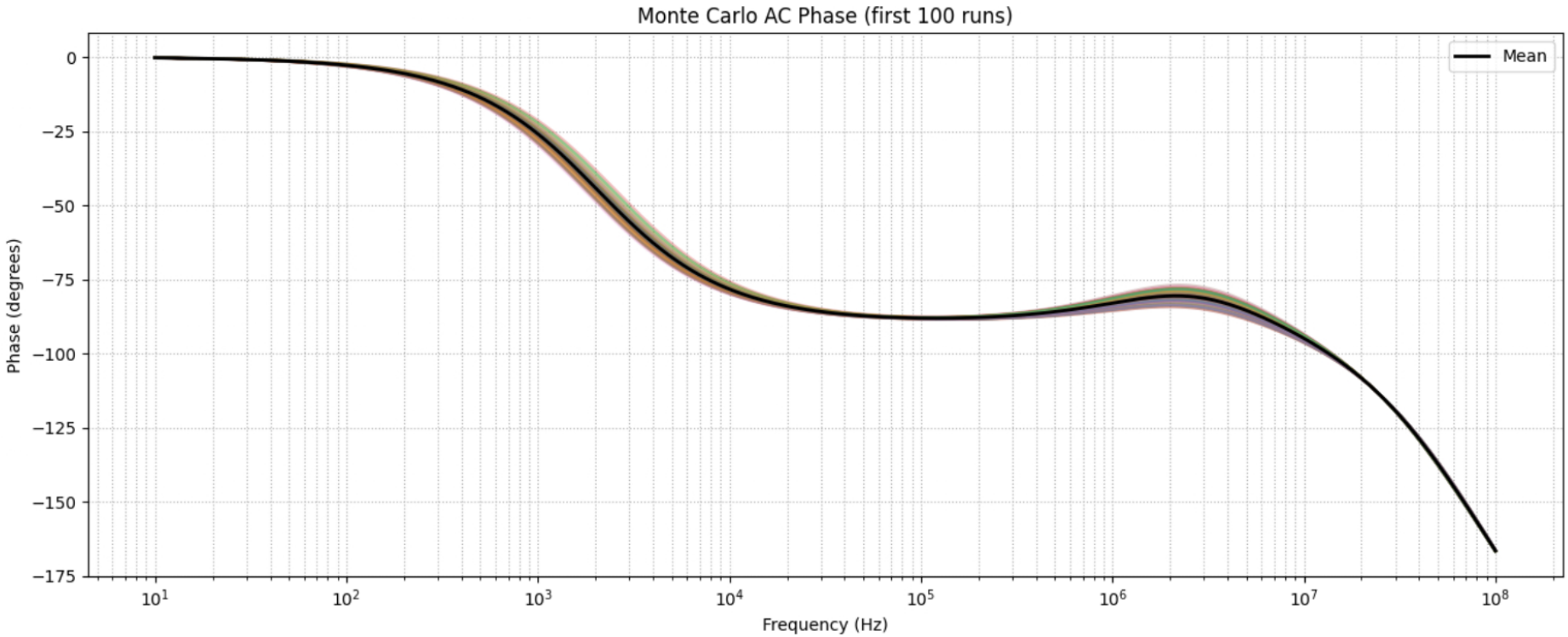


Figure: Monte-Carlo simulation of phase at TT corner

Process Corners - Monte Carlo Analysis

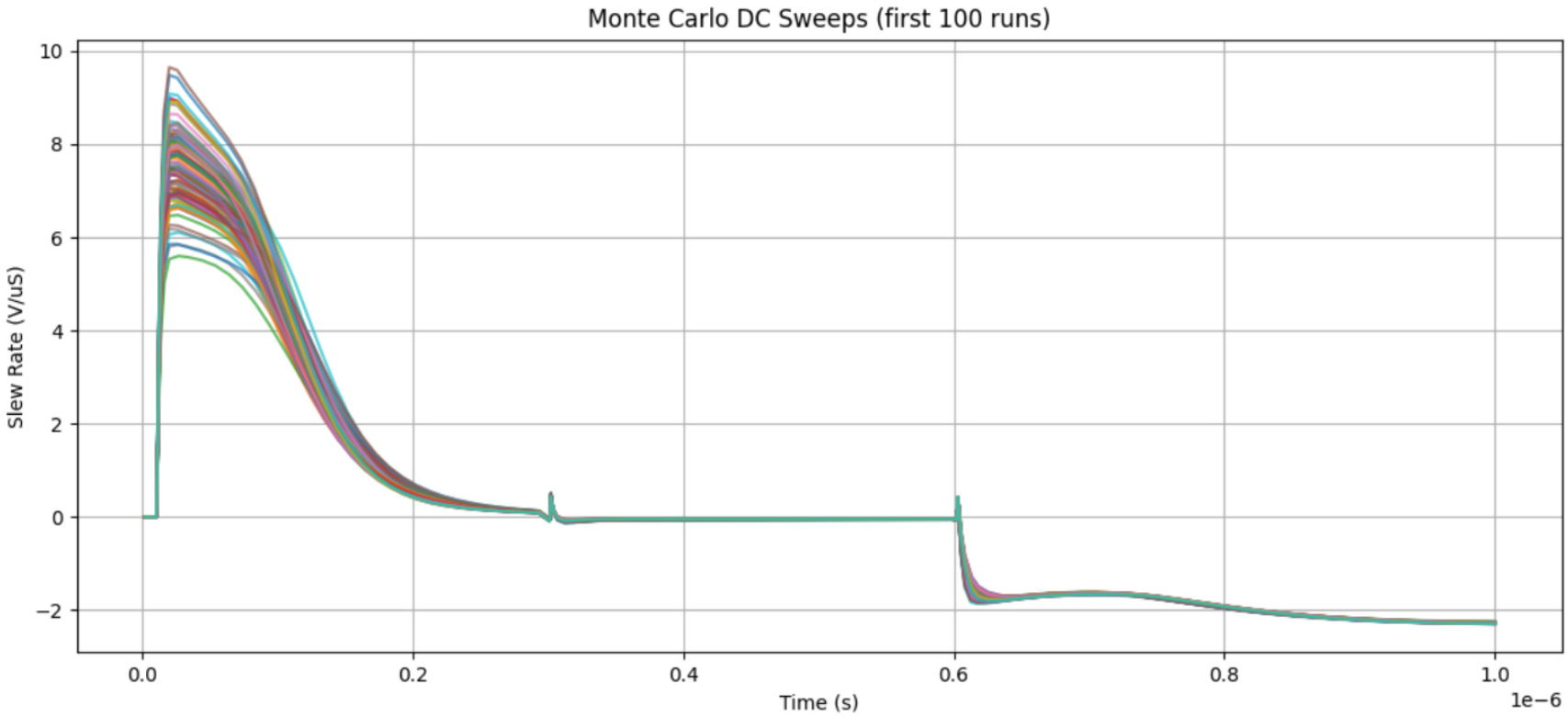


Figure: Monte-Carlo simulation of positive and negative slew rate at TT corner

Layout Design

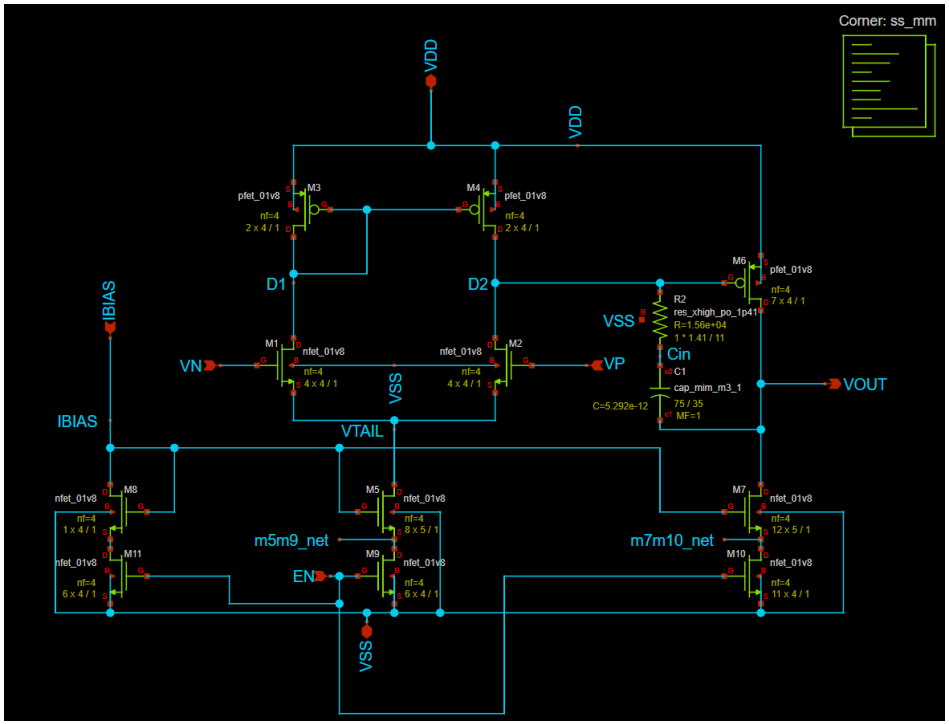


Figure: Schematic

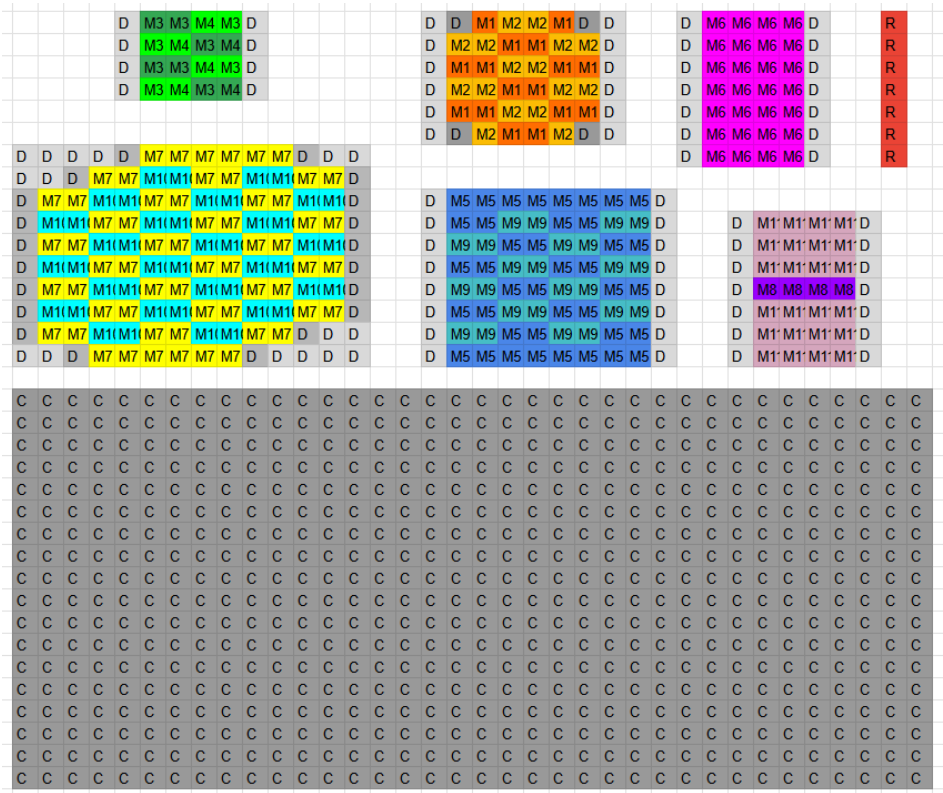


Figure: Floor plan of the layout

Layout Design

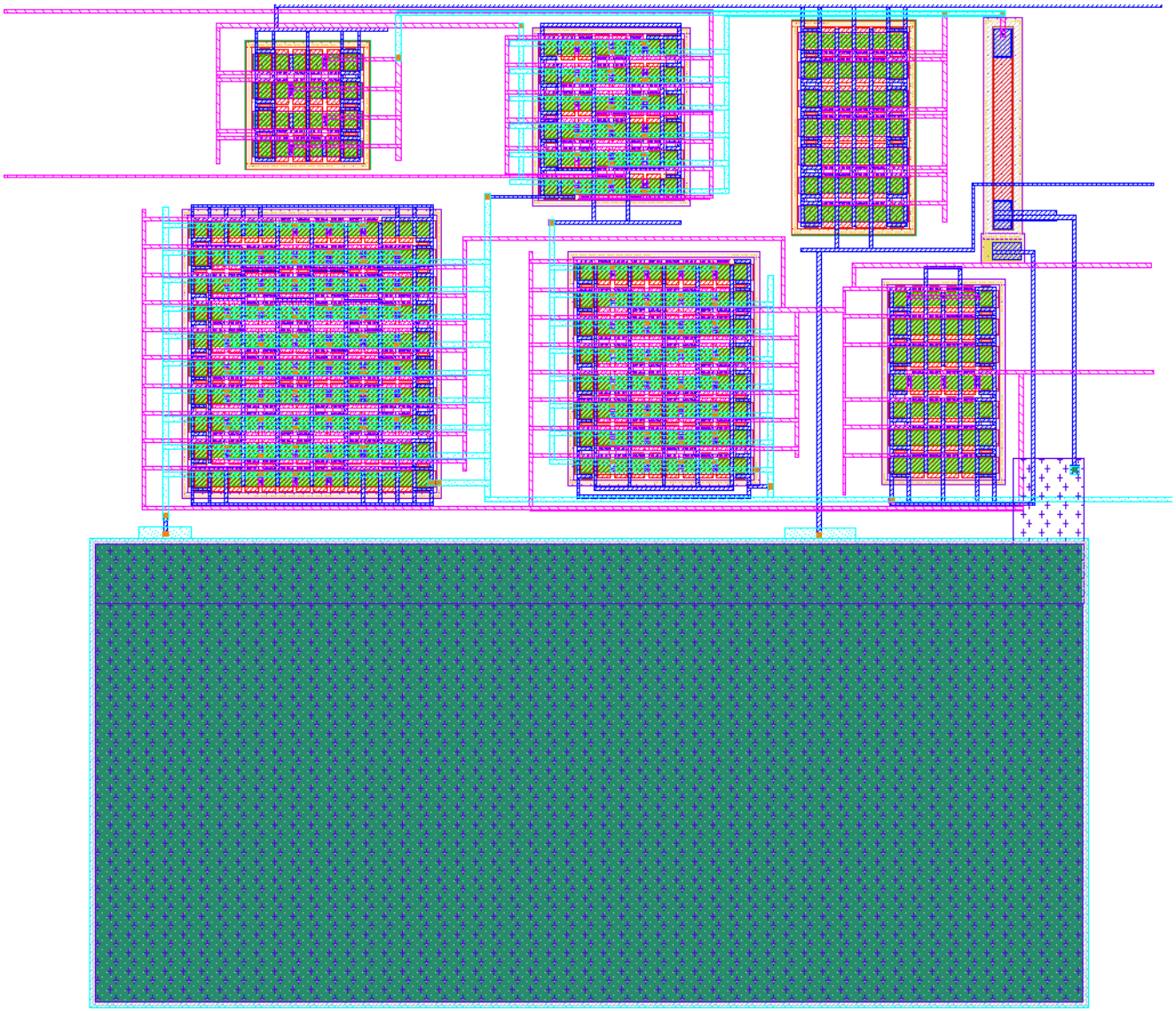


Figure: Final Layout of the OpAmp

Layout Design

- Common centroid and symmetry for differential pair and current mirrors
- Guard rings and dummy devices for parasitic minimization
- Total layout area: $88 \times 76\ \mu m^2$

Post-Layout Verification

- Parasitic extraction (RC) using SKY130 tools
- Post-layout simulations:
  - DC, AC, transient verified
  - Specs mostly met; quiescent current slightly above target

Table: Post-Layout Simulations based on PEX, xschem

Parameter	**Achieved**	**Target**
Quiescent Current	$109.8\mu A$	$< 100\mu A$
Slew Rate	$1.2 V/\mu s$	$> 1\ V/\mu s$
Input Offset	0.0265 mV	< 3 mV
Disable Current	194.5 pA	< 2 nA

CACE Simulation

Parameter	Tool	Result	Min Limit	Min Value	Typ Target	Typ Value	Max Limit	Max Value	Status
Area	magic_area	area					11200 μm^2	6689.038 μm^2	Pass ✅
Width	magic_area	width					140 µm	88.275 µm	Pass ✅
Height	magic_area	height					80 µm	75.775 µm	Pass ✅
Magic DRC	magic_drc	drc_errors					0	0	Pass ✅
Netgen LVS	netgen_lvs	lvs_errors					0	0	Pass ✅
KLayout DRC feol	klayout_drc	drc_errors					0	0	Pass ✅
KLayout DRC beol	klayout_drc	drc_errors					0	0	Pass ✅
KLayout DRC full	klayout_drc	drc_errors					0	0	Pass ✅
Antenna Checks	magic_antenna_check	antenna_violations					0	0	Pass ✅

Figure: CACE

Performance Summary

Parameter	**Achieved**	**Target**	**Status**
DC Gain	71.373 dB	$\geq$ 60 dB	Pass
GBW	10.004 MHz	$\geq$ 1 MHz	Pass
Phase Margin	82.275°	$>$ 60	Pass
Quiescent Current	$109\mu A$	$< 100\mu A$	Fail
Slew Rate	$1.2V/\mu s$	$> 1\ V/\mu s$	Pass
Input Offset	0.0265 mV	$<$ 3 mV	Pass
Disable Current	194.5 pA	$<$ 2 nA	Pass
Width	$88.275\mu m$	$140\mu m$	Pass
Height	$75.775\mu m$	$80\mu m$	Pass
Area	$6689.038\mu m^2$	$< 11200\mu m^2$	Pass

Design Trade-offs

- Trade-off between quiescent current and negative slew rate
- Achieved slightly higher quiescent current to meet slew rate target
- Future improvement: optimize negative slew rate without increasing power

Conclusion

- Designed and implemented a low-power, two-stage opamp in SKY130 PDK
- Specs met for DC gain, GBW, phase margin, slew rate, area, and disable current
- Post-layout verification confirms robustness across corners and parasitic effects
- Demonstrates open-source analog IC design flow from schematic to layout

Acknowledgment

- Thanks to Analog IC Student Design Contest '25 and Tiny Tapeout initiative
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