Design Rules Verification Report

Filename : C:\Users\Public\Documents\Altium\LED Chaser\LED Chaser.PcbDoc

Warnings 0
Rule Violations 7

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.25mm) (All),(All)	0
Clearance Constraint (Gap=0.25mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	5
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.1mm) (Max=0.2mm) (Preferred=0.2mm) (All)	0
Width Constraint (Min=0.2mm) (Max=0.3mm) (Preferred=0.3mm) ((InNet('VCC') OR InNet('GND')))	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	1
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.1mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	1
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	7

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net NetC2_1 Between Pad C2-1(24.5mm,18mm) on Multi-Layer And Pad U2-5(25.186mm,32.184mm) on Multi-Layer
Un-Routed Net Constraint: Via (2mm,2mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.
Un-Routed Net Constraint: Via (2mm,64mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.
Un-Routed Net Constraint: Via (63mm,3mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.
Un-Routed Net Constraint: Via (63mm,64mm) from Top Layer to Bottom Layer Dead Copper - Net Not Assigned.

Hole To Hole Clearance (Gap=0.254mm) (All),(All)
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad C1-1(24mm,22mm) on Multi-Layer And Via (24mm,22mm) from Top Layer to

Net Antennae (Tolerance=0mm) (All)
Net Antennae: Track (6.084mm,43.1mm)(9.084mm,43.1mm) on Bottom Layer