Submission Date: 1/03/2020 **Experiment No:1**

Analog Experiment-1

Title:

The transconductance of NMOS and PMOS transistors biased in the saturation region of operation.

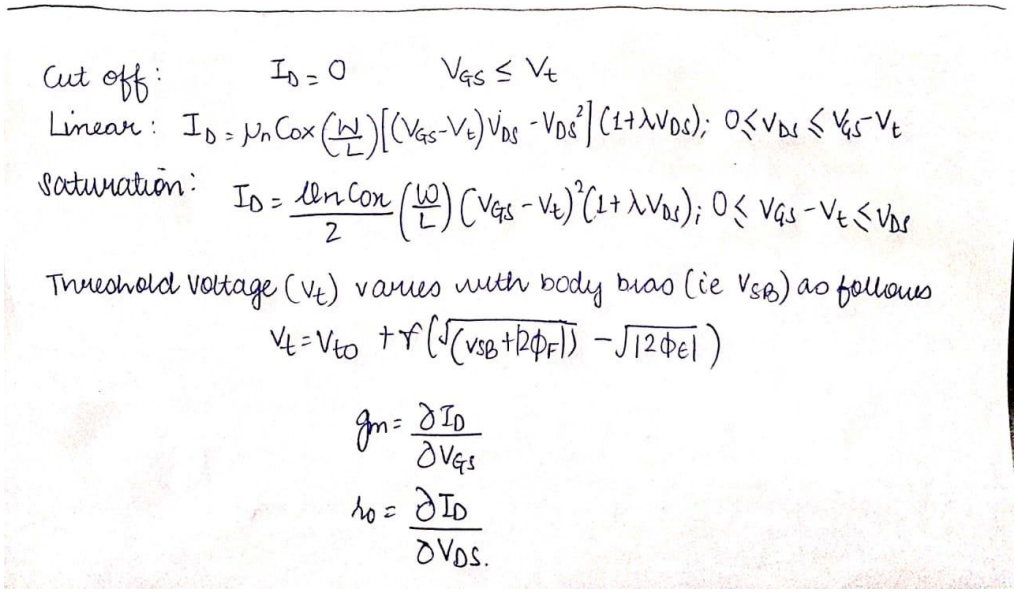
Objective:

To plot the input and output characteristic plots and to find the transconductance and the output resistance of NMOS and PMOS transistors biased in the saturation region.

Software Used: Pspice

Theory

MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) are voltage controlled 4 terminal active devices. Unlike passive elements such as resistors or capacitors, MOSFETs need an external drive (technically it is called biasing) to function desirably. The body contact remains connected to either the source terminal of the device or to the power supply (i.e. VDD or GND). We have three terminals to play with. Apply input between two terminals and get output from any two terminals, keeping one terminal common (Figure.1). We shall plot characteristic curves in order to determine characteristic parameters such as transconductance and output resistance.



Cut off: $I_D = 0 \qquad V_{GS} \le V_t$

Linear: $I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS}-V_t)V_{DS} - V_{DS}^2\right](1+\lambda V_{DS});\ 0 \le V_{DS} \le V_{GS}-V_t$

Saturation: $I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS}-V_t)^2(1+\lambda V_{DS});\ 0 \le V_{GS}-V_t \le V_{DS}$

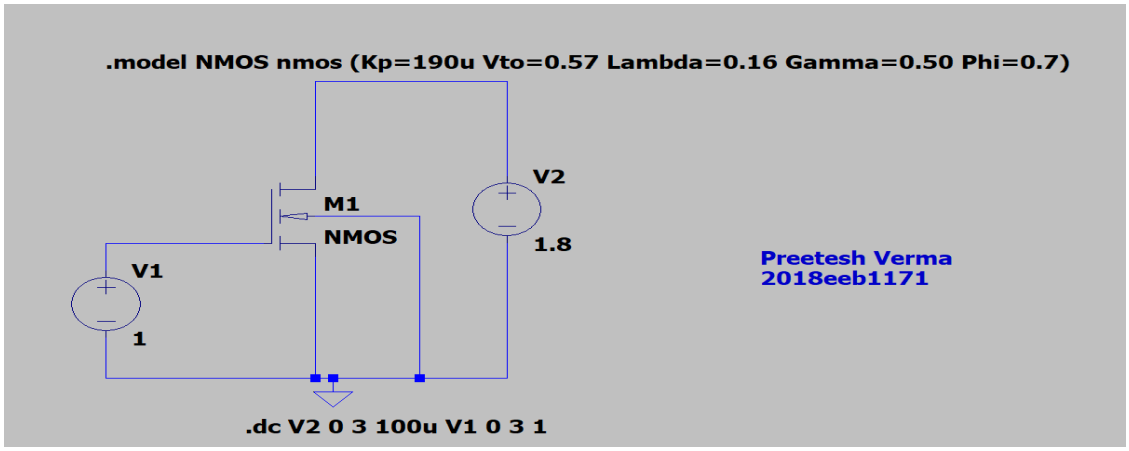
Threshold voltage (V_t) varies with body bias (ie V_{SB}) as follows

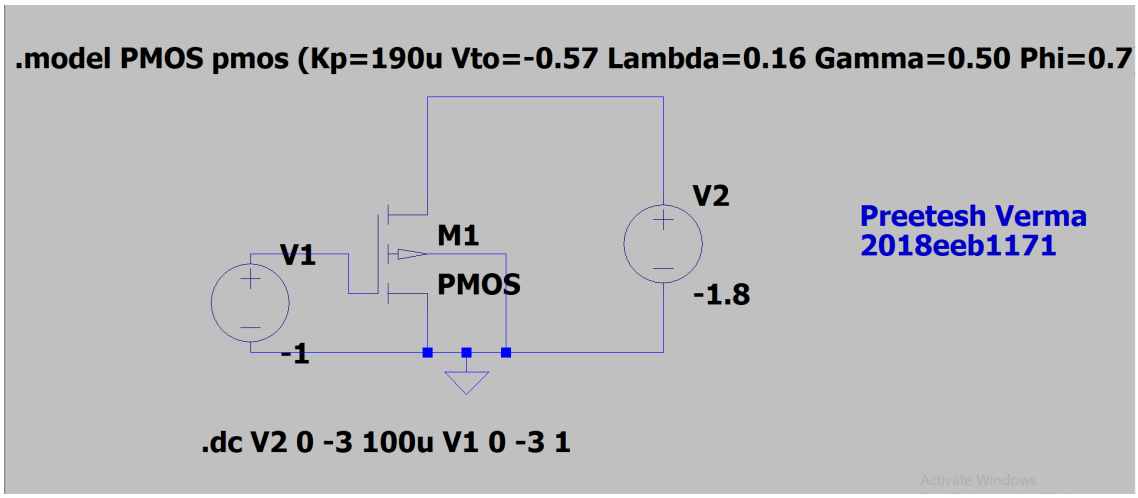
$$V_t = V_{to} + \gamma\left(\sqrt{(V_{SB}+|2\phi_F|)} - \sqrt{|2\phi_F|}\right)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$r_o = \frac{\partial I_D}{\partial V_{DS}}.$$

Circuit Diagram:





Procedure:

1. First set up the Pspice software and open a new schematic diagram.
2. Select the NMOS/PMOS component.
3. Attach two Voltage Source Components for the Gate and Drain.
4. Connect the Ground to complete the circuit.
5. Give directives to the diagram such as .model to define the various parameters of the device and .dc to vary the voltage of one of the ends.
6. .model ensures that we are using the PMOS or the NMOS.
7. .dc helps us to vary the voltages in steps.
8. Run the schematic and plot the traces of the required entities.
9. Repeat the process with the two voltage sources being replaced with each other.

Assumptions

I have used the default value for parameters for the PMOS and NMOS such as length, width etc.

Observation Table

NMOS:

Transconductance
(Vgs varied from 1 V to 3 V with a step 0.1mV)

S.No.	Vds (V)	Gm(micro ohm inverse)
0	0	0
1	1	220
2	2	500
3	3	822

Output Resistance
(Vds varied from 1 V to 3 V with a step 0.1mV)

S.No.	Vgs (V)	Ro^{-1}(micro ohm inverse)	Ro (Mega ohms)
0	0	0	0
1	1	2.40	0.4166
2	2	31.21	0.0320
3	3	89.44	0.1118

PMOS:

Transconductance
(Vgs varied from 1 V to 3 V with a step 0.1mV)

S.No.	Vds (V)	Gm(micro ohm inverse)
0	0	0
1	-1	220.00
2	-2	502.12
3	-3	843.76

Output Resistance
(Vds varied from 1 V to 3 V with a step 0.1mV)

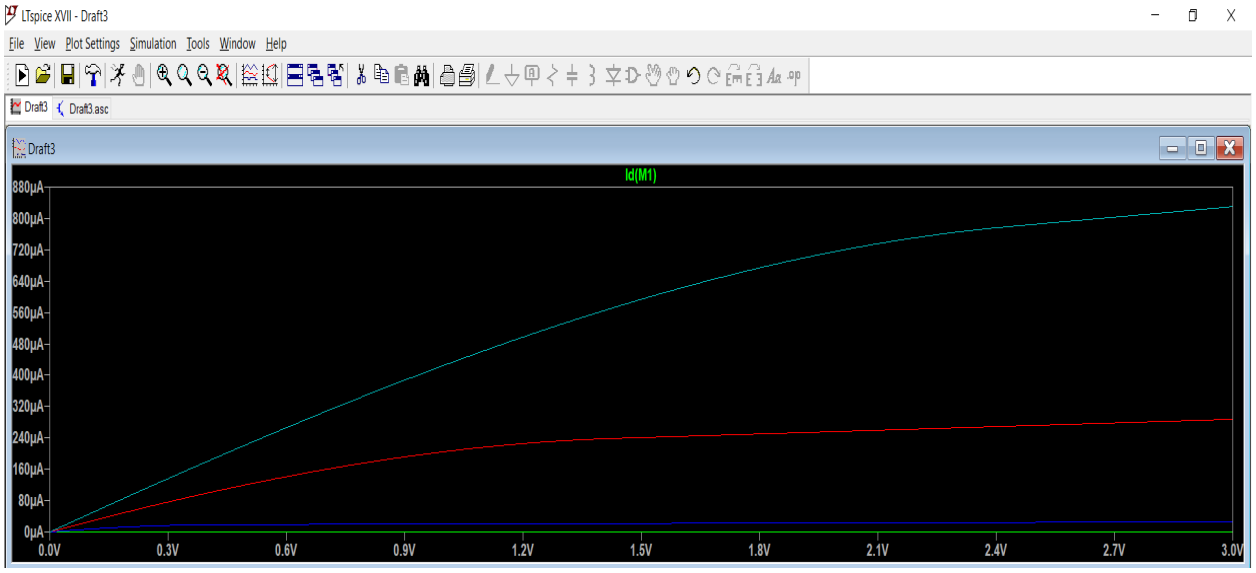
S.No.	Vgs (V)	Ro^{-1}(micro ohm inverse)	Ro (Mega ohms)
0	0	0	0

1	-1	3.04	0.32
2	-2	31.81	0.031
3	-3	90.04	0.011

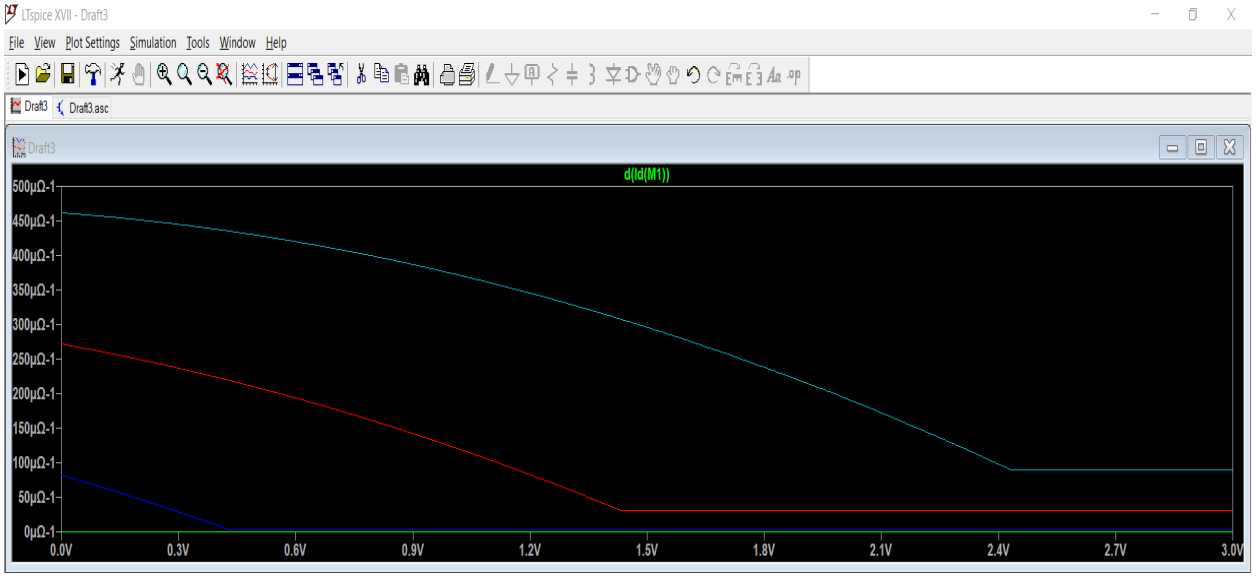
Graphs

NMOS:

Output Resistance

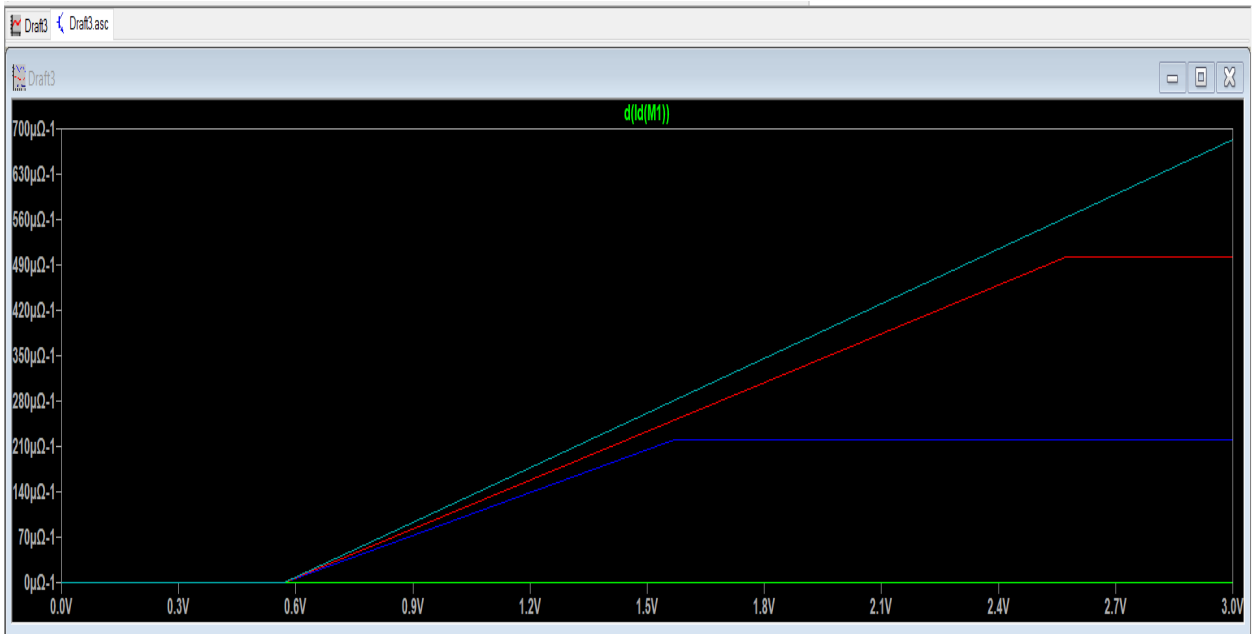


Id vs Vgs

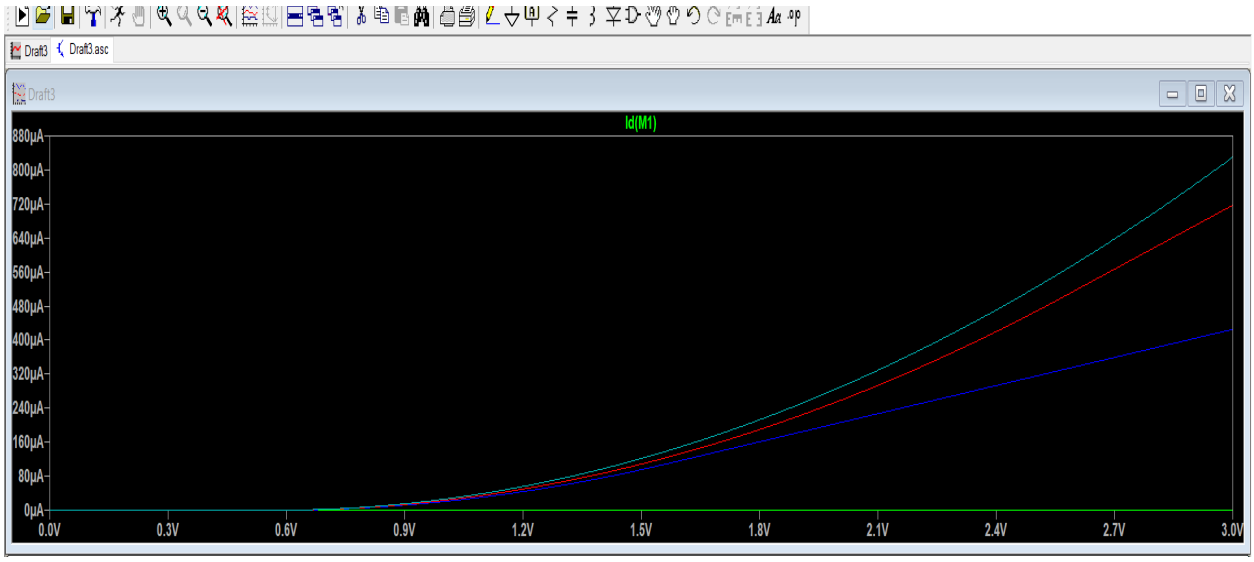


d(Id)/d(Vds) vs Vgs

Transconductance



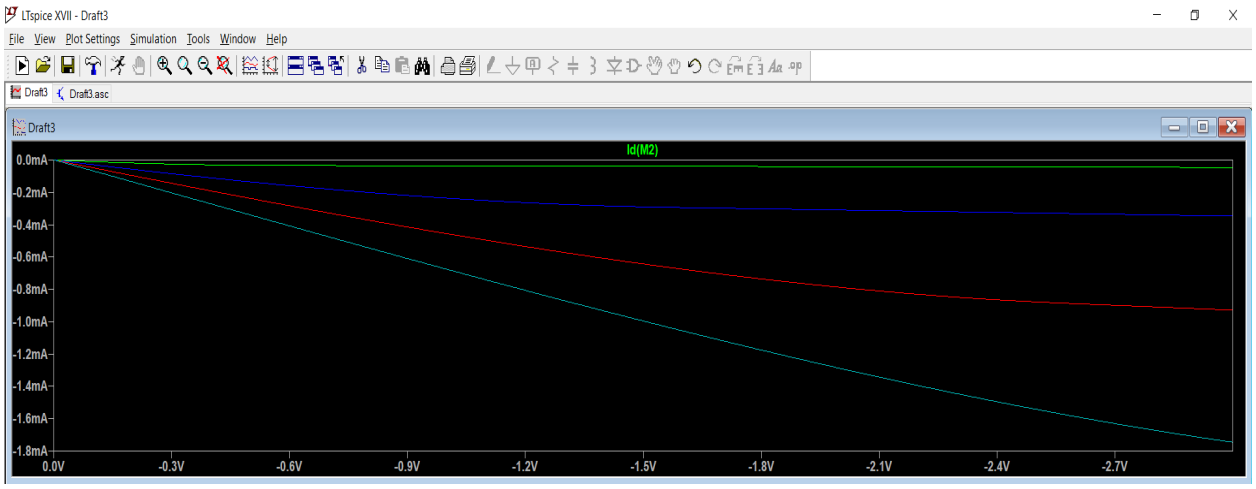
d(Id)/d(Vgs) vs Vds



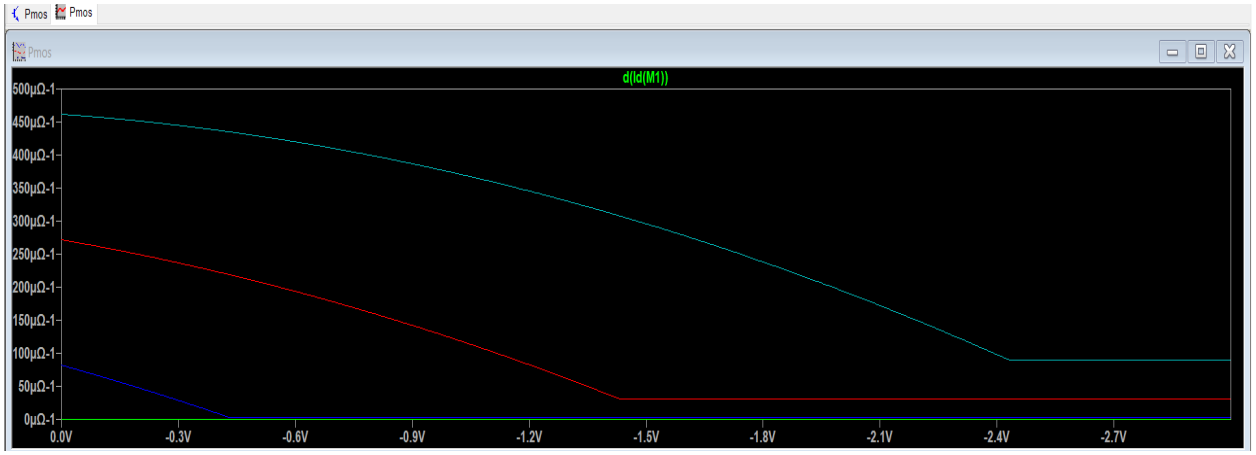
Id vs Vds

PMOS

Output Resistance

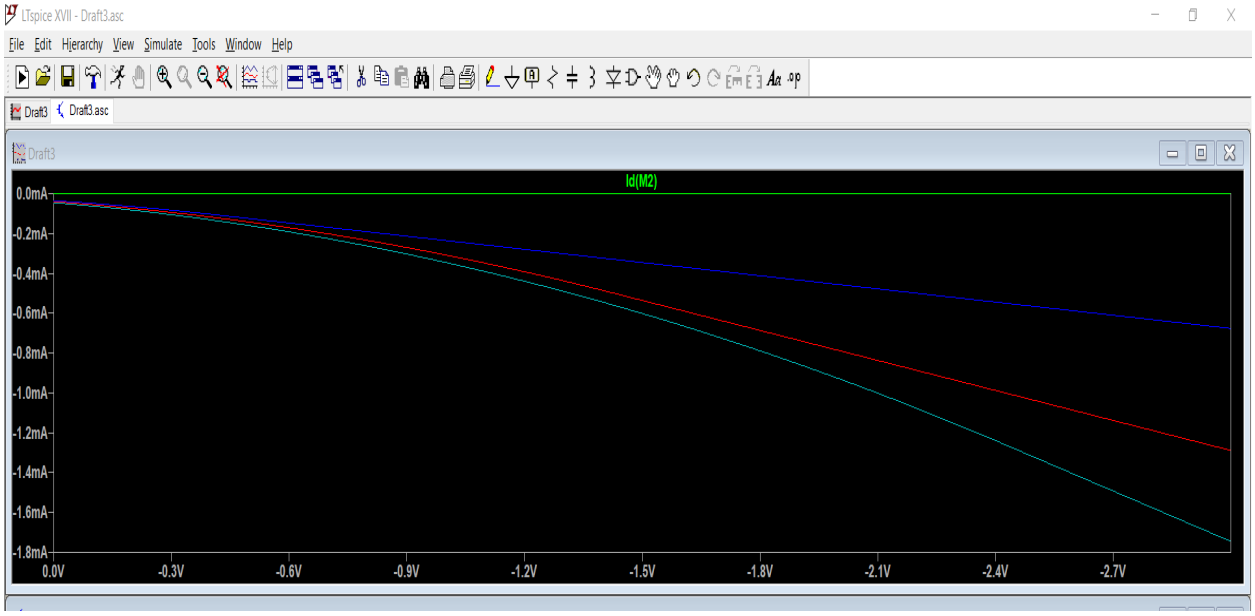


Id Vs Vgs

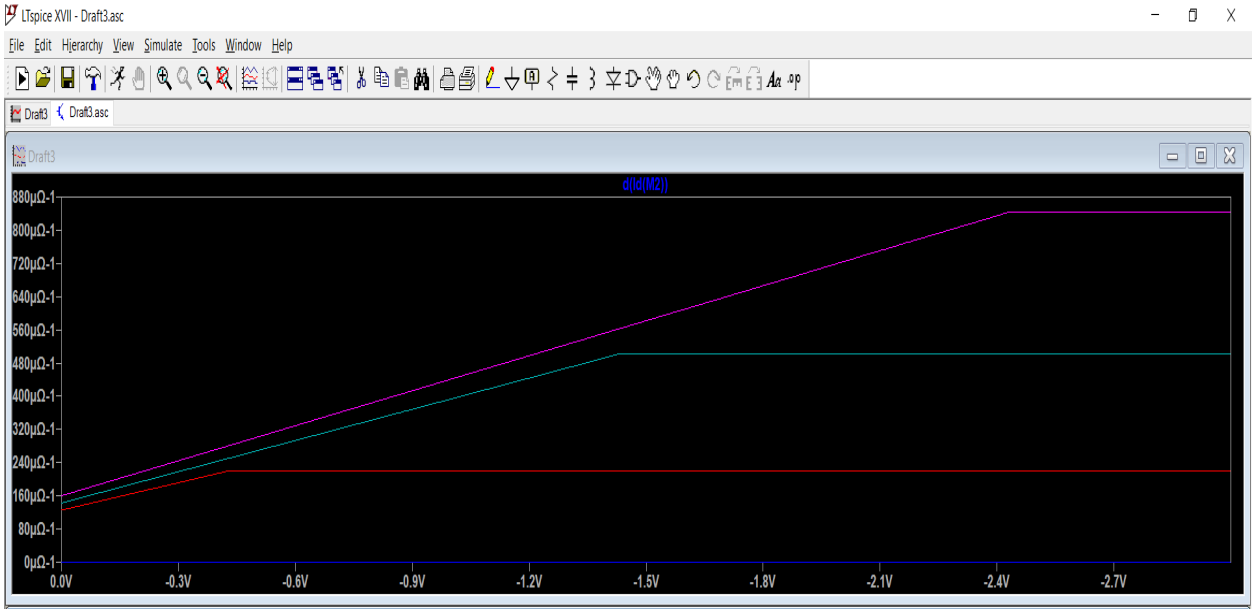


d(Id)/d(Vds) vs Vgs

Transconductance



Id vs Vds



d(Id)/d(Vgs) Vs Vds

Note:

On keeping various different values of Vsb we had seen a few changes in the result as the body effect does play a role in determining the final values. Like if we keep the value of the Vsb = Vgs then there won't be current as it increases the threshold voltage and if we keep values that are less than Vgs then the value of rd reduces in the presence of Vsb.

Results:
The parameters turned out to be the same for both PMOS and NMOS.
Output Resistance decreases with an increase in Vgs.
Transconductance increases with an increase in Vds.

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