Control Engineering
Experiment - 4

Controller design on MATLAB platform by analog frequency response.

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Aim of the experiment

The project requires the design of a cascade lead-lag transfer function for a given analog sun-seeker transfer function, according to desired specifications provided.

Theory

All the time domain methods are convenient to work in situations where the existing output of an OLTF and desired output by the required CLTF are known in terms of response measures through experiments but there are several systems where we don't have the freedom to apply any inputs we want(i.e. experiments) and are susceptible to a large range of disturbances.

To tackle such issues frequency-domain methods are used through designs by **Bode Diagram** or by **Nyquist Diagram.**

Bandwidth is defined as the frequency between the limits (within which the system is expected to perform) at which the power of the output signals drops to half its maximum value.

The main advantage of frequency domain designs by magnitude and phase variations has to do with the additive and subtractive characteristics which they provide.

Transfer Function :

In this experiment, we were provided with an Open Loop Transfer Function for sun-seeker control system as:

$$G_{OL}(s) = \frac{2500k}{s^2 + 25s}$$

To meet the second design requirement, we are provided with an all-pass compensator of the form

$$G_c(s) = \frac{1 + aTs}{a*(1 + Ts)}$$

to cascade with the given OLTF.

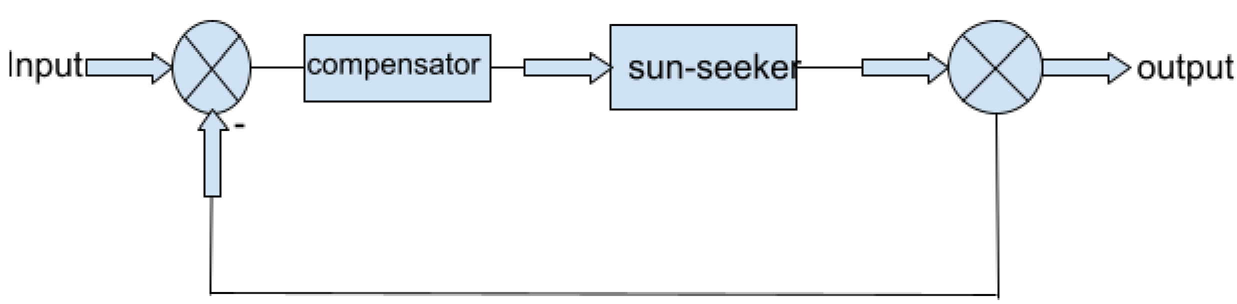


Fig.-Block Diagram of Compensated Sun seeker Control System

Design Requirements and Constraints

There are two performance requirements for the CLTF operation

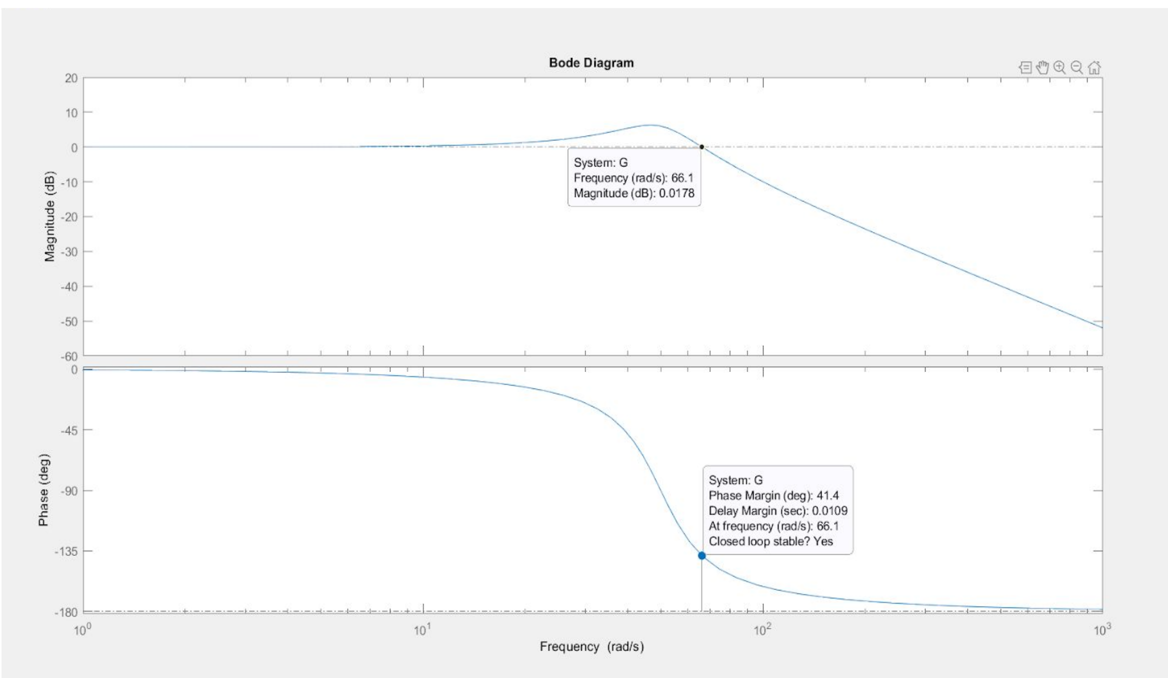
- The steady-state error to a ramp input at reference tilt angle is derived (by the usual Final Value Theorem), to be 0.01/K. This must always assume a value of 0.01 or less.
- The phase margin of the system should be greater than 45° for stability

The minimum value permitted for K is unity.

Plot and Analysis

For steady-state error design constraint:
Using the final value theorem,
$e_{ss} = \lim_{s \to 0} sE(s)$, where E(s) is the error signal between the reference to the actual tilt angle.
The steady-state error came out to be equal to 0.01/K and for all the values of K>=1, steady-state ramp input error will be <=0.01. This satisfies our criteria for steady-state error constraint.

Moving on to the second performance requirement, we first plot the uncompensated bode plot for the closed-loop transfer function at k=1. Here is the plot for the same:



Plot 1: Uncompensated phase margin plot

The uncompensated system for K=1 has a phase margin of 41.4 as shown in the bode plot. So, we can tell that a minimum of $45^{\circ} - 41.4^{\circ} = 3.6^{\circ}$ additional phase margin needs to be introduced by the compensator.

To get this additional phase margin we go through a systematic approach of varying K, a and T. We can rewrite the compensator transfer function as :

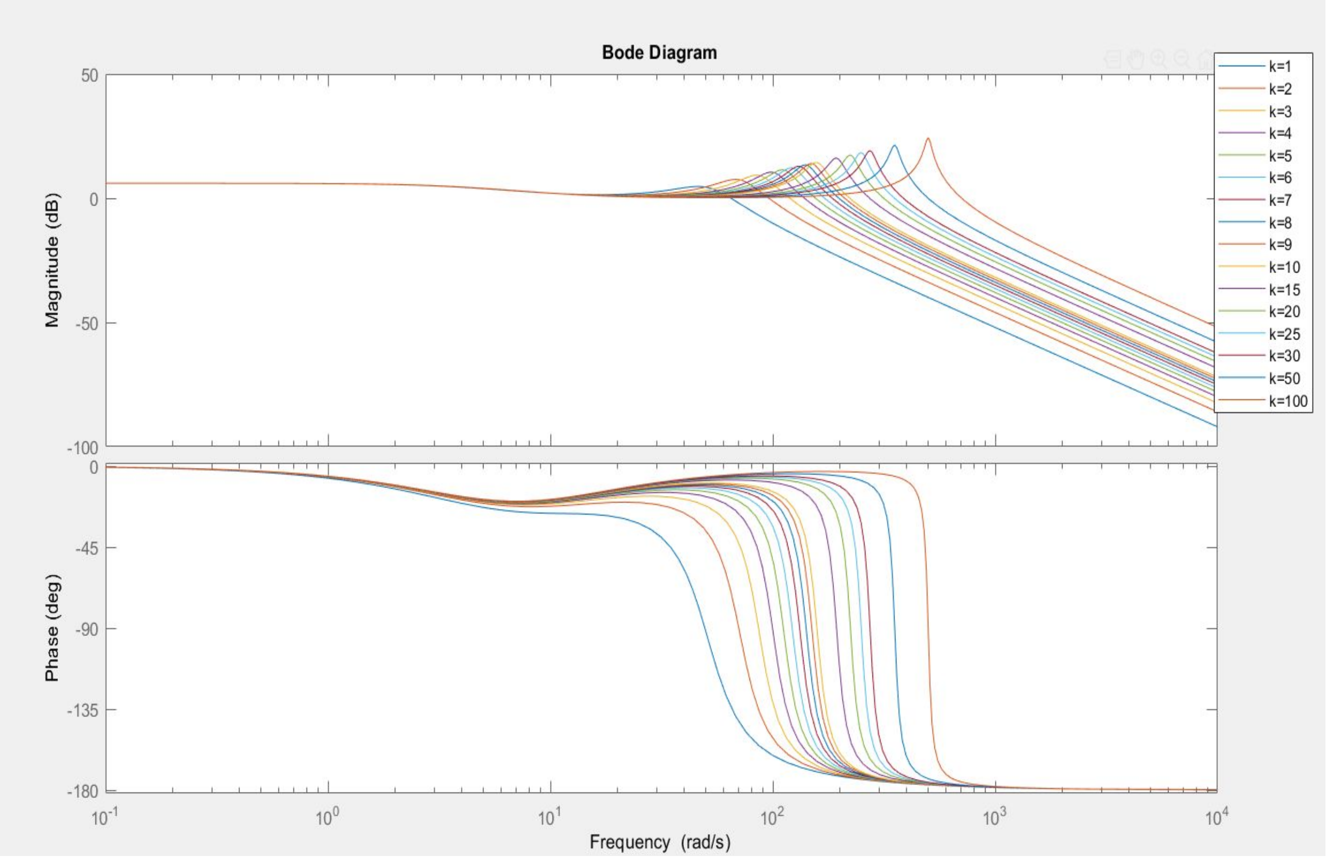
$$G_c(s) = \frac{\frac{1}{aT}+s}{\frac{1}{T}+s}$$

which gives us zero and a pole for the compensator at s = - 1/aT and s = -1/T respectively. We consider the lead condition first i.e. the compensator zero is closer to the origin as compared to the compensator pole, or to say a > 1.

Case 1: a > 1, a lead condition for compensator

In this, we first observe the plot for different values of K to get a rough idea of the variation of phase margin with respect to K for the given case.

Here we have taken a=2, t=0.1 and for K we have taken a range of values as 1 to 10 ,15 ,20 ,25 ,30 , 50 ,100.



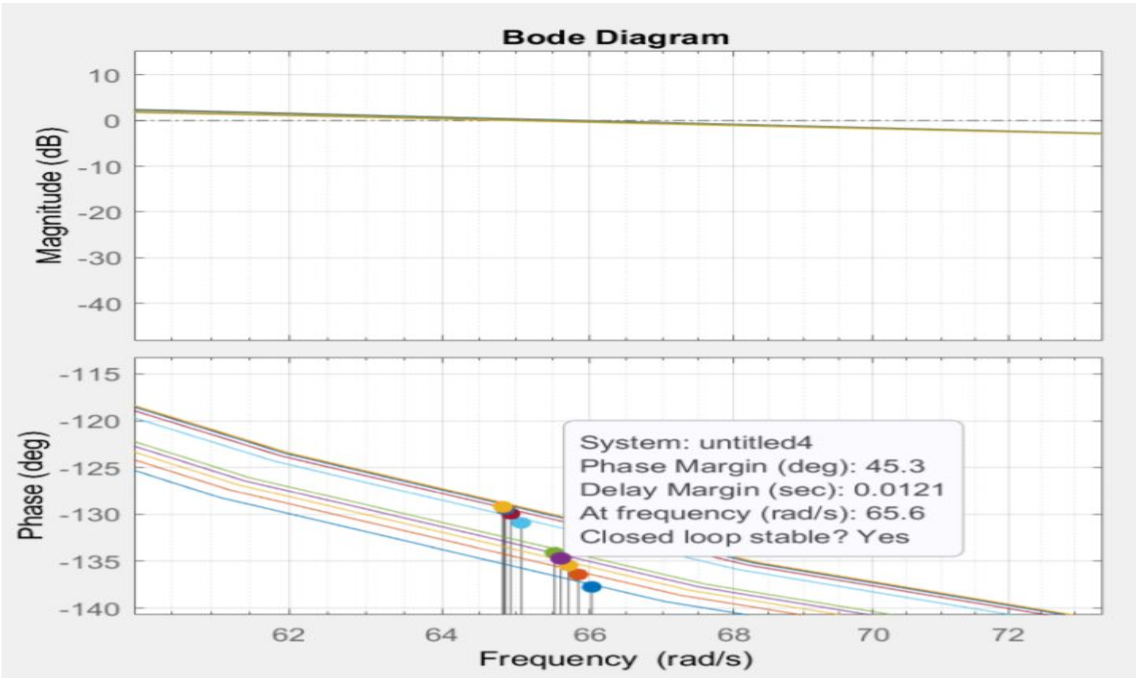
Plot 2 : a= 2; t=0.1 ; and varying K

In plot 2 we observe that we achieve a phase margin greater than 45 degrees for values only close to 1.

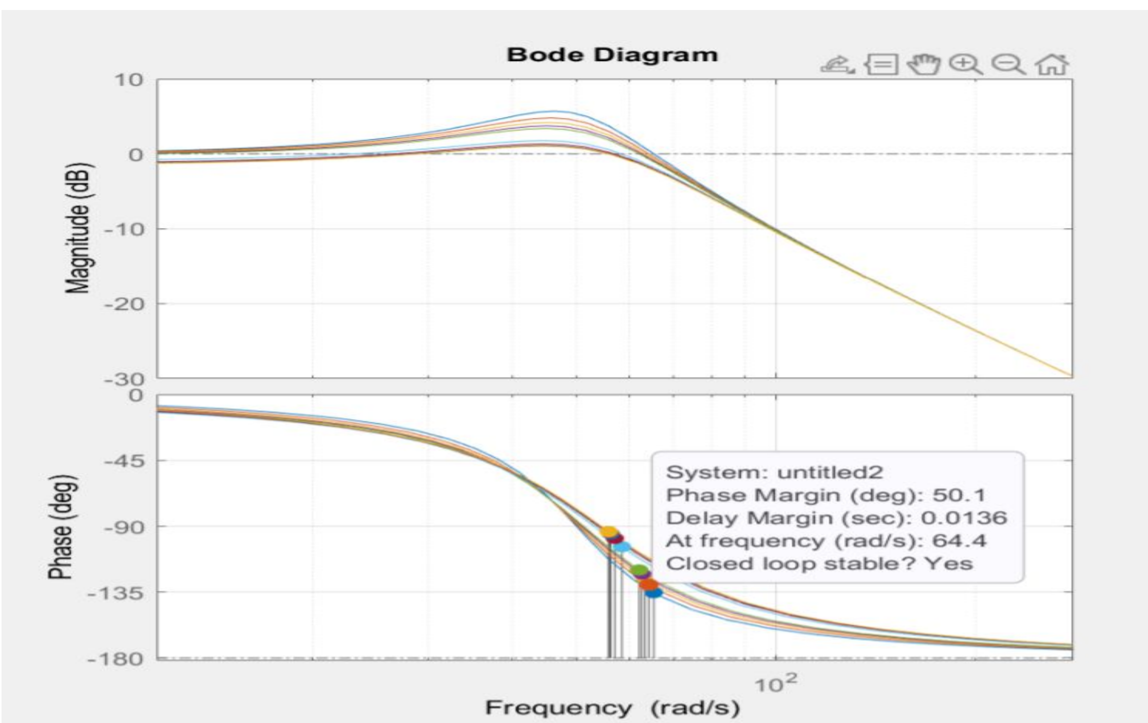
Now further we have two situations as T>1 and T<1 for further analysis categorically

Case 1.a: a>1 ,T<1

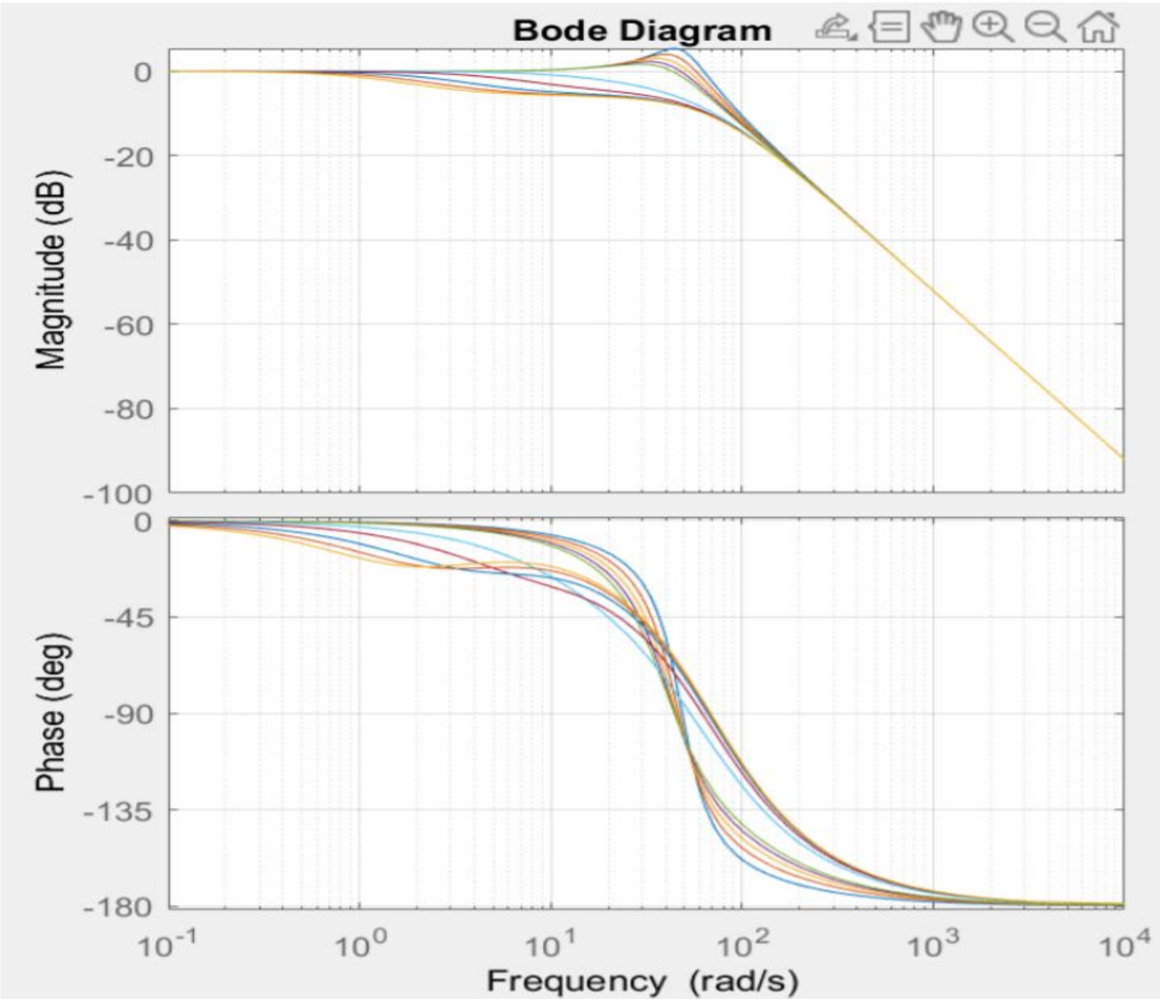
Now fixing K=1 and fixing T for some values and varying a for a range of values.



Plot 3: K=1, T=0.2, and different values of a >1



Plot 4: k=1, T=0.05, and different values of a >1



Plot 5: K=1, T=0.01, and different values of a >1

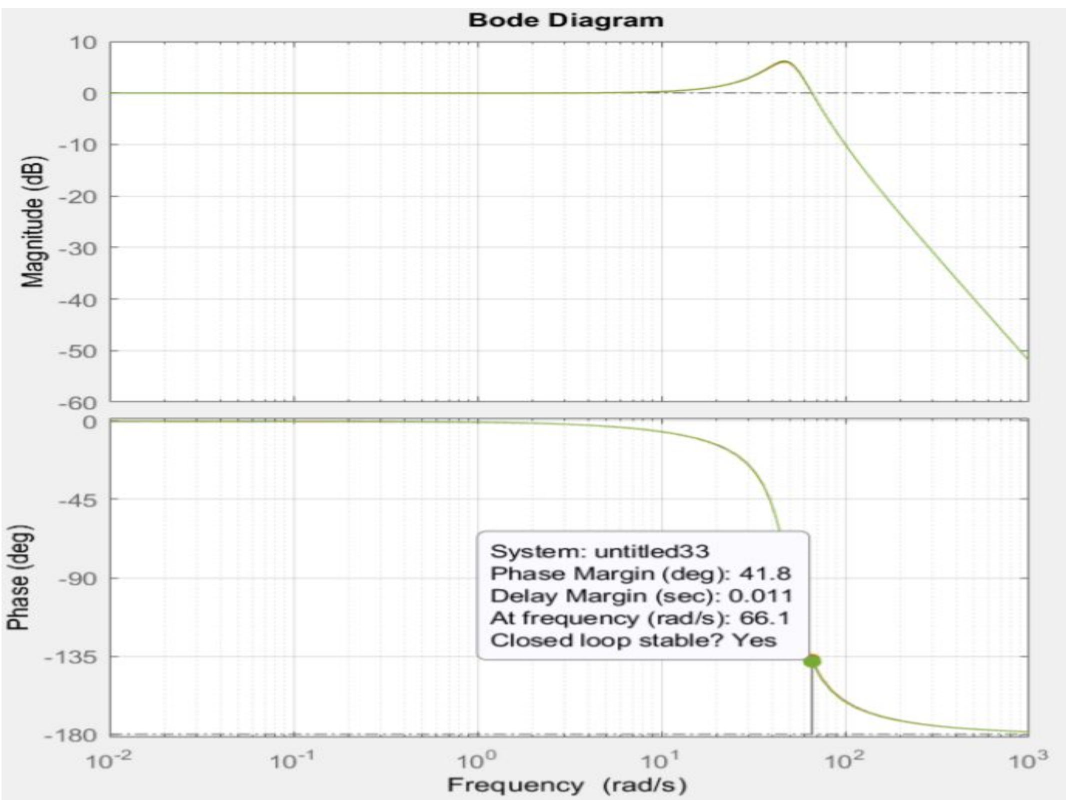
Phase margins for different values of 'a' and 'T' are tabulated below for the analysis of above graphs.

a\T	**0.8**	**0.5**	**0.3**	**0.2**	**0.1**	**0.05**	**0.01**
1.1	41.6	41.7 deg	42.0	42.3	43.1	44.7	48.3
1.3	41.9	42.3	42.9	43.6	45.8	50.1	60.8
1.5	42.2	42.7	43.5	44.6	47.8	54.2	72.1
1.7	42.4	43	44.0	45.3	49.3	57.5	82.4
1.9	42.5	43.2	44.4	45.9	50.6	60.2	92
5	43.3	44.4	46.5	49.1	57.2	76.1	unstable
10	43.5	44.8	47.1	50.1	59.4	81.8	unstable

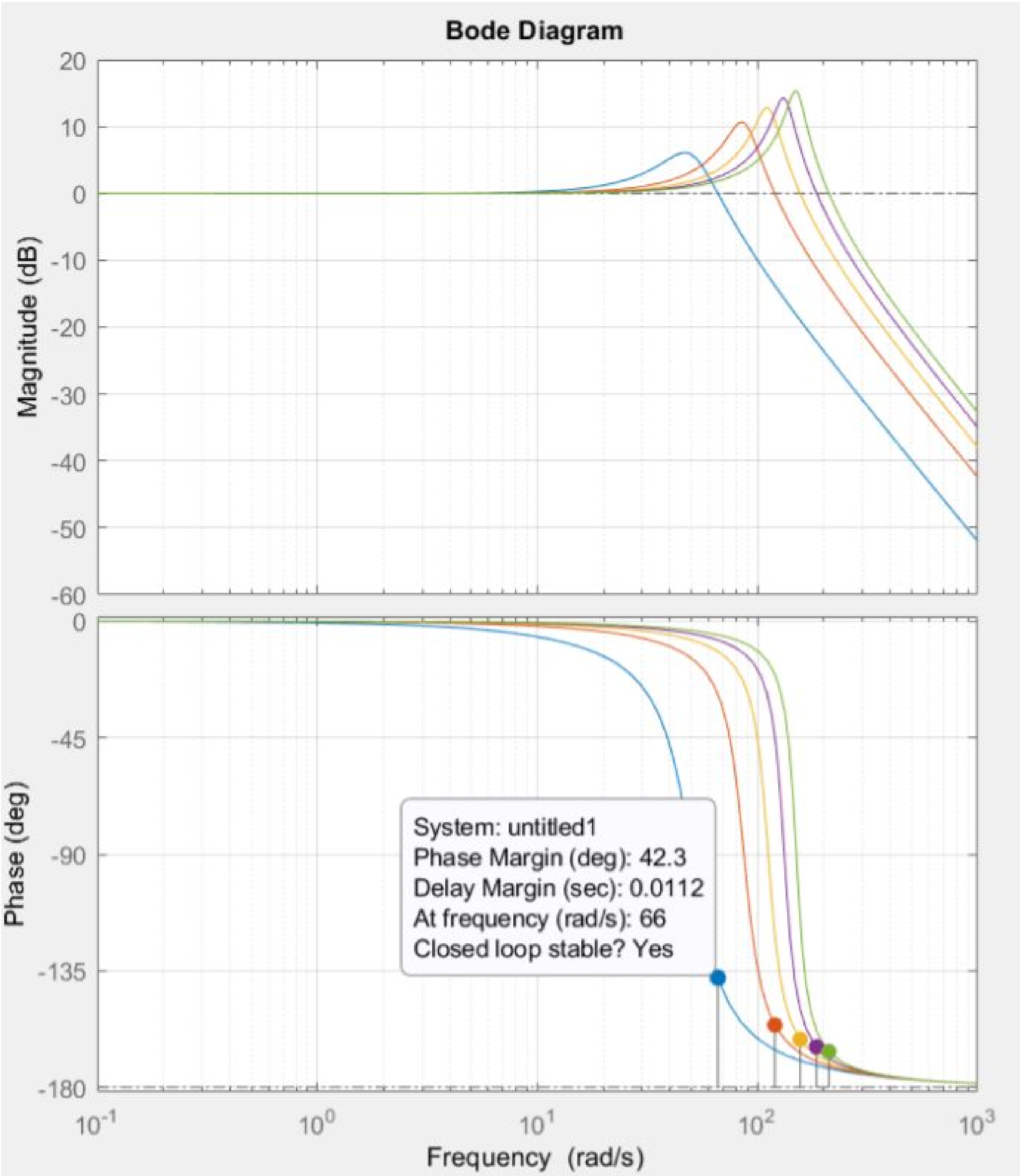
20	43.6	45.0	47.4	50.5	60.4	84.4	unstable
30	43.7	45.0	47.5	50.7	60.7	85.9	unstable
40	43.7	45.1	47.6	50.8	61.0	86.5	unstable
50	43.7	45.1	48.0	51.0	61.3	87.2	unstable

From the above table we observe that we get phase margin greater than 45 for
a) T = 0.5 and a $\geq$ 20
b) T = 0.3 and a > 5
c) T = 0.2 and a >1.7
d) T = 0.1 and a> 1.3
e) T = 0.05 and a> 1.3
f) T = 0.01 and a> 1.1 and a < 5
We can generalise the solution that we get desired performance for 0.03 $\leq$ T $\leq$ 0.5 for the values of 'a' as defined above. For the values T $\leq$ 0.03, at the higher values of 'a' , the system becomes unstable.

Case 1.b: a>1 ,T>1



Plot 6: K=1; T=2,3,5; and various values of a>1



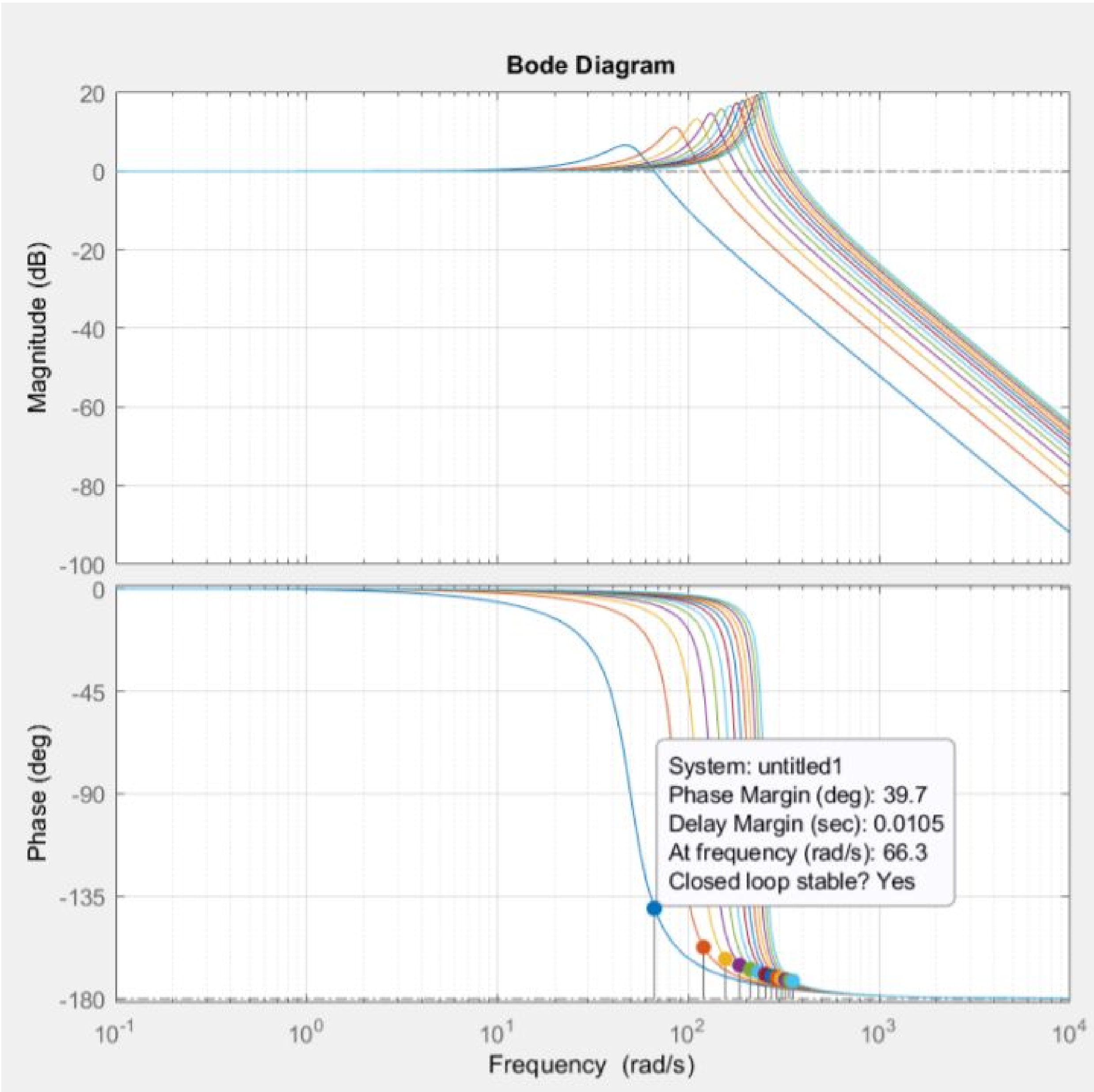
Plot 7

In plot 6 we observe overlapping plots with a maximum phase margin of 41.8. This doesn't satisfy the performance requirements.

So we try to vary K in plot7, but observe a previous result that phase margin decreases on increasing K. Thus we do not get any point in a>1 and T>1 subcase which can fulfil the performance requirements.

Case 2: a < 1

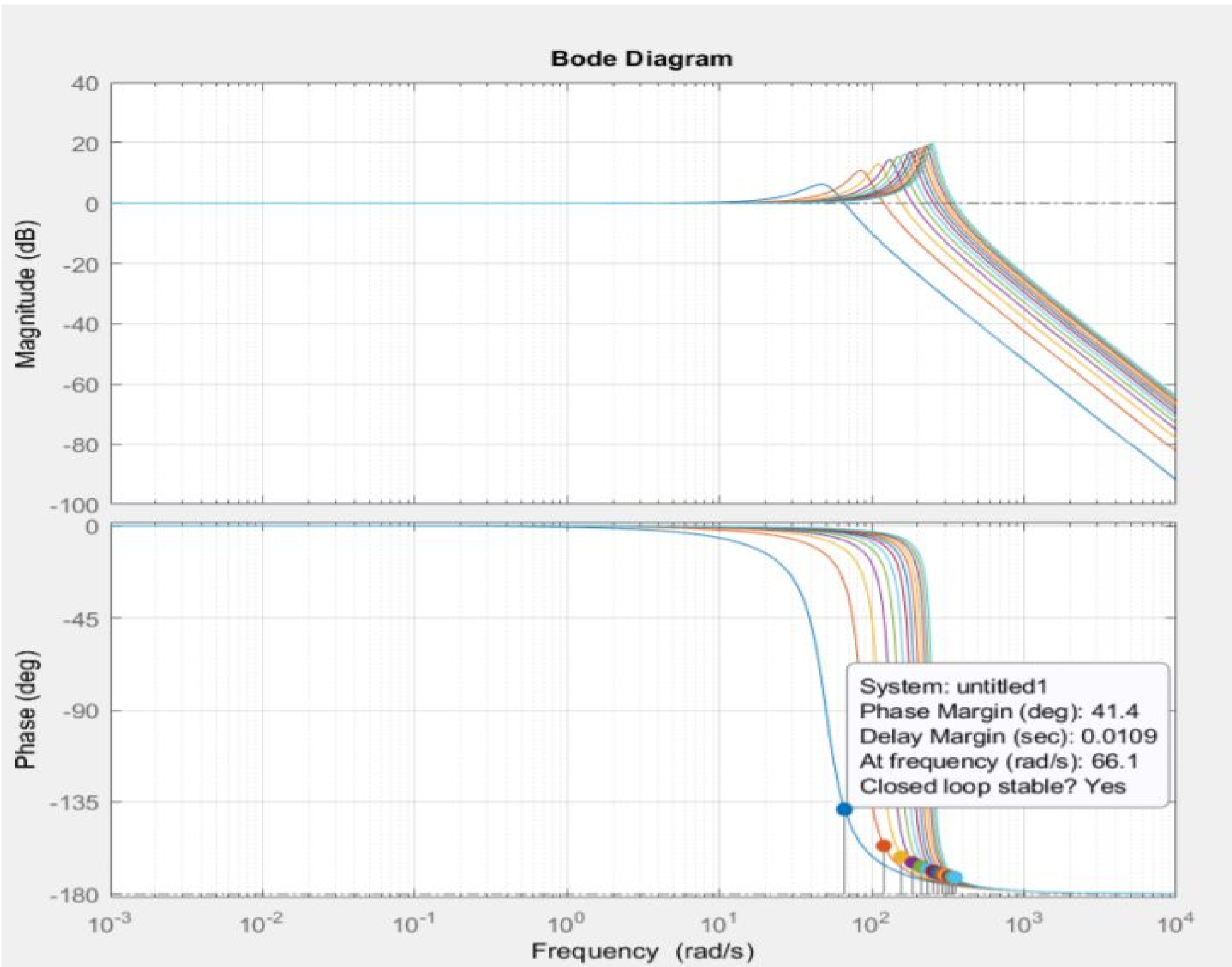
We plot the following for different values of K at a =0.1 and t=10.



Plot 8

We observe that we are not able to get the desired phase margin for any K.

So in the next plot, we increase the value of T to get to the limiting condition of phase margin for the lag compensator. The following plot is for different values of K at a =0.1 and t=1000.



Plot 9

Plot 9 shows us that the maximum phase margin possible for a lag compensator is 41.4 which is the same as the uncompensated phase margin in plot 1. This happens because as we increase T to a large value(T>>a), the zero and pole of the compensator tend to overlap and cancel each other resulting in a non-cascaded OLTF.

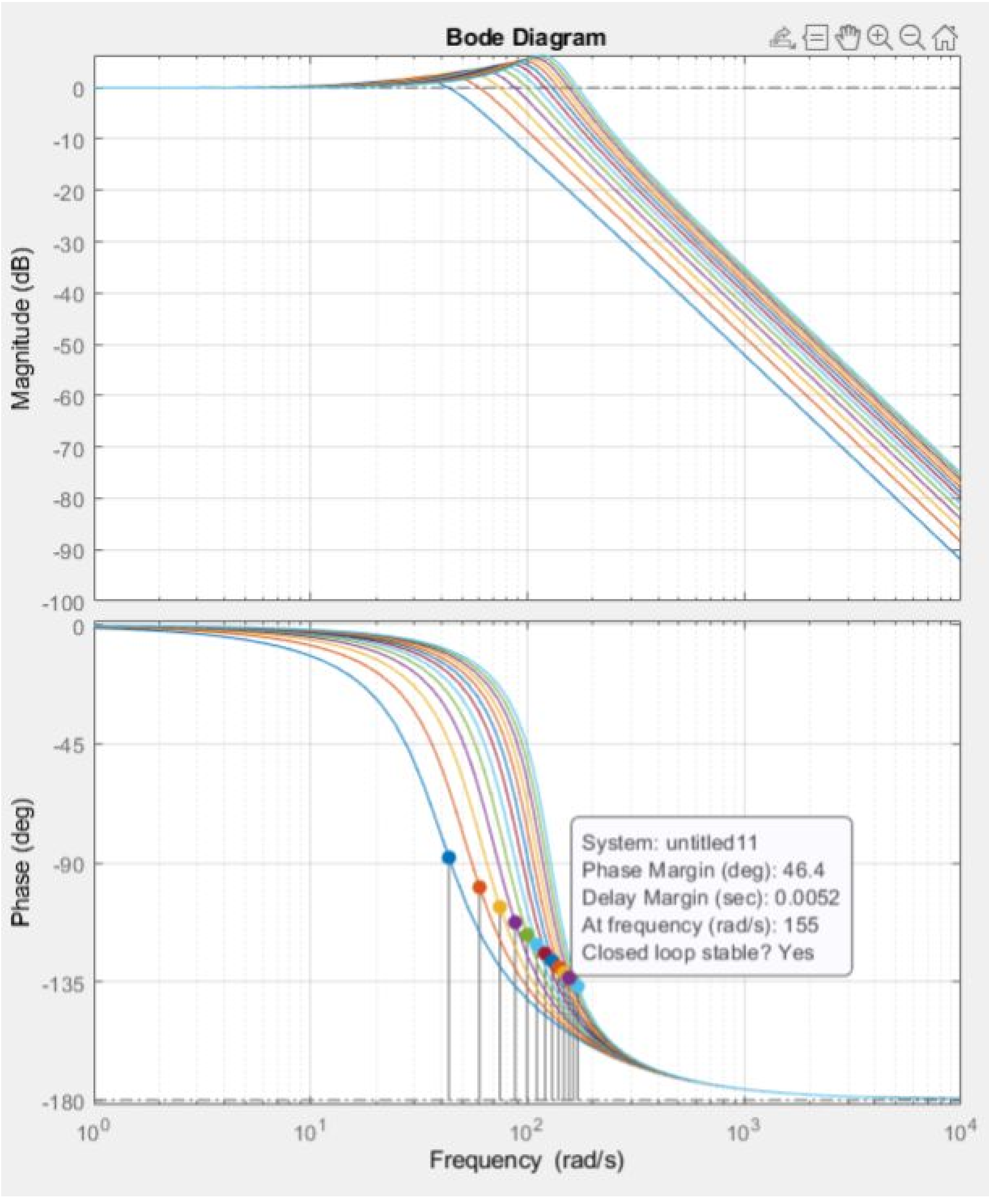
The observation goes well with terminology. A lag compensator is apt to produce a phase lag, whereas our design requirement requires a minimum phase lead of 3.6 degrees. Thus we shall not be able to use the lag condition for our system.

For a<1 and T<1, we are not getting any value that can satisfy our system requirements.

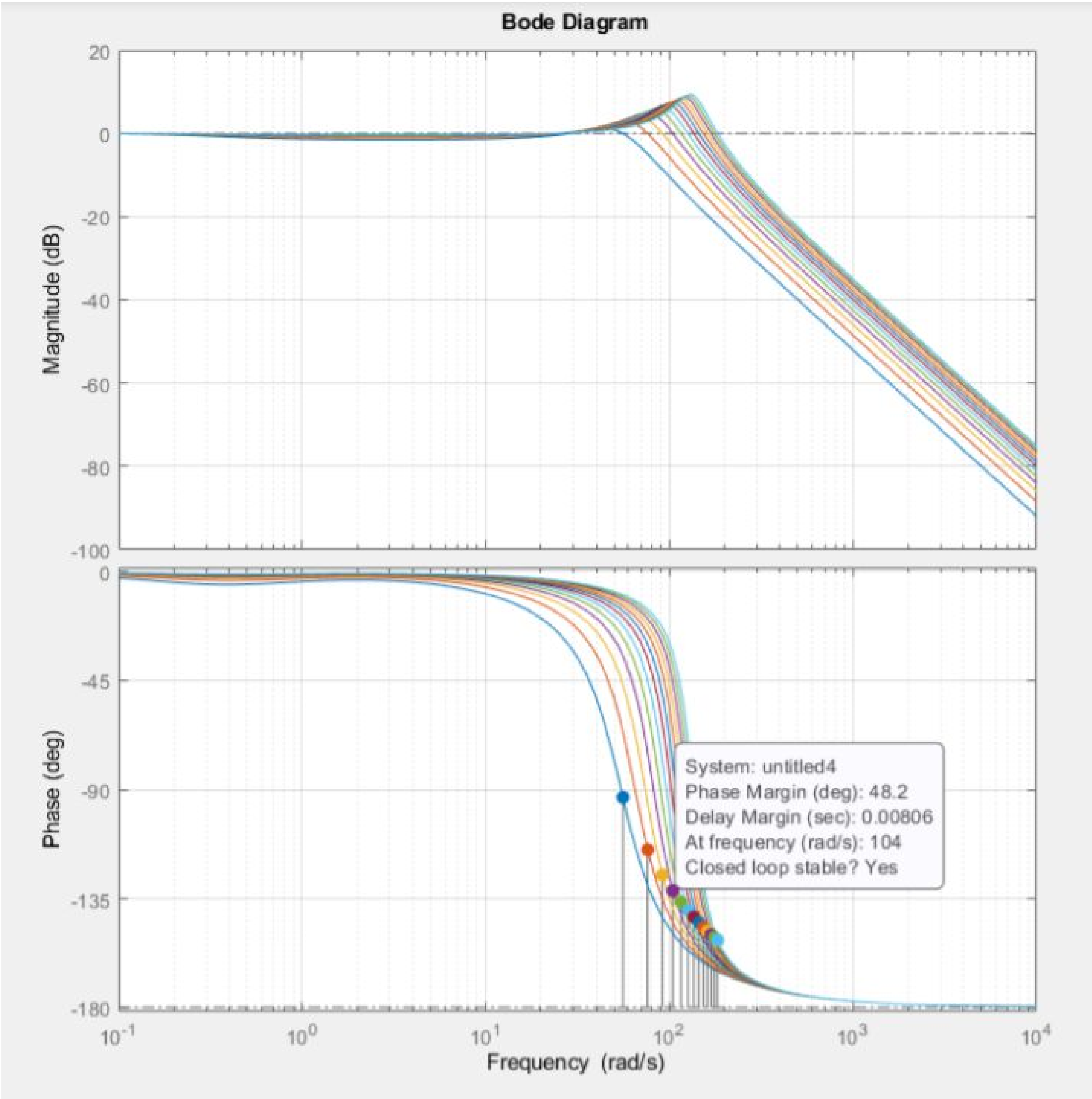
For $a<0.07$ and $T<0.5$, we are getting an unstable system with negative phase margin values.

Attaining higher values of K

In an attempt to get a precise value of steady-state error we may require larger values of K. So we try to increase K for those values of a and T which have the highest (as phase margin decreases on increasing K).



Plot 10 : a = 1.8, T=0.01 and different values of K (Phase Margin = 92° when K=1)



Plot 11 : a = 50, T=0.05 and different values of k (Phase Margin = 86.8 0 when K=1)

Table for analysis

Phase Margin	a = 1.9, T=0.01	a = 50, T=0.05
K = 1.0	92.0	86.8
K = 1.5	80.7	65.1
K = 2.0	73.2	54.7

K = 2.5	67.4	48.2
K = 3.0	58.8	43.6
K = 3.5	55.6	40.1
K = 4.0	52.8	37.3
K = 4.5	50.4	35.0
K = 5.0	48.3	33.1
K = 5.5	46.4	31.5
K = 6.0	44.7	30.1
K = 6.5	43.2	28.5
K = 7.0	41.7	27.1

On theoretical value, we can take the maximum value of K as 5.5, and even increase it by decreasing the value of $T < 0.01$.
Thus we can say we can take maximum K as 2.5 in the condition of $a = 50$ and $T = 0.05$ and K=5.5 for the a=1.9, T=0.01.

Steady-State error Design constraint:

We have designed our cascaded control system from the perspective of phase margin requirements. After cascading with a compensator, steady-state error to a ramp input is now changed accordingly.

$$e_{ss} = \lim_{s \to 0} sE(s)$$

For ramp input, this is equal to,

$$e_{ss} = \lim_{s \to 0}\left(\frac{1}{s(G_{OL}(s) * G_c(s))}\right) = \frac{0.01}{(\frac{K}{a})}$$

This implies that to satisfy steady-state error constraint, $(K/a) \geq 1$.
So, we can say that system will work perfectly for $2.0 \leq K \leq 5.5$ for a=1.9 and T=0.01.
Similarly, other ranges of K can also be obtained at specific values of a and T.

Observation and Discussion

1. Here, we are trying to design our control system as per the given constraints with the help of Bode plots which provide us with two important parameters to check the stability of the system i.e., ***Gain margin*** and ***Phase margin.*** In our system, design requirements were for the phase margin which is now fulfilled using a compensator. Greater will the phase margin greater will be the stability of the system. It refers to the phase which can be increased or decreased without making the system unstable.

2. The performance requirement of the value 0.01/K is always less than or equal to 0.01 is always satisfied considering the constraint of K >= 1 in an uncompensated system. But by adding a compensator, the steady-state error is changed to (0.01a/K). So, we can pick only those values which satisfy (K/a)>=1.
3. The uncompensated phase margin is 41.4. Thus we require a minimum of 3.6 (45 - 41.4) additional phase margin needs to be introduced by the compensator to get the desired performance.
4. We get the performance requirement of phase margin greater than 45 in the lead condition for a(range of 'a' different for different values of T) when T ∊ [0.03,0.5].
5. We do not get the performance required for any value of K, a, T in the lag condition.
6. To get a precise value of ramp input error, we can increase the value of K from 2.0 to 5.5 for a=1.9 and T=0.01. At different values of 'a>1' and T<1, we can have similar ranges for K.