Submission Date: 6/05/2021 **Experiment No:8**

Analog Experiment-8

Title:

Design of Sample and Hold circuits and plotting FFT of output waveforms.

Objectives:

- Design a sample and hold(S/H) circuit using a NMOS switch such that the output of the S/H settles to within 1% of the input within 25ns for a step input of 0.6 V and load capacitor of 20pF.
    - ❖ Find the 1% settling time of the designed S/H for an input of 300mV, 900mV and 1.2V.
    - ❖ Simulate this S/H for an input sine wave of 10K frequency and 100mV amplitude. Plot the fast fourier transform of the sampled output, clock waveform and input signal in matlab.
- Use a NMOS-PMOS complementary switch(pass transistor) to obtain the S/H. Find the 1% settling time of the designed S/H for an input of 300mV, 900mV and 1.2V.

Components/Tools Required

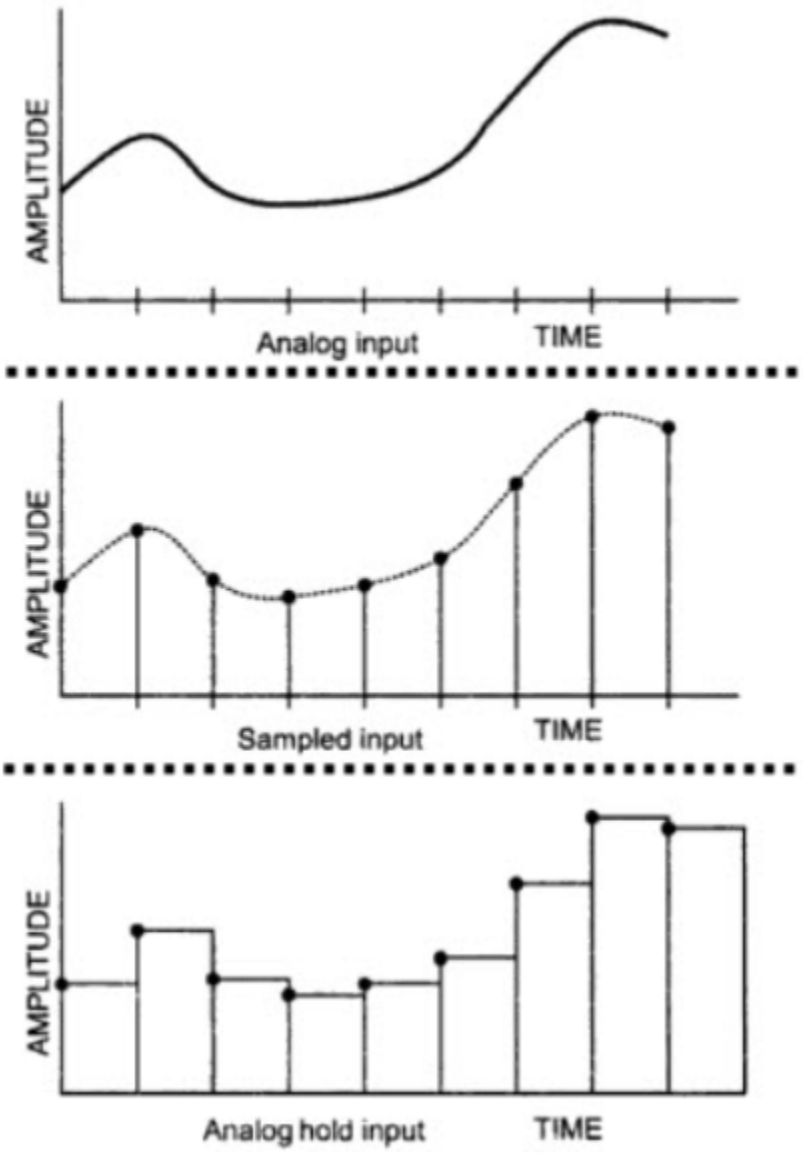
Ltspice, MATLAB

Theory :

- A Sample and Hold Circuit,(S/H Circuit or S & H Circuit) is used with an Analog to Digital Converter to sample the input analog signal and hold the analog signal which has been sampled.
- In the S&H Circuit, the input analog signal is sampled for a short interval of time, usually for 10μS to 1μS. Till the arrival of the next input analog signal (to be sampled), the previously sampled value is held, the duration of which(holding the value) may range between few milliseconds to few seconds.
- **Applications:**
- Analog to Digital Converter Circuits (ADC)
- Digital Interface Circuits
- Operational Amplifiers

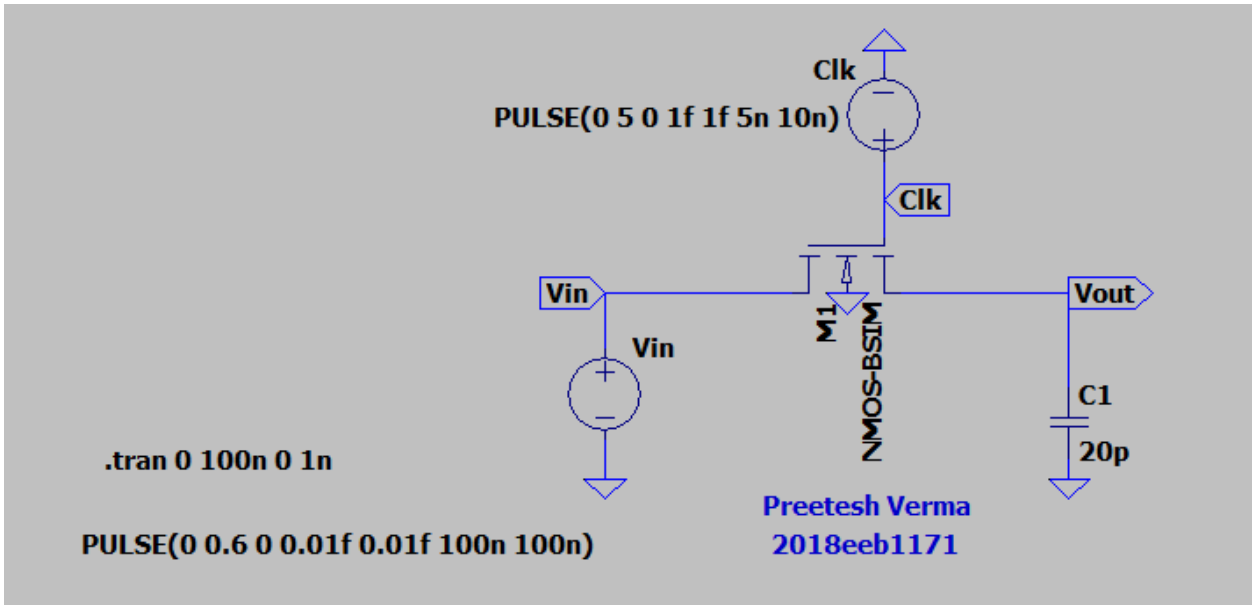
- Analog De-multiplexers
- Data distribution systems
- Storage of outputs of multiplexers
- Pulse Modulation System

Figure below shows the output and input of S/H circuits.

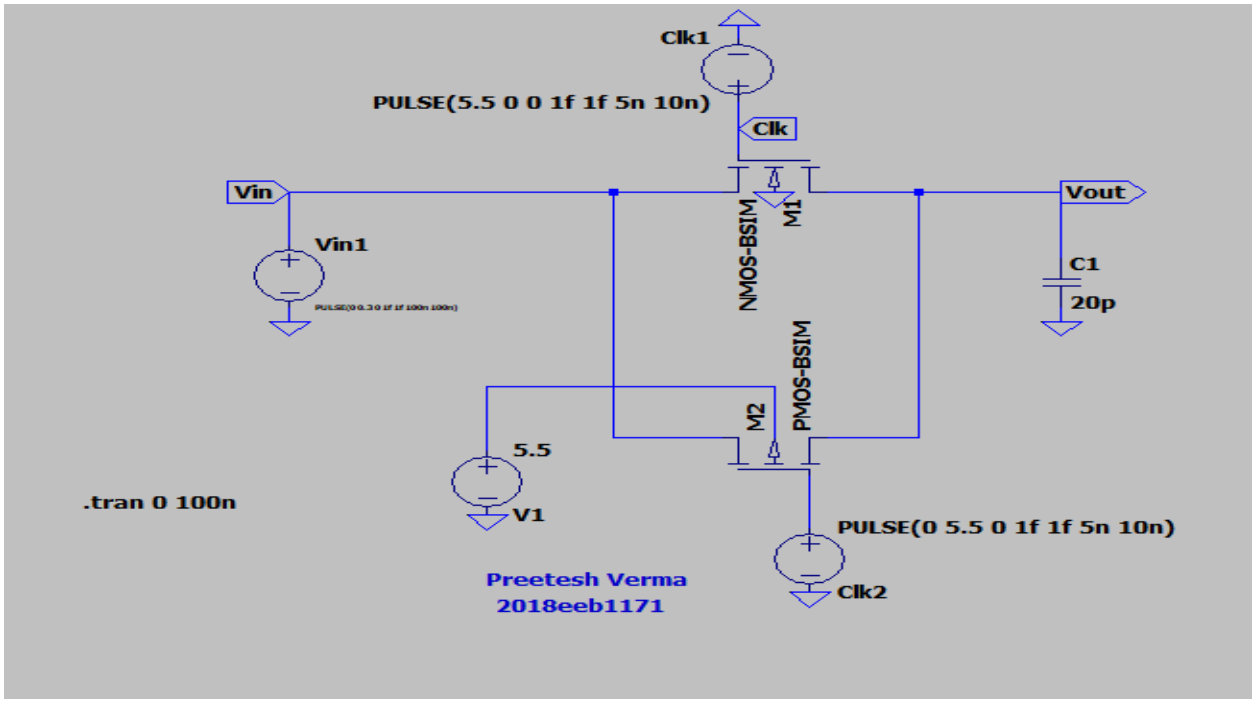


Circuit Diagram:

- S/H circuit using NMOS

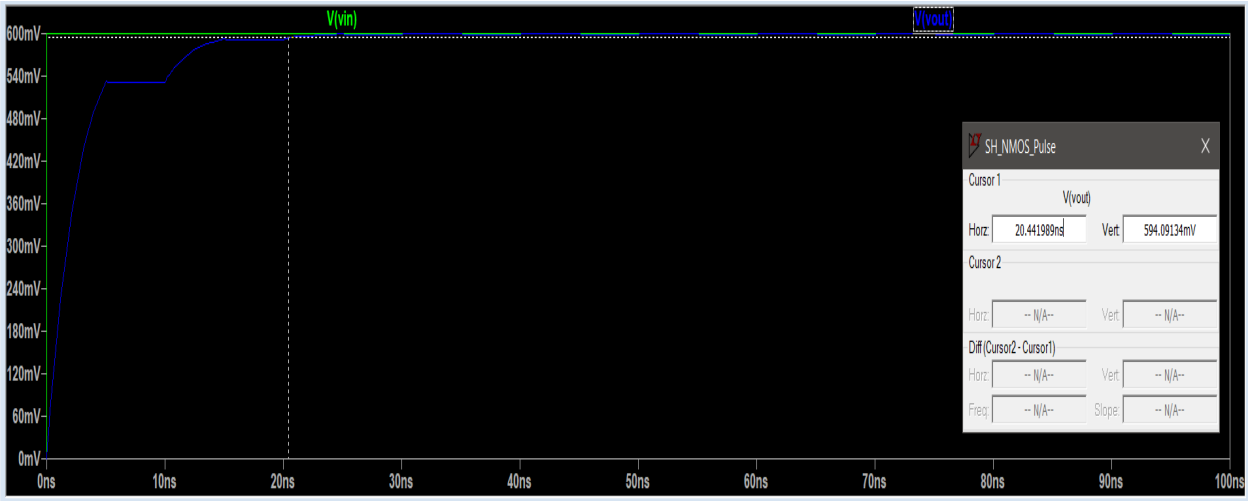


- S/H circuit using Pass Transistor

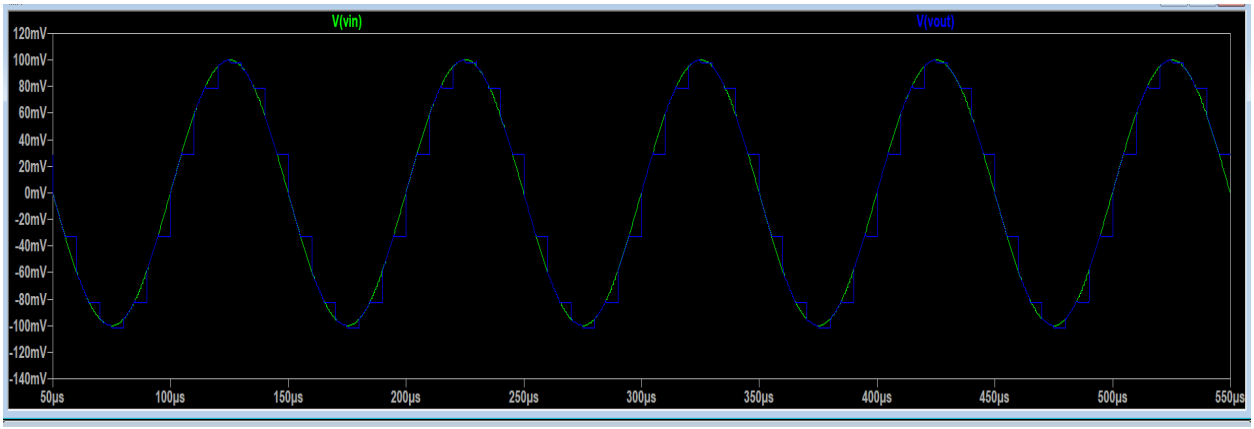


Waveforms:

- S/H using NMOS

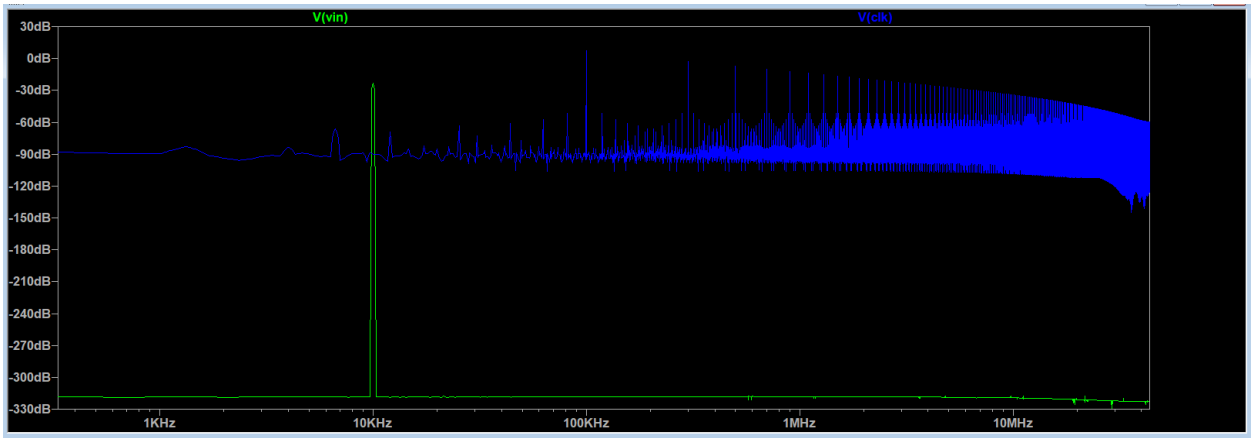


Pulse input : Vout : 1 % settling time = 20.44ns(<25 ns)

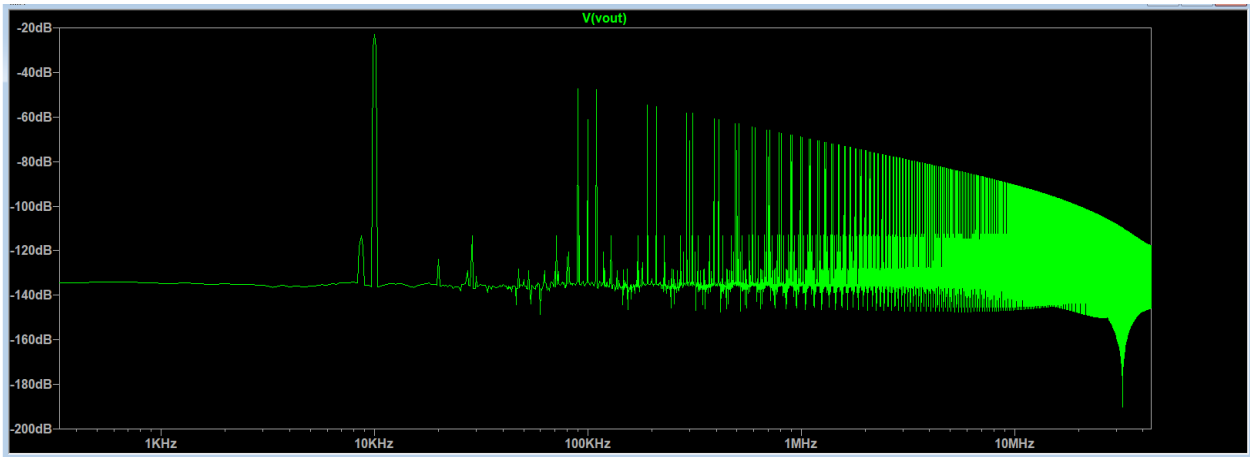


Sine input : 1 KHz and 100V

FFT of PassTransistor NMOS S/H

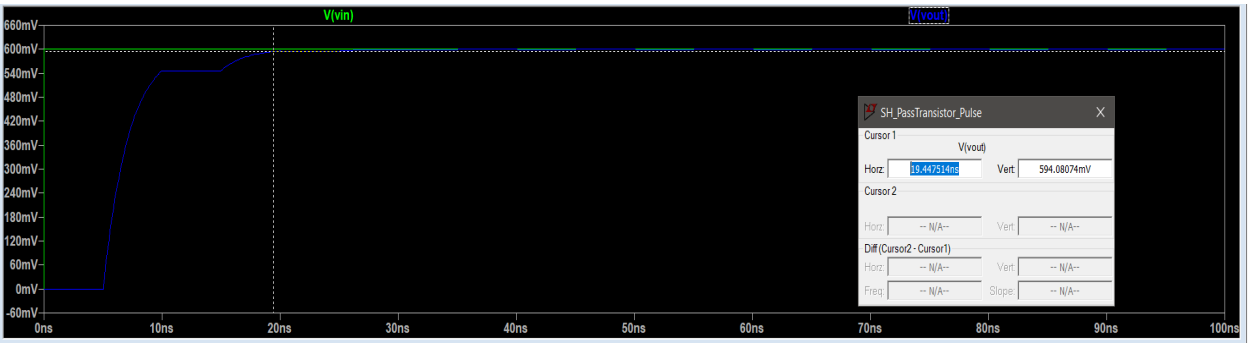


FFT of input Sine wave and clock pulse

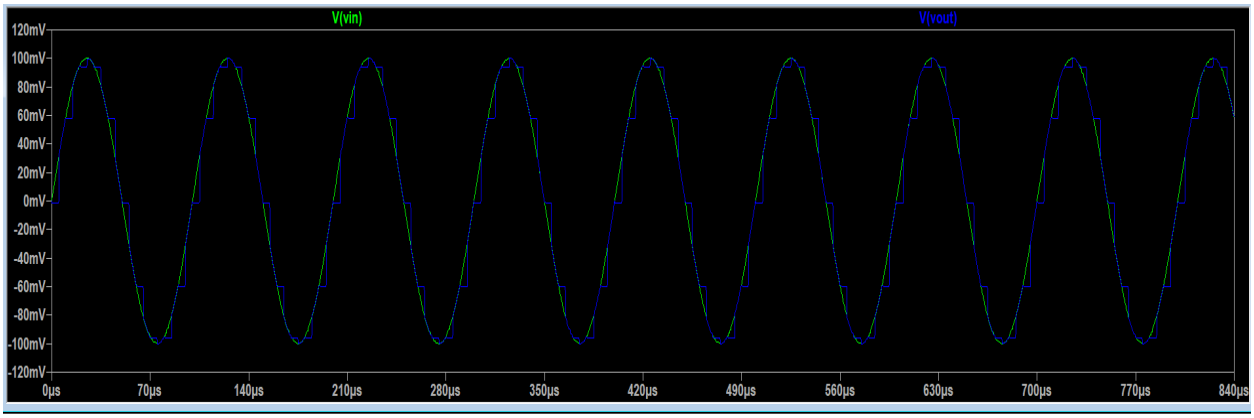


FFT of S/H output

- S/H using PassTransistor

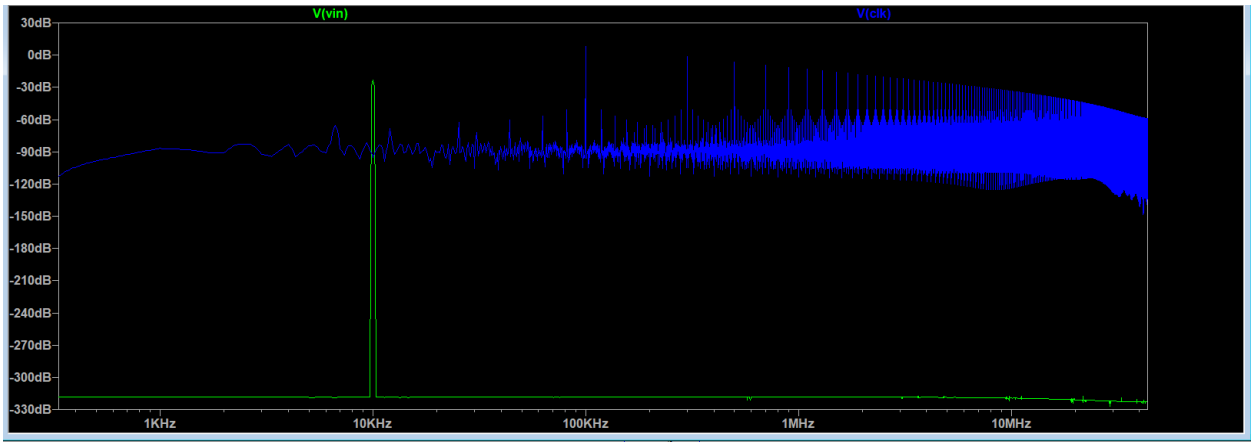


Pulse input : Vout : 1 % settling time = 19.44 ns(<25 ns)

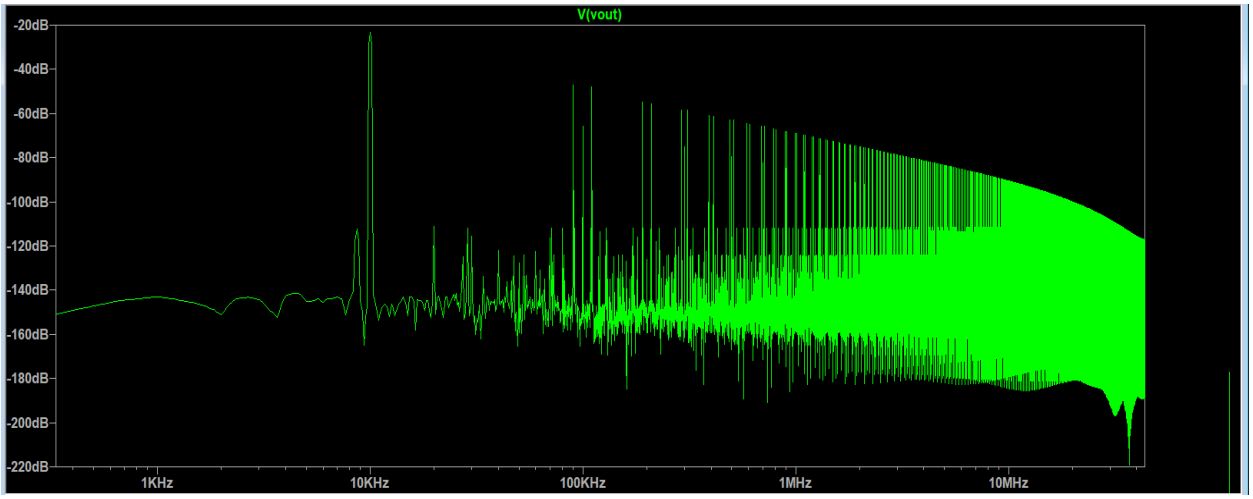


Sine input : 1 KHz and 100V

FFT of PassTransistor S/H



FFT of input Sine wave and clock pulse



FFT of S/H output

Results:

Input Voltage(in V)	1% Settling Time (NMOS)	1% Settling Time (PassTransistor)
0.3	20.3 ns	19.4 ns
0.6	20.41 ns	19.44 ns
0.9	20.92 ns	19.48 ns
1.2	21.17 ns	19.54 ns

Observations :

- Settling time increases in both NMOS and PassTransistor by increasing Voltage.
- Rate of increase of voltage is less in PassTransistor Logic.