Integrated Circuit Technology

Fall Semester-2019

Project : Fabrication of CMOS Using N-WELL Process

-By
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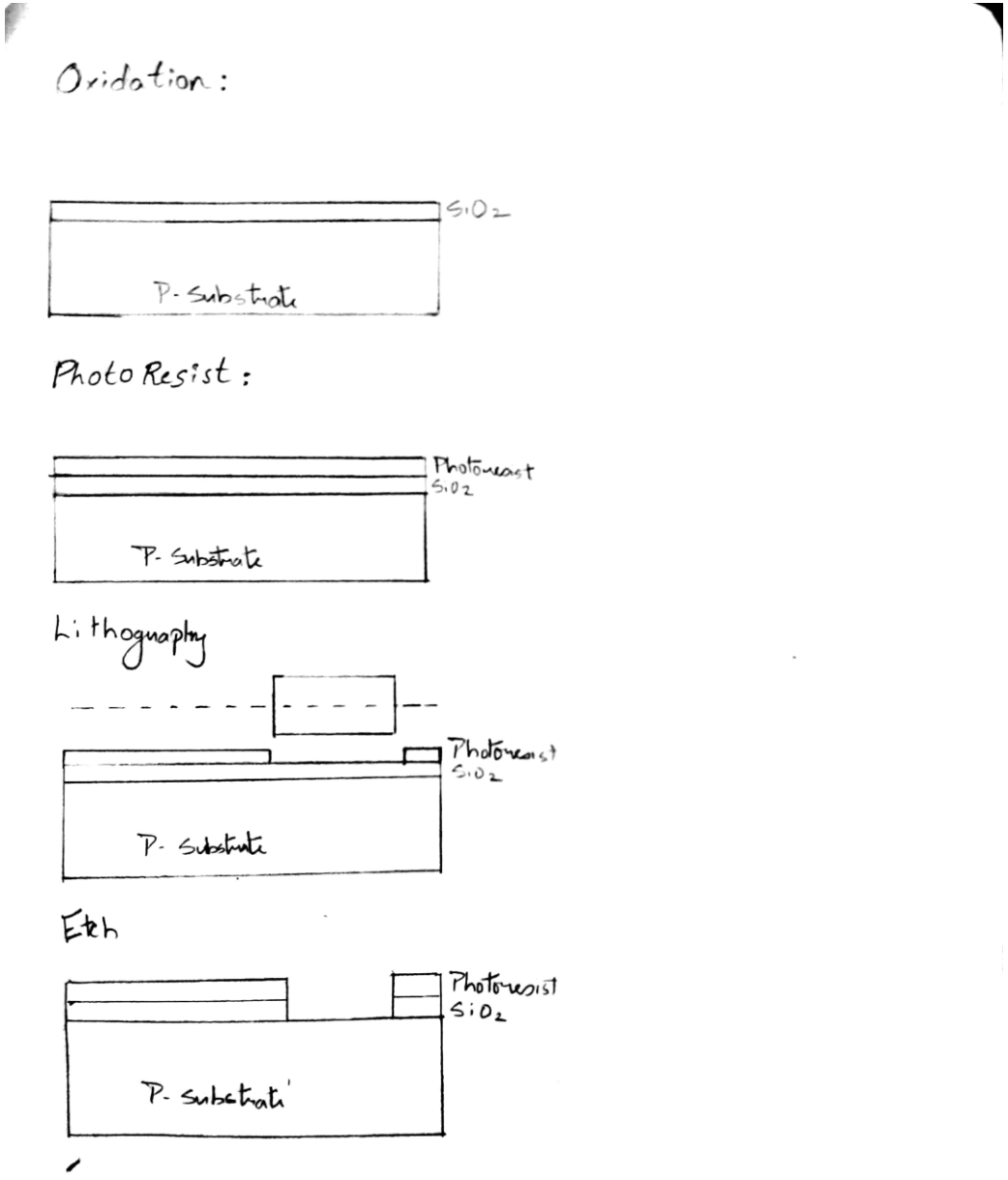
Fabrication Layout:

Oxidation:

Photoresist:

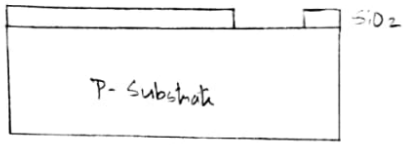
Mask-1 for N-WELL:

Etching:



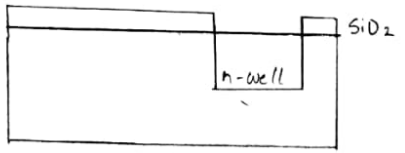
Strip photoresist

Strip Photoresist:



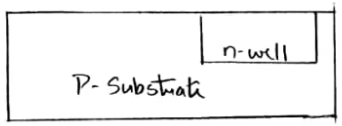
Diffusion of N-WELL layer:

n - well



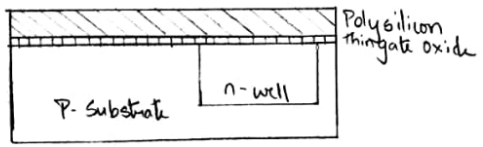
Strip Oxide

Removal of oxide layer:

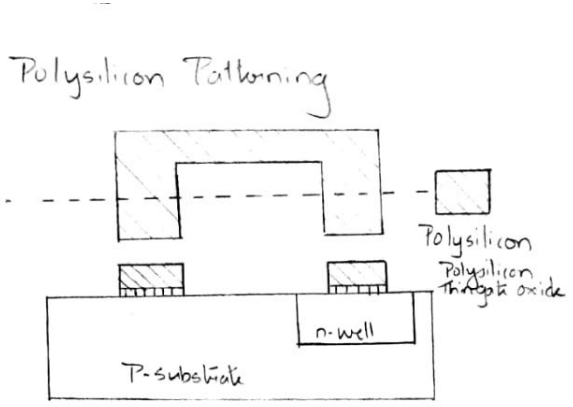


Polysilicon

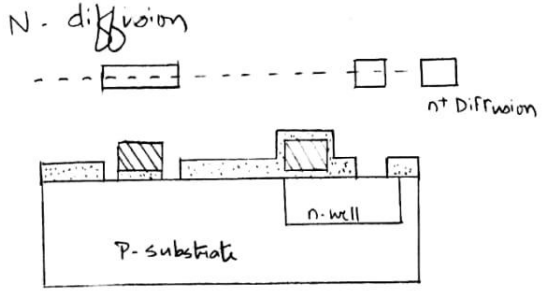
CVD Polysilicon layer:



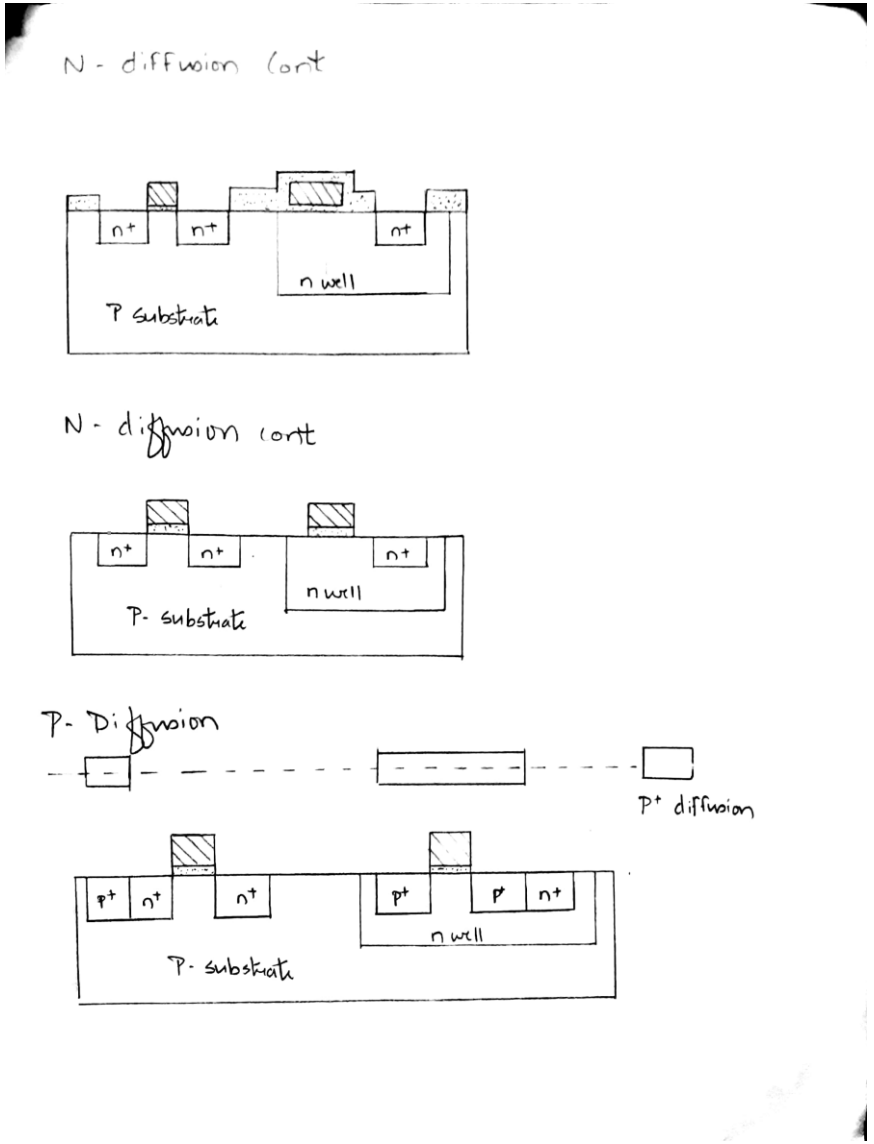
Mask patterning for polysilicon:



Mask Patterning for N+ Diffusion:



N+ Diffusion:

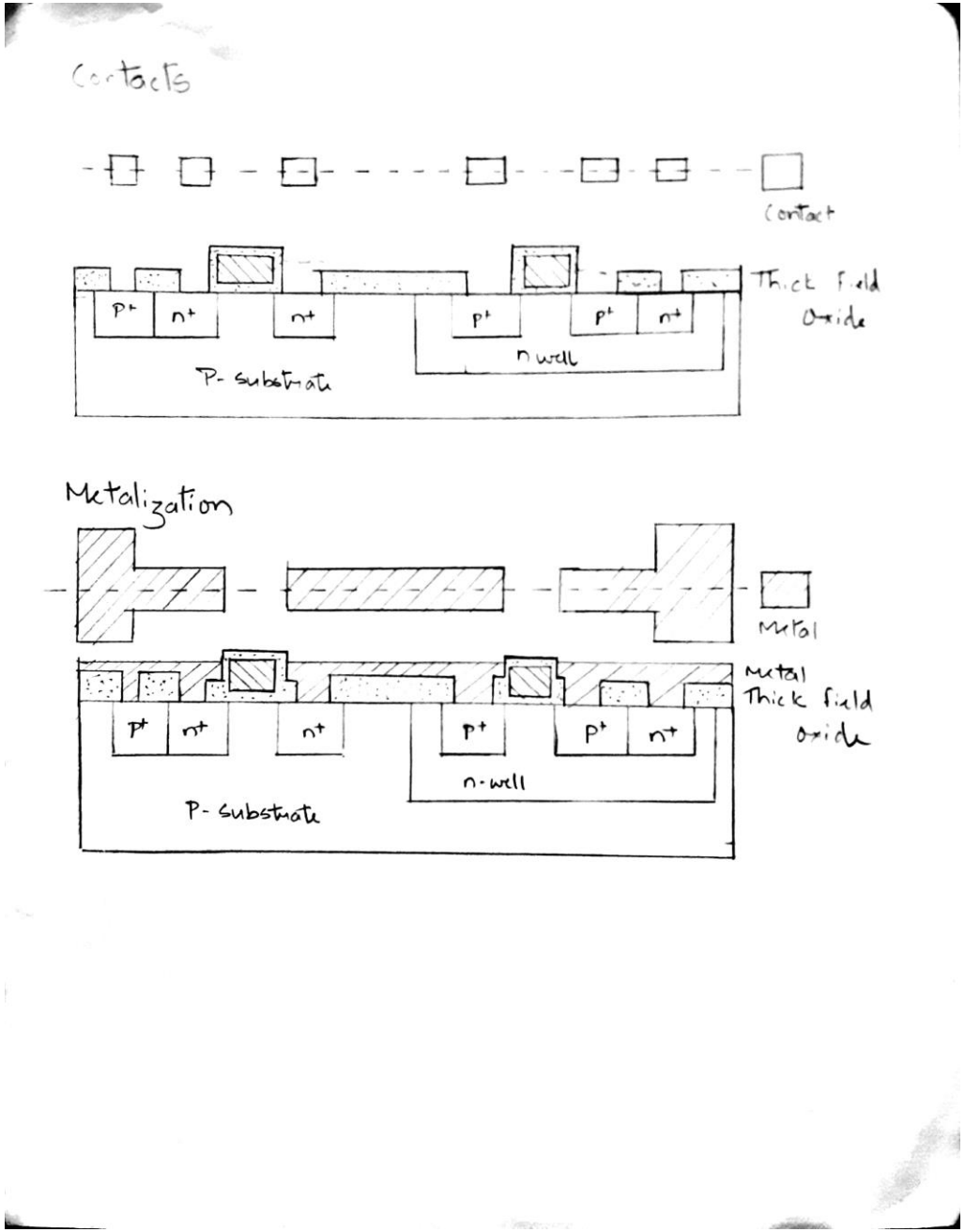


Removal of Oxide layer:

Mask Patterning for P+ Diffusion:

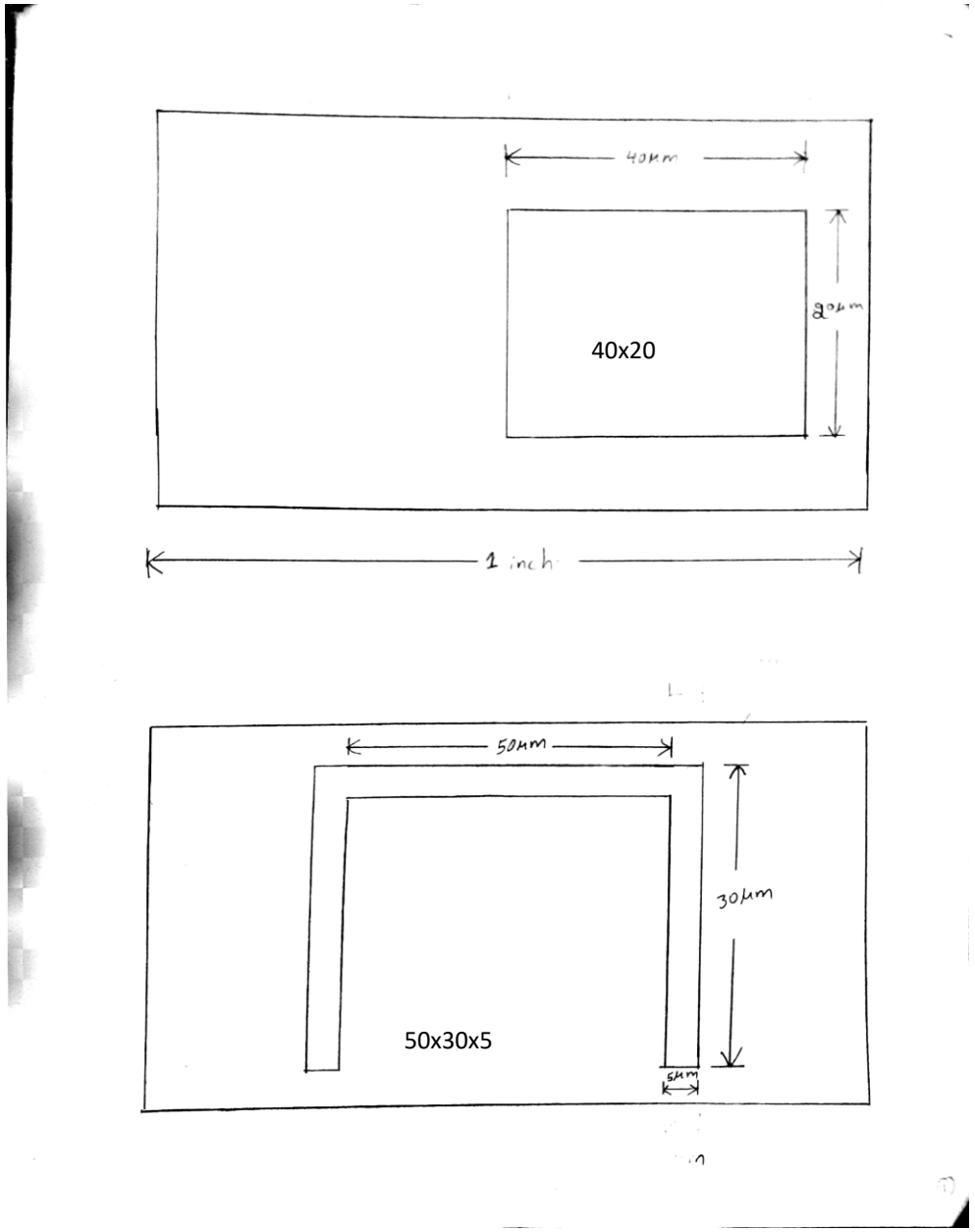
Contact Holes Patterning:

Metallization:



Masks:

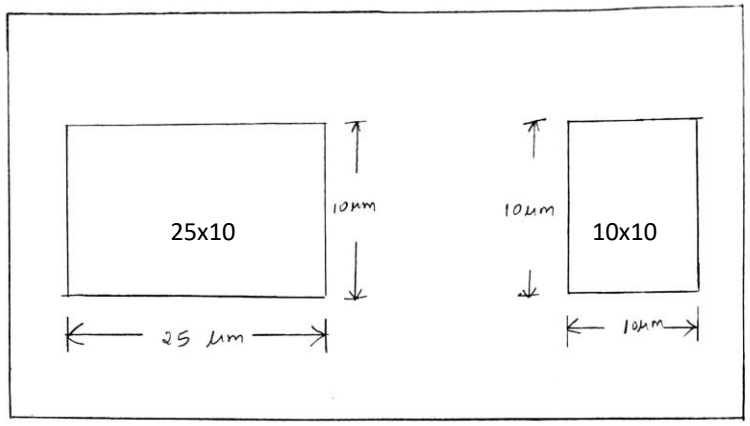
Mask1: N-WELL



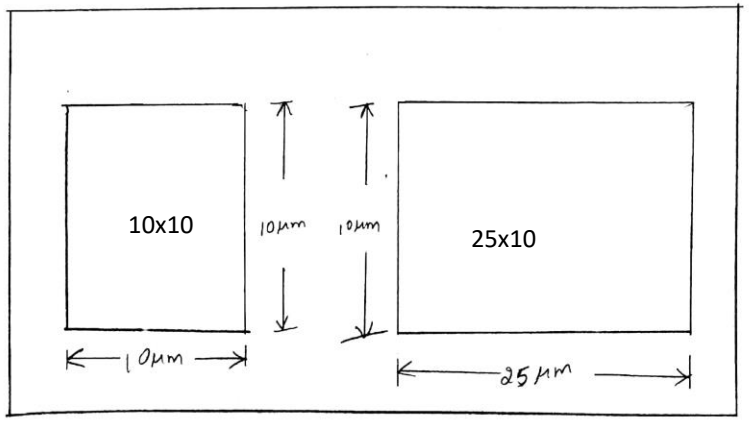
Mask2: Polysilicon

*All the dimensions are in Microns

Mask3 : N+

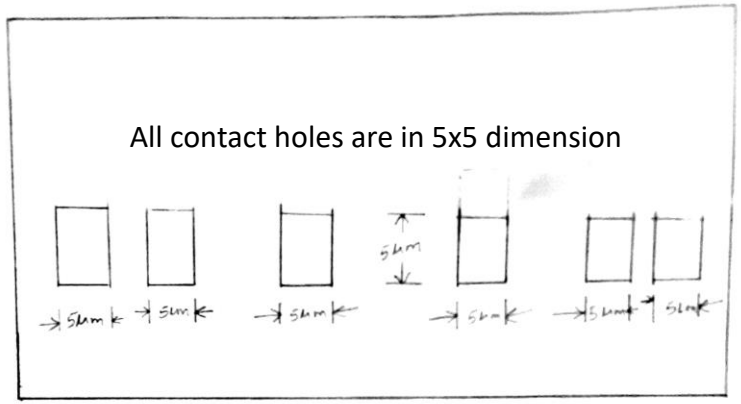


Mask4 : P+

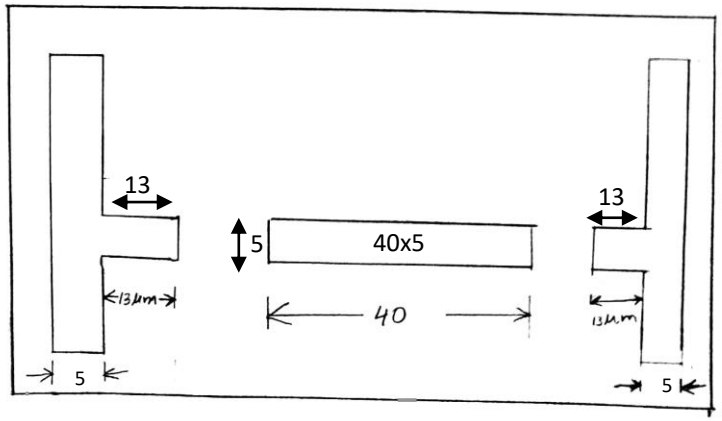


*All the dimensions are in Microns

Mask 5:Contact Holes

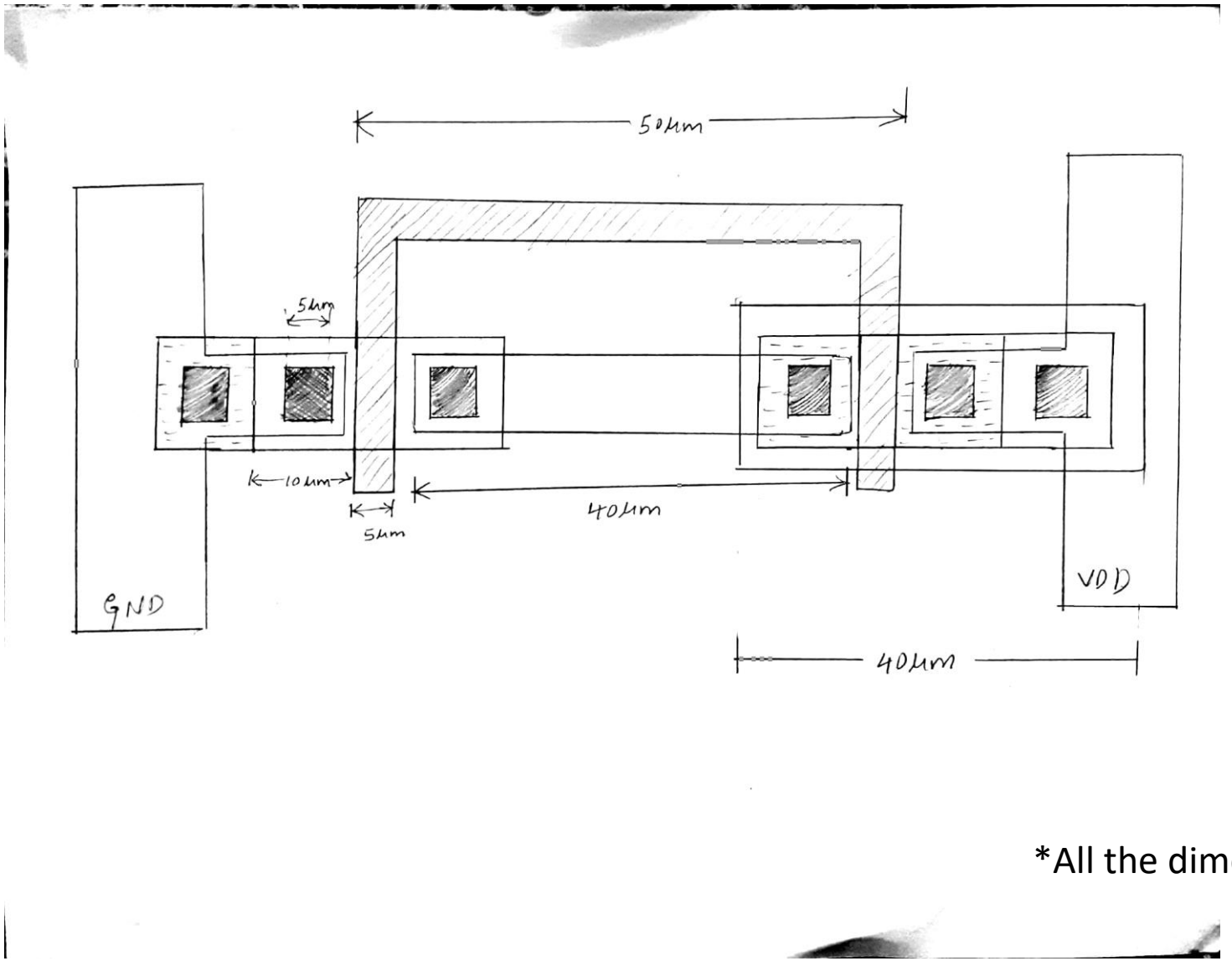


Mask6: Metallization

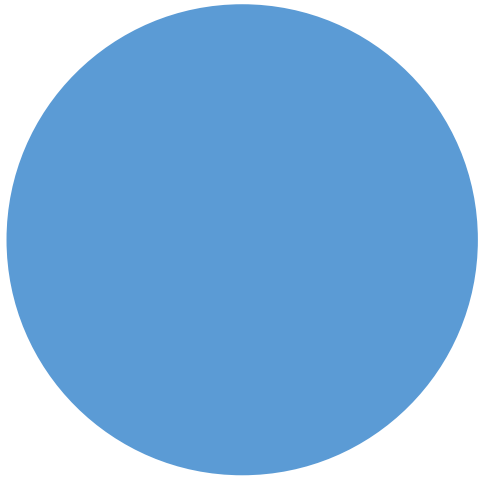
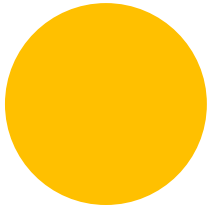


*All the dimensions are in Microns

Total Mask Set:



*All the dimensions are in Microns

-Thank You-