BEEE LAB MANUAL

Department of Electronics and Communication Engineering

Amrita VishwaVidyapeetham, Amaravati Campus

Basic Electrical and Electronics Engineering Laboratory

(Common to B.Tech. CSE-AI)

Department of Electronics and Communication Engineering

Verified by **Approved by**

General lab guidelines and safety instructions during lab session

- Carry out the experiments in such a way that nobody will be injured or hurt.
- Carry out the experiments in such a way that the equipment will not be damaged or destroyed.
- Follow all written and verbal instructions carefully. If you do not understand the instructions, the handouts and the procedures, ask the instructor or teaching assistant.
- Never work alone! You should be accompanied by your laboratory partner and/or the instructors/teaching assistants all the time.
- Perform only those experiments you find in the instructions or authorized by the instructors.
- Unauthorized experiments are prohibited.
- The workplace has to be tidy before, during and after the experiment.
- Read the handout and procedures before starting the experiments.
- Intentional misconduct will lead to exclusion from the lab.
- Never hurry. Haste causes many accidents.
- Always see that power is connected to your equipment through a circuit breaker.
- Connect the power source last. Disconnect the power source first.
- Never make wiring changes on live circuits.
- No food or drinks are allowed in the lab.

Exp. No.	Name of the Experiments	Date	Signature
1	Resistor Color Code		
2	Verification of Kirchhoff's law		
3	Verification of Superposition Theorem		
4	VI characteristics of PN junction		
5	Familiarization of DSO		
6	Clipper		
7	Clampers		
8	Implementation of Half wave and Full wave rectifier using PN junction diode		
9	Transistor as a switch		
10	Implementation of inverting and non-inverting amplifiers using Op-amp		

Experiment 1
Resistor Colour Code

Aim: To verify the given set of resistance values using colour code.

Apparatus:

S.NO	Device	Quantity
1	Resistors	5
2	Capacitors	5
3	Breadboard	1

Theory:

There are two ways to find the resistance value of a resistor. The color bandson the body of the resistor tell how much resistance it has. As shown in the following diagrams figure (1), there are 5-band resistors and 4-band resistors. Formboth 5- and 4-band resistors, the last band indicates tolerance in table (1). Consult with the "Resistor Tolerance" in the table (2) chart to find the tolerance value.

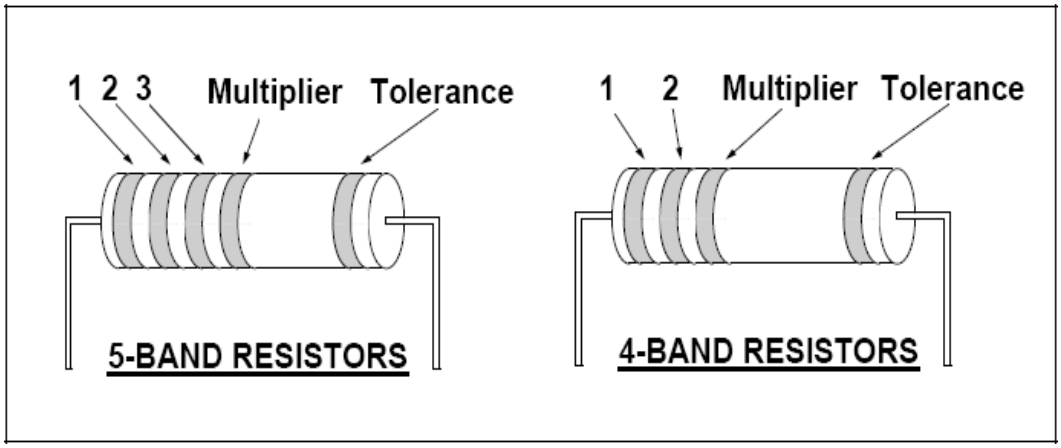


Figure 1: 5- Band and 4- Band resistors

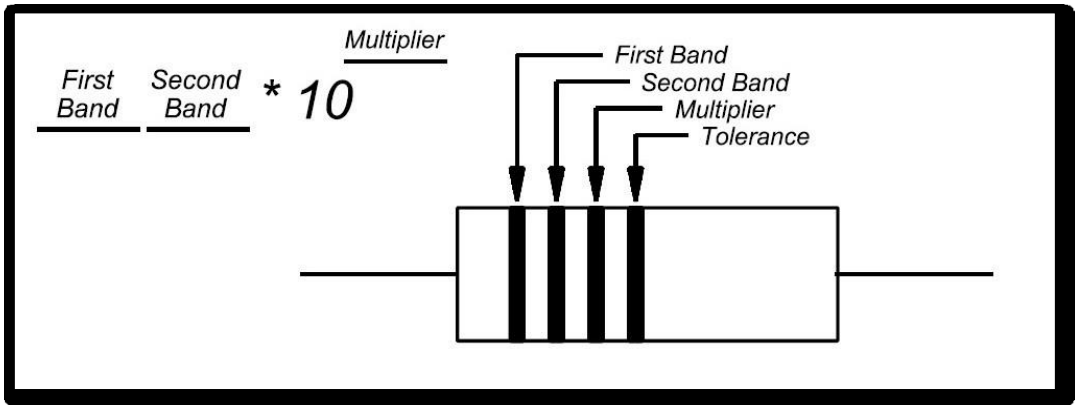


Figure 2: Method to identify the first color on the resistor

COLOR	FIRST BAND	SECOND BAND	MULTIPLIER	TOLERANCE
BLACK		0	$10^0 = 1$	
BROWN	1	1	$10^1 = 10$	
RED	2	2	$10^2 = 100$	
ORANGE	3	3	$10^3 = 1000$	
YELLOW	4	4	$10^4 = 10000$	
GREEN	5	5	$10^5 = 100000$	
BLUE	6	6	$10^6 = 1000000$	
VIOLET	7	7	$10^7 = 10000000$	
GREY	8	8	$10^8 = 100000000$	
WHITE	9	9	$10^9 = 1000000000$	
GOLD			$10^{-1} = 0.1$	5%
SILVER			$10^{-2} = 0.01$	10%
NO COLOR				20%

Table 1: Value of colors on the resisto

Color	Tolerance
Silver	± 10%
Gold	± 5%
Red	± 2%
Brown	± 1%
Green	± 0.5%
Blue	± 0.25%
Violet	± 0.1%
Gray	± 0.05%

Table 2: Value of tolerance band

Procedure:

1. Resistors are cylindrical and have leads extending from each end.
2. Look at the resistor so the group of three or four colour bands are on the left side.
3. Read the band's colour from left to right.
4. The value of the resistor colour code system is recorded.
5. In another way, the central Knob of the digital multi meter is adjusted to get the appropriate measurement value.
6. The value of the resistor shown in the digital multi meter is recorded.

Resistor 1:

Band	Colour	Significant digit
1st band		
2nd band		
Multiplier		
Tolerance		

Theoretical value:

Upper value: **Lower value:**

Practical value:

Resistor 2:

Band	Colour	Significant digit
1st band		
2nd band		
Multiplier		
Tolerance		

Theoretical value:

Upper value: **Lower value:**

Practical value:

Resistor 3:

Band	Colour	Significant digit
1st band		
2nd band		
Multiplier		
Tolerance		

Theoretical value:

Upper value: **Lower value:**

Practical value:

Resistor 4:

Band	Colour	Significant digit
1st band		
2nd band		
Multiplier		
Tolerance		

Theoretical value:

Upper value: **Lower value:**

Practical value:

Resistor 5:

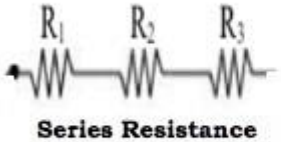
Band	Colour	Significant digit
1st band		
2nd band		
Multiplier		
Tolerance		

Theoretical value:

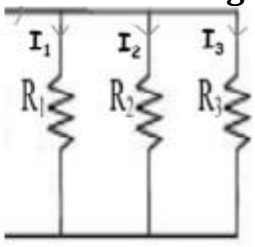
Upper value: **Lower value:**

Practical value:

Resistor Series and Parallel circuit diagram

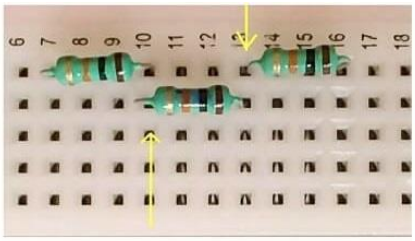


Series Resistance

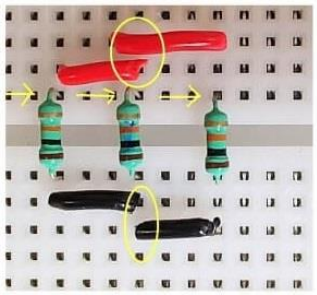


Parallel Resistance

Series and Parallel Resistor Connection



Series



Parallel

-

Formula:

Series $R_{total}=R_1+R_{2+}R_{3.}$

Calculated	Measured

Parallel $R_{total=}R_1*R_2*R_3/R_1+R_2+R_3$

Calculated	measured

–

Result:-

Experiment 2
Verification of Kirchhoff's law

AIM: To verify the Kirchhoff's voltage law and Kirchhoff's current law for the given circuit.

APPARATUS REQUIRED:

S.No	Name of the equipment	Range	Type	Quantity
1	RPS	0-30V	-	1
2	Voltmeter	0-20 V	Digital	1
3	Ammeter	0-20mA	Digital	1
4	Bread board	-	-	1
5	Connecting wires	-	-	Required number.
6	Resistors	4.7k Ω		1 NO
		4.7kΩ		1 NO
		10kΩ		1 NO

Circuit diagrams:

Given circuit:

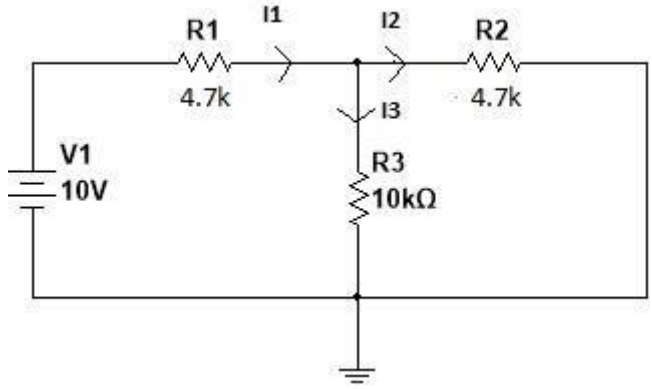


Fig (1)

KVL:

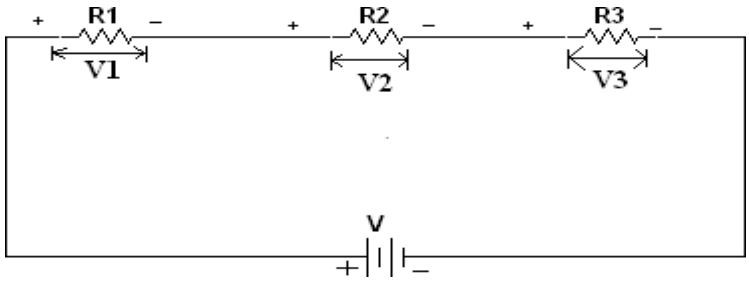


Fig (1)

Practical circuit:

For V_1

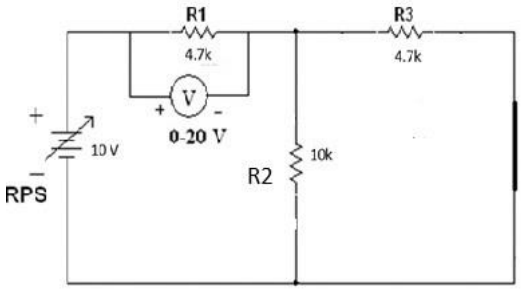


Fig (1a)

For V_2

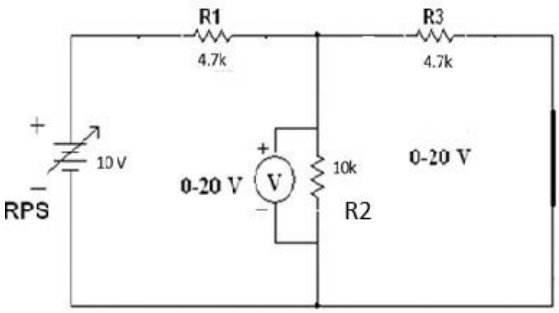


Fig (1b)

For V_3

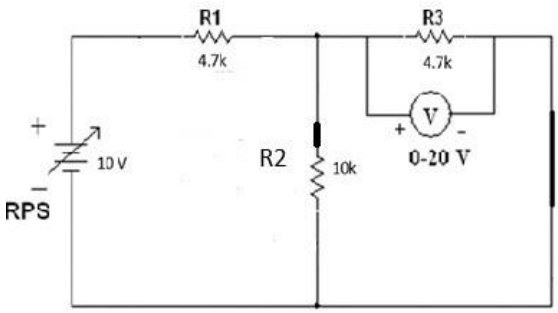


Fig (1c)

KCL:

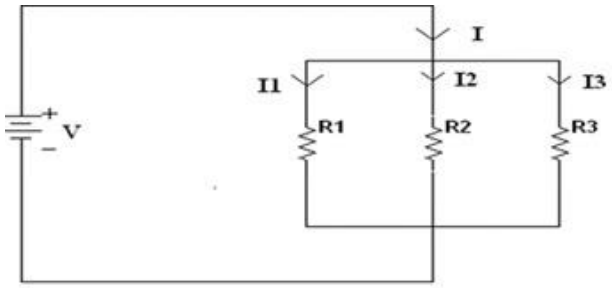


Fig (2)

Practical circuit:

For I_1

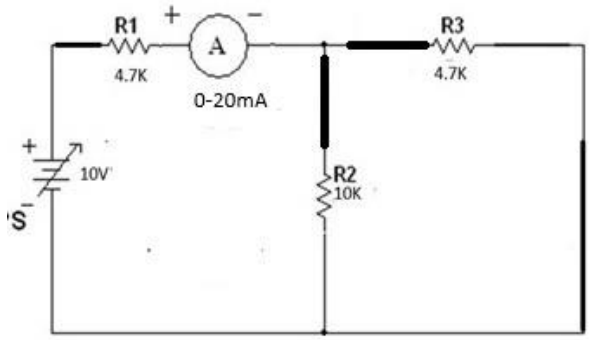


Fig (2a)

For I_2

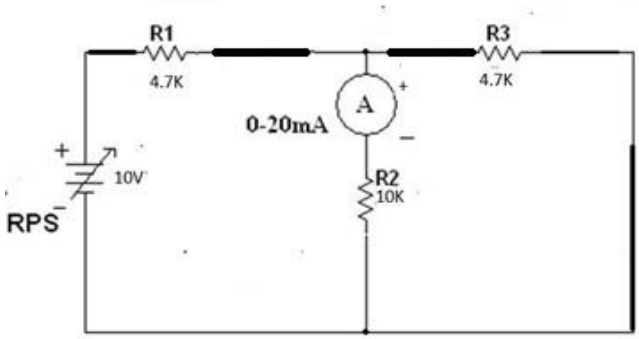


Fig (2b)

For I_3

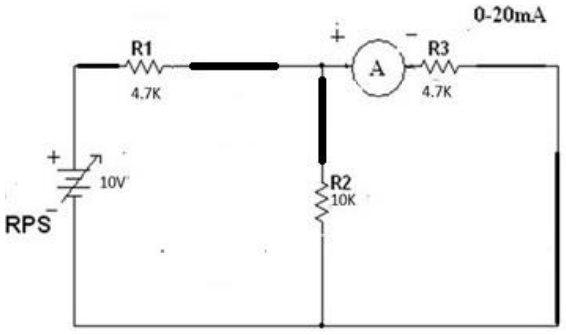


Fig (2c)

Theory:

a) Kirchhoff's Voltage law states that the algebraic sum of the voltage around any closed path in a given circuit is always zero. In any circuit, voltage drops across the resistors always have polarities opposite to the source polarity. When the current passes through the resistor, there is a loss in energy and therefore a voltage drop. In any element, the current flows from a higher potential to lower potential. Consider the fig (1a) shown above in which there are 3 resistors are in series. According to kickoff's voltage law….

$$\mathbf{V = V_1 + V_2 + V_3}$$

b) Kirchhoff's current law states that the sum of the currents entering a node equal to the sum of the currents leaving the same node. Consider the fig (1b) shown above in which there are 3 parallel paths. According to Kirchhoff's current law...

$$\mathbf{I = I_1 + I_2 + I_3}$$

Procedure:

1. Kirchhoff's Voltage law:
    1. Connect the circuit as shown in fig (2a).
    2. Measure the voltages across the resistors.
    3. Observe that the algebraic sum of voltages in a closed loop is zero.
2. Kirchhoff's current law:
    1. Connect the circuit as shown in fig (2b).
    2. Measure the currents through the resistors.
    3. Observe that the algebraic sum of the currents at a node is zero.

Observations:

KVL:

S.NO	Voltage Across Resistor	Theoretical	Practical

KCL:

S.NO	Current Through Resistor	Theoretical	Practical

PRECAUTIONS:

1. Avoid loose connections.
2. Keep all the knobs in minimum position while switch on and off of the supply.

RESULT:

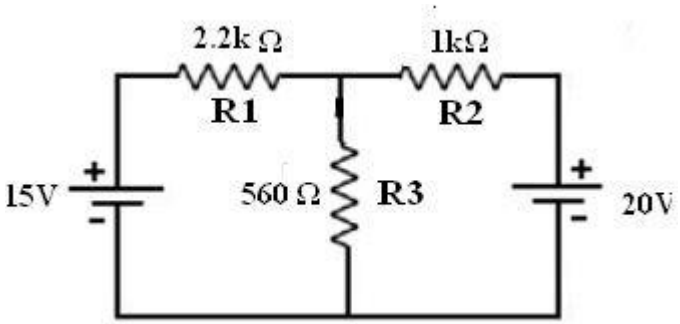
Experiment 3
Verification of Superposition Theorem

AIM: To verify the superposition theorem for the given circuit.

Apparatus Required:

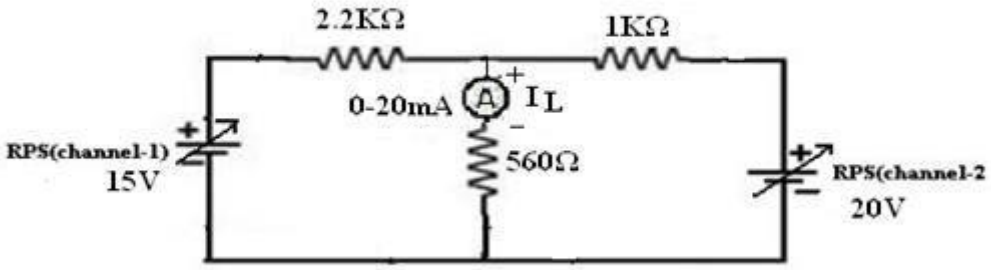
S.No	Name Of The Equipment	Range	Type	Quantity
1	Bread board	-	-	1 NO
2	Ammeter	(0-20)mA	Digital	1 NO
3	RPS	0-30V	Digital	1 NO
4	Resistors	2.2k Ω		1 NO
		1k Ω		1 NO
		560 Ω		1 NO
5	Connecting Wires	-	-	As required

CIRCUIT DIAGRAM:



Practical Circuits:

When V_1 & V_2 source acting (To find I_L):-



Fig(1)

When V_1 Source Acting (To Find I_L^I)

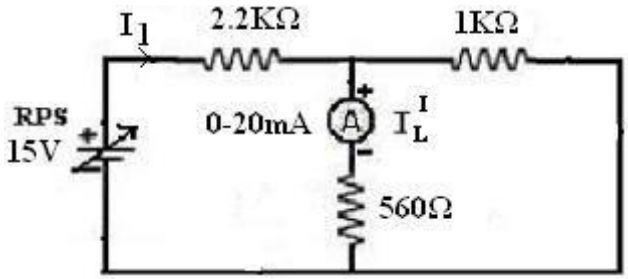


Fig (2)

WhenV_2 source acting (To find I_L^{II}):

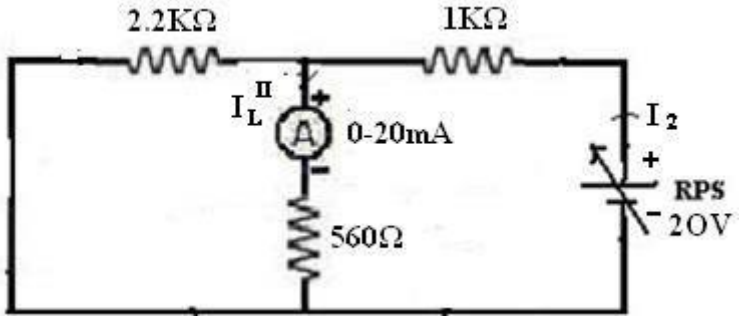


Fig (3)

Theory:

SUPERPOSITION THEOREM:

Superposition theorem states that in a lumped,inear, bilateral network consisting more number of sources each branch current(voltage) is the algebraic sum all currents (branch voltages), each of which is determined by considering one source at a time and removing all other sources. In removing the sources, voltage and current sources are replaced by internalresistances.

PROCEDURE:

1. Connect the circuit as per the fig (1).
2. Adjust the output voltage of sources X and Y to appropriate values (Say 15V and20Vrespectively).
3. Note down the current (I_L) through the 560 0hm resistor by using the ammeter.
4. Connect the circuit as per fig (2) and set the source Y (20V) to 0V.
5. Note down the current ($I_L^{I)}$ through 560ohm resistor by using ammeter.
6. Connect the circuit as per fig(3) and set the source X (15V) to 0V and source Y to 20V.
7. Note down the current (I_L^{II}) through the 560 ohm resistor branch by using ammeter.
8. Reduce the output voltage of the sources X and Y to 0V and switch off the supply.
9. Disconnect the circuit.

THEORITICAL CALCULATIONS

From Fig(2)

$$I_1 = V_1/(R_1+(R_2//R_3))$$

$$I_L^{I} = I_1^{*}R_2/(R_2+R_3)$$

From Fig(3)

$$I_2 = V_2/(R_2+(R_1//R_3))$$

$$I_L^{II} = I_2^{*}R_1/(R_1+R_3)$$

$$I_L = I_L^{I} + I_L^{II}$$

TABULAR COLUMNS:

From Fig(1)

S. No	Applied voltage (V_1) Volt	Applied voltage (V_2) Volt	Current I_L (mA)

From Fig(2)

S. No	Applied voltage (V_1) Volt	Current I_L^{I} (mA)

From Fig(3)

S. No	Applied voltage (V_2) Volt	Current I_L^{II} (mA)

S.No	Load current	Theoretical Values	Practical Values
1	When Both sources are acting, I_L		
2	When only source X is acting, I_L^{I}		
3	When only source Y is acting, I_L^{II}		

PRECAUTIONS:

1. Initially keep the RPS output voltage knob in zero volt position.
2. Set the ammeter pointer at zero position.
3. Take the readings without parallax error.
4. Avoid loose connections.
5. Avoid short circuit of RPS output terminals.

RESULT:

Experiment 4

V-I Characteristics of P-N Junction Diode

Aim:

1. To plot Volt-Ampere Characteristics of Silicon P-N Junction Diode and Zener diode.
2. To find cut-in Voltage for Silicon P-N Junction diode and to find Zener break-down voltage inreverse biased condition.

Apparatus:

S.NO	Device	Specification	Quantity
1.	P-N Diode Zener Diode	IN4007	1
2	Resistors	470Ω,1K	1
4	Bread Board		1
5	Connecting wires as required		
6	Digital Ammeter Digital Voltmeter		1 1
7	Regulated Power Supply	(0-30v)	1

Theory:

Donor impurities (pentavalent) are introduced into one-side and acceptor impurities into the other side of a single crystal of an intrinsic semiconductor to form a p-n diode with a Junction called depletion region (this region is depleted off the charge carriers). This Region gives rise to a potential barrier called ***Cut- in Voltage***. This is the voltage across the diode at which it starts conducting. It can conduct beyond this Potential.

The P-N junction supports unidirectional current flow. If the +ve terminal of the input supply is connected to anode (P-side) and –ve terminal of the input supply is connected to cathode (N-side) then diode is said to be forward biased. In this condition the height of the potential barrierat the junction is lowered by an amount equal to given forward biasing voltage. Both the holesfrom p-side and electrons from n-side cross the junction simultaneously and constitute a forwardcurrent (***injected minority current*** – due to holes crossing the junction and entering N-side of the diode, due to electrons crossing the junction and entering P-side of the diode). Assuming current flowing through the diode to be very large, the diode can be approximated as short- circuited switch. If –ve terminal of the input supply is connected to anode (p-side) and +ve terminal of the input supply is connected to cathode (n-side) then the diode is said to be reverse biased. In this condition an amount equal to reverse biasing voltage increases the height of the potential barrierat the junction. Both the holes on p-side and electrons on n-side tend to move away from the junction thereby increasing the depleted region. However, the process cannot continue indefinitely, thus a small current called ***reverse saturation current*** continues to flow in the diode. This small current is due to thermally generated carriers. Assuming current flowing through thediode to be negligible, the diode can be approximated as an open circuited switch.

The volt-ampere characteristics of a diode explained by following equation:

$$\mathbf{I = I_0 (e^{V/(\eta V_T)} - 1)}$$ **where**

I = current flowing in the diode I_0 = reverse saturationcurrent, V = voltage applied to the diode

V_T = volt-equivalent of temperature = kT/q = T/11,600 = 26mV (@ room temp).

η = 1 (for Ge) and 2 (for Si)

It is observed that Ge diode has smaller cut-in-voltage when compared to Si diode. The reversesaturation current in Ge diode is larger in magnitude when compared to silicon diode.

Procedure:

Forward Biased Condition:

1. Connect the circuit as shown in figure (1) using silicon PN Junction diode.
2. Vary V_f gradually in steps of 0.1 volts up to 5volts and note down the correspondingreadings of I_f.
3. Step Size is not fixed because of non-linear curve and vary the X-axis variable (i.e. ifoutput variation is more, decrease input step size and vice versa).
4. Tabulate different forward currents obtained for different forward voltages.

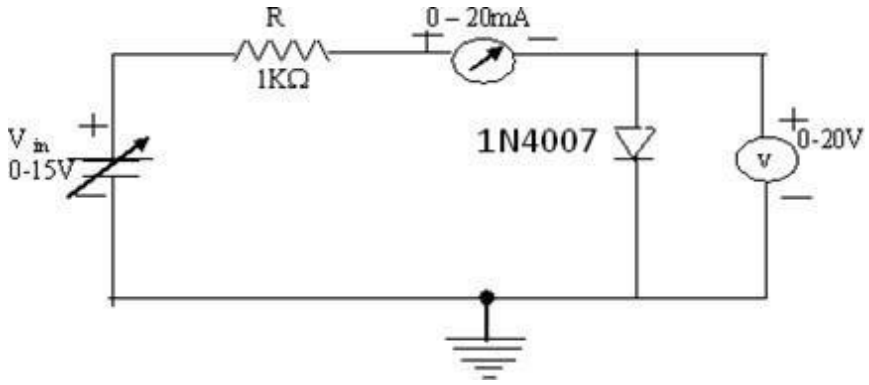


Fig-1 forward bias of the pn junction diode

Observations

Si diode in forward biased conditions

Sl.No	RPS Voltage(v)	Forward Voltage acrossthe diode V_f (volts)	Forward current through the diode I_f (mA)
1	0.1		
2	0.2		
3	0.3		
4	0.4		
5	0.5		
6	0.6		
7	0.7		
8	0.8		
9	0.9		
10	1		
11	2		
12	3		
13	4		
14	5		
15	6		
16	7		
17	8		
18	9		
19	10		

Model Graph:

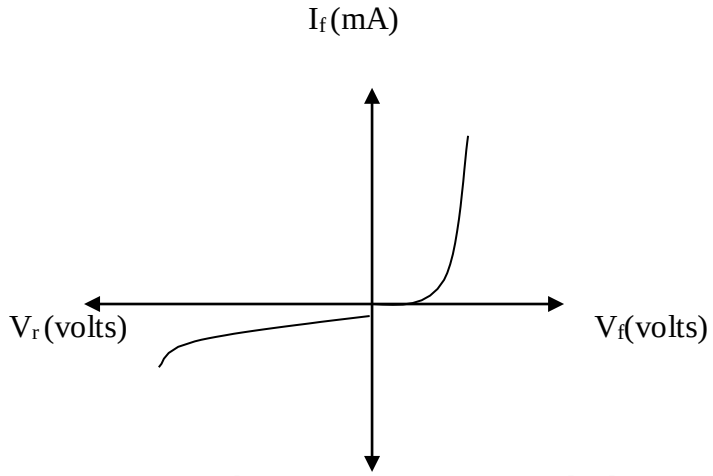


Fig-2(V-I Characteristics pn junction diode**)**

Precautions:

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

Reverse Biased Condition:

1. Connect the circuit as shown in figure (3) using silicon PN Junction diode.
2. Vary V_R gradually in steps of 1 volt up to 10 volts and note down the corresponding readings of I_R.
3. Step Size is not fixed because of non-linear curve and vary the X-axis variable (i.e. if output variation is more, decrease input step size and vice versa).
4. Tabulate different Reverse currents obtained for different Reverse voltages.

Circuit Diagram:

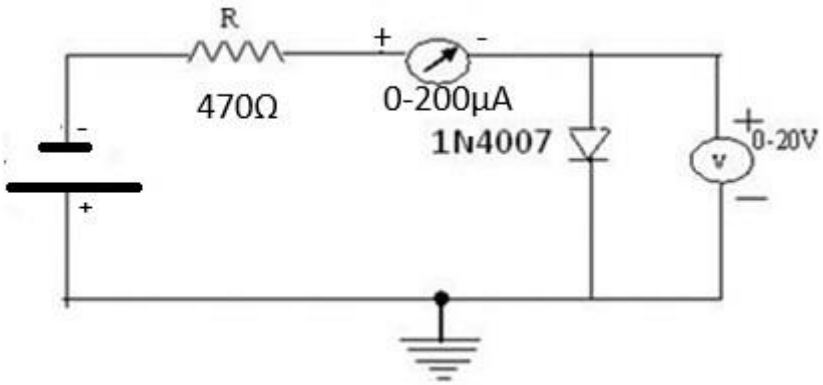


Fig 3 -Reverse Bias of PN junction diode

Procedure:

Reverse biased condition:

1. Connect the circuit as shown in Fig (2).
2. Vary V_{zr} gradually and note down the corresponding readings of $I_{zr.}$
3. Tabulate different reverse currents obtained for different reverse voltages.

Observations:

Zener diode in reverse biased conditions:

Sl.No	RPS Voltage(v)	Reverse Voltage across the diode V (volts)	Reverse current through the diode I(mA)
1	1		
2	2		
3	3		
4	4		
5	5		
6	6		
7	7		
8	8		
9	9		
10	10		

Model Graph:

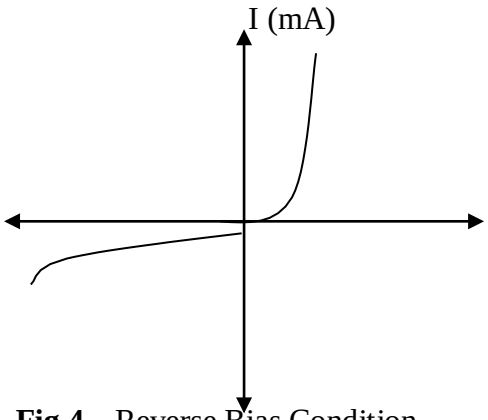


Fig 4 – Reverse Bias Condition

Precautions:

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

Inference:

- In the reverse biased mode, zener diode has large breakdown voltage and though the current increases, the voltage remains constant. Thus, it acts as a voltage regulator.

Result:

a. PN diode Cut in voltage = … V

b. PN diode Cut off voltage = … V

Graph Sheet:

EXPERIMENT 5
Familiarization of DSO

Aim: To familiarize Equipment voltmeter milli and micro ammeter DC supply and DSO.

Apparatus

SLNO	Equipment	Specification	Qty
1	DSO	50MHZ	1
6	Probes		1
7	Connecting wires		

DSO:-

1) Generate a sine wave with 1KHz Frequency and $5v_{p-p}$ and measure it using cursors, measurement option, manually.
2) Generate a square wave with 5KHz Frequency and $5v_{p-p}$ and measure it using cursors, measurement option, manually.
3) Generate a triangle wave with 1KHz Frequency and $5v_{p-p}$ and measure it using cursors, measurement option, manually.
4) Generate a trigger using trigger option measurement option, manually.

Waveform	Cursor value	Measurement option value	Manual value
Sine	$V_{PP=}$ **Freq=**	$V_{PP=}$ **Freq=**	$V_{PP=}$ **Freq=**
Square	$V_{PP=}$ **Freq=**	$V_{PP=}$ **Freq=**	$V_{PP=}$ **Freq=**
Triangle	$V_{PP=}$ **Freq=**	$V_{PP=}$ **Freq=**	$V_{PP=}$ **Freq=**
Trigger	$V_{PP=}$ **Freq=**	$V_{PP=}$ **Freq=**	$V_{PP=}$ **Freq=**

Result:

Experiment 6

CLIPPERS

AIM: - To study the various clippers using diodes.

APPARATUS:

S.NO	Device	Specification	Quantity
1.	P-N Diode Zener Diode	IN4007	2
2	Resistors	5.6KΩ	1
4	Bread Board		1
5	DSO	(0-20) MHz	1
6	Probes		3
7	Regulated Power Supply	(0-30v)	1
8	Connecting wires as required		

Theory: Clipping circuits consists of both linear elements like resistors and also non-linear elements like diodes or transistors, but does not contain energy-storage elements like capacitors. Clipping circuits are used to select, that part of waveform for the purpose of transmission which lies above or below the reference level. Thus a clipper circuit can remove certain portions and thus a change in the wave shape of the signal can be obtained.

Clippers are broadly classified into two types as (i) Shunt Clippers (ii) Series Clippers. In Shunt Clippers, the diode forms a parallel path across the output and in series Clippers the diode forms a series path connecting the input and output.

The Shunt Clippers are again classified asPositive Peak Clipping without reference voltage.

(i) Negative Peak Clipping without reference voltage.

(ii) Positive Peak Clipping above reference level.

(iii) Negative Peak Clipping below reference level.

(iv) Positive base clipping (clipping below reference level).

(v) Negative base clipping (clipping above reference level).

For diode clippers, the approximations of a diode are considered.

(a) When $V_i < V_R+V_\gamma$, diode is reverse biased (OFF). The output will follow the input voltage.

(b) When $V_i > V_R+V_\gamma$, diode is forward biased and the output is equal to (V_R+V_γ)

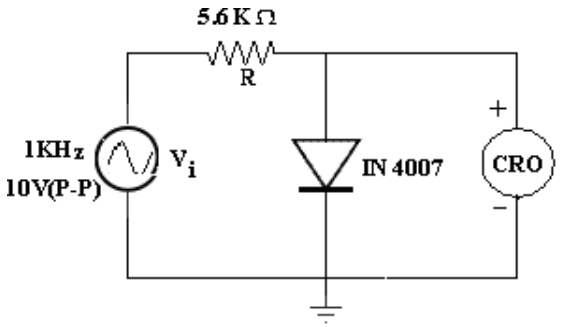
Where V_R is Reference voltage

V_γ is cut in voltage of the diode

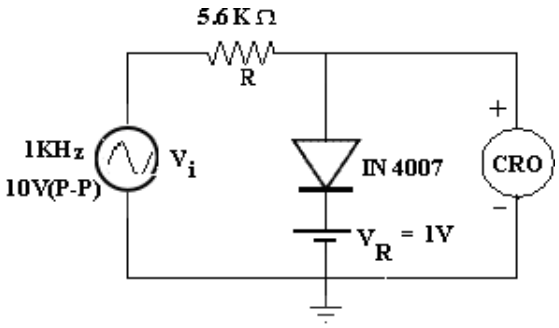
Thus for shunt clippers, when the diode is ON, output voltage level is constant and when the diode is OFF, output follows the input. Shunt clippers may be used to clip low input voltages. Double diode clippers are also called as two level clippers which are used to clip at two different levels of the input signal.

CIRCUIT DIAGRAM:

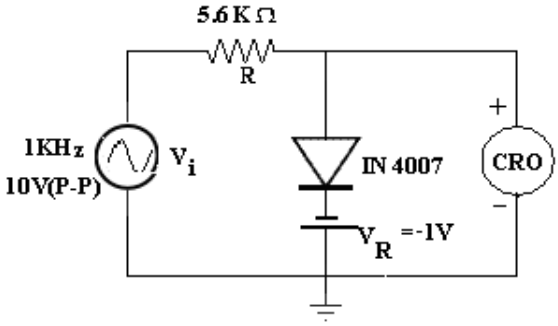
Positive clipping:



With out reference:



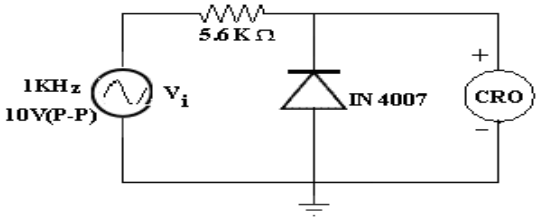
With Positive reference:



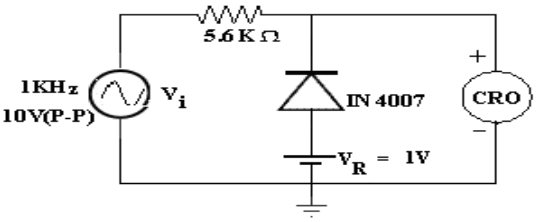
With Negative reference:

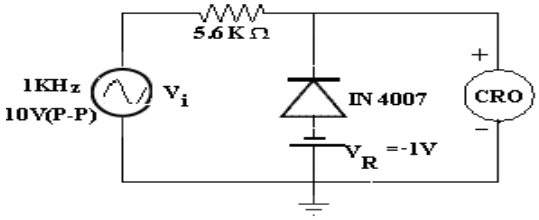
Negative clipping:

With out reference:

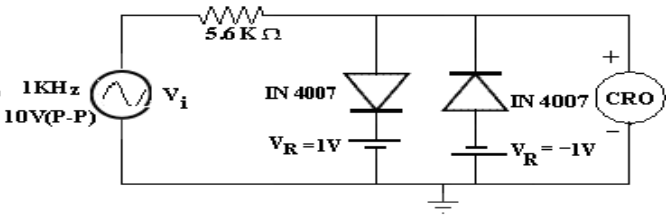


With Positive reference:





With Negative reference:



Siicer:

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Connect the function generator at the input of the circuit.
3. Apply the sine wave with a desired magnitude.
4. Observe the output wave forms and note down the readings.
5. Repeat steps 1 to 4.

OBSERVATIONS

POSITIVE CLIPPERS

S.NO	CASE	THEORITICAL VALUE	PRACTICAL VALUE
1			
2			
3			-

NEGATIVE CLIPPERS

S.NO	CASE	THEORITICAL VALUE	PRACTICAL VALUE
1			
2			
3			

Result:-

Graph sheet:

Experiment 7
clampers

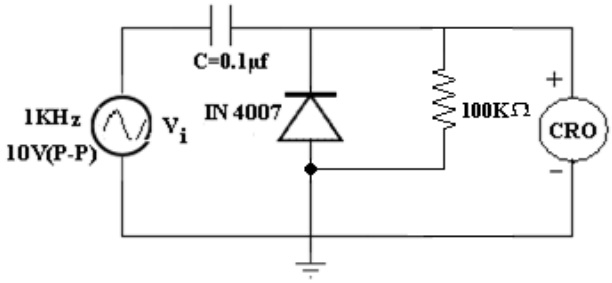
AIM: - To study the various clampers using diodes.

APPARATUS:-

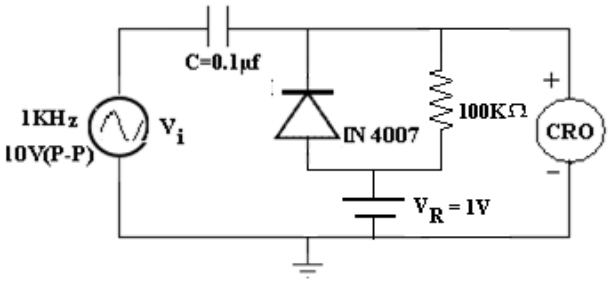
S.NO	Device	Specification	Quantity
1.	P-N Diode Zener Diode	IN4007	1
2	Resistors	100KΩ	1
3	Capacitors	0.1µf	1
4	Bread Board		1
5	DSO	(0-20) MHz	1
6	Probes		3
7	Regulated Power Supply	(0-30v)	1
8	Connecting wires as required		

CIRCUIT DIAGRAM:

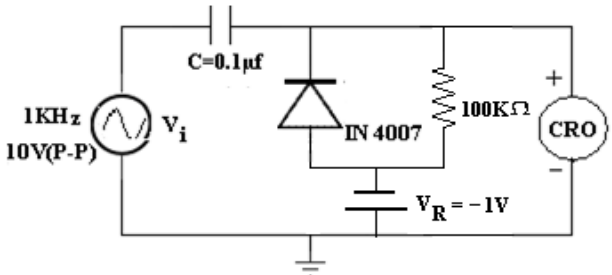
Positive clamping



Positive clamping without reference:

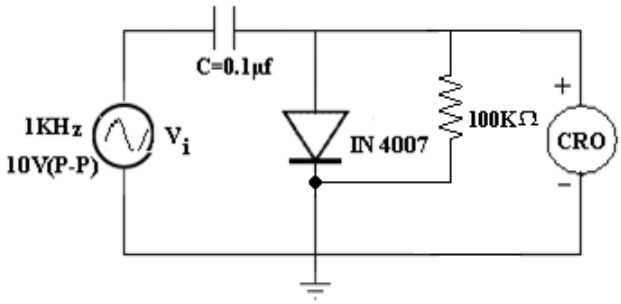


Positive clamping withPositive reference:

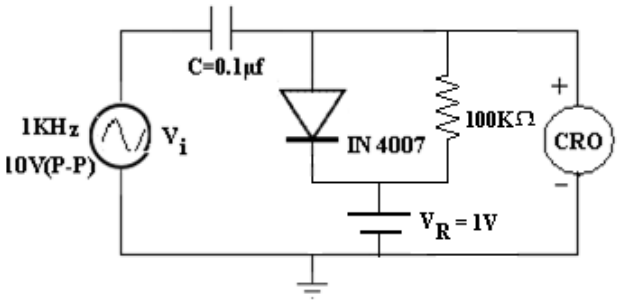


Positive clamping with Negative reference:

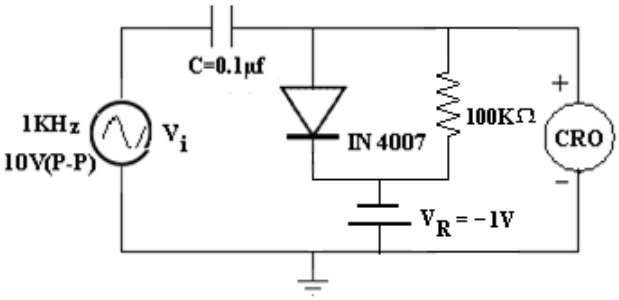
NEGATIVECLAMPING



Negative clamping without reference:



Negative clamping withPositive reference:



Negative clamping with Negative reference:

PROCEDURE:

1. Connect the circuit as per the first circuit diagram with both the channels of CRO showing the input and output.
2. Apply the input wave of $10V_{(p-p)}$ with frequency 1 KHz to the circuit.
3. Adjust the both channels of CRO to ground position and then in DC position.
4. Draw the input and output wave forms and indicate the clamping level.
5. Repeat steps 1,2,3,4 for reaming clamping circuits

OBSERVATIONS:

POSSITIVE CLAMPERS

S.NO	CASE	THEORITICAL VALUE	PRACTICAL VALUE
1	WITHOUT REFERENCE		
2	WITH +Ve REFERENCE		
3	WITH -Ve REFERENCE		

NEGATIVE CLAMPERS

S.NO	CASE	THEORITICAL VALUE	PRACTICAL VALUE
1	WITHOUT REFERENCE		
2	WITH +Ve REFERENCE		
3	WITH -Ve REFERENCE		

Precautions:

1. Check the connections before giving the supply.

Result:

Graph sheet:

Experiment 8
Half Wave Rectifier and Full Wave Rectifier

Aim: To examine the input and output waveforms of a half wave rectifier and full waverectifier without filter.

Apparatus:

S.NO	Device	Specification	Quantity
1	Step down Transformer Silicon Diodes	(6-0-6)/(9-0-9) V 1N 4007	1 2
2	Digital storage oscilloscope	(0-20) MHz	1
3	Resistors	1K	1
4	Connecting wires		

Theory:

Half Wave Rectifier:

During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage.
During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e., the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the halfwave rectified o/p voltage is the value measured on dc voltmeter.
For practical circuits, transformer coupling is usually provided for two reasons.

1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus, preventing shock hazards in the secondary circuit.

Full Wave Rectifier:

The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2is reverse biased. The diode D1 conducts and current flows through load resistor RL. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor RL in the same direction. There is a continuous current flow through the load resistor RL, during both the half cycles and will getunidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one-way) currentto the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one-half cycle (180 degree).

Procedure:

Half Wave Rectifier without filter

1. Connect the circuit as shown in Figure (a).
2. Keep the load resistance, R_L to 1K and note down the readings of input and output voltages through oscilloscope.
3. Readings are tabulated as per the tabular column.

Full-wave Rectifier without filter

1. Connect the circuit as shown in the Figure (b).
2. Keep the load resistance R_L to 1K and note the readings of input and output voltages through Oscilloscope.
3. Readings are tabulated as per the tabular column

Circuit diagram & Model graph:

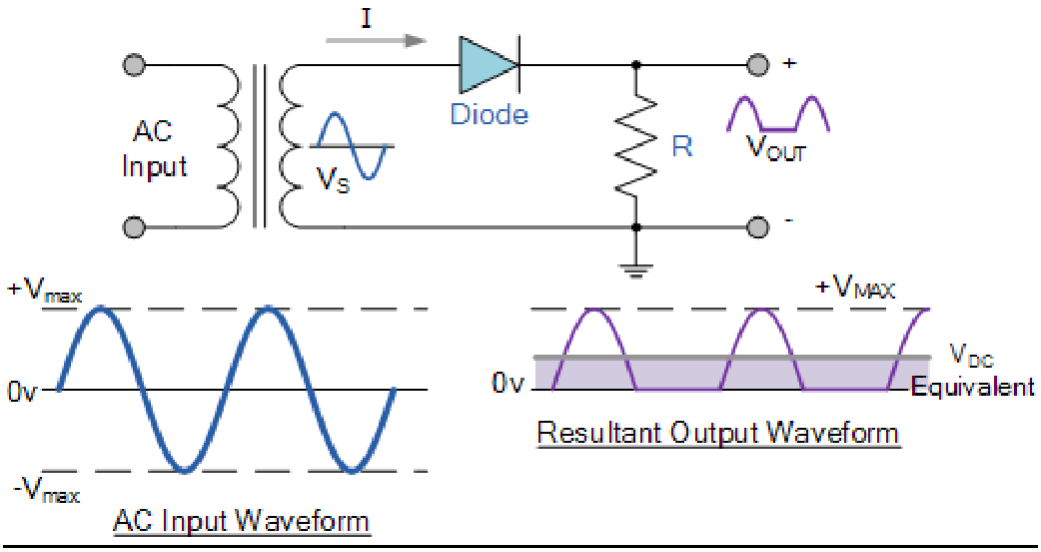


Fig (1): Half Wave Rectifier without Filter

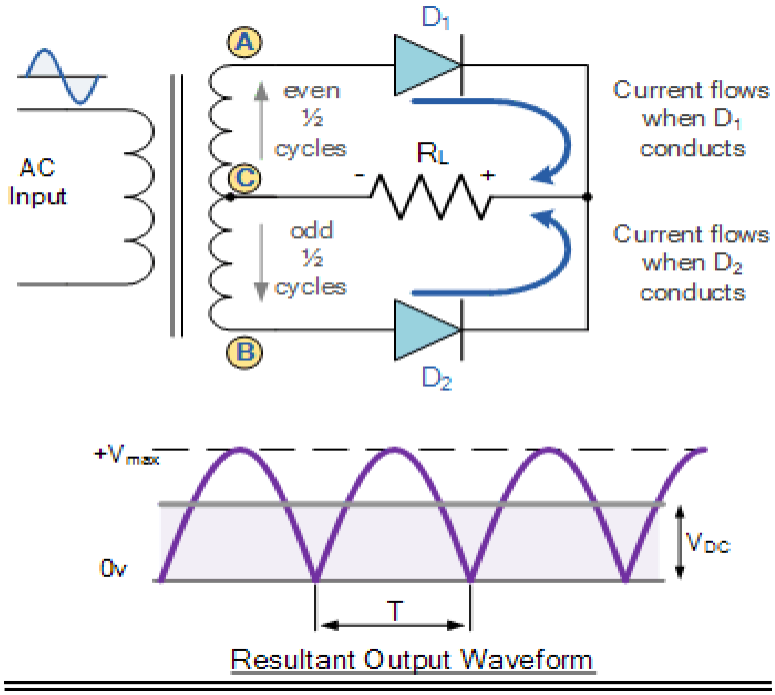


Fig (2): Full Wave Rectifier without Filter

Observation:

Half Wave Rectifier without Filter

S.NO	Load Resistance (R_L)	Input Voltage Peak (V_{in})	Output Voltage Peak (V_o)
1	1KΩ		

Full wave Rectifier (Center-tap) Without Filter

S.NO	Load Resistance (R_L)	Input Voltage Peak (V_{in})	Output Voltage Peak (V_o)
1	1KΩ		

Precautions:

No loose contacts at the junctions.

Equipment of correct ranges must be used for precision.

Result:

Graph Sheet:

Experiment 9

TRANSISTOR AS A SWITCH

AIM: To check the operation of Transistor as a switch.

APPARATUS:

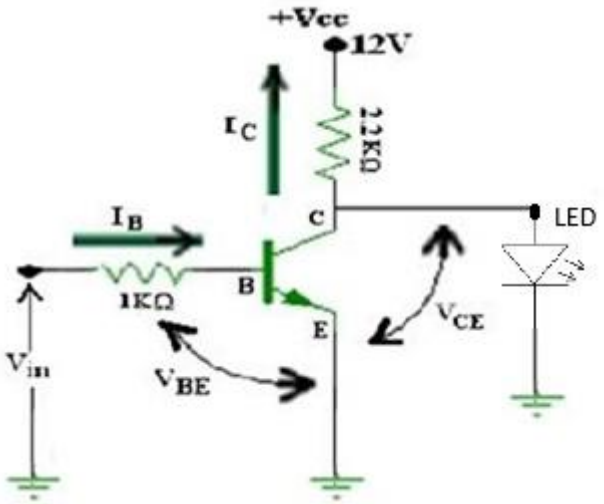
S.NO	Device	Specification	Quantity
1	Transistor	BC107	1
2	Resistors	2.2K,1 K	1
4	Bread Board		1
5	LED		
6	Connecting wires as required		
7	DSO & Probes		1
8	Regulated Power Supply		1

Theory:

The transistor acts as a switch to connect and to disconnect the load R_L from the source V_{CC}. It acts as an open switch when both the junctions are reverse biased and acts as a closed switch when both the junctions are forward-biased. Thus it operates between Cut-off and saturation region to function as a switching element. In Cut-off region, a small reverse, saturation current flows across the junction. The region to the left of the ordinate $V_{CB} = 0$ and above $I_E = 0$ in CB configuration is the saturation region. In this region, the voltage across the junction is small.

In Common-Emitter configuration, the input switching signal current or voltage is small in comparison with the switched output current or voltage. Hence the Common-Emitter configuration is mostly used for switching configuration.

CIRCUIT DIAGRAMS:



PROCEDURE:

DC ANALYSIS:

1. Connect the circuit as per the circuit diagram.

2. The Vcc of (+12V) and the input voltage of zero volts from the R>P>S is given as input to the circuit.

3. Note down VBE and VCE using VOLT METER.

4. Change the input voltage to 5V and note down VBE and VCE.

AC ANALYSIS:

1. Connect the circuit as per the circuit diagram.

2. Keeping Vcc at +12V and give square wave of 5V(p-p) with 1kHz frequency from function generator as input to the circuit.

3.Observe the wave form on CRO for VBE & VCE and note down the readings.

Tabular coloum:-

DC ANALYSIS

S.NO	Vi(V)	V_{CC}(V)	V_{BE}(V)	V_{CE}(V)	Transistor position
1	0	12	0	12	
2	5	12	0.5	0	

AC ANALYSIS

S.NO	Vi(V)	V_{CC}(V)	V_{BE}(V)	V_{CE}(V)	Transistor position
1	+2.5	12	0.5	0	
2	-2.5	12	-2.5	12	

RESULT

Experiment 10

Inverting and Non-Inverting Operational Amplifiers

Aim:

To study the following linear applications of op-amp:

1. Inverting amplifier.
2. Non – inverting amplifier.

Apparatus:

S.NO	Device	Specification	Quantity.
1	Op-amp	IC741	1
2	Resistors	1K,10K	1
4	Bread Board		1
5	Connecting wires as required		
6	DSO& Probes Function Generator Multi meter		1 1 1
7.	Dual Power Supply	0-30V	1

Theory:

Inverting Amplifier:

This is the most widely used of all the Op-amp circuits. The output Vout is fed back to the inverting input through the Rf – Ri network as shown in figure where Rf is the feedback resistor. The input signal Vin is applied to the inverting input terminal through Ri and noninverting input terminal of Op-amp is grounded. The output V0 is given by

Vout = Vin *(- Rf / Ri) where, the gain of amplifier is (-Rf / Ri).

The negative sign indicates a phase-shift of 180 degrees between Vin and Vout. The effective input impedance is Ri. An inverting amplifier uses negative feedback to invert and amplify a voltage. The Ri, Rf resistor network allows some of the output signal to be returned to the input. Since the output is 180° out of phase, this amount is effectively subtracted from the input, thereby reducing the input into the operational amplifier. This reduces the overall gain of the amplifier and is dubbed negative feedback.

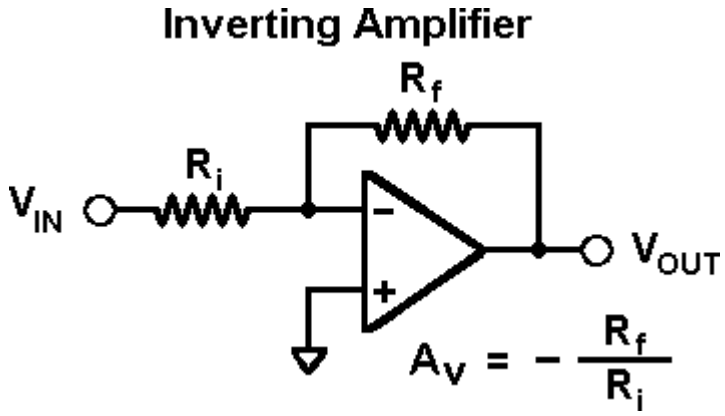


Fig 1. Inverting Configuration

Model graph:

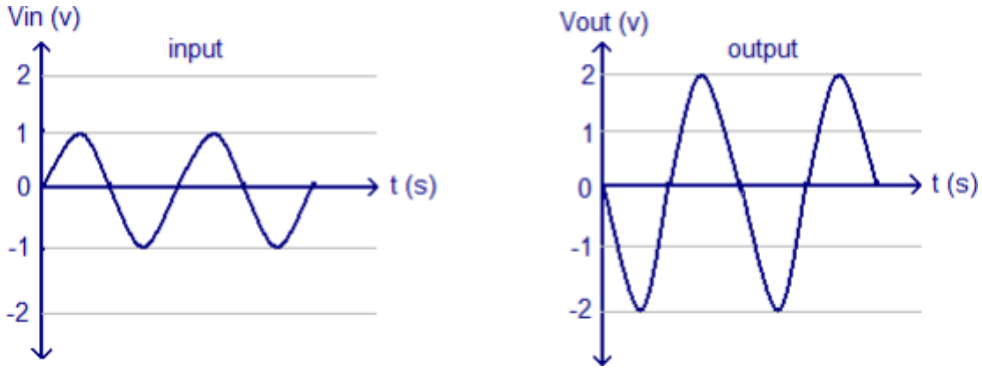


Fig 2. Inverting configuration model wave form

Observation:

S.NO	Frequency in Hz	Rf	Theoretical Vout	Measured Vout
1	1K	1K		
2		10K		

Non-Inverting Amplifier:

The circuit diagram of non-inverting amplifier is as shown in Fig 2. Here the input goes to the non-inverting input and a voltage divider returns a fraction of the output voltage to the inverting input. Pick the same resistors that you used inverting configuration, and construct the circuit. Measure Vin and Vout, determine the gain and compare to the theoretical value for the gain of this circuit,

$$Vout / Vin = 1 + (Rf / Rin)$$

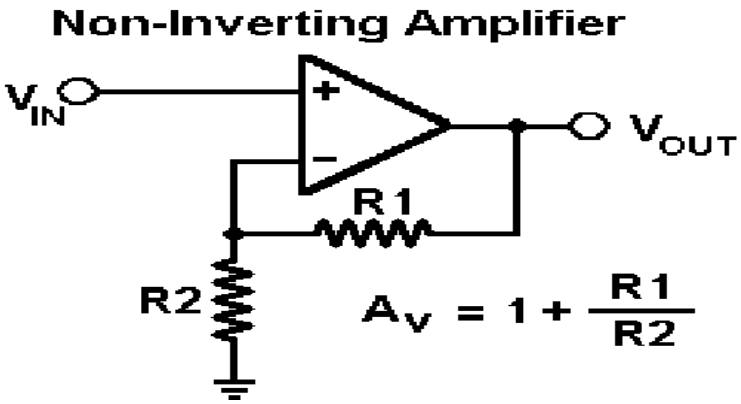


Fig-3: Non Inverting configuration

Model graph:

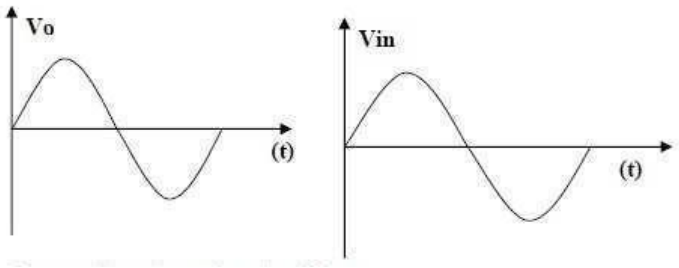


Fig-4. Non Inverting configuration model wave form

Procedure:

1. Connect the circuit for inverting amplifier as given in the figure above On bread board.
2. Connect the input terminal of the op-amp (terminal 2 for inverting amplifier and terminal 3 for non-inverting amplifier) to wave generator and output terminal (pin number 6) to DSO.
3. Apply +15 V at pin 7 and -15 V at pin 4.
4. Give the input from function generator sinusoidal 1V peak to peak 1khz and observe the output on DSO. Note down the peak voltages of input and output.

Observation:

S.NO	Frequency in Hz	Rf	Theoretical Vout	Measured Vout
1	1K	1K		
2		10K		

Result:

Graph sheet: