Efficient 6T SRAM Cell Using Skywater 130nm

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***Abstract*— This paper presents an optimized design of a 6-transistor (6T) Static Random Access Memory (SRAM) cell using Skywater 130nm technology. The design reduces power consumption while ensuring high-speed data access, addressing the needs of AI workloads in GPUs and edge AI devices. Techniques such as adaptive refresh rates, dynamic voltage scaling, and leakage minimization enhance energy efficiency without compromising speed or reliability, enabling sustainable performance for AI applications.**

***Keywords*—** 6T SRAM, energy efficiency, AI memory, Skywater 130nm, low power, AI acceleration

I. INTRODUCTION

The exponential growth of AI applications requires high-performance memory solutions that are both fast and energy-efficient. Static Random Access Memory (SRAM) is essential in AI hardware due to its low latency and high-speed access. However, as AI workloads expand, power efficiency becomes increasingly critical, particularly in mobile and edge devices with limited battery life. This paper presents the design and optimization of a 6T SRAM cell using the Skywater 130nm process, tailored specifically for AI-driven applications. By incorporating power-saving techniques, this design addresses the energy challenges of AI, contributing to sustainable hardware solutions for edge AI accelerators, GPUs, and neural network processing units.

II. PRINCIPLE OF GENERATION

A 6T SRAM cell comprises two cross-coupled inverters and two access transistors, forming a bistable flip-flop circuit for data storage. This configuration enables fast access times, making it suitable for high-speed applications. However, at the 130nm node, the design requires careful optimization to manage leakage and dynamic power, particularly under the intensive loads typical in AI applications

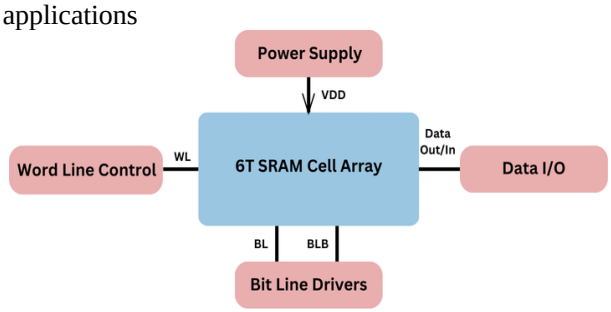

Fig. 1 Block Diagram of 6T SRAM Cell

III. IMPLEMENTATION

Adaptive Refresh Rates: Adjusts the refresh rate based on usage, reducing unnecessary power consumption for cells not frequently accessed.

- **Dynamic Voltage Scaling (DVS)**: Adjusts voltage in real-time based on operational load, allowing the cell to save power during idle periods.
- **Leakage Reduction Techniques**: Techniques like reverse body biasing and optimized transistor sizing are applied to control leakage current, significantly reducing standby power.

Circuit Diagram:

The diagram below shows the 6T SRAM configuration, with the layout of cross-coupled inverters (P1, P2, N1, N2) and access transistors (N3, N4). Each inverter's output connects to the input of the other, forming the stable storage nodes (Q, Q'), with controlled access through WL and BL/BLB.

Parameters:

- **VDD** = 1.2V
- **PMOS (P1, P2)**: Larger W/L ratios (e.g., 2:1) for drive strength.
- **NMOS (N1, N2)**: Balanced W/L ratios (e.g., 1:1) for stability.
- **NMOS (N3, N4)**: Sized for speed in accessing data.

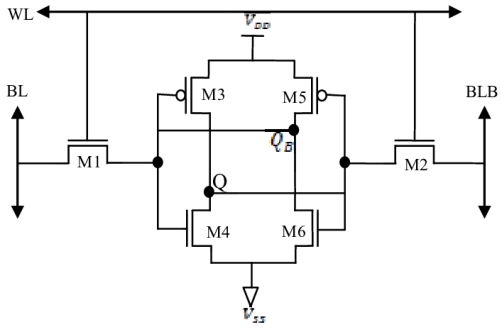

Fig. 2 6T SRAM Cell

IV. ISSUES & IMPROVEMENTS

SRAM stability in the 130nm node faces challenges due to process variability, including inconsistent transistor dimensions and doping concentrations, which can compromise data retention and access speeds critical for reliable AI applications. Future improvements focus on error correction techniques and further optimization of transistor sizes to enhance low-power performance. Additionally, implementing dynamic voltage scaling and adaptive refresh strategies can reduce power consumption while maintaining data integrity. These advancements will benefit AI applications, such as providing efficient temporary memory storage for GPU caches, enhancing response time in edge AI accelerators, reducing energy consumption in neural network training buffers, and extending battery life in mobile AI inference engines.

V. CONCLUSION & FUTURE SCOPE

This 6T SRAM cell, designed with power efficiency in mind on the Skywater 130nm process, meets the demands of energy-efficient AI applications. By integrating adaptive refresh rates, voltage scaling, and leakage reduction techniques, the design addresses critical power challenges in AI hardware. Future work will explore hybrid memory designs to further enhance power efficiency, ensuring sustainable AI hardware solutions for next-generation applications.

VI. REFERENCES

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