PHYSICAL DESIGN PROJECT

WEEK -2

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Batch : G3_Integrated VLSI Design
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06-03-2025

1. Run 4-bit counter using openlane flow and figure out the maximum frequency achieved

To add our custom designs into Openlane, we follow these steps:

https://openlane.readthedocs.io/en/latest/usage/designs.html

This is the main design file of a synchronous 4-bit up-down counter with control input as mode

```
module counter4bit (
    input wire mode,      // Mode: 1 for up, 0 for down
    input wire clk,       // Clock signal
    input wire rst,       //reset
    output reg [3:0] q    //output
);

always @(posedge clk or negedge rst) begin
    if (rst)
        q <= 4'b0000;
    else begin
        if (mode) begin
            $display("UP COUNTING");
            q <= q + 1'b1;
        end else begin
            $display("DOWN COUNTING");
            q <= q - 1'b1;
        end
    end
end

endmodule
```

Testbench for the design to test simulations

```
21  module tb;
22      reg clk;
23      reg rst;
24      reg mode;
25      wire [3:0] q;
26
27      counter4bit uut (
28          .mode(mode),
29          .clk(clk),
30          .rst(rst),
31          .q(q)
32      );
33
34      always #5 clk = ~clk;
35
36      initial begin
37          clk = 0;
38          rst = 0;
39          mode = 0;
40
41          #10 rst = 1;
42          #40 rst = 0;
43          mode = 1;
44          #50;
45          mode = 0;
46          #50;
47
48          rst = 1;
49          #10 rst = 0;
50
51          #50;
52          $finish;
53      end
54
55      initial begin
56          $monitor("Time = %0t | Mode = %b | Q = %b", $time, mode, q);
57      end
58  endmodule
```

Output simulation :

Starting the OpenLane Environment

```
preethi-grace@HP-245-G7-Notebook:~/OpenLane$ make mount
cd /home/preethi-grace/OpenLane && \
	docker run --rm -v /home/preethi-grace:/home/preethi-grace -v /home/preethi-grace/OpenLane:/openlane -v /home/preethi-gra
ce/OpenLane/empty:/openlane/install -v /home/preethi-grace/.volare:/home/preethi-grace/.volare -e PDK_ROOT=/home/preethi-grace/.v
olare -e PDK=sky130A  --user 1000:1000 -e DISPLAY=:1 -v /tmp/.X11-unix:/tmp/.X11-unix -v /home/preethi-grace/.Xauthority:/.Xautho
rity --network host --security-opt seccomp=unconfined -ti efabless/openlane:e73fb3c57e687a0023fcd4dcfd1566ecd478362a-amd64
OpenLane Container (1.1.1):/openlane%
```

Creating a 4-bit counter design in OpenLANE:

./flow.tcl -design counter4bit -init_design_config -add_to_designs -config_file config.tcl

```
OpenLane Container (1.1.1):/openlane% ./flow.tcl -design counter4bit -init_design_config -add_to_design
OpenLane v1.1.1 (e73fb3c57e687a0023fcd4dcfd1566ecd478362a)
All rights reserved. (c) 2020-2024 Efabless Corporation and contributors.
Available under the Apache License, version 2.0. See the LICENSE file for more details.

[SUCCESS]: openlane/counter4bit/config.json created with the default configuration. Please update the values as you see fit.
OpenLane Container (1.1.1):/openlane%
```

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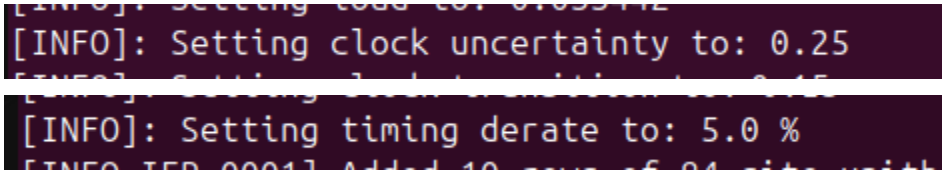
Copied the .v file of our design in the designs/counter4bit folder we have created

https://openlane.readthedocs.io/en/latest/reference/interactive_mode.html

a. Capture the uncertainty value, derate value defined in the design



b. List the worst slack value in each stage of the STA report -take

08-03-2025

STAGE	WORST SETUP SLACK (ns)	WORST HOLD SLACK(ns)
Synthesis	2.11	0.23
Floorplan	-	-

Placement	1.95	0.22
CTS	1.85	0.09
Routing	1.93	0.29
Signoff	0.36	0.14

Max frequency achieved at clock period = 3.8ns
Max Frequency = 263.16 MHz

c. List the power of each stage

STAGE	**POWER (Watts)**
Synthesis	$1.45x\ 10^{-4}$
Floorplan	$1.0x\ 10^{-9}$(found in logs)
Placement	GP : $1.47x10^{-4}$, DP: $1.25x10^{-4}$
CTS	$2.84x10^{-4}$
Routing	$2.95x10^{-4}$
Signoff	$3.01x10^{-4}$

d. List the area of the design in each stage

STAGE	**AREA (μm^2)**
Synthesis	306.544000
Floorplan	-
Placement	322
CTS	345
Routing	375.36
Signoff	435.418

e. Route length of signal and clock

09-03-2025

```
set filename "/home/preethi-grace/OpenLane/designs/counter_4_bit/runs/run1/reports/routing/27-wire_lengths.csv"
set file_handle [open "$filename" r]
set clk_sum 0.0 ;
set data_sum 0.0 ;
set total_sum 0.0  ;

gets $file_handle ;
while { [gets $file_handle data ] >=0} {
        set net [lindex [split $data ","] 0];
        set length_um [lindex [split $data ","] 1];
        set total_sum [expr {$total_sum + $length_um}];
        if {[string match "*clk" $net]} {
                set clk_sum [expr {$clk_sum + $length_um}];
        }
        set data_sum [expr {$total_sum - $clk_sum}];
}
close $file_handle
puts "Total clock wire length : $clk_sum um "
puts "Total data wire length : $data_sum um"
puts "Total wire length in the design: $total_sum um"
```

```
preethi-grace@HP-245-G7-Notebook:~/Downloads/SURE TRUST/PROJECT/WEEK_2_ASSIGNMENT$ tclsh clk_length.tcl
Total clock wire length : 98.65 um
Total data wire length : 410.21000000000015 um
Total wire length in the design: 508.8600000000001 um
```

f. Worst IR drop percentage and top 10 worst IR drop cells

```
set file1 [open "/home/preethi-grace/OpenLane/designs/counter_4_bit/runs/run1/reports/signoff/34-irdrop-VPWR.rpt" r]
set file2 [open "/home/preethi-grace/OpenLane/designs/counter_4_bit/runs/run1/reports/signoff/34-irdrop-VGND.rpt" r]

set vpwr_val {}
set vgnd_val {}

# Read VPWR file and storing values with the whole line
while { [gets $file1 line] >= 0 } {
    set value [lindex [split $line ","] 5]  ;
    if { $value != "" } {
        lappend vpwr_val [list $value $line]  ;
    }
}

# Read VGND file and storing values with the whole line
while { [gets $file2 line] >= 0 } {
    set value [lindex [split $line ","] 5]  ;
    if { $value != "" } {
        lappend vgnd_val [list $value $line]  ;
    }
}

# Sorting values in ascending order by taking reference of last column
set vpwr_val [lsort $vpwr_val]
set vgnd_val [lsort $vgnd_val]

puts "Top 10 least IR Drop values for VPWR:"
for {set i 0} {$i < 10 && $i < [llength $vpwr_val]} {incr i} {
    puts "[lindex [lindex $vpwr_val $i] 1]"
}
```

```
}

puts "Top 10 least IR Drop values for VGND:"
for {set i 0} {$i < 10 && $i < [llength $vgnd_val]} {incr i} {
    puts "[lindex [lindex $vgnd_val $i] 1]"
}

close $file1
close $file2
```

```
preethi-grace@HP-245-G7-Notebook:~/Downloads/SURE TRUST/PROJECT/WEEK_2_ASSIGNMENT$ tclsh least_irdrop.tcl
Top 10 least IR Drop values for VPWR:
_52_,VPWR,li1,27.8300,24.4800,1.799934
clkbuf_0_clk,VPWR,li1,27.1400,24.4800,1.799934
clkbuf_1_1__f_clk,VPWR,li1,26.6800,35.3600,1.799940
output5,VPWR,li1,27.6000,35.3600,1.799940
_56_,VPWR,li1,22.5400,24.4800,1.799944
clkbuf_1_0__f_clk,VPWR,li1,26.6800,13.6000,1.799944
FILLER_0_8_41,VPWR,li1,25.3000,35.3600,1.799947
_54_,VPWR,li1,25.3000,13.6000,1.799948
FILLER_0_4_15,VPWR,li1,15.1800,24.4800,1.799953
FILLER_0_4_27,VPWR,li1,18.1700,24.4800,1.799953
Top 10 least IR Drop values for VGND:
FILLER_0_1_61,VGND,li1,36.3400,16.3200,0.000020
FILLER_0_1_73,VGND,li1,40.9400,16.3200,0.000020
FILLER_0_2_60,VGND,li1,35.8800,16.3200,0.000020
FILLER_0_2_72,VGND,li1,40.4800,16.3200,0.000020
FILLER_0_2_80,VGND,li1,42.5500,16.3200,0.000020
PHY_EDGE_ROW_1_Right_1,VGND,li1,43.4700,16.3200,0.000020
PHY_EDGE_ROW_2_Right_2,VGND,li1,43.4700,16.3200,0.000020
output4,VGND,li1,32.6600,16.3200,0.000024
_54_,VGND,li1,25.3000,16.3200,0.000025
FILLER_0_1_15,VGND,li1,15.1800,16.3200,0.000026
```

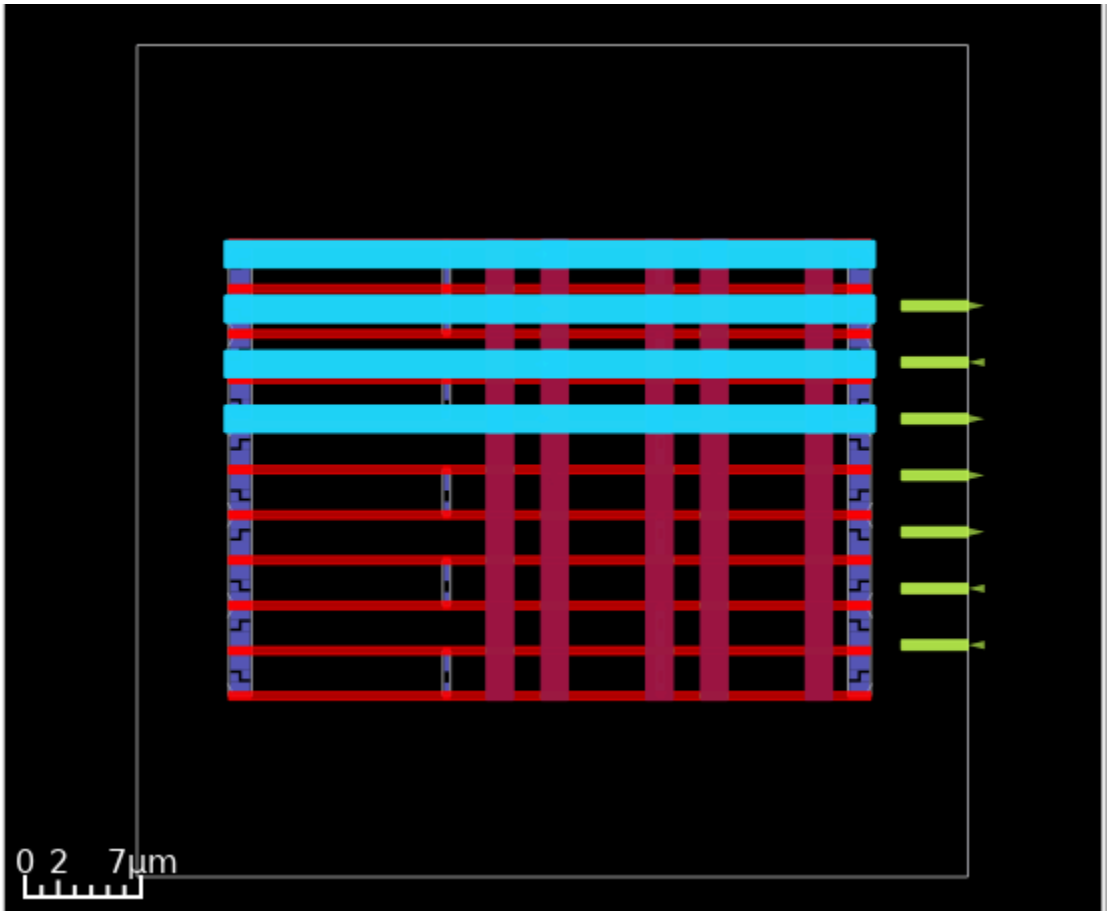
g. The design utilization at each stage

STAGE	UTILIZATION (%)
Synthesis	-
Floorplan	-
Placement	31
CTS	33
Routing	36
Signoff	-

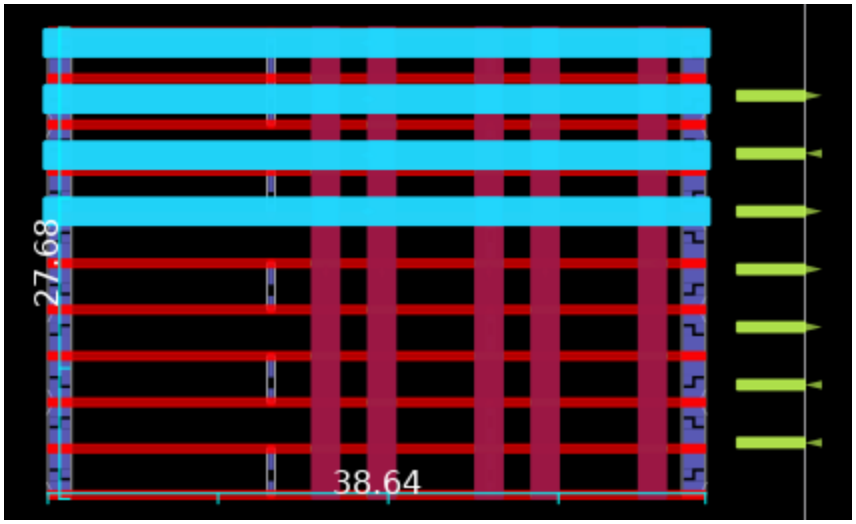
10-03-2025

2. Explore the GUI option share the image of Floorplan -Placement - CTS and Route stage with below information

a. Floorplan :

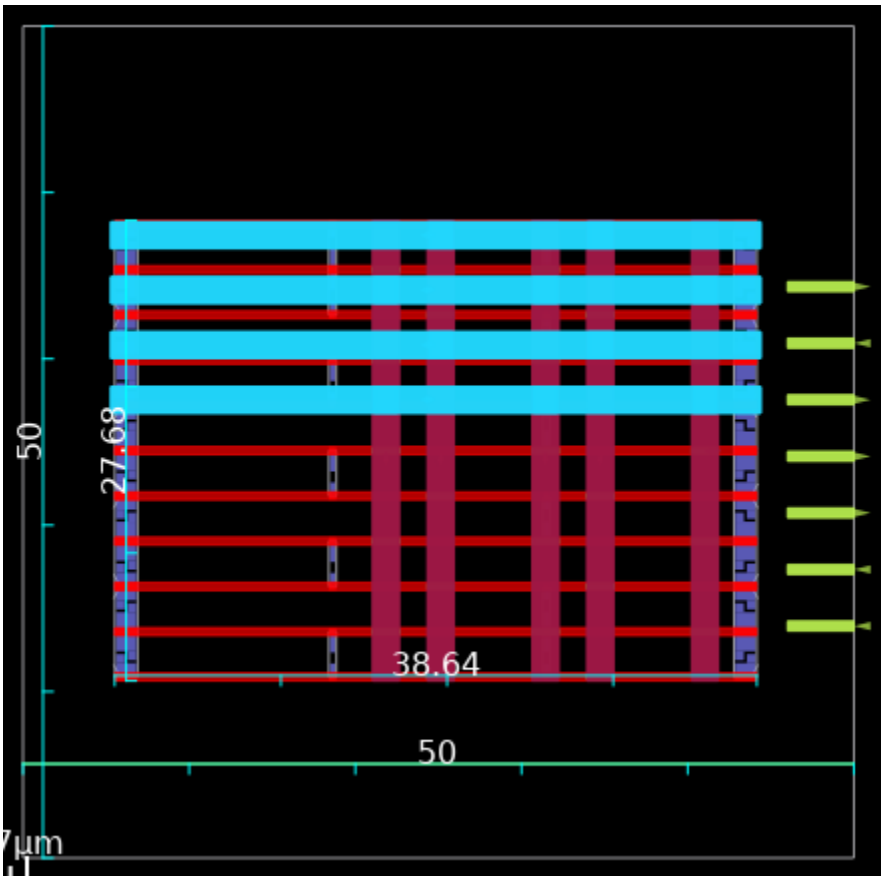


i. Measure the core width and height



Width of core = 38.64 um
Height of core = 27.68 um

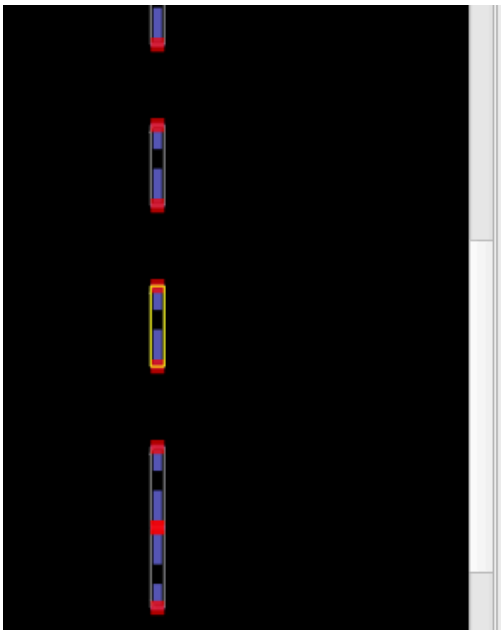
ii. Measure the die width and height



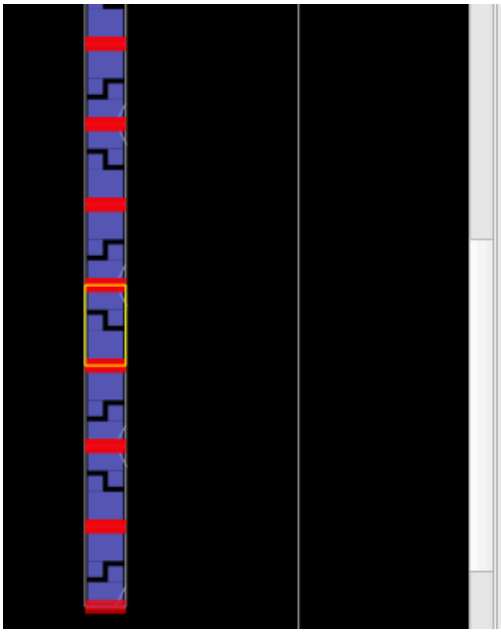
Width of die = 50 um
Height of die = 50 um

iii. Report different variety of physical only cells at floorplan stage

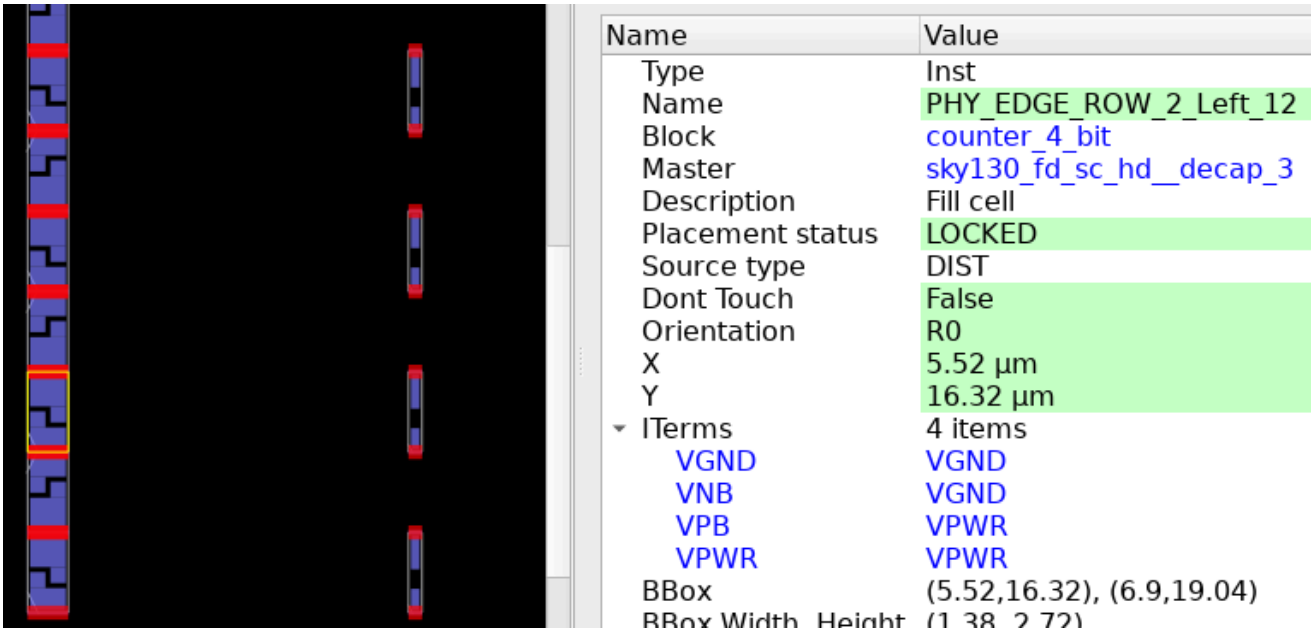
11-03-2025



Name	Value
Type	Inst
Name	TAP_TAPCELL_ROW_3_24
Block	counter_4_bit
Master	sky130_fd_sc_hd__tapvpwrvgnd_1
Description	Tap cell
Placement status	LOCKED
Source type	DIST
Dont Touch	False
Orientation	MX
X	31.28 µm
Y	19.04 µm
ITerms	2 items
VGND	VGND
VPWR	VPWR
BBox	(31.28,19.04), (31.74,21.76)
BBox Width, Height	(0.46, 2.72)

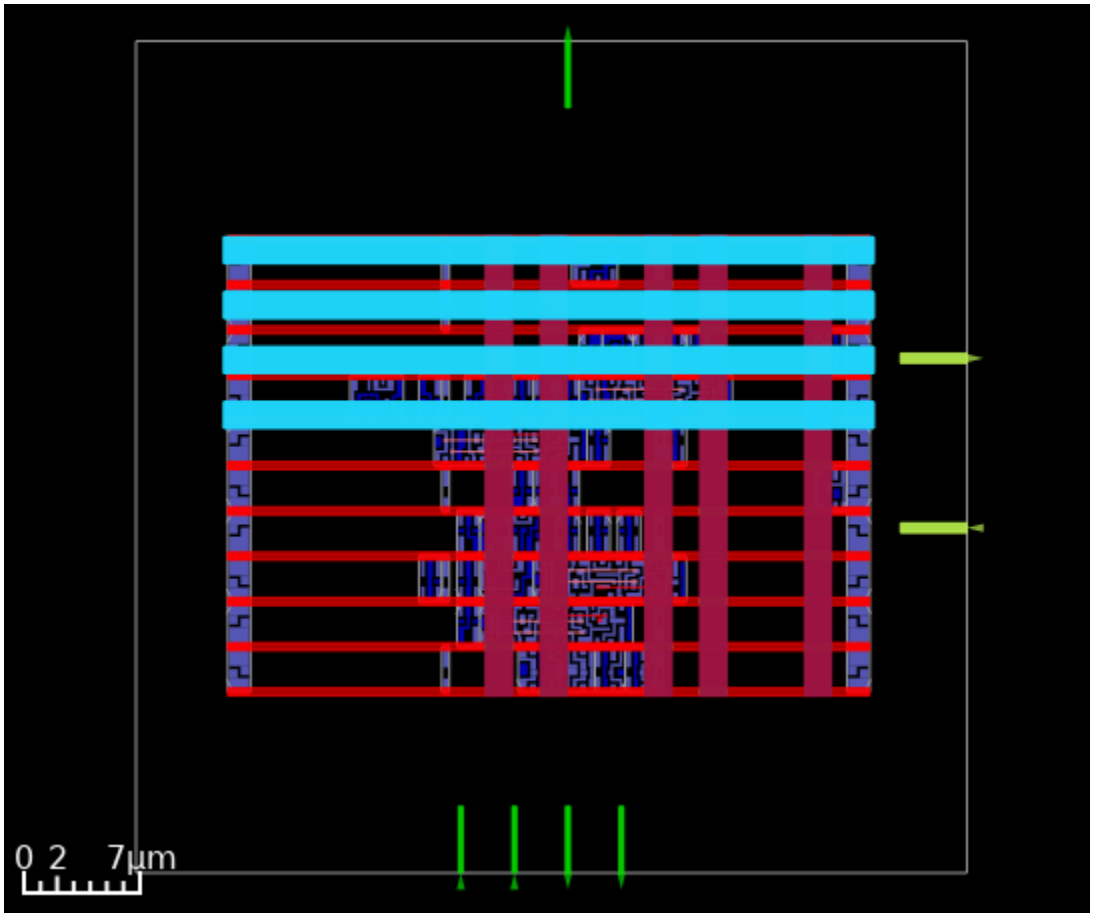


Name	Value
Type	Inst
Name	PHY_EDGE_ROW_3_Right_3
Block	counter_4_bit
Master	sky130_fd_sc_hd__decap_3
Description	Fill cell
Placement status	LOCKED
Source type	DIST
Dont Touch	False
Orientation	R180
X	42.78 µm
Y	19.04 µm
ITerms	4 items
VGND	VGND
VNB	VGND
VPB	VPWR
VPWR	VPWR
BBox	(42.78,19.04), (44.16,21.76)
BBox Width, Height	(1.38, 2.72)

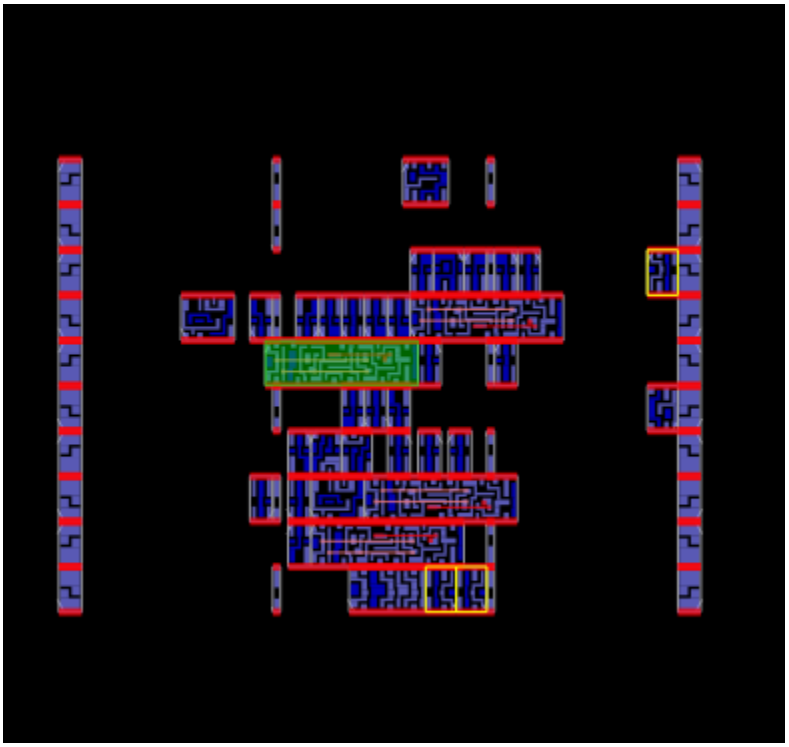


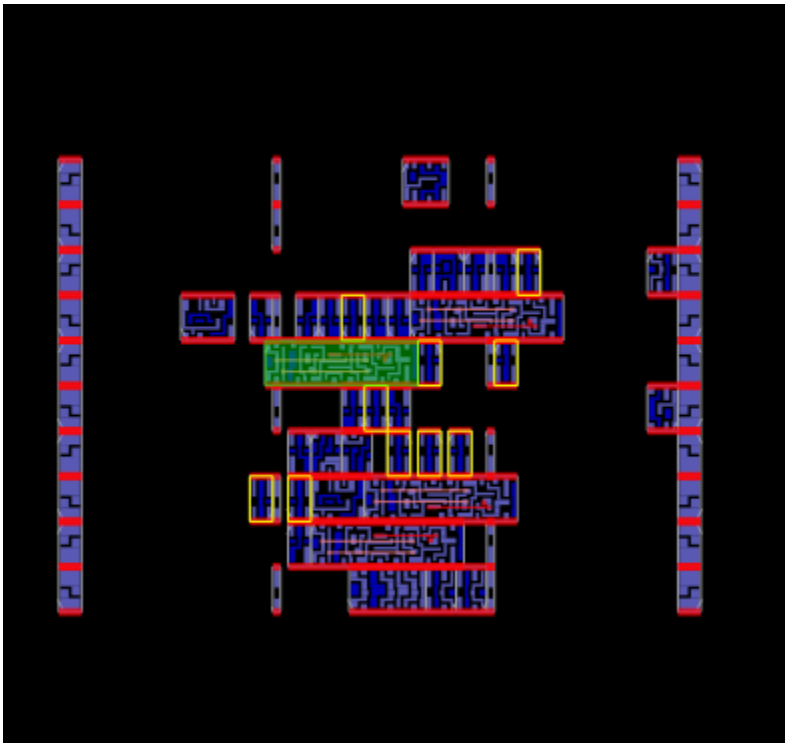
Name	Value
Type	Inst
Name	PHY_EDGE_ROW_2_Left_12
Block	counter_4_bit
Master	sky130_fd_sc_hd__decap_3
Description	Fill cell
Placement status	LOCKED
Source type	DIST
Dont Touch	False
Orientation	R0
X	5.52 µm
Y	16.32 µm
ITerms	4 items
VGND	VGND
VNB	VGND
VPB	VPWR
VPWR	VPWR
BBox	(5.52,16.32), (6.9,19.04)
BBox Width, Height	(1.38, 2.72)

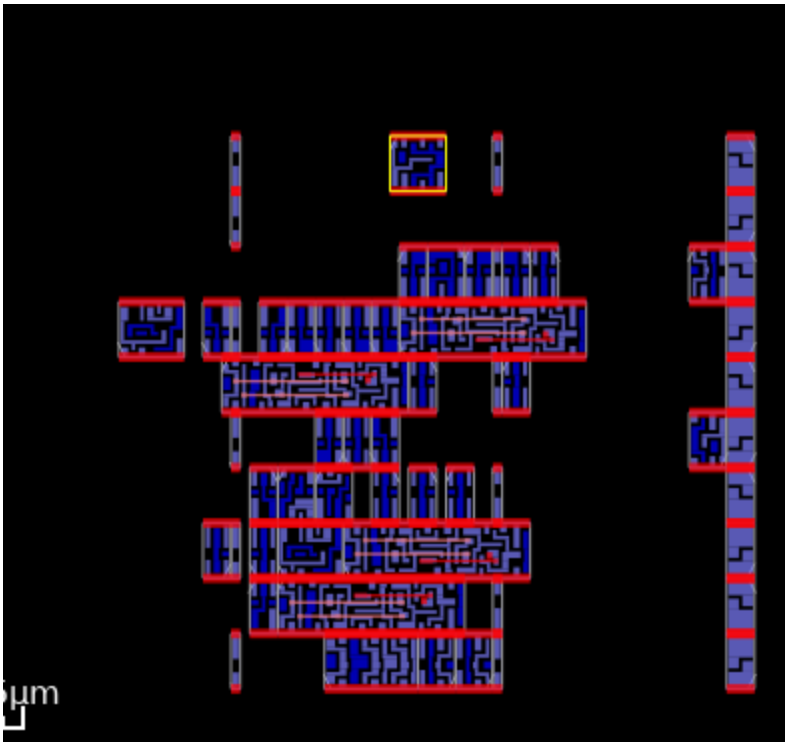
b. Placement



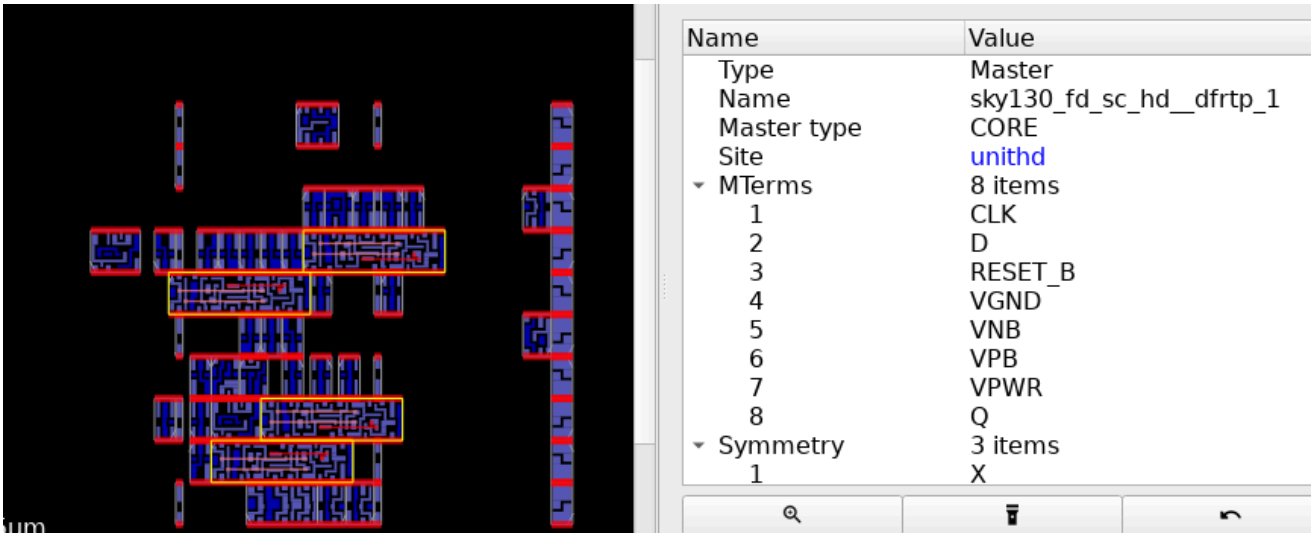
i. Highlight the buffers and inverters in the design



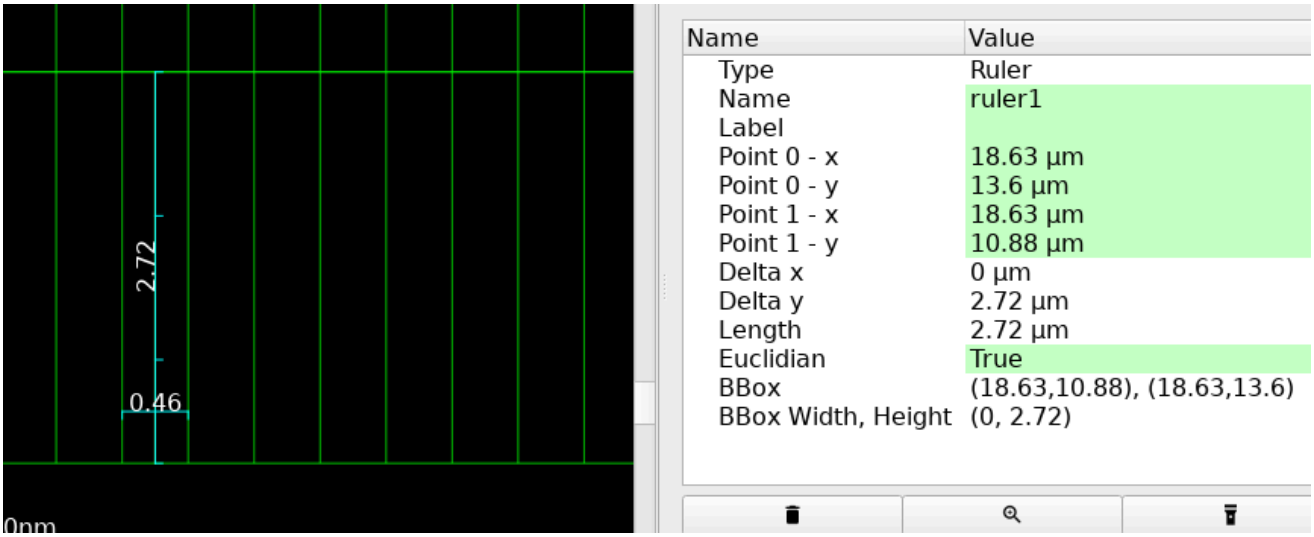




ii. Highlight the flops in the design

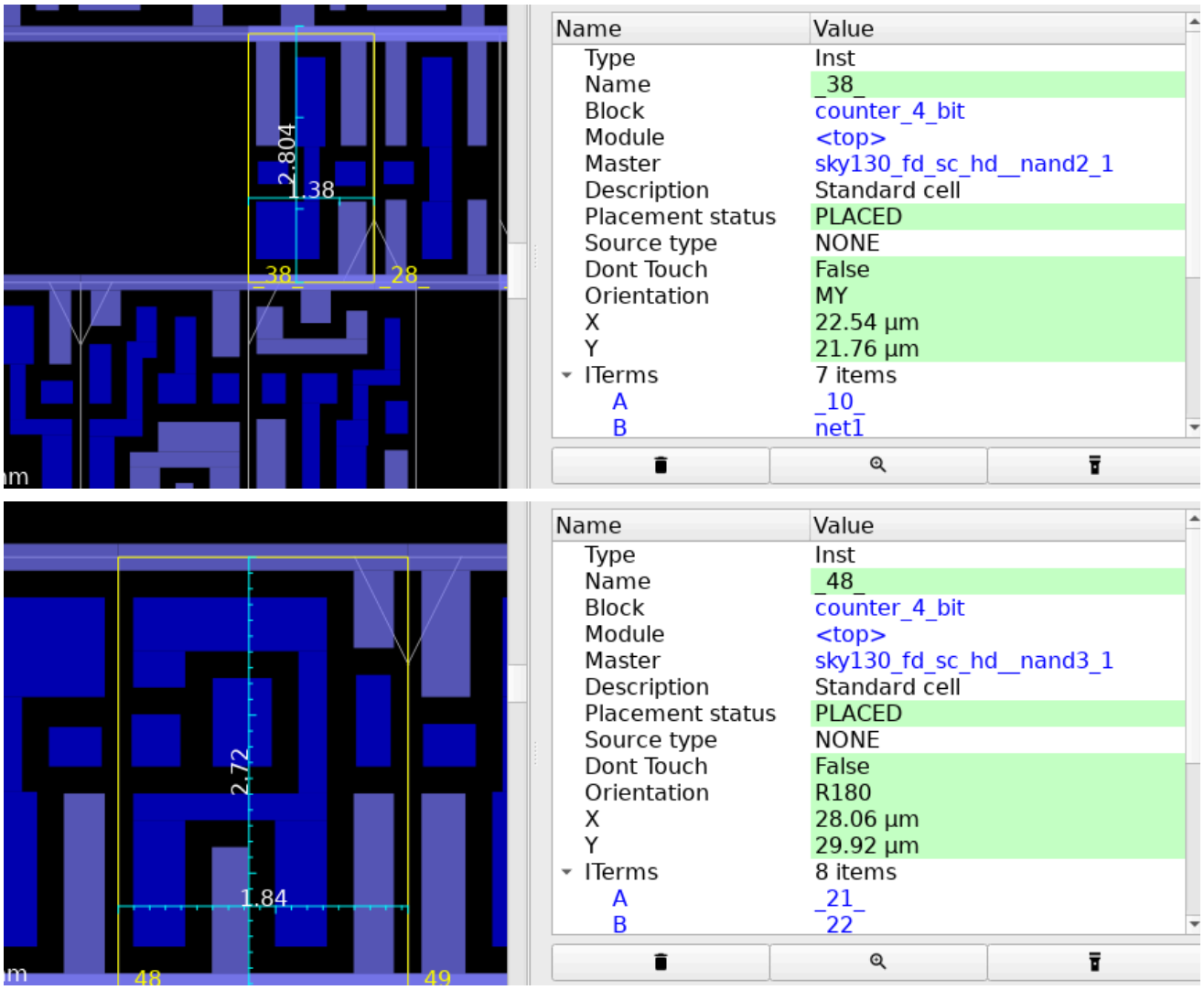


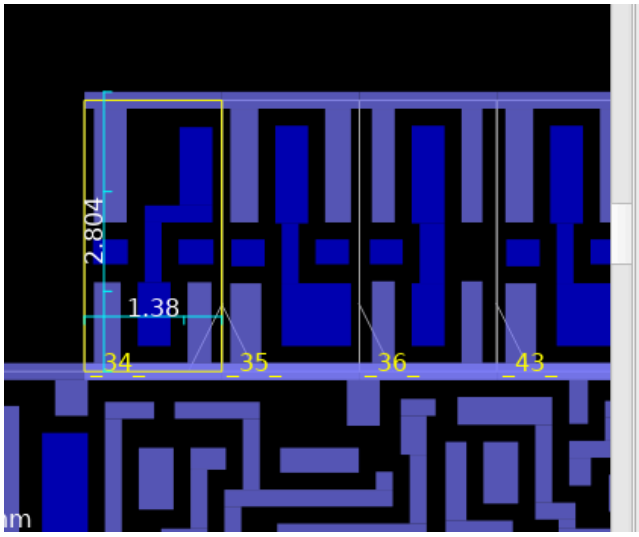
iii. Capture the site row and measure the height and width



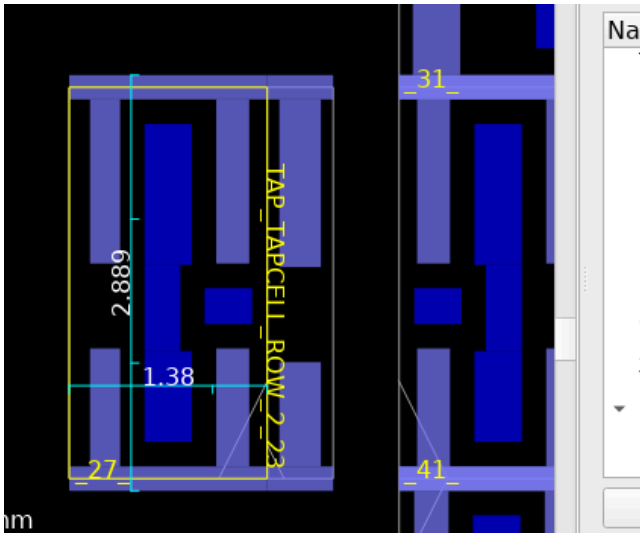
Width = 0.46 um
Height = 2.72 um

iv. Find the different library cell heights and widths

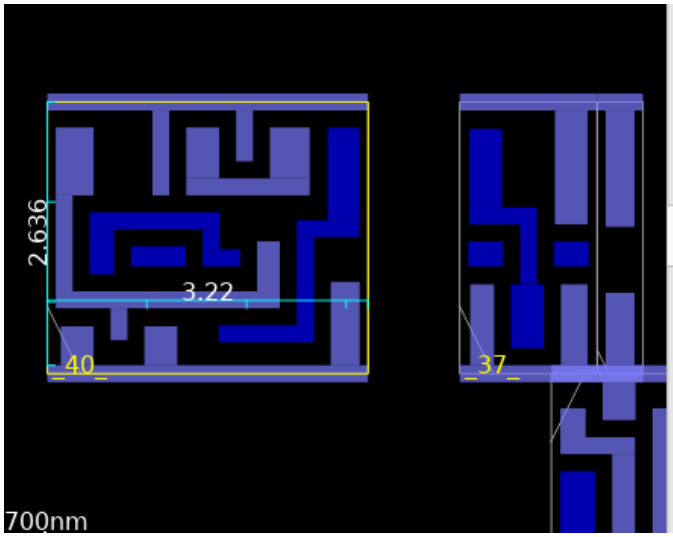




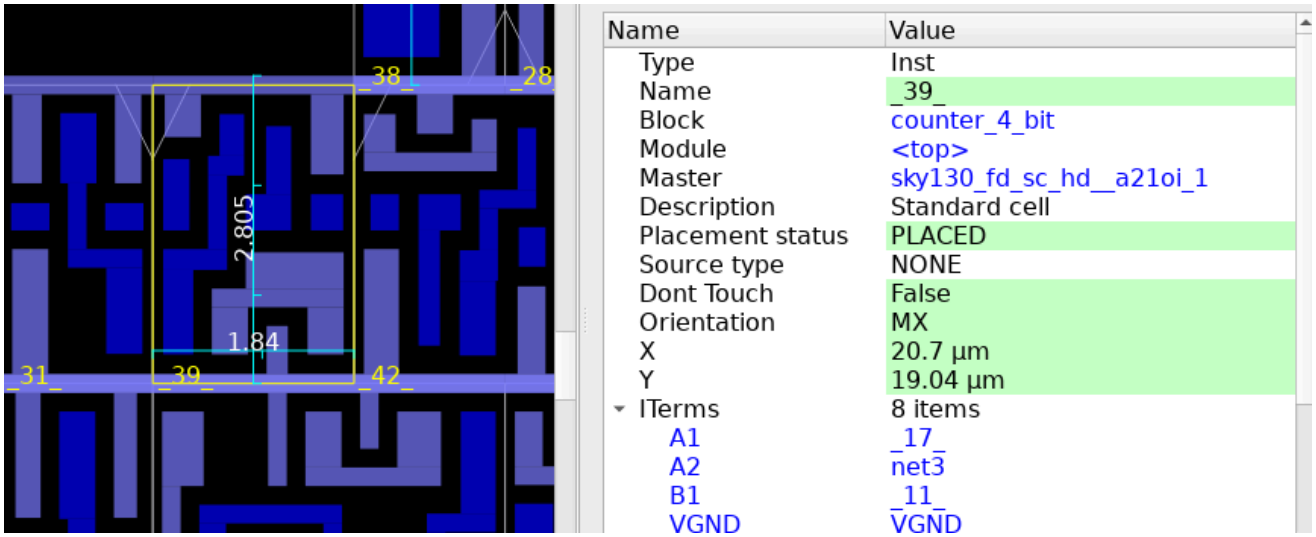
Name	Value
Type	Inst
Name	_34_
Block	counter_4_bit
Module	<top>
Master	sky130_fd_sc_hd__nor2_1
Description	Standard cell
Placement status	PLACED
Source type	NONE
Dont Touch	False
Orientation	MY
X	19.78 µm
Y	27.2 µm
ITerms	7 items
A	net1
B	net5



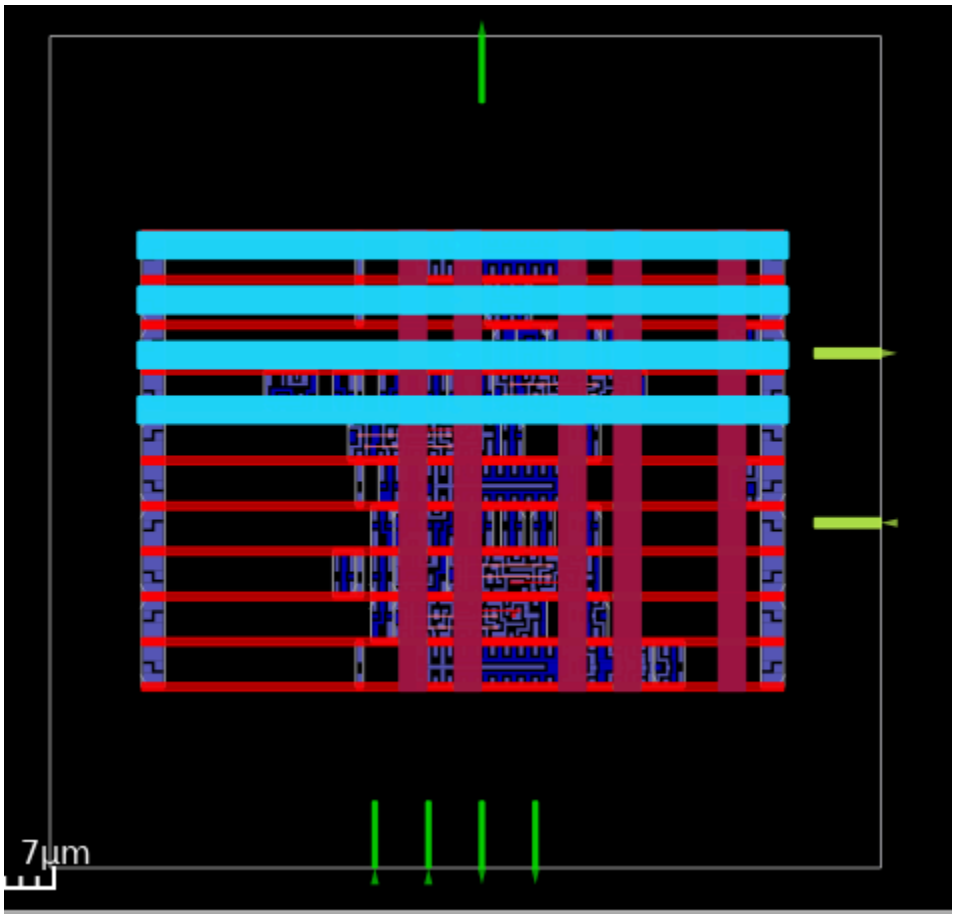
Name	Value
Type	Inst
Name	_27_
Block	counter_4_bit
Module	<top>
Master	sky130_fd_sc_hd__inv_2
Description	Standard cell
Placement status	PLACED
Source type	NONE
Dont Touch	False
Orientation	MY
X	17.02 µm
Y	16.32 µm
ITerms	6 items
A	net3
VGND	VGND



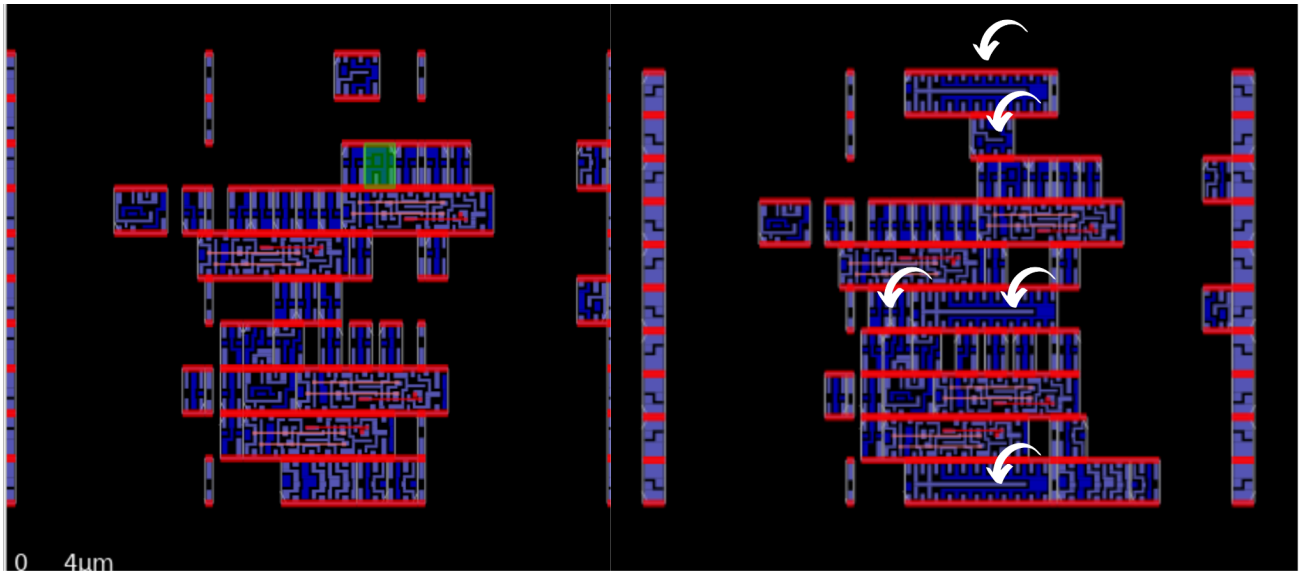
Name	Value
Type	Inst
Name	_40_
Block	counter_4_bit
Module	<top>
Master	sky130_fd_sc_hd__xor2_1
Description	Standard cell
Placement status	PLACED
Source type	NONE
Dont Touch	False
Orientation	R0
X	12.88 µm
Y	27.2 µm
ITerms	7 items
A	_16_
B	_18_


_38_
_28
2.805
1.84
_31_
_39_
_42_
Name
Value
Type
Inst
Name
_39_
Block
counter_4_bit
Module
<top>
Master
sky130_fd_sc_hd__a21oi_1
Description
Standard cell
Placement status
PLACED
Source type
NONE
Dont Touch
False
Orientation
MX
X
20.7 µm
Y
19.04 µm
ITerms
8 items
A1
_17_
A2
net3
B1
_11_
VGND
VGND

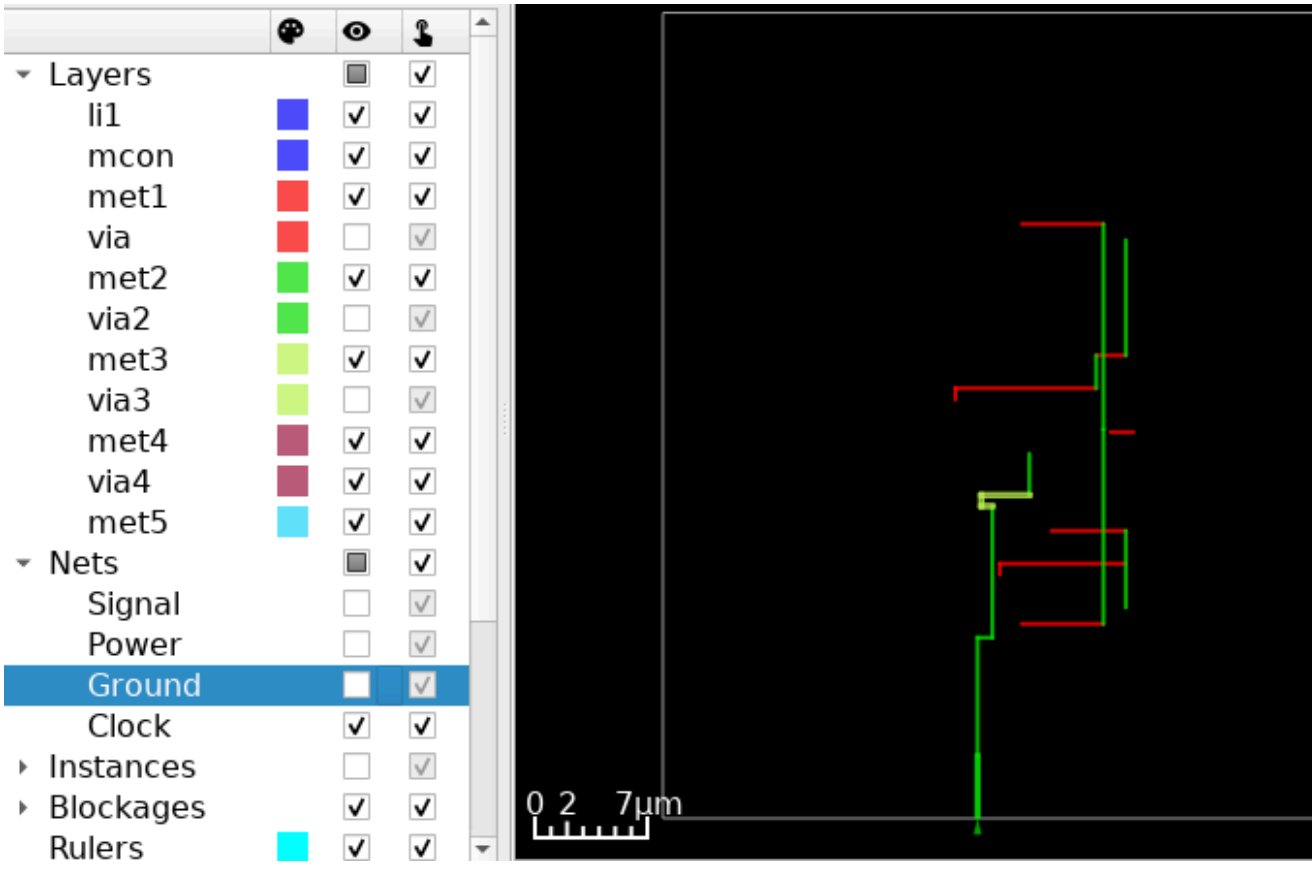
c. CTS


7µm

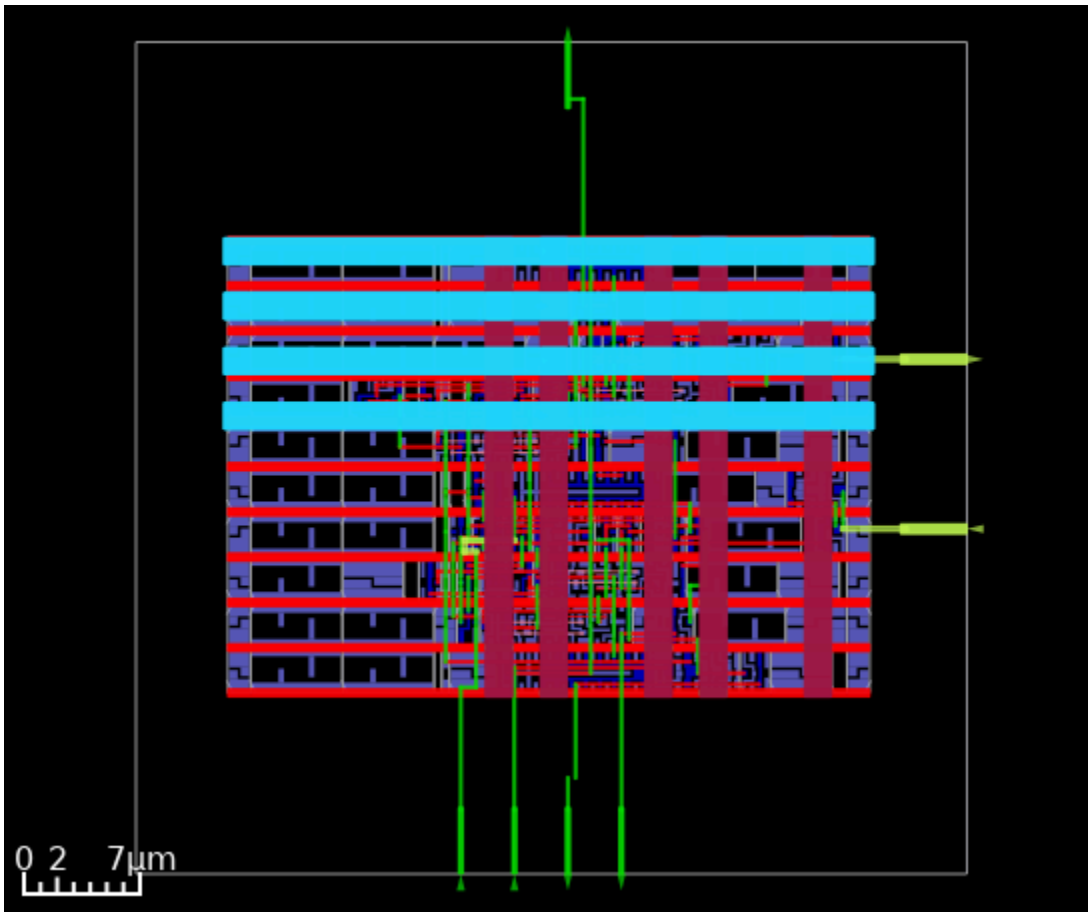
i. Highlight the CTS added buffer/inverter



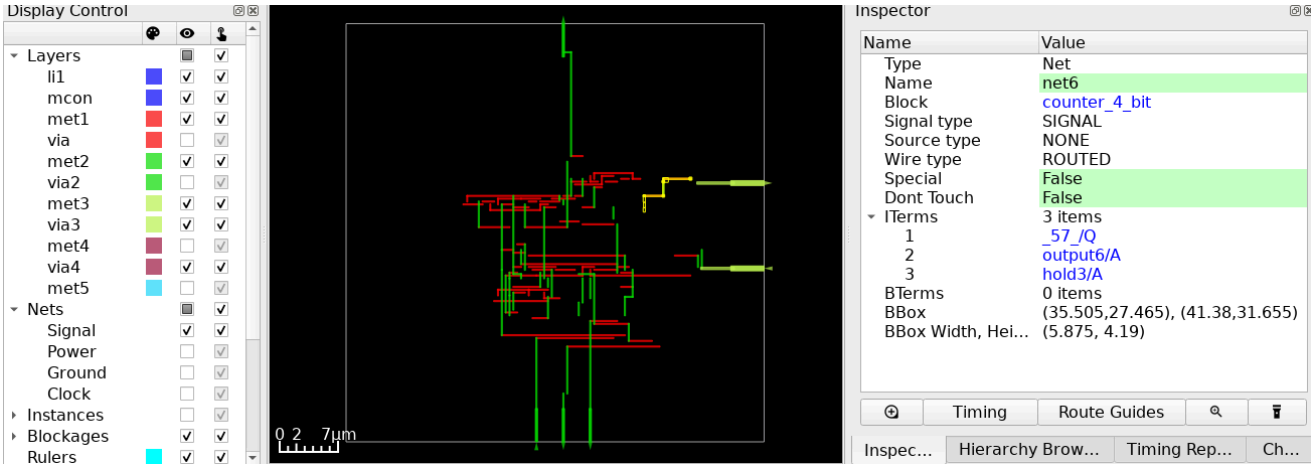
ii. Highlight the clock routing and its metal layer usage



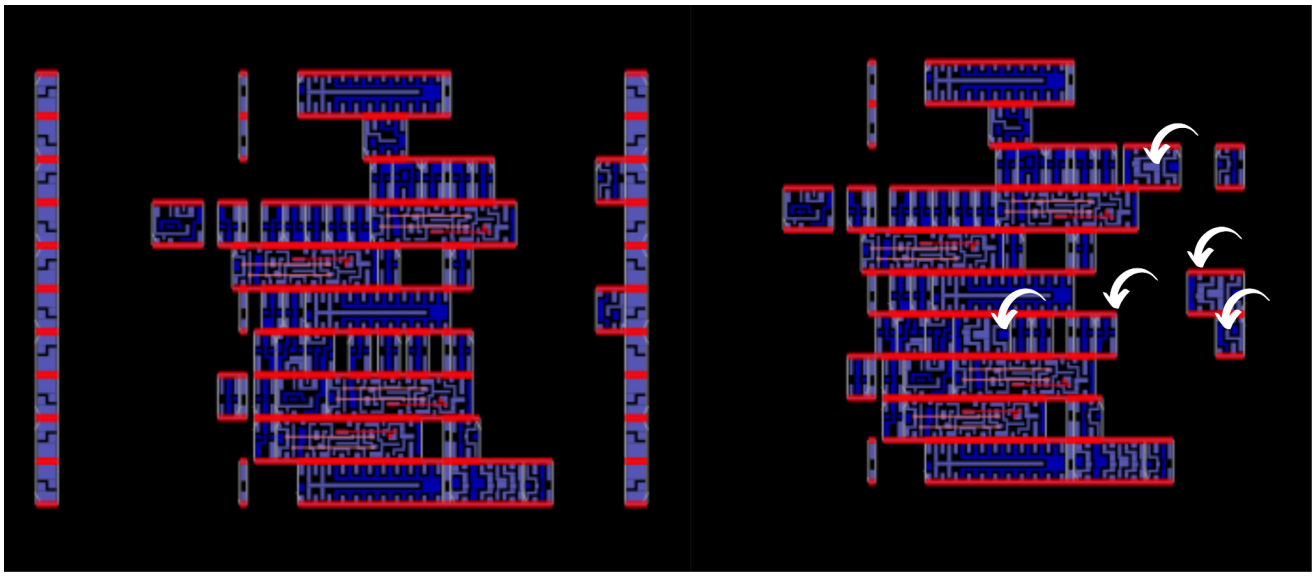
d. Routing



i. Highlight the signal routing and its metal layers



ii. Figure out the newly added buffer/inverter in the routing stage



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3. Setup the flow with the below features

a. Do pnR for 32-bit up-down counter 6ns clock period

b. Set the uncertainty of the design to 10% of your clock frequency
c. Set derate value to 3%

```
[INFO]: Setting clock uncertainty to: 0.6
[INFO]: Setting clock transition to: 0.15
[INFO]: Setting timing derate to: 3.0 %
```

d. Utilization of floorplan to 70%
e. Insert two columns of tap cells
f. Enable core ring in the design
g. CTS target skew to 5% of the clock period

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For inserting two rows of tap cells, if we tried to increase the spacing design, encountering atmost 900+ DRC errors, we can predict that for these specifications of the design, it needs more than two tap cell columns for solving latchup issues for cells, currently design has 4 column which is automatically inserted by openlane.

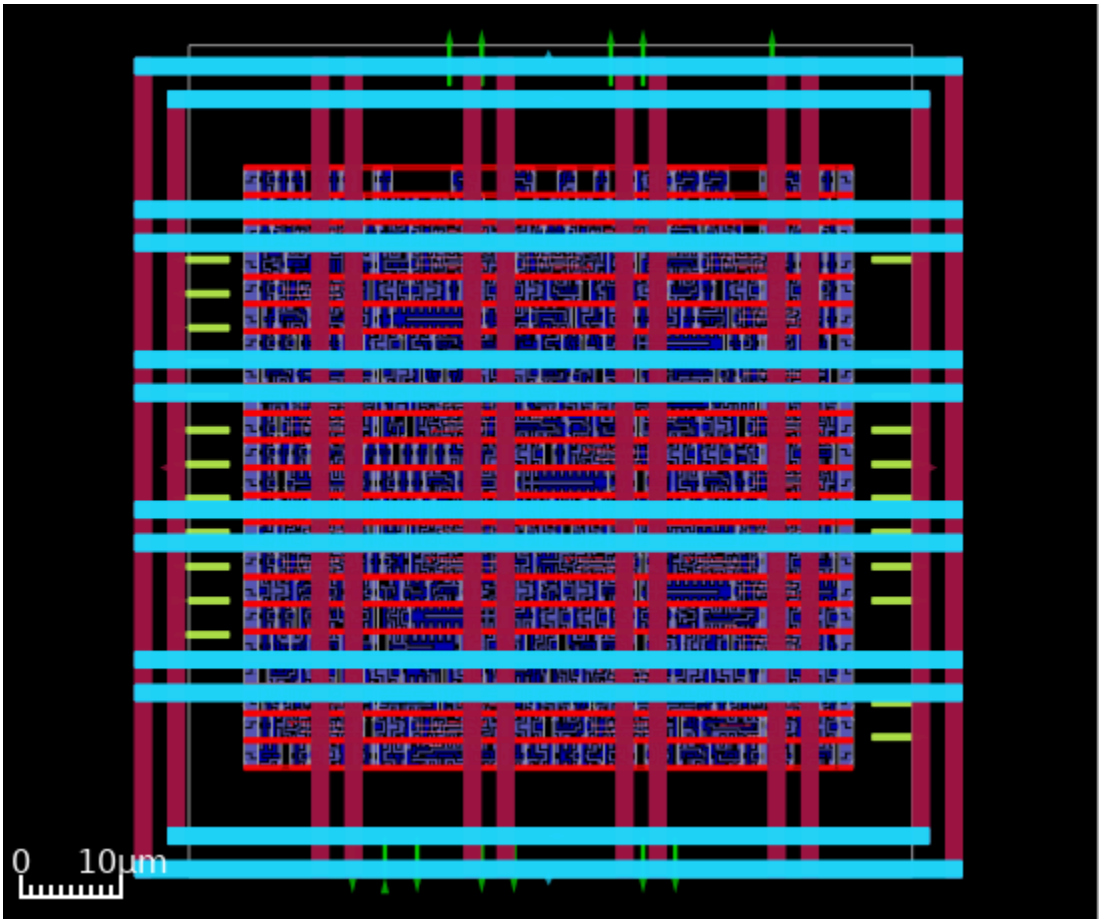
```
set ::env(DESIGN_NAME) {counter}
set ::env(VERILOG_FILES) [glob $::env(DESIGN_DIR)/src/*.v]
set ::env(CLOCK_PORT) "clk"
set ::env(CLOCK_PERIOD) "6.0"
set ::env(SYNTH_CLOCK_UNCERTAINTY) "0.6"
set ::env(SYNTH_TIMING_DERATE) "0.03"
set ::env(FP_CORE_UTIL) 70
set ::env(FP_PDN_CORE_RING) 1
set ::env((FP_TAPCELL_DIST) 15
set ::env(FP_PDN_MULTILAYER) {1}

set tech_specific_config "$::env(DESIGN_DIR)/$::env(PDK)_$::env(STD_CELL_LIBRARY)_config.tcl"
if { [file exists $tech_specific_config] == 1 } {
    source $tech_specific_config
}
```

For Clock skew, the parameter is removed from the open lane.

`CTS_TARGET_SKEW`	**Removed: No longer supported by underlying utility**: The target clock skew in picoseconds. (Default: `200` ps)

Except for these 2 specifications, I have completed the design flow for the 32-bit counter.



This is the final layout of a 32-bit counter design with given specifications.