TELETEXT TIMING CHAIN

The SAA5020 is an MOS N-channel integrated circuit which performs the timing functions for a teletext system.

The SAA5020 is a 24-lead device which provides the necessary timing signals to the teletext page memory and to the Character Generator (SAA5050 series). It works in conjunction with the Video Processor Circuit (SAA5030) and the Teletext Acquisition and Control Circuit (SAA5040 series). The operation of the SAA5020 maintains the synchronisation between the teletext system and the incoming video signal.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current	I_{DD}	typ.	20	mA
Operating ambient temperature range	T_{amb}		−20 to +70	°C

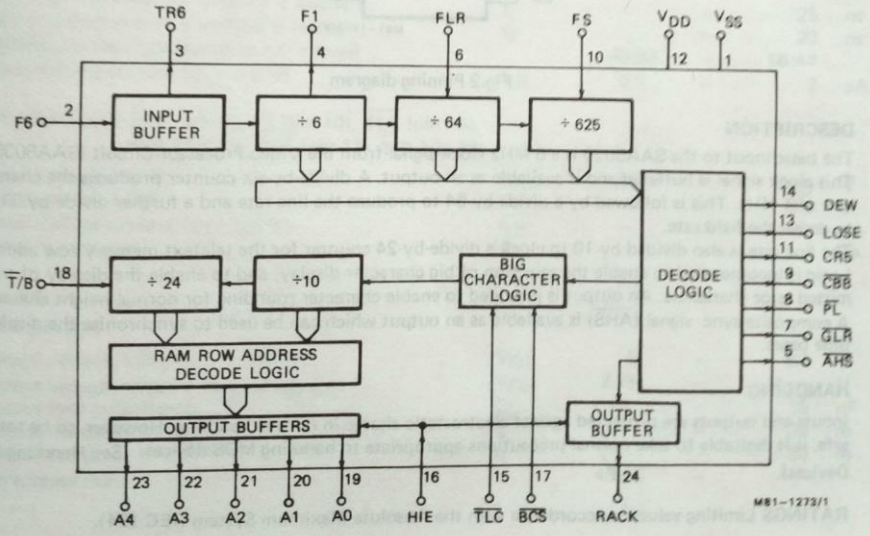

Fig.1 Block diagram

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)

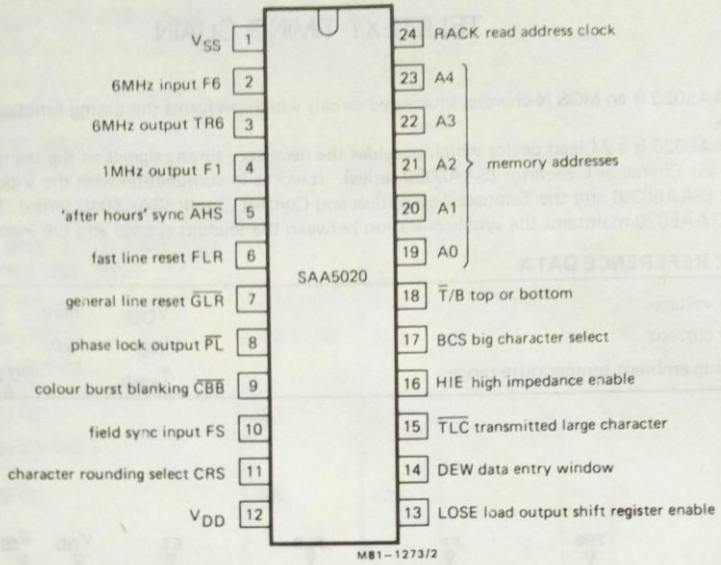

Fig.2 Pinning diagram

DESCRIPTION

The basic input to the SAA5020 is a 6 MHz clock signal from the Video Processor Circuit (SAA5030). This clock signal is buffered and is available as an output. A divide-by-six counter produces the character rate of 1 MHz. This is followed by a divide-by-64 to produce the line rate and a further divide by 312/313 to derive the field rate.

The line rate is also divided by 10 to clock a divide-by-24 counter for the teletext memory row addresses. Logic is incorporated to enable the selection of big character display, and to enable the display of transmitted large characters. An output is provided to enable character rounding for normal height characters. A composite sync. signal ($\overline{AHS}$) is available as an output which can be used to synchronise the display time bases.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. (See Handling MOS Devices).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Voltages (with respect to pin 1)

			min.	max.	
Supply voltage	(pin 12)	V_{DD}	−0.3	7.5	V
Input voltage	All inputs (pins 2, 6, 10, 15, 16, 17, 18)	V_I	−0.3	7.5	V

RATINGS (continued)

		min.	typ.	max.	
Output voltage (pins 3, 4, 5, 7, 11, 13, 14)	V_O	−0.3		7.5	V
(pins 16, 19, 20, 21, 23, 24)	V_O	−0.3		7.5	V
(pins 8, 9)	V_O	−0.3		13.2	V
Temperatures					
Storage temperature range	T_{stg}		−20 to +125		°C
Operating ambient temperature range	T_{amb}		−20 to +70		°C

CHARACTERISTICS

Supply voltage (pin 12)	V_{DD}	4.5	–	5.5	V
The following characteristics apply at T_{amb} = 25 °C and V_{DD} = 5 V unless otherwise stated.					
Supply current	I_{DD}	–	20	50	mA
Inputs					
6 MHz - F6 (pin 2)					
Input voltage; HIGH	V_{IH}	3.5	–	6.5	V
Input voltage; LOW	V_{IL}	Note 1	–	0	V
Rise time (between 0 V and 3.5 V levels)	t_r	–	–	25	ns
Fall time (between 0 V and 3.5 V levels)	t_f	–	–	20	ns
Mark/space ratio (measured at 1.5 V level)		40:60	–	56:44	
Input leakage current (V_I = 5.5 V)	I_{IR}	0.2	–	2	μA
All other inputs FLR (pin 6), FS (pin 10), $\overline{\text{TLC}}$ (pin 15), HIE (pin 16), BCS (pin 17), T/$\overline{\text{B}}$ (pin 18)					
Input voltage; HIGH	V_{IH}	2.0	–	V_{DD}	V
Input voltage; LOW	V_{IL}	0	–	0.8	V
Input leakage current (V_I = 5.5 V)	I_{IR}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Outputs					
TR6 (pin 3)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance	C_L	–	–	15	pF
Output rise time	t_r	–	–	30	ns
Output fall time (Note 2)	t_f	–	–	30	ns
Mark/space ratio		40:60	–	–	

		min.	typ.	max.	
F1 (pin 4)					
Output voltage; LOW (I_{OL} = 100 μA) Note 4	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.75	–	V_{DD}	V
Output load capacitance	C_L	–	–	35	pF
Output rise time | Note 2	t_r	–	–	50	ns
Output fall time | Note 2	t_f	–	–	30	ns
Mark/space ratio		–	–	60:40	
Delay time (measured from rising edge of TR6) Note 3	t_d	7	–	60	ns
$\overline{\text{AHS}}$ (pin 5)					
Output voltage; LOW (I_{OL} = 100 μA) Note 5	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 200 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time | Note 2	t_r	–	–	100	ns
Output fall time | Note 2	t_f	–	–	100	ns
Delay time (falling edge measured from F1 rising edge) Note 3		0	–	300	ns
$\overline{\text{GLR}}$ (pin 7)					
Output voltage; LOW (I_{OL} = 0.9 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	40	pF
Output rise time | Note 2	t_r	–	–	60	ns
Output fall time | Note 2	t_f	–	–	50	ns
Delay time Note 3	t_d	0	–	200	ns
$\overline{\text{PL}}$ (pin 8) (Open drain)					
Output voltage; LOW (I_{OL} = 2 mA)	V_{OL}	–	–	1.0	V
Output current in off state (V_O = 6 V)	I_O	–	–	10	μA
Output load capacitance	C_L	–	–	30	pF
Output fall time Note 2	t_f	–	–	100	ns
Delay time Note 3	t_d	0	–	250	ns
$\overline{\text{CBB}}$ (pin 9) (Open drain)					
Output voltage; LOW (I_{OL} = 1 mA)	V_{OL}	0	–	1.0	V
Output current in off state (V_O = 6 V)	I_O	–	–	10	μA
Output load capacitance	C_L	–	–	30	pF
Output fall time Note 2	t_f	–	–	200	ns
Delay time Note 3	t_d	0	–	250	ns
CRS (pin 11)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time | Note 2	t_r	–	–	1	μs
Output fall time | Note 2	t_f	–	–	1	μs

		min.	typ.	max.	
LOSE (pin 13)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	30	pF
Output rise time | Note 2	t_r	–	–	50	ns
Output fall time | Note 2	t_f	–	–	50	ns
Delay time (measured from F1 falling edge) Note 3	t_d	0	–	250	ns
DEW (pin 14)					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	VDD	V
Output load capacitance	C_L	–	–	42	pF
Output rise time | Note 2	t_r	–	–	200	ns
Output fall time | Note 2	t_f	–	–	200	ns
Delay time (measured from falling edge of $\overline{CBB}$) Note 3	t_d	7.5		8.5	μs
A0,A1,A2 (pins 19, 20 and 21) 3-state					
Output voltage; LOW (I_{OL} = 100 μA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	85	pF
Output rise time | Note 2	t_r	–	–	1	μs
Output fall time | Note 2	t_f	–	–	1	μs
Delay time (measured from falling edge of $\overline{CBB}$) Note 3	t_d	–	–	10	μs
Leakage current in 'off' state (V_O = 5.5 V)	I_{IR}	–	–	10	μA
High impedance switching time					
Into high impedance state		0	–	0.9	μs
From high impedance state		1	–	2.9	μs
A3,A4 (pin 22 and 23) 3-state					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V
All other parameters are as for A_0 to A_2					
RACK (pin 24) 3-state					
Output voltage; LOW (I_{OL} = 1.6 mA)	V_{OL}	0	–	0.4	V
Output voltage; HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	–	V_{DD}	V
Output load capacitance	C_L	–	–	40	pF
Output rise time | Note 2	t_r	–	–	60	ns
Output fall time | Note 2	t_f	–	–	300	ns
Delay time (measured from dalling edge of F1) Note 3	t_d	150	–	280	ns
Leakage current in 'off' state (V_O = 5.5 V)	I_{IR}	–	–	10	μA
High impedance switching time					
Into high impedance state		1	–	2.9	μs
From high impedance state		0	–	0.9	μs

CHARACTERISTICS (continued)

Notes

1. This input incorporates an internal clamping diode, nominal $V_{IL(min)} = -0.5$ V.

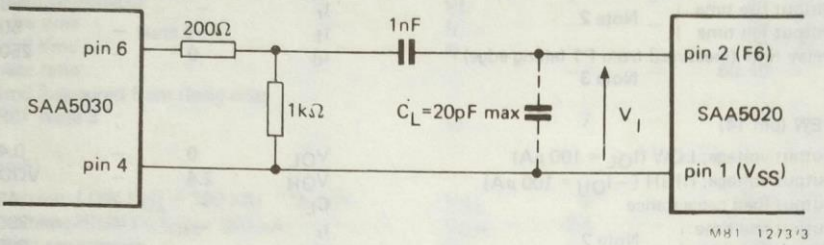

Fig.3 Capacitive coupling network for F6

2. Rise and fall times are measured between the 0.8 V and 2.0 V levels unless otherwise stated.
3. All delay times are measured from the rising edge of F1 unless otherwise stated.
   All delay times are measured at the 1.5 V level on the input to either the 2.0 V level on the rising edge of the output of the 0.8 V level on the falling edge of the output.
4. I_{OL} may be increased to 1 mA if load capacitance is less than 10 pF.
5. I_{OL} may be increased to 1.6 mA. Delay time will be increased to 350 ns max.

APPLICATION DATA

The function is quoted against the corresponding pin number.

For details of output waveforms see Fig.5

Pin No.

1. V_{SS} Ground – 0 V.
2. **F6**

   This input is the 6 MHz master clock signal and is used to derive the basic timings for the teletext display. It contains an internal diode clamp.
3. **TR6**

   This output is the 6 MHz character dot rate clock signal for the SAA5050 Teletext Character Generator.
4. **F1**

   This output is a 1 MHz character repetition rate clock signal for the SAA5040 Teletext Acquisition and Control device and the SAA5050 Teletext Character Generator.
   This output is synchronous with TR6, with a positive-going edge occuring at time zero of the line.
5. **$\overline{\text{AHS}}$ After hours sync**

   This output signal is an internally generated TV compound sync signal which may be used to synchronise the display (Fig.4).
6. **FLR Fast line reset**

   This input from the SAA5030 Video Processor is used to reset the internal TV line rate counter. It is a positive-going pulse of approximately 4.6 μs duration, and occurs during initial set-up of the phase-locked system.

7. $\overline{\text{GLR}}$ **General line reset**

This output is a TV line frequency signal used for reset and clock functions in the SAA5040 Teletext Acquisition and Control device, and the SAA5050 Teletext Character Generator. It is a 1 μs negative-going pulse commencing 5 μs from the start of each line.

8. $\overline{\text{PL}}$ **Phase lock**

This line frequency output signal to the SAA5030 Video Processor is used to phase lock the 6 MHz display system clock to the incoming television video signal. It is a 4 μs negative-going pulse commencing at 62 μs into line.

9. $\overline{\text{CBB}}$ **Colour burst blanking**

This output signal is used to reset internal data processing and sync circuits within the SAA5030 Video Processor. It is an 8 μs negative-going pulse starting at time zero of the line.

10. **FS Field sync**

This input signal from the SAA5030 Video Processor is used to reset the field rate counter, to maintain correct field sync with incoming video.

11. **CRS Character rounding select**

This output signal to the SAA5050 Teletext Character Generator is required for correct character rounding of small characters within the character generator. The output is HIGH for even fields (0-313 lines) and LOW for odd fields (314-625 lines).

12. V_{DD} **+ 5 V Supply**

This is the power supply input to the circuit.

13. **LOSE Load output shift register enable**

This output signal to the SAA5050 Teletext Character Generator is used to reset internal control character flip-flops prior to the start of each display line. This signal also defines the character display period. It is a positive-going pulse of duration 40 μs after the start of the line and occurs on lines 49 to 288 and 362 to 601 only.

14. **DEW Data entry window**

This output defines the period during which data may be extracted from the incoming television signal and written into the page memory. This signal is required by the SAA5040 Teletext Acquisition and Control device and the SAA5050 Teletext Character Generator. This is a positive-going pulse commencing at the end of line 5 and finishing at end of line 22 and similarly for lines 318 and 335.

15. $\overline{\text{TLC}}$ **Transmitted large character**

This input from the SAA5050 Teletext Character Generator is to enable the correct display of large characters under broadcast control. It is HIGH for normal character display and must be taken LOW for large character display.

16. **HIE High impedance enable**

This input when taken HIGH will switch the address and address clock (RACK) outputs to their high impedance state. For normal teletext operation this input should be connected to the DEW output (pin 14).

APPLICATION DATA (continued)

17. **$\overline{\text{BCS}}$ Big character select**

This input from the SAA5040 Teletext Acquisition and Control circuit is used to enable the correct display of large characters. It must be HIGH for normal character display and taken LOW for large character display.

18. **$\overline{\text{T}}$/B Top or bottom select**

This input from the SAA5040 Teletext Acquisition and Control device controls the RAM row address logic for correct operation of page display when large character display has been selected under user control. It must be LOW for the top half to be displayed, and HIGH for the bottom half.

19, 20
21, 22
23 **A0 to A4 Memory addresses**

These 3-state outputs to the teletext memory provide the RAM row addresses during the display period (i.e. TV lines 49 to 288 - 362 to 601 inclusive). These outputs switch to the high impedance state when HIE (pin 16) is taken HIGH. All address outputs are LOW during line 40.
During display period the outputs provide a binary count sequence which is increased every ten lines in small character mode and every twenty lines in large character mode. If any row contains transmitted large characters the address is incremented by two after 20 lines.

24. **RACK Read address clock**

This 3-state output is a 1 MHz clock occuring during the display period of the line only. This output is used to clock the external RAM address counter during the display period. The output will switch to the high impedance state when HIE (pin 16) is taken HIGH. The clock starts with a positive edge 14.65 μs from the start of a line and finishes with a negative-going edge at 53.15 μs.

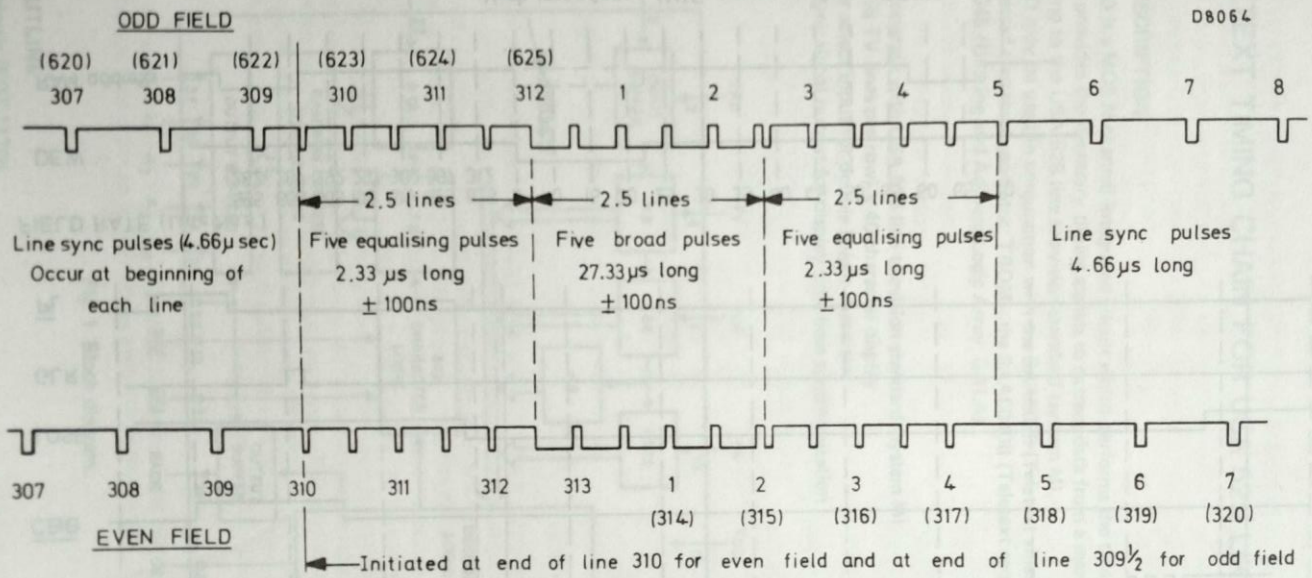

Fig.4 After hours sync waveforms ($\overline{AHS}$)

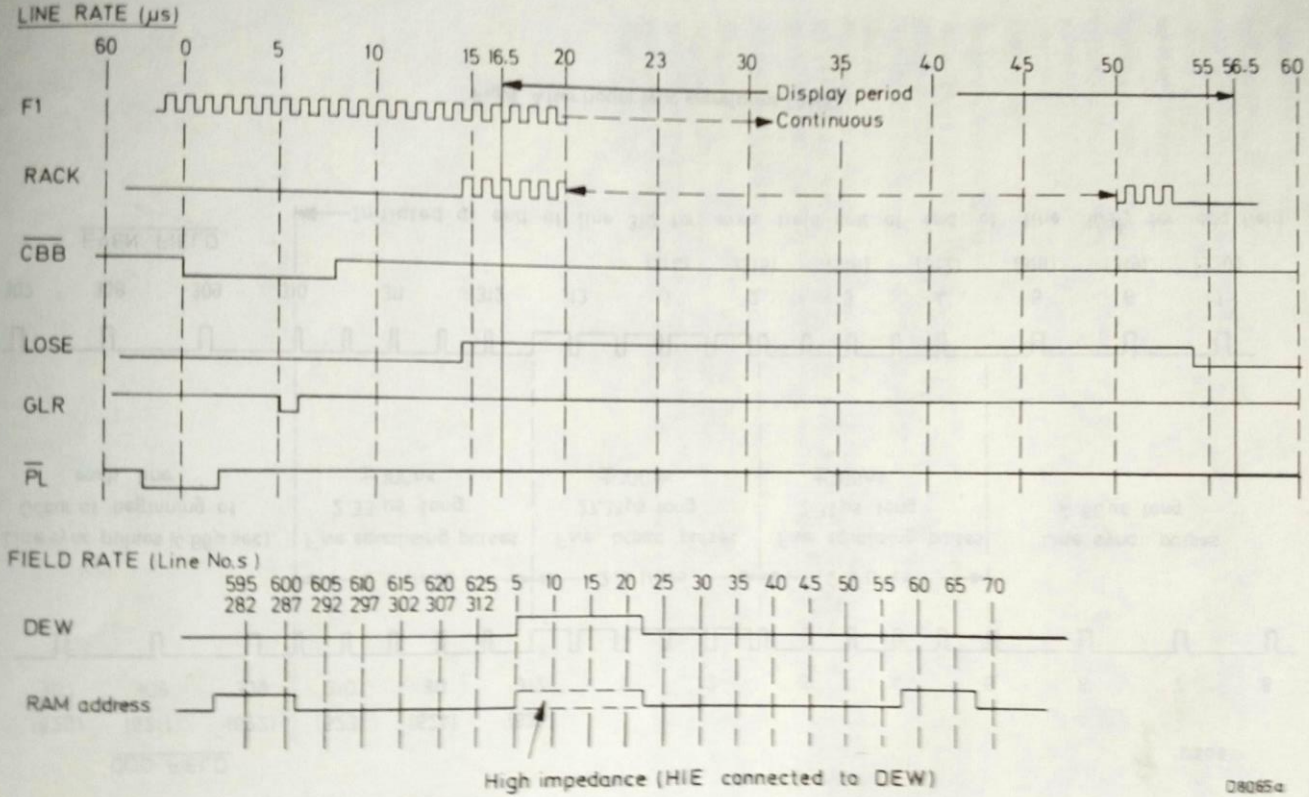

Fig.5 SAA5020 Output waveforms