Design and Implementation of 2 input NAND gate using CMOS

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Abstract

In this paper, I am going to Design and Implement 2 input NAND gate using CMOS Technology and I will also implement it using 28nm technology. NAND gate is a universal logic gate that gives output low only when all inputs are high. Here we will be implementing 2 input NAND gate which will give single output based on inputs. We can verify the output using Circuit Wave forms. This complete design and implementation are done using VLSI technology which has features such as high speed, low cost and small size.

1 Reference Circuit Details

NAND gate is a universal logic gate. The output of NAND gate is low only when all inputs are high. Here we will be implementing a 2 input NAND gate which will have inputs A and B and single output Y. The equation for this circuit will be $\overline{A.B}$. The output Y will be low only when input A and B both are high. In other three combinations of inputs, the output Y will be high (Fig 1). The circuit will consist of 2 PMOS and 2 NMOS (Fig 2). Each PMOS will be connected to one input and both PMOS will be connected in parallel. Both the NMOS will be connected in series with the PMOS circuit. Gates of each NMOS will be connected to one of the inputs. Output can be obtained at the junction of PMOS and NMOS circuits.

We will implement the circuit using 28nm technology. In the circuit waveform (Fig 3) we can verify the above circuit.

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Fig (1) Truth table for NAND gate

2 Reference Circuit

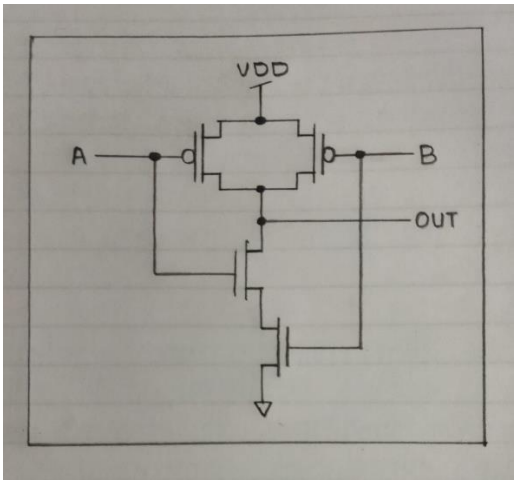

Fig (2). Reference Circuit of NAND gate using CMOS

3 Reference circuit waveform

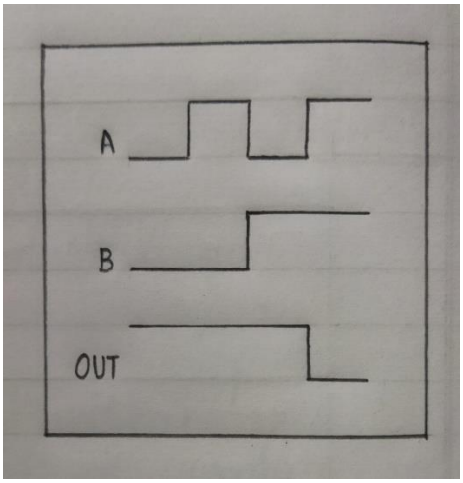

Fig (3) Reference waveform for NAND gate

References

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