

# DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING



(Autonomous College Affiliated to the University of Mumbai) NAAC Accredited with "A" Grade (CGPA: 3.18)

Academic Year: 2022-2023

Name:	Prerna Sunil Jadhav
Sap Id:	60004220127
Class:	T. Y. B.Tech (Computer Engineering)
Course:	Processor Organization and Architecture (POA)
Course Code:	DJ19CEL502
Experiment No.:	05

AIM: Assembly program for 16-bit addition/subtraction using direct, Immediate & register

addressing mode.

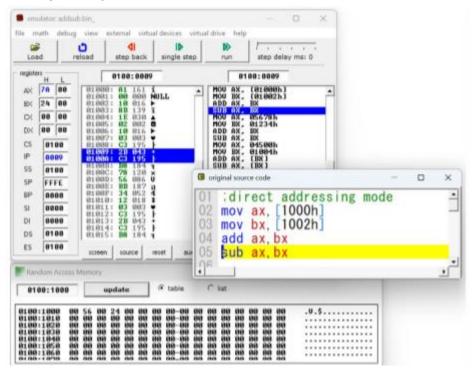
### ADDITION:

### CODE:

org 1000h mov ax,[1000h] mov bx,[1002h] add ax,bx mov ax,1234h mov bx,0005h add ax,bx mov ax,1234h mov bx,1000h add ax,[bx]

## **OUTPUT**:

### ADDITION-DIRECT:





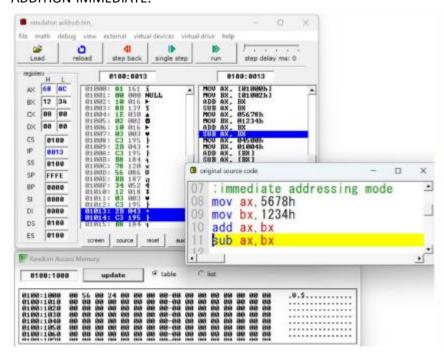
# DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING



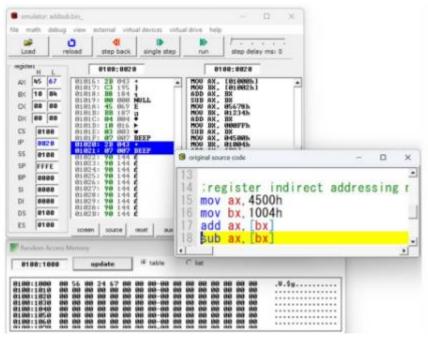


Academic Year: 2022-2023

#### **ADDITION-IMMEDIATE:**



### ADDITION-REGISTER INDIRECT





# DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING



(Autonomous College Affiliated to the University of Mumbai) NAAC Accredited with "A" Grade (CGPA: 3.18)

Academic Year: 2022-2023

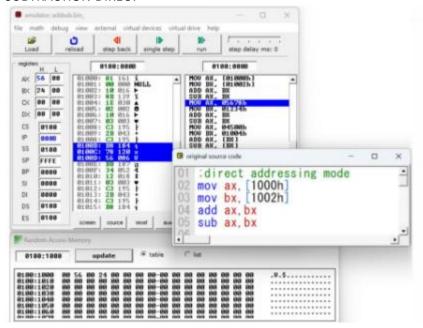
### SUBTRACTION:

### CODE:

org 1000h mov ax,[1000h] mov bx,[1002h] sub ax,bx mov ax,1234h mov bx,0005h sub ax,bx mov ax,1234h mov bx,1000h sub ax,[bx]

#### **OUTPUT:**

### SUBTRACTION-DIRECT





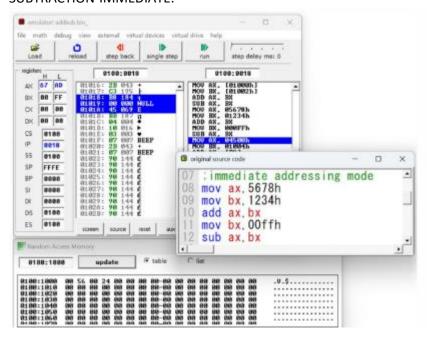
## DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING





Academic Year: 2022-2023

#### SUBTRACTION-IMMEDIATE:



#### SUBTRACTION-REGISTER INDIRECT:

