

NAME: PRERNA SUNIL JADHAV
SAPID: 60004220127
BRANCH: COMPUTER ENGINEERING

COURSE CODE: DJ19CEC805

COURSE: DIGITAL ELECTRONICS

TERMWORK ASSIGNMENT

(Q1) convert and present $(45)_{10}$ in hexadecimal, binary and octal.

Soln:

To convert $(45)_{10}$ to Binary divide 45 by 2 as binary has base 2 until quotient is 0
Quotient Remainder

<u>45</u>	22	10	
<u>22</u>	11	0	
<u>11</u>	5	1	
<u>5</u>	2	1	
<u>2</u>	1	0	
<u>1</u>	0	1	

$$\therefore (45)_{10} = (101101)_2$$

To convert into octal,

$$(45)_{10} = \underline{\underline{(101101)}_2} = (55)_8$$

↓ ↓
5 5

To convert into Hexadecimal,

$$(45)_{10} = \underline{\underline{(101101)}_2} = (2D)_{16}$$

↓ ↓
2 D

Q2

b) Perform following operation using 2's complement:
 $(86)_{10} - (22)_{10}$

Soln:

converting $(86)_{10}$ and $(22)_{10}$ into binary

Quotient	Remainder	Quotient	Remainder
$\frac{86}{2}$	43	0	↑
$\frac{43}{2}$	21	1	↑
$\frac{21}{2}$	10	1	↑
$\frac{10}{2}$	5	0	↑
$\frac{5}{2}$	2	1	↑
$\frac{2}{2}$	1	0	↑
$\frac{0}{2}$	0	1	

$$\therefore (86)_{10} = (1010110)_2$$

$$\therefore (22)_{10} = (10110)_2$$

Now,

Performing 2's complement of $(0010110)_2$

1's complement $\rightarrow 1101001$

2's complement $\rightarrow 1101010$

Now, performing subtraction using 2's complement

$$\therefore (86)_{10} = (1010110)_2$$

$$\therefore (22)_{10} = (10110)_2 \rightarrow 2\text{'s complement} = (1101010)_2$$

$$(+) \quad \begin{array}{r} 1101010 \\ \hline \end{array}$$

$$\text{carry} \rightarrow \boxed{1} \quad \begin{array}{r} 1000000 \\ \hline \end{array}$$

Here, carry generated is 1, which indicates that the answer is positive and need to ignore it.

$$\therefore (1000000)_2 = (64)_{10}$$

$$\therefore (86)_{10} - (22)_{10} = (64)_{10} = (1000000)_2$$

Q3

b) short note on HAMMING code.

Soln: Hamming code is a block code that is capable of detecting up to two simultaneous bit error and correcting single bit errors. It was developed by R.W. Hamming for error correction. In this coding method, the source encodes the messages by inserting redundant bits within the message. These redundant bits are extra bits that are generated & inserted at a specific positions in the message itself to enable error detection and correction. When the destination receives the message, it performs recalculations to detect errors and find the bit position that has error.

Encoding a message by Hamming code

Step 1: Calculating the number of redundant bit

Step 2: Getting Positioning the redundant bits -

Placed at bit positions of powers of 2
i.e., r_0, r_1, r_2, r_3, r_4 etc.

Step 3: Calculating the value of each redundant bit

These bits are parity bits, which are the extra bits that makes the no. of 1's either even or odd. There are two types of parity -

1) Even parity : Here, the total no. of bits in the message is made even

2) Odd parity : Here, the total no. of bits in the message is made odd.

Decoding a message in Hamming code, here receiver performs recalculations to detect, errors and correct them. Steps are -

Step 1: calculation of the no. of redundant bits
 $2^r \geq m + r + 1$, where $m = \text{no. of data bits}$,
 $r = \text{no. of redundant bits}$.

Step 2: Positioning the redundant bits

The r redundant bits placed at bit position of powers of 2, i.e., 1, 2, 4, 8, 16 etc

Step 3: Parity checking

Parity bits are calculated based upon the data bits & the redundant bits using the same rule as during generation. Thus,

$$C_1 = \text{Parity } (1, 3, 5, 7, 9, 11 \text{ and so on})$$

$$C_2 = \text{Parity } (2, 3, 6, 7, 10, 11 \text{ and so on})$$

$$C_3 = \text{Parity } (4-7, 12-15, 20-23 \text{ and so on})$$

Step 4: Error Detection and correction

The decimal equivalent of parity bits binary values is calculated. If it is 0, there is no error. Otherwise, the decimal value gives the bit position which has error. For example, if $C_1 C_2 C_3 C_4 = 1001$, it implies that the data bit at position 9, decimal equivalent of 1001, has error. The bit is flipped to get the correct message.

Ex: Assuming even parity state, received code is

P_1	D_6	D_5	P_4	D_3	P_2	P_1
1	0	1	1	0	1	1

$$\left\{ \begin{array}{l} P_4: D_5 \ D_6 \ D_7 \\ 1 \quad 1 \quad 0 \quad 1 \end{array} \right. \rightarrow \text{odd}$$

$P_4 = 1$

$$\left[\begin{array}{cccc} P_2 & P_3 & D_6 & D_7 \\ 1 & 0 & 0 & 1 \end{array} \right]$$

$P_2 = 0$

$$\left[\begin{array}{cccc} P_1 & P_3 & D_5 & S_7 \\ 1 & 0 & 1 & 1 \end{array} \right]$$

$$P_1 = 1$$

$$\therefore P_4 \ P_2 \ P_1 = (101)_2 = 5_{10}$$

5th bit has error

$$\therefore (1001011)_2 \text{ is correct}$$

Q4

b)

- i) Minimize and Implement following POS using universal gates.

$$Y = (A+B)(A+C)(B+C)$$

Soln: $Y = (A+B)(A+C)(B+C)$

$$Y = (AA + AB + AC + BC)(B+C)$$

$$Y = AAB + ABB + ABC + BBC + AAC + ABC + ABC + BBC$$

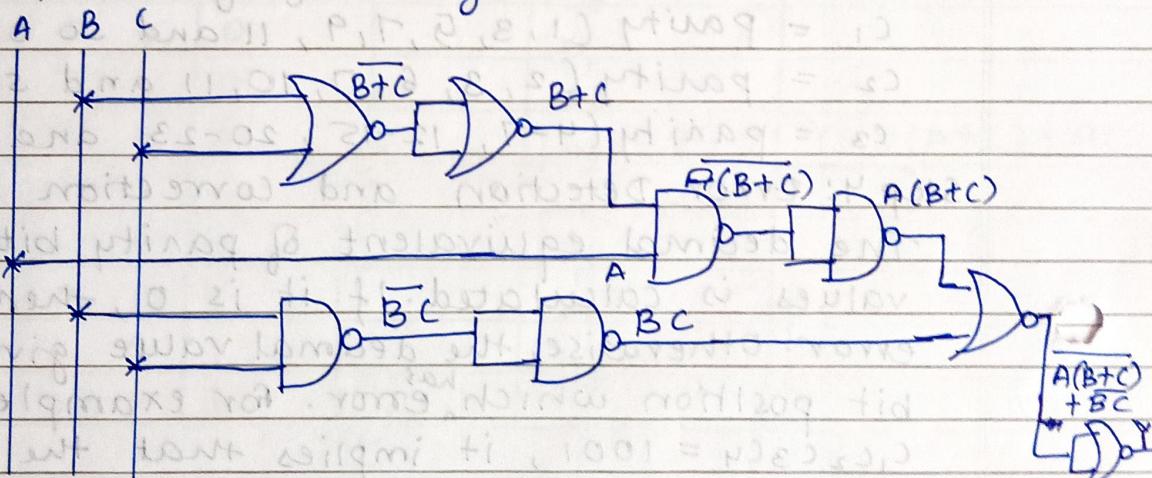
$$Y = AB + ABC + BC + AC \quad [\because A \cdot A = A] \quad [\because A + A = A]$$

$$Y = AB(1+C) + BC + AC$$

$$Y = AB + BC + AC \quad [\because 1+A=1]$$

$$Y = A(B+C) + BC$$

Implementation using Universal Gates:



2) Minimize and implement following POS using multiplexer

$$Y = (A+B)(A+C)(B+C)$$

Soln: $Y = (A+B)(A+C)(B+C)$

$$Y = AAB + ABB + ABC + BBC + AAC + ABC + ABC + BCC$$

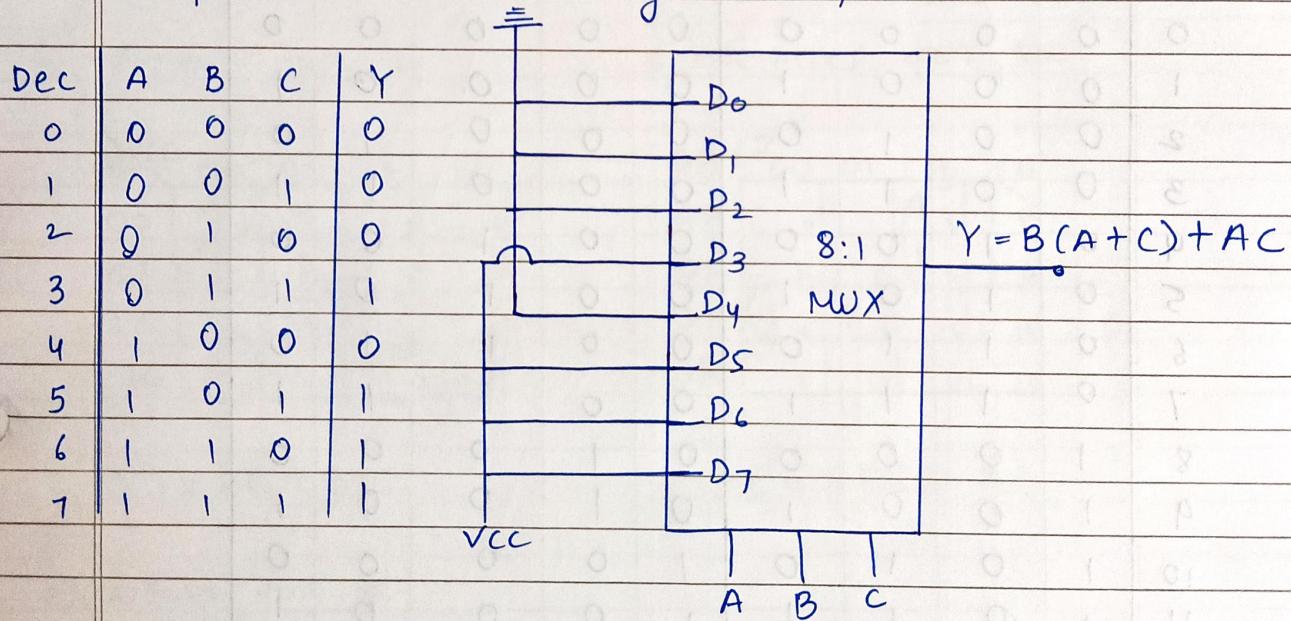
$$Y = AB + ABC + BC + AC$$

$$Y = AB(1+C) + BC + AC$$

$$Y = AB + BC + AC$$

$$Y = B(A+C) + AC$$

Implementation using Multiplexer



Q5

b)

1. Implement binary to BCD code converter using gates.

Soln: the input is a 4-bit binary code (A B C D) so 16 (2^4) combination are possible. Hence the output should have 8 bit, but first three bits will all be 0 for all combinations of inputs, the output can be treated as 5-bit BCD code (W X Y Z E).

Truth Table.

Dec	Binary				BCD				
	A	B	C	D	W	X	Y	Z	E
0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	1
2	0	0	1	0	0	0	0	1	0
3	0	0	1	1	0	0	0	1	1
4	0	1	0	0	0	0	1	0	0
5	0	1	0	1	0	0	1	0	1
6	0	1	1	0	0	0	1	1	0
7	0	1	1	1	0	0	1	1	1
8	1	0	0	0	0	1	0	0	0
9	1	0	0	1	0	1	0	0	1
10	1	0	1	0	1	0	0	0	0
11	1	0	1	1	1	0	0	0	1
12	1	1	0	0	1	0	0	1	0
13	1	1	0	1	1	0	0	1	1
14	1	1	1	0	1	0	1	0	0
15	1	1	1	1	1	0	1	0	1

Drawing of K-Map for each output

Two nodes not overlapping position

a) K-Map for W

AB\CD	00	01	11	10
00	0 ₀	0 ₁	0 ₃	0 ₂
01	0 ₄	0 ₅	0 ₇	0 ₆
11	1 ₁₂	1 ₁₃	1 ₁₅	1 ₁₄
10	0 ₈	0 ₉	1 ₁₁	1 ₁₀

$$\therefore W = AB + AC$$

b) K-Map for X

AB\CD	00	01	11	10
00	0 ₀	0 ₁	0 ₃	0 ₂
01	0 ₄	0 ₅	0 ₇	0 ₆
11	0 ₁₂	0 ₁₃	0 ₁₅	0 ₁₄
10	1 ₈	1 ₉	0 ₁₁	0 ₁₀

$$\therefore X = A\bar{B}\bar{C}$$

c) K-Map for Y

AB\CD	00	01	11	10
00	0 ₀	0 ₁	0 ₃	0 ₂
01	1 ₄	1 ₅	1 ₇	1 ₆
11	0 ₁₂	0 ₁₃	1 ₁₅	1 ₁₄
10	0 ₈	0 ₉	0 ₁₁	0 ₁₀

$$\therefore Y = \bar{A}B + BC$$

d) K-Map for Z

AB\CD	00	01	11	10
00	0	1	1 ₃	1 ₂
01	4	5	1 ₇	1 ₆
11	1 ₁₂	1 ₁₃	1 ₁₅	1 ₁₄
10	8	9	11	10

$$\therefore Z = ABC + \bar{A}C$$

e) K-Map for E

AB\CD	00	01	11	10
00	0	1 ₁	1 ₃	2
01	4	5	1 ₇	C
11	12	13	15	14
10	8	9	11	10

$$E = D$$

Minimized Expression for each output

$$W = AB + AC \quad (P)$$

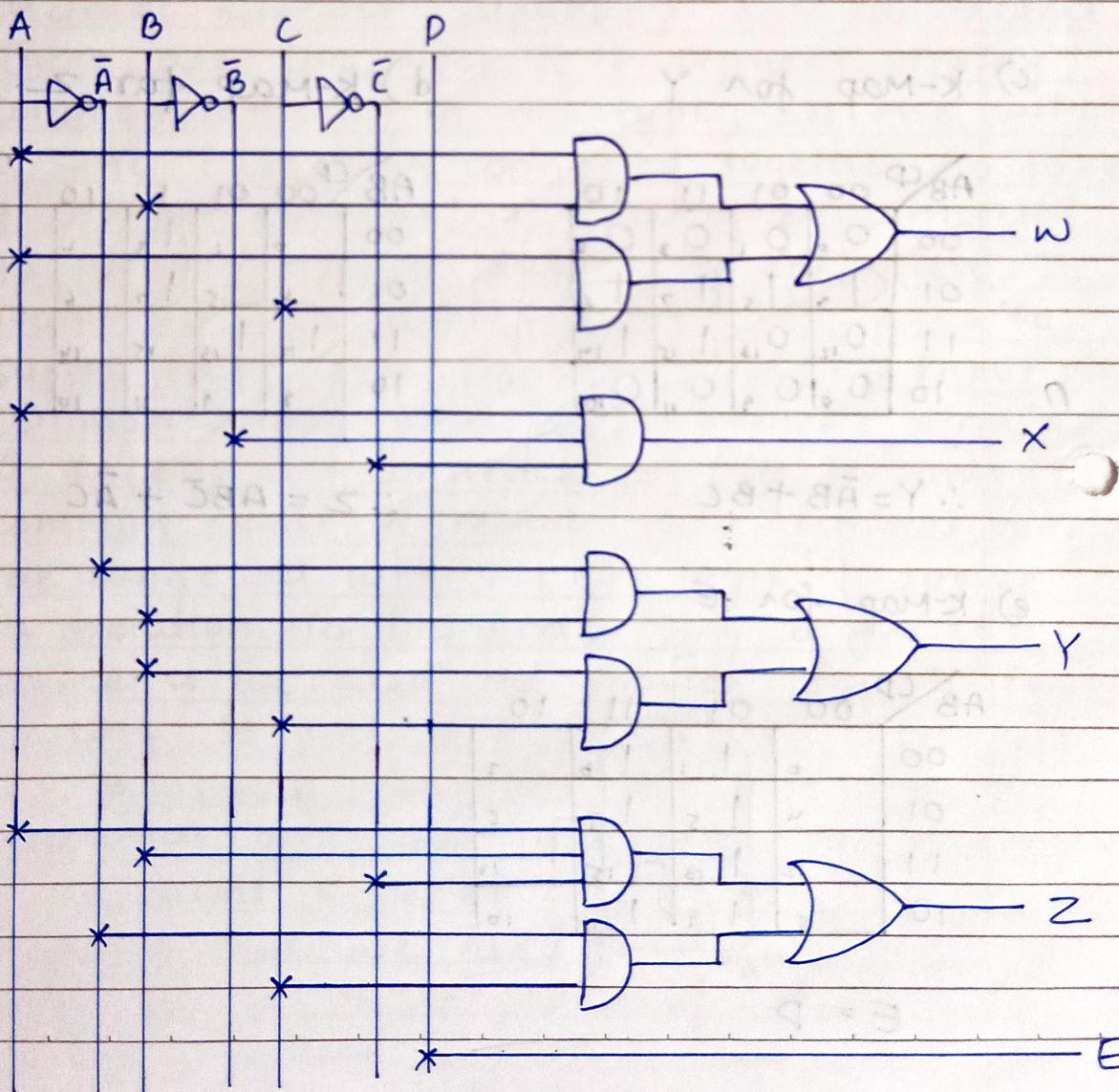
$$X = A\bar{B}\bar{C}$$

$$Y = \bar{A}B + BC \quad (Q)$$

$$Z = ABC\bar{C} + \bar{A}\bar{C} \quad (R)$$

$$E = D \quad (S)$$

Logic circuit Diagram (Binary to BCD code converter)



Q5

b)

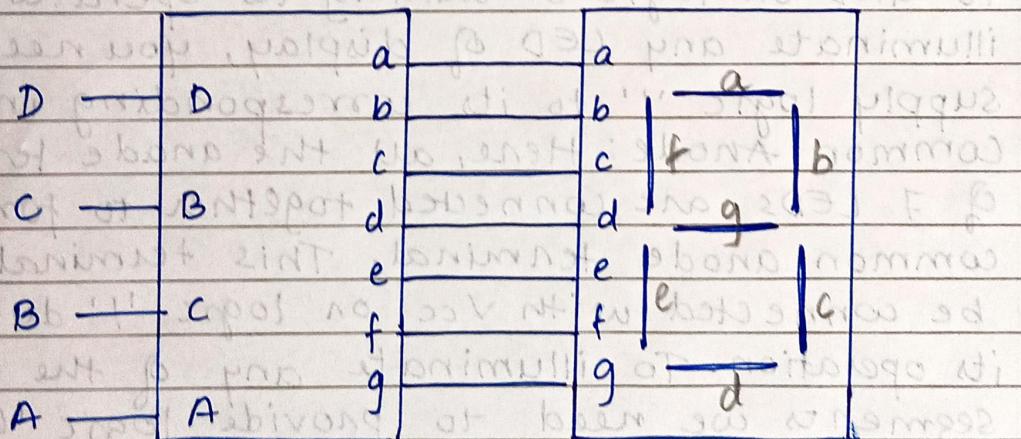
2) Short note on BCD to 7 segment display converter (single stage)

Soln: → BCD to 7-segment display decoder is a special decoder which can convert binary coded decimal into another form which can be easily displayed through a 7-segment display. 7 segment display is a digital device that can be used for displaying decimal number, alphabets and characters. There are two types of 7-segment display

- Common Cathode: In this type, all the cathodes of the 7 LEDs are connected together to form a common terminal. It should be connected to GND or logic '0' during its operation. To illuminate any LED of display, you need to supply logic '1' to its corresponding input pin.
- Common Anode: Here, all the anode terminals of 7 LEDs are connected together to form common anode terminal. This terminal should be connected with Vcc or logic '1' during its operation. To illuminate any of the LED segments we need to provide logic '0' to it.
- Working: It has 7 pins, "a", "b", "c", "d", "e", "f", "g" which illuminate the according to what we want to display. For example if we want 0 to be displayed then we need to turn on "a", "b", "c", "d", "e", "f", & turn off "g".

Truth table.

INPUT				OUTPUT							
Désp	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	1	1	1	1	1	0
1	0	1	0	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0	1
3	0	0	0	1	0	1	0	1	0	0	1
4	0	1	0	0	0	0	1	0	0	0	1
5	0	1	0	1	0	0	1	0	0	0	1
6	0	1	1	0	0	0	0	0	0	0	1
7	0	1	1	1	1	1	1	1	0	0	0
8	1	0	0	0	0	1	1	1	1	0	0
9	1	0	0	0	1	1	0	1	1	1	1



BCD to seven segment decoder for 7 segment LED display