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DIGITAL ELECTRONICS
Experiment No.: 07

AIM:

Study of Flip Flops using ICs

APPARATUS REQUIRED:

- Breadboard
- Connecting Wires
- Resistors
- LEDs
- Power Supply (DC)
- IC 7473 for T FLIP FLOP
- IC 7474 for D FLIP FLOP
- IC 7476 for JK FLIP FLOP
- IC 7400 for RS FLIP FLOP

THEORY:

A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying input.

RS Flip Flop:

The basic NAND gate RS flip flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs. The RS flip flop actually has three inputs, SET, RESET and its current output Q relating to its current state.

D Flip Flop:

A D flip flop has a single data input. This type of flip flop is obtained from the SR flip flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop.

- **J-K Flip Flop:**

In a RS flip-flop the input R=S=1 leads to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also the outputs are complemented of each other. This would lead to creation of a J-K flip flop.

- **T Flip Flop**:

T flip-flop is known as toggle flip-flop. The T flip-flop is modification of the J-K flip-flop. Both the JK inputs of the JK flip – flop are held at logic 1 and the clock signal continuous to change.

Procedure:

1. Assemble the circuits one after the other on the breadboard as per the circuit diagrams. The breadboard should also be grounded and connected to a power supply.
2. The ICs are to be connected properly to a power supply and ground following the schematics for the ICs.
3. Input combinations should be provided using the connecting wires by connecting to ground for a LOW value and power for HIGH value to be given to the IC input.
4. Turn on power of the experimental circuit.
5. For each input combination, the logic state of the normal and complementary outputs as indicated by the LEDs(ON=1;OFF=0),the results have to be recorded in a table.
6. Compare results with the characteristic tables.
7. When the experiment is successfully undertaken, the experimental circuits are to be shut down.

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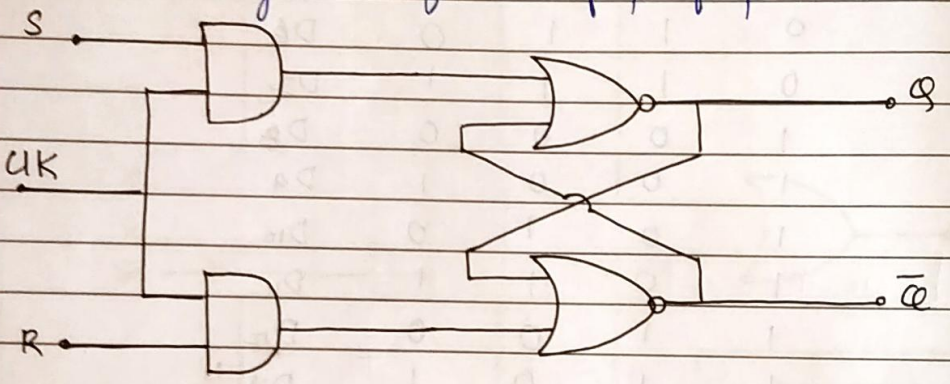
* Circuit Diagram of SR flip flop:



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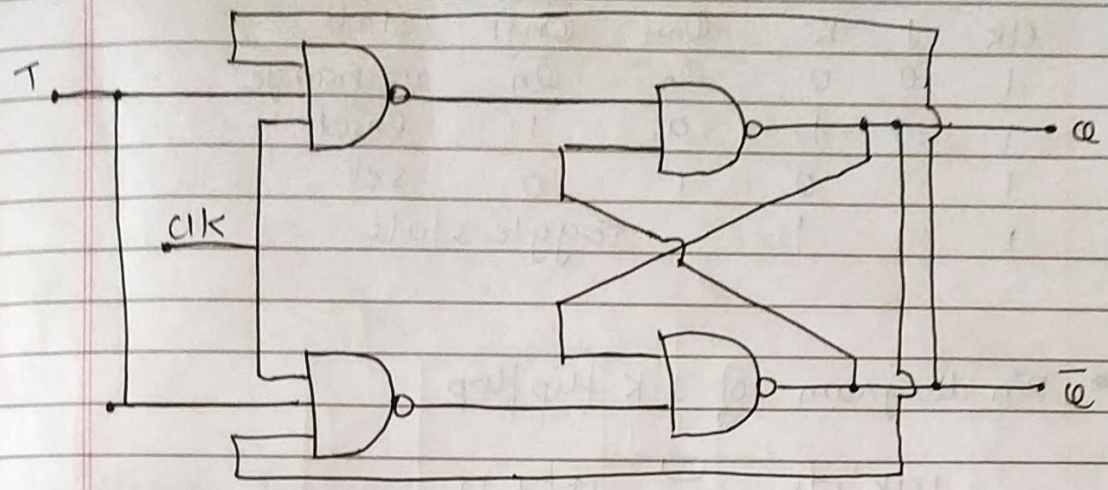
* Truth table:

Clock	S	R	Qn+1	State
0	X	X	Qn	X
1	0	0	Qn	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	X	Invalid state

So, when clk is high and if 'R' is on then state will reset & if set is high then state will be set but if both set & reset are high then it will cause an invalid state.

Circuit Diagram of T-flip flop



Truth table of T flip flop

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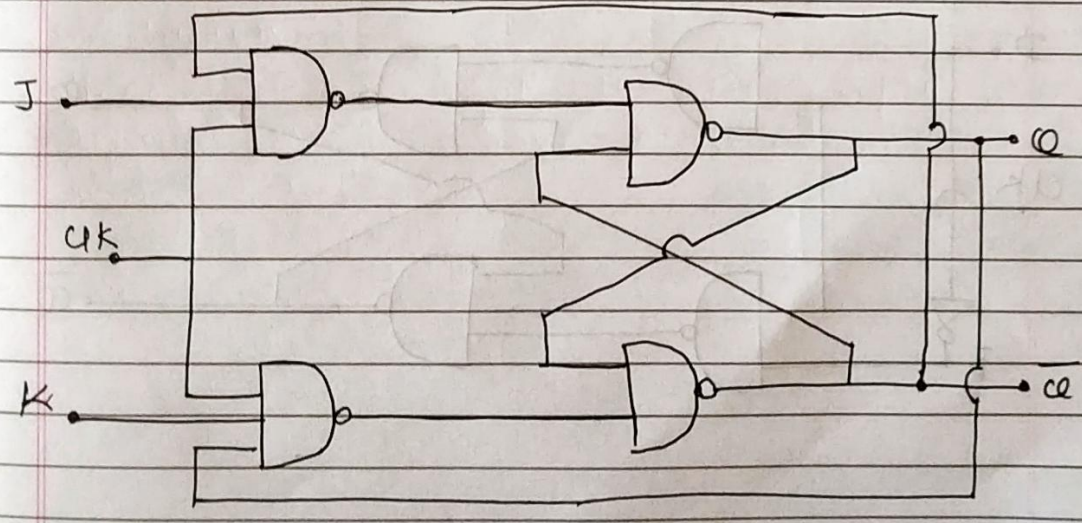
Clk	T	Q_{n+1}	$\overline{Q_{n+1}}$	
0	x	x	x	
1	0	Q_n	$\overline{Q_n}$	} Toggle condition
1	1	$\overline{Q_n}$	Q_n	

Circuit Diagram of J-K flip flop



* Truth Table of J-K flip flop

Clk	J	K	Q_{n+1}	$\overline{Q_{n+1}}$	State
1	0	0	Q_n	$\overline{Q_n}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Toggle state		

* Pin diagram of J-K flip flop

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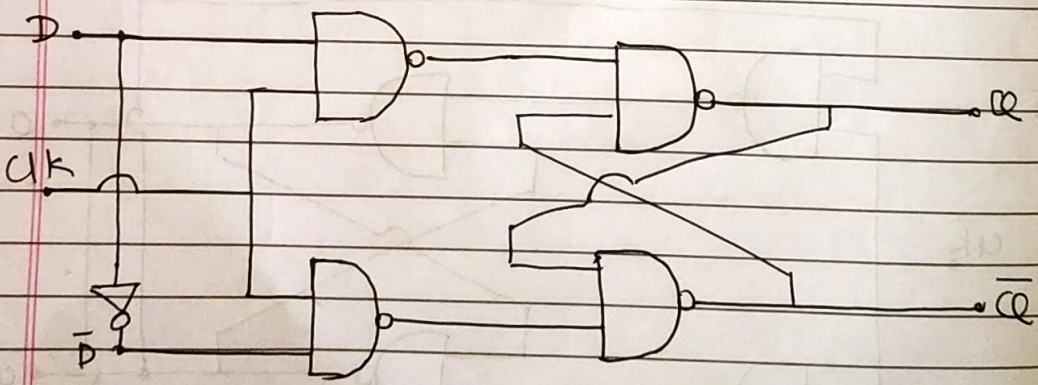
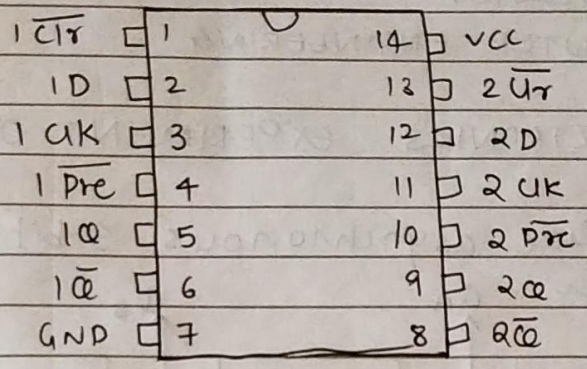
* Circuit Diagram of D flip flop



Pin Diagram

* ~~Truth table~~ for D flip flop



* Truth table for D flip flop

CLK	D	Qn+1
0	X	X
1	0	0
1	1	1

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Conclusion:

Verification of truth table & diagram of RS, J-K, T & D flip flops using nand & not gate ics and analyzation of the circuit of RS, J-K, T, D flip flops with the help of LEDs display is undertaken & the results are noted.