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BRANCH: Computer Engineering
DIGITAL ELECTRONICS
Experiment No.: 08

- **AIM:**

To realize asynchronous 3-bit Up Counter

- **APPARATUS REQUIRED:**

Breadboard, IC 7474(D flip flop), CRO, Function Generator, wires (for connection), LED board, Power Supply.

- **THEORY:**

A Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in UP counter a counter increases count for every rising edge of clock. Not only counting, but a counter can also follow the certain sequence based on our design like any random sequence 0,1,3,2… .They can also be designed with the help of flip flops. They are used as frequency dividers where the frequency of given pulse waveform is divided. Counters are sequential circuit that count the number of pulses can be either in binary code or BCD form. The main properties of a counter are timing, sequencing, and counting. Counter works in two modes: Up counter (An up-counter counts events in increasing order), Down counter (A down-counter counts stuff in the decreasing order)
Counters are broadly divided into two categories:

1) Asynchronous Counter

In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops.It is evident from timing diagram that Q0 is changing as soon as the rising edge of clock pulse is encountered, Q1 is changing when rising edge of Q0 is encountered(because Q0 is like clock pulse for second flip flop) and so on. In this way ripples are generated

through Q0,Q1,Q2,Q3 hence it is also called RIPPLE counter. A ripple counter is a cascaded arrangement of flip flops where the output of one flip flop drives the clock input of the following flip flop .

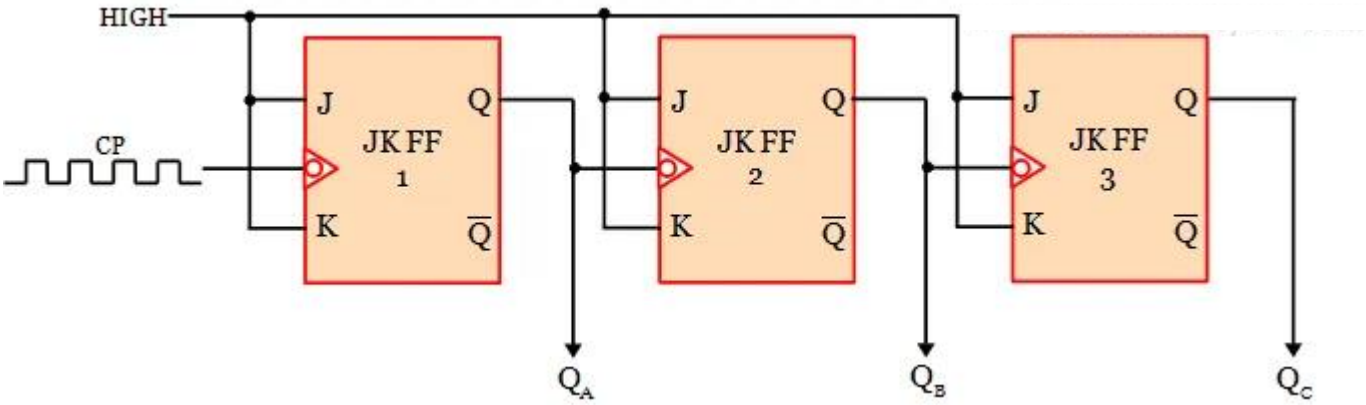
2) Synchronous Counter

Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.

- **3-bit asynchronous up counter**

The 3-bit asynchronous or ripple up counter is similar to the 2-bit ripple up counter. Here for a 3-bit counter, an additional flip-flop is added. Thus, for the 3-bit asynchronous counter, 3 T-flip-flops are used.

This counter consists of 2^3 = 8 count states(000, 001, 010, 011, 100, 101, 110, 111). The counter counts the incoming pulses starting from 0 to 7.



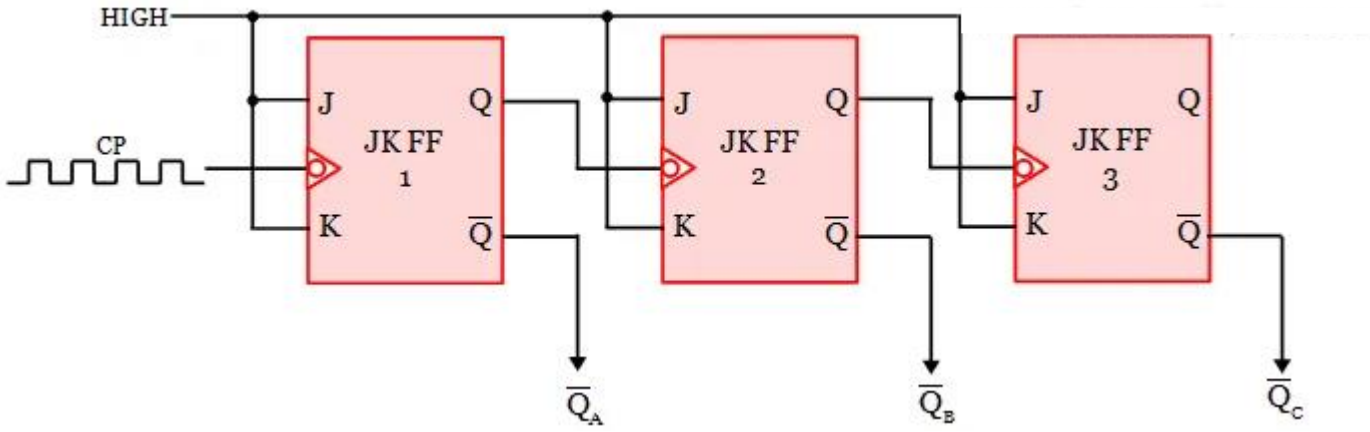
The above circuit shows the circuit diagram of a 3-bit asynchronous up counter, in which the clock pulse is given as clock input for JK FF1. For the other flip-flops, the clock input is fed from the output of previous flip-flops. The clock pulse count is noted at the output of each flip-flop(QCQBQA), where QA is the LSB, and QC is the MSB. The operation is the same as the 2-bit asynchronous up counter. At the falling edge of each clock pulse, the output of JF FF1 toggles. For each logic HIGH output(QA = 1) of JK FF1, at its falling edge, JK FF2 will toggle the output(QB). Similarly, for each logic HIGH output(QB = 1) of JK FF2, JK FF3 will toggle the output(QC).

3-bit asynchronous down counter

The down counter will count the clock pulses from maximum value to zero. In other words, for each clock pulse, the count value is decremented.

The below diagram shows the 3-bit asynchronous down counter. Since it is a 3-bit counter, 3 negative edge-triggered flip-flops are used. The clock pulse input is given only to the first flip-flop. The clock input of the remaining flip-flops is triggered by the Q output of the previous flip-flop.

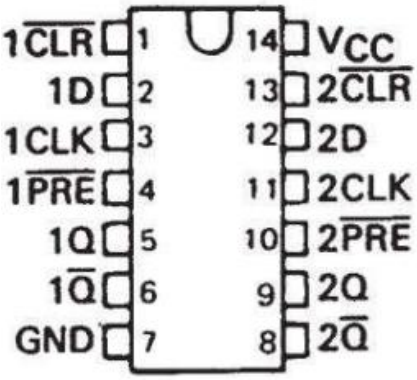
Since it is down counter, the 3-bit count value is measured from the (QC'QB'QA'), where QC' is the MSB and QA' is the LSB.



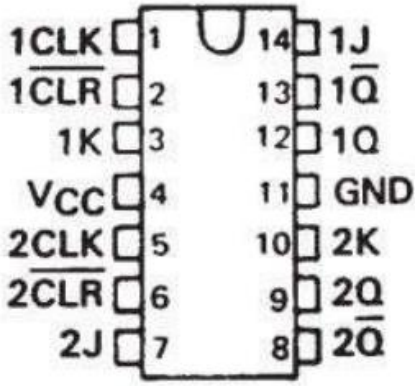
The operation is the same as that of the 3-bit asynchronous up counter. If the output is taken at the normal Q output of each flip flop, then it is an up counter. If the output is taken at the complemented output (Q') of each flip flop, it is said to be the down counter.

PIN Diagram:

D Flip flop



JK Flip flop



Procedure:

In practical's for 3 bit up counter we used rising edge D flip flop.

1) First take the breadboard and connect the 2 IC 7474 (D flip flop) on the breadboard.
2) Connect 1'Q bar' to 2CLK and 2'Q bar' to 1CLK (2nd IC) and connect the 1'Qbar' of 2nd IC in similar fashion.
3) Now Connect 1'Q bar' to 1D (1st IC) and 2'Q bar' to 2D(1st IC) and connect the 1'Qbar' of 2nd IC to 1D(2nd IC).
4) Also give VCC to all the clears(CLR) and preset(PRE) of the flip flops used.
5) Now give clock pulse to 1CLK (1st IC) using the function generator (Also check the frequency of the clock pulse using CRO).
6) Give VCC and GND to pin 14 and pin 7 respectively.
7) Now connect the cathode of consecutive 3 LED from LED board to 1Q (1st IC), 2Q(1st IC), 1Q(2nd IC) respectively this is our output terminals and connect the anode(gnd) to GND.
8) Now turn on the switch of power supply (Give 5V) and the function generator (use square waves having frequency 1hz).
9) Check whether the counter is counting from 0 to 7 and then counting in loop of 0 to 7.

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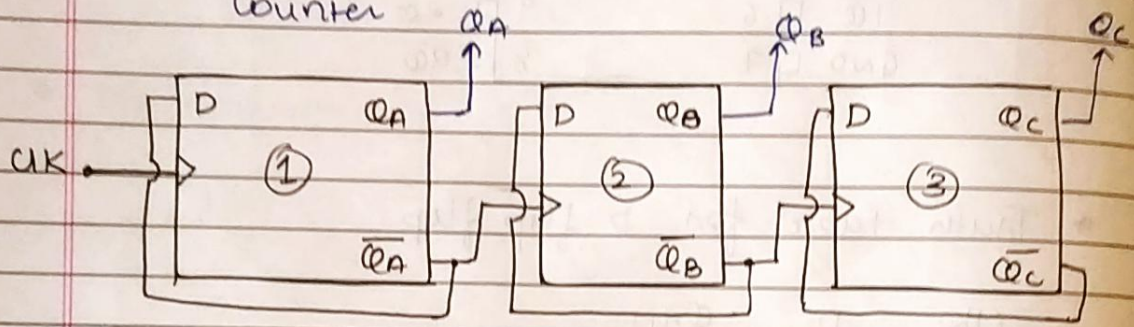

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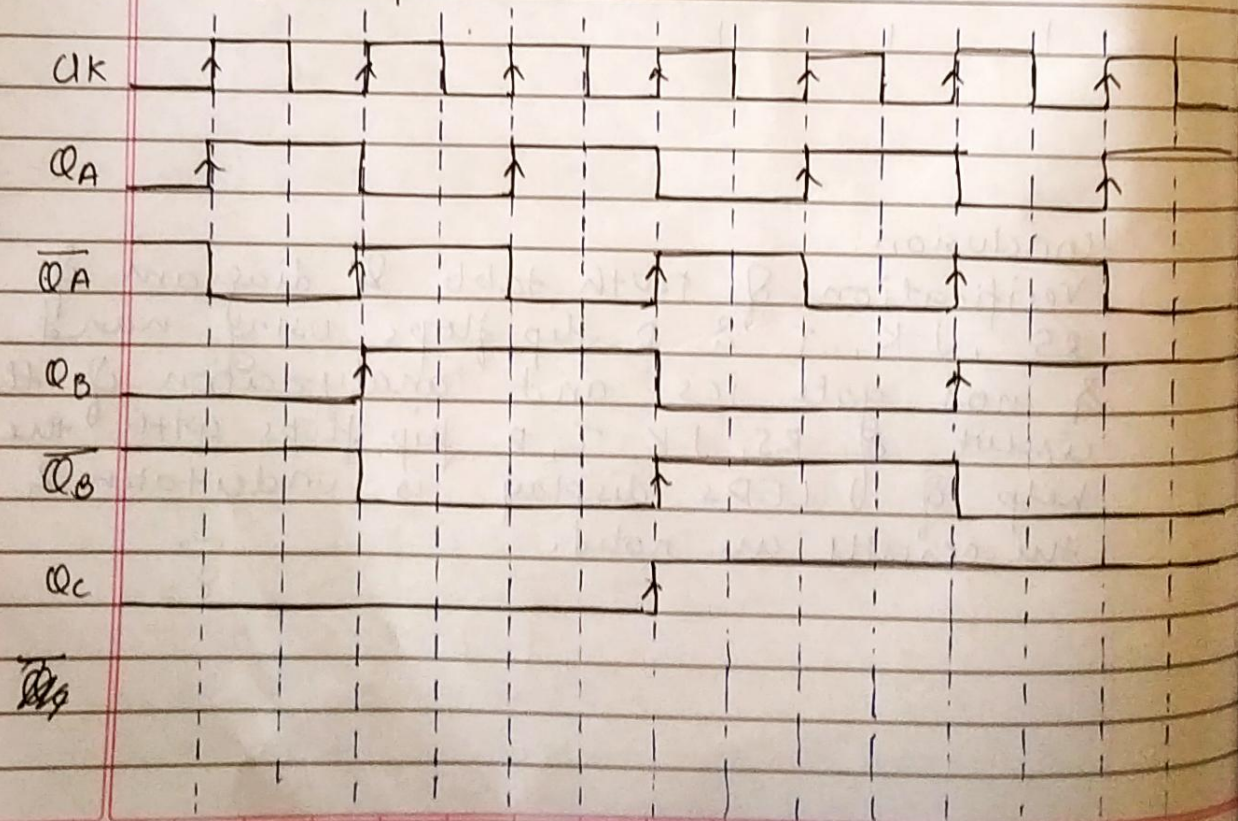
Timing Graph



Truth Table

count	Q_C	Q_B	Q_A	Decimal Output
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7
8	0	0	0	0

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Conclusion:
Thus 3 bit asynchronous up counter was designed & verified.