INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT10Triple 3-input NAND gate

Product specification
File under Integrated Circuits, IC06

December 1990





Triple 3-input NAND gate

74HC/HCT10

FEATURES

· Output capability: standard

I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT10 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT10 provide the 3-input NAND function.

QUICK REFERENCE DATA

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT		
STWIBUL	PARAMETER	CONDITIONS	НС	нст	ONL	
t _{PHL} / t _{PLH}	propagation delay nA, nB, nC to nY	C _L = 15 pF; V _{CC} = 5 V	9	11	ns	
C _I	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	12	14	pF	

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_O)$$
 where:

 f_i = input frequency in MHz

f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

$$\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$$

2. For HC the condition is $V_I = GND$ to V_{CC}

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 V$.

ORDERING INFORMATION

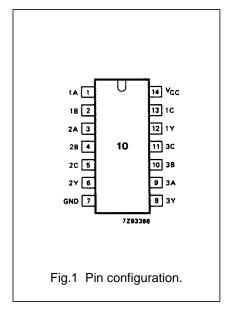
See "74HC/HCT/HCU/HCMOS Logic Package Information".

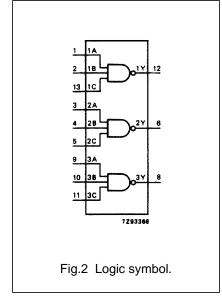
Triple 3-input NAND gate

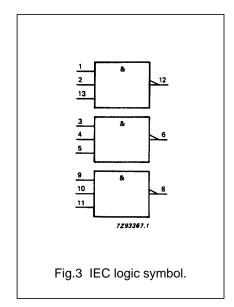
74HC/HCT10

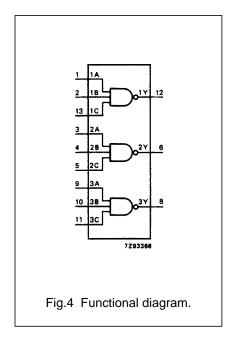
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
12, 6, 8	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V _{CC}	positive supply voltage









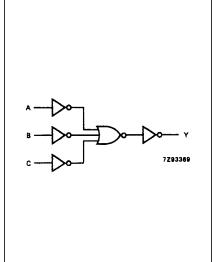


Fig.5 Logic diagram (one gate).

FUNCTION TABLE

1	INPUTS	OUTPUT			
nA	nB nC		nY		
L	L	L	Н		
L	L	Н	Н		
L	Н	L	Н		
L	Н	Н	Н		
Н	L	L	Н		
Н	L	Н	Н		
Н	Н	L	Н		
Н	Н	Н	L		

Notes

H = HIGH voltage level
 L = LOW voltage level

Philips Semiconductors Product specification

Triple 3-input NAND gate

74HC/HCT10

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER	T _{amb} (°C) 74HC							LIMIT	TEST CONDITIONS	
SYMBOL											WAVEFORMS
		+25			-40 to + 85		-40 to + 125		UNIT	V _{CC} (V)	WAVEFORWIS
		min.	typ.	max.	min.	max.	min.	max.		(-)	
t _{PHL} / t _{PLH}	propagation delay		30	95		120		145		2.0	
	nA, nB, nC to nY		11	19		24		29	ns	4.5	Fig.6
			9	16		20		25		6.0	
t _{THL} / t _{TLH}	output transition time		19	75		95		110		2.0	
			7	15		19		22	ns	4.5	Fig.6
			6	13		16		19		6.0	

Triple 3-input NAND gate

74HC/HCT10

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

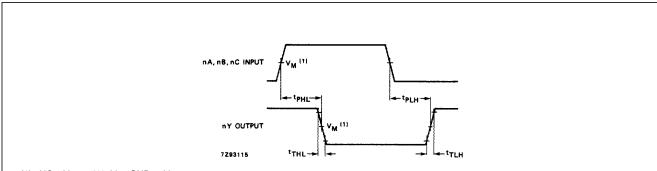
INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC	1.5

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF}$

SYMBOL	PARAMETER	T _{amb} (°C)								TEST CONDITIONS		
		74HCT									WAVEFORMS	
		+ 25		-40 to + 85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.		()		
t _{PHL} / t _{PLH}	propagation delay nA, nB, nC to nY		14	24		30		36	ns	4.5	Fig.6	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6	

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig. 6 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.