Overview of the Simulation of a L1Cache:

Split L1 cache (L1 data cache & L1 instruction cache)
32-bit processor (can be used with up to 3 other processors in a shared memory configuration)

L1 instruction cache:

- 2-way set associative
- 16K sets of 64-byte lines
- LRU replacement policy
- Shared L2 cache
- Inclusivity (Items in L1 are in L2)

L1 data cache:

- 4-way set associative
- 16K sets of 64-byte lines
- Write-back using write allocate
  - Must check “dirty-bit” to see if victim cache line is modified
  - Write victim cache line back to memory
- 1st write is write-though
  - Data in cache isn't the only current copy (memory is up to date)
  - Over-write victim cache line with new cache line (change tag bits)

Statistics for the Cache:

- Number of cache reads
- Number of cache writes
- Number of cache hits
- Number of cache misses
- Cache hit ratio

Implement the MESI protocol the L1 cache communicating with shared L2 cache:

Modified (Modified from the previous version)
Exclusive (Only cache with this data)
Shared (Shares data with other cache)
Invalid (Non-cache item)

What needs to be displayed:

- Return data to L2 <address>
- Write to L2 <address>
- Read from L2 <address>

From the Trace file (for testing):

n address

Where n is:

- 0 read data request to L1 data cache
- 1 write data request to L1 data cache
- 2 instruction fetch (a read request to L1 instruction cache)
- 3 invalidate command from L2
- 4 data request from L2 (in response to snoop)
- 8 clear the cache and reset all state (and statistics)

- 9 print contents and state of the cache (allow subsequent trace activity)