SAHYADRI
COLLEGE OF ENGINEERING & MANAGEMENT
An Autonomous Institution
MANGALURU

USN										

AM522I2A

Fifth Semester B.E. Degree Examination, 2024

Model Question Paper
ADVANCED RISC MACHINES

Time: 3 hrs. **Max. Marks: 100**

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Q. No.		Questions	Marks	BL/CO
		Module I		
1	a.	With the help of bit layout diagram explain current program status register with each field of ARM	08	CL2/CO1
	b.	Along with neat diagram of an ARM based embedded device, explain the four main hardware components	07	CL2/CO1
	c.	Discuss ARM bus technology	05	CL2/CO1
		OR		
2	a.	Define Pipelining? With a diagram explain ARM7, ARM9 Pipelining concept.	08	CL2/CO1
	b.	With the neat diagram, explain the ARM core data flow. Briefly describe the structure of ARM registers.	07	CL2/CO1
	c.	Explain the role of RISC Machines in modern computer architecture.	05	CL2/CO1
		Module II		
3	a.	Discuss any five Barrel shifter operations. Illustrate the role of Barrel shifter with suitable example.	08	CL2/CO2
	b.	Develop an ALP to find the sum of first 10 integer numbers	06	CL3/CO2
	c.	Show the post condition when MOVS instruction shifts register R1 right by one bit and result is stored in R0. Where R0=0X 00FFEE02, R1= 0X 80000001 and cpsr=nzcvqiFt. Justify your answer.	06	CL3/CO2
		OR		
4	a.	Discuss the single-register and multi register load-store addressing modes.	08	CL2/CO2
	b.	Develop and ALP to generate a table of 10 using look-up table.	06	CL3/CO2
	c	Show the post content of the registers R1, R4 and sp. If content of R1=0X 00000002, R4= 0X 00000003 sp=0x00100080 before execution of the instruction. STEMD sp! , {R1, R4}. Justify your answer.	06	CL3/CO2
		Module III		
		Explain the role of thumb instructions, how are they different from other ARM instructions.	5	CL2/CO3
5	a.	Explain the different data processing instructions of Thumb Instruction Set with appropriate examples.	8	CL2/CO3
	b.	Given mem32[0x 90000]=0x 00000001	7	CL3/CO3

		Mem32[0x90004]=0x 00000002 Mem32[0x90008]=0x 00000003 LDR R0,[R1,R4] If R1= 0x 00900000 R4= 0x 00000004. Write the contents of register R0, R1 and R4 post execution of instruction. Justify your answer.		
		OR		
6	a.	Explain ARM-Thumb interworking	5	CL2/CO3
	b.	Explain the different software interrupt instruction of Thumb instruction set with appropriate examples.	8	CL2/CO3
	c.	Given Mem32[0x80000] = 0x00000010 Mem32[0x80004] = 0x00000020 Mem32[0x80008] = 0x00000030 LDR R3, [R4, #0x04]! LDR R5, [R6], #0x04 **.** What will be the contents of registers R1, R3, R4, R5, and R6 after the execution of these instructions? Explain your answer, focusing on the different addressing modes used.	7	CL3/CO3
		Module IV		
7	a.	Differentiate between Bootloader and Firmware	6	CL2/CO4
	b.	Develop a program to demonstrate IRQ exception.	6	CL3/CO4
	c.	Develop an ARM assembly program that demonstrates the use of an SWI handler for performing a context switch. The program should implement the following: 1. Save the current context (registers) before entering the SWI handler. 2. Inside the SWI handler, mask off the upper 8 bits of the SWI instruction and pass the SWI number to a jump table. 3. The jump table should branch to an event handler corresponding to the SWI number. 4. After handling the SWI, restore the saved context and return control back to the original caller.	8	CL3/CO4
		OR		
8	a.	Explain the process of how the device driver program is executed.	6	CL2/CO4
	b.	Discuss how context switching takes place by giving appropriate examples.	6	CL2/CO4
	c.	Develop an ARM assembly program that implements a round-robin scheduler for a system with MAX_NUMBER_OF_TASKS. The scheduler should increment the task counter t each time it is called and reset t to 0 when it reaches the MAX_NUMBER_OF_TASKS. Use a context switch function to simulate switching tasks, and print the task ID for the current task being scheduled."	8	CL3/CO4

Module V				
9	a.	Demonstrate how to deploy a simple TensorFlow Lite model for predicting a sine wave onto a microcontroller	07	CL3/CO5
	b.	Define TinyML and discuss how it differs from traditional machine learning approaches?	07	CL2/CO5
	c.	What are the main steps involved in building a simple neural network model for regression using Keras in TinyML?	06	CL2/CO5
OR				
10	a.	Demonstrate how to deploy a simple TensorFlow Lite model for classifying motion gestures onto a microcontroller	07	CL3/CO5
	b.	Why is code generation for TensorFlow Lite preferred in embedded systems, and what are its limitations?	07	CL2/CO5
	c.	How can latency be optimized in TinyML models running on microcontrollers?	06	CL2/CO5

Cognitive Levels of Bloom's Taxonomy

No.	CL1	CL2	CL3	CL4	CL5	CL6
Level	Remember	Understand	Apply	Analyze	Evaluate	Create

Course Outcomes

CO1	Design and program ARM-based embedded systems with a solid understanding of RISC architecture, ARM design principles, processor fundamentals, and embedded system hardware and software.	CL3
CO2	Utilize the ARM instruction set, including data processing, branch, load-store, software interrupt instructions, and program status register instructions, enabling them to develop efficient and optimized software for ARM-based embedded systems	CL3
CO3	Use Thumb instruction set to create compact and efficient code for ARM-based embedded systems	CL3
CO4	Design and work with firmware and bootloaders, and comprehend the fundamental components of embedded operating systems.	CL3
CO5	Design, build, and deploy machine learning models on microcontrollers for various applications.	CL3