ES 215: Assignment 2

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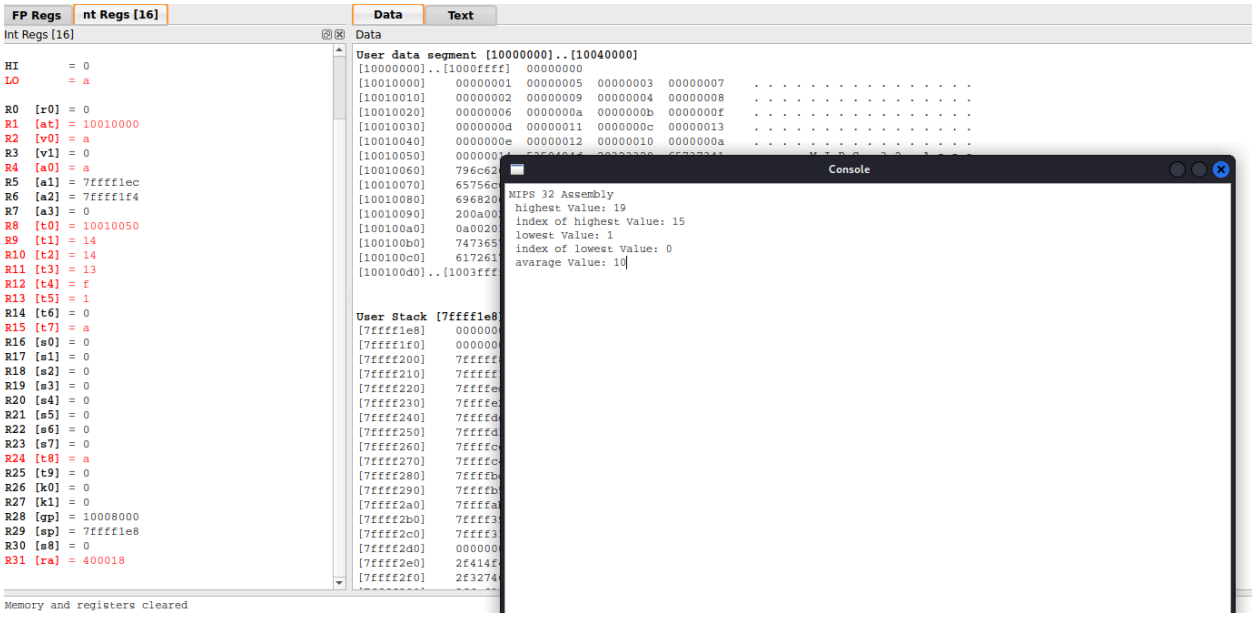
[Github Link]

Q1. **MIPS32 assembly that computes the Highest value & index, Lowest value & index and Average value of an Array A[0..20].**

Github file Q1.s

Took an array of size 20.



Q2. **Consider a dual core processor. Program A completes in 6 seconds on core 1 and has a CPI of 6 and program B completes in 5 seconds on core 2 and has a CPI of 5. Both cores run at 1 GHz. What is the combined throughput of the processor?**

Program A has CPI of 6 and takes 6 seconds on a 1 GHz processor on core 1.

For core 1 with program A :
Suppose program A has x instructions then,

6x cycles as CPI is 6.
6 seconds with 1GHz processors.

$$6 * x = 6 * 10^9$$

$$x = 10^9 \ instructions$$

So program A has 10^9 instructions.

Throughput, $T_1 = \frac{10^9 \ instructions}{6 \ seconds} = 1/6 * 10^9 \ Instructions \ per \ second$

Similarly, For core 2 with program B :
Suppose program B has x instructions then,

5x cycles as CPI is 6.
5 seconds with 1GHz processors.

$$5 * x = 5 * 10^9$$

$$x = 10^9 \ instructions$$

So program B has 10^9 instructions.

Throughput, $T_2 = \frac{10^9 \ instructions}{5 \ seconds} = 1/5 * 10^9 \ Instructions \ per \ second$

Total throughput of processor = Throughput of core 1 + Throughput of core 2

$$= (1/6 + 1/5) * 10^9 \ IPS$$

$$= 11/30 * 10^9 \ IPS = 3.67 * 10^9 \ IPS$$

Q3. **Say a processor X runs at 2 GHz and a program (Program A) executes 10 billion instructions with avg. CPI of 3. Compute how long this program ran for? Now, suppose we got another processor Y with a clock frequency of 4 GHz. Program A on this new processor executes 7 billion instructions with an average CPI of 5. What is the speedup (if any) of program A on processor Y over processor X?**

For processor X -> 2 GHz -> 2 billion cycles per second

Program A with processor X:

Number of instructions = 10 billion

avg. CPI = 3

total number of cycles required = 30 billion cycles

Time with processor X $= \frac{30\ billion\ cycles}{2\ billion\ cycles\ per\ second} = 15\ seconds$

So program A will require 15 seconds with processor X.

Now, for processor Y -> 4 GHz -> 4 billion cycles per second

Program A with processor Y:

Number of instructions = 7 billion

avg. CPI = 5

total number of cycles required = 35 billion cycles

Time with processor Y $= \frac{35\ billion\ cycles}{4\ billion\ cycles\ per\ second} = 8.75\ seconds$

So program A will require 8.75 seconds with processor Y.

Speedup = $\frac{execution\ time\ on\ X}{execution\ time\ on\ Y} = 15/8.75 = 1.714$

Q4. **Consider a Processor with 1 GHz. Program A executes 9 billion instructions on this processor and has an average CPI of 1.5. With a newly designed processor that can run at 2 GHz, the execution time of Program A dropped to a quarter of the original value. What is the average CPI of Program A on the new design?**

$$Execution\ time\ = \frac{Num\ of\ instructions * CPI}{Cycle\ frequency\ of\ processor}$$

$$exeTime_1 = 4 * exeTime_2$$

$$\frac{9 * 10^9 * 1.5}{10^9} = 4 * \frac{9 * 10^9 * x}{2 * 10^9}$$

$$x = 0.75$$

Average CPI of program A on new design is 0.75.

Q5. **Suppose a processor consumes 80 watts of power (Note: it is the total power) while running at 2 GHz and the operating voltage of this processor is 5V.**

Total power = 80 W
Clock frequency = 2GHz
Operating voltage = 5V

Assuming static power is 25 % of the total power.
Then dynamic power = 60 W and Static power = 20 W

a) **How much dynamic power would the same processor consume if the frequency were to be frequency to 5 GHz?**

Dynamic power is proportional to frequency,
So for 5 GHz frequency,

Dynamic power = $\frac{5 * 10^9}{2 * 10^9} * 60 = 150\,W$

b) **With technology scaling, consider that operating voltage drops to 2V. Now for the 2GHz processor, what is the overall power consumption with this design and what fraction of the power can be attributed to static power?**

static power is proportional to the voltage.

New static power = $\frac{2}{5} * 20 = 8\,W$

Also dynamic power is proportional to square of voltage.

New dynamic power = $(\frac{2}{5})^2 * 60 = 9.6\,W$

So new total power = $9.6 + 8 = 17.6\,W$

Fraction of static power = 8/17.6 = 0.455

Grace Question:

Part a)

Files are uploaded on the github.

Part b)

Preprocessed files for MIPS architecture are generally expected to be larger than those for x86 architecture. This is because the MIPS architecture may require more intermediate code or expanded macros during preprocessing compared to x86. Compiled files for MIPS architecture may tend to be larger or similar in size compared to those for x86 architecture. This could be due to variations in the generated assembly code, optimizations, or instructions used by the compiler for each architecture. Assembled files for MIPS architecture may be expected to be smaller or similar in size compared to those for x86 architecture. This difference could stem from differences in instruction sets, encoding, or optimizations performed during the assembly process. Binary executable files for MIPS architecture are generally expected to be smaller or similar in size compared to those for x86 architecture. This difference could be influenced by various factors such as compiler optimizations, runtime libraries, and differences in executable formats.