

# BJT AC Analysis

## Equivalent Circuits

Text Book

Electronic Devices and Circuit Theory

*by R Boylestad and L Nashelsky*

# Ac analysis steps

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In summary, therefore, the ac equivalent of a network is obtained by:

1. *Setting all dc sources to zero and replacing them by a short-circuit equivalent*
2. *Replacing all capacitors by a short-circuit equivalent*
3. *Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2*
4. *Redrawing the network in a more convenient and logical form*

In the sections to follow, the  $r_e$  and hybrid equivalent circuits will be introduced to complete the ac analysis of the network of Fig. 7.5.

# Ac analysis: Common-emitter

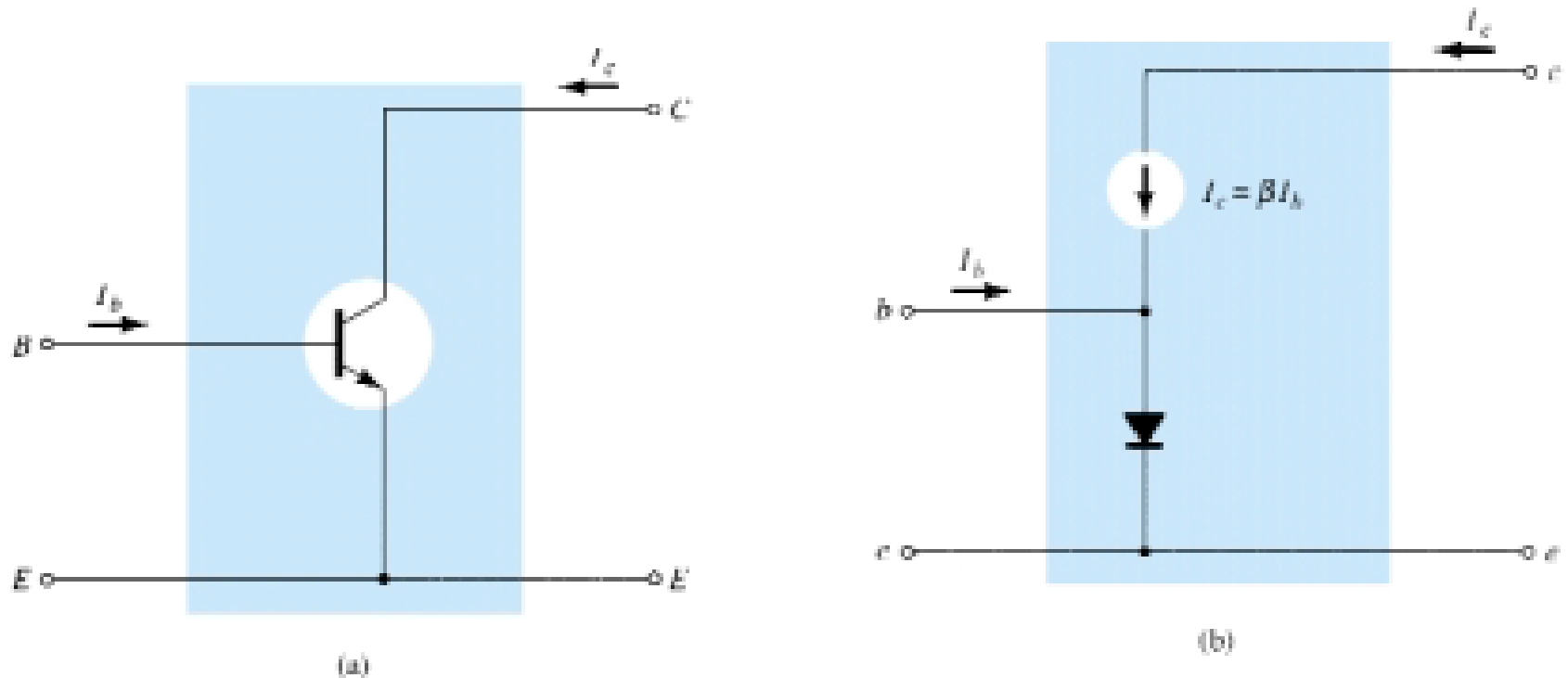


Figure 7.21 (a) Common-emitter BJT transistor; (b) approximate model for the configuration

$$I_c = \beta I_b$$

The current through the diode is therefore determined by

$$I_e = I_c + I_b = \beta I_b + I_b$$

and

$$I_e = (\beta + 1)I_b$$

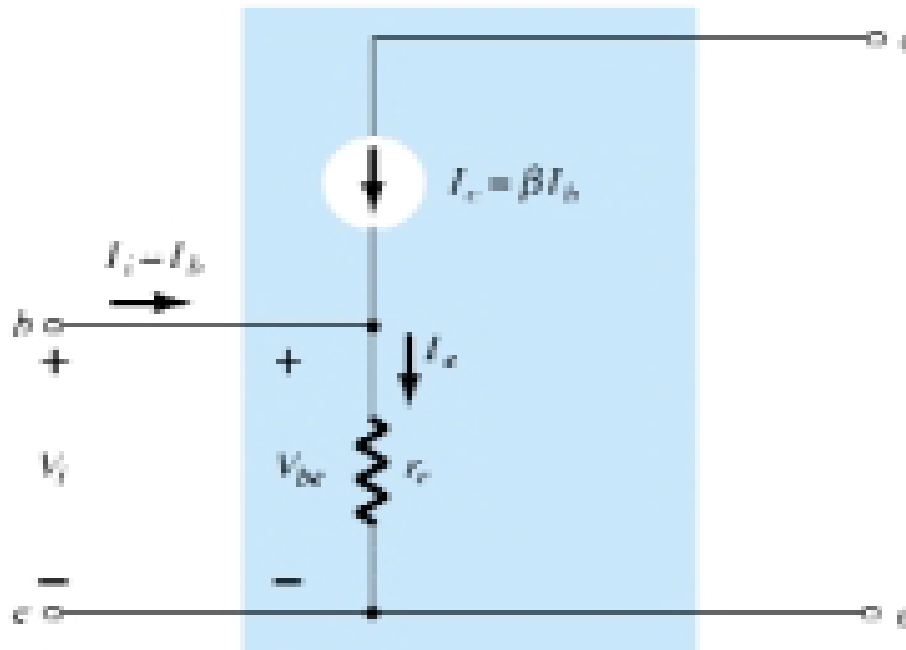
# Ac analysis: Common-Emitter

$$I_e \cong \beta I_b$$

The input impedance is determined by the following ratio:

$$Z_i = \frac{V_i}{I_i} = \frac{V_{be}}{I_b}$$

$$V_i = V_{be} = I_e r_e \cong \beta I_b r_e$$



$$Z_i = \frac{V_{be}}{I_b} \cong \frac{\beta I_b r_e}{I_b}$$

$$Z_i \cong \beta r_e \quad \text{CE}$$

# Ac analysis: Common-Emitter

For the output impedance, the characteristics of interest are the output set of Fig. 7.24. Note that the slope of the curves increases with increase in collector current. The steeper the slope, the less the level of output impedance ( $Z_o$ ). The  $r_e$  model of Fig. 7.21 does not include an output impedance, but if available from a graphical analysis or from data sheets, it can be included as shown in Fig. 7.25.

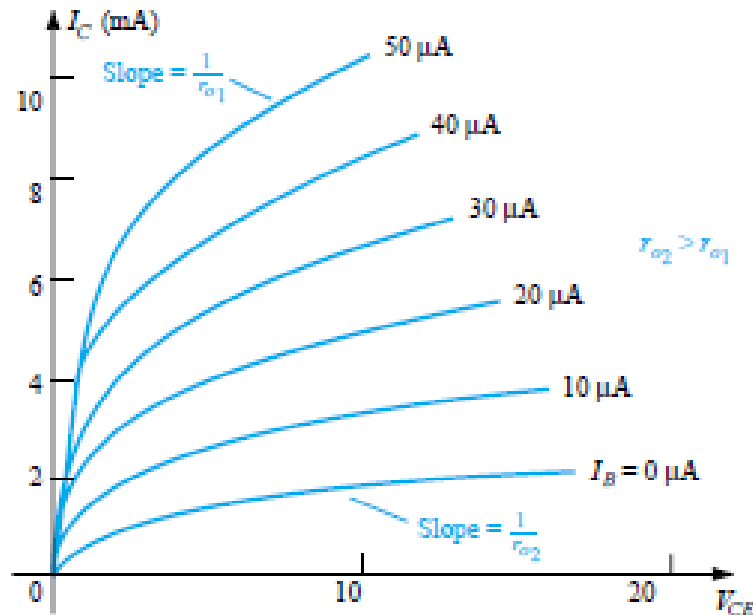


Figure 7.24 Defining  $r_o$  for the common-emitter configuration.

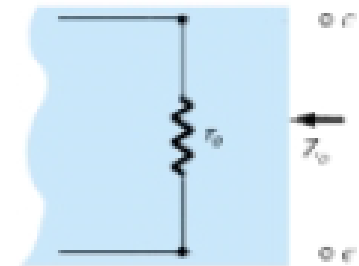


Figure 7.25 Including  $r_o$  in the transistor equivalent circuit.

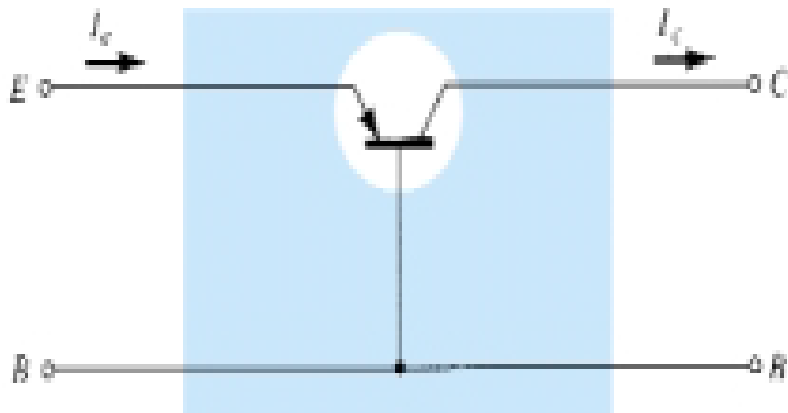
For the common-emitter configuration, typical values of  $Z_o$  are in the range of 40 to 50 k $\Omega$ .

For the model of Fig. 7.25, if the applied signal is set to zero, the current  $I_c$  is 0 A and the output impedance is

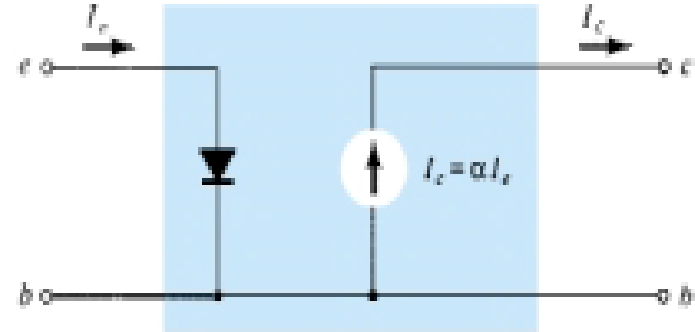
$$\boxed{Z_o = r_o}_{CE} \quad (7.20)$$

That means, output looks open circuit results in to consider an output impedance. Here,  $r_o$  is chosen as example.

# Ac analysis: Common-Base

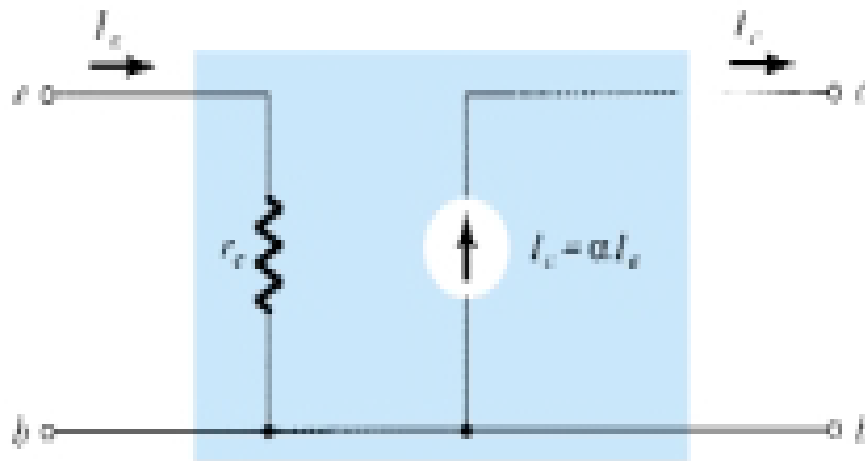


(a)



(b)

Figure 7.16 (a) Common-base BJT transistor; (b)  $r_e$  model for the configuration



$$r_e = \frac{26 \text{ mV}}{I_E}$$

# Ac analysis: Common-Base

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Due to the isolation that exists between input and output circuits of Fig. 7.17, it should be fairly obvious that the input impedance  $Z_i$  for the common-base configuration of a transistor is simply  $r_e$ . That is,

$$\boxed{Z_i = r_e} \quad \text{CB} \quad (7.12)$$

*For the common-base configuration, typical values of  $Z_i$  range from a few ohms to a maximum of about 50  $\Omega$ .*

For the output impedance, if we set the signal to zero, then  $I_e = 0$  A and  $I_c = \alpha I_e = \alpha(0 \text{ A}) = 0$  A, resulting in an open-circuit equivalence at the output terminals. The result is that for the model of Fig. 7.17,

$$\boxed{Z_o \cong \infty \Omega} \quad \text{CB} \quad (7.13)$$

# Ac analysis: Common-Base

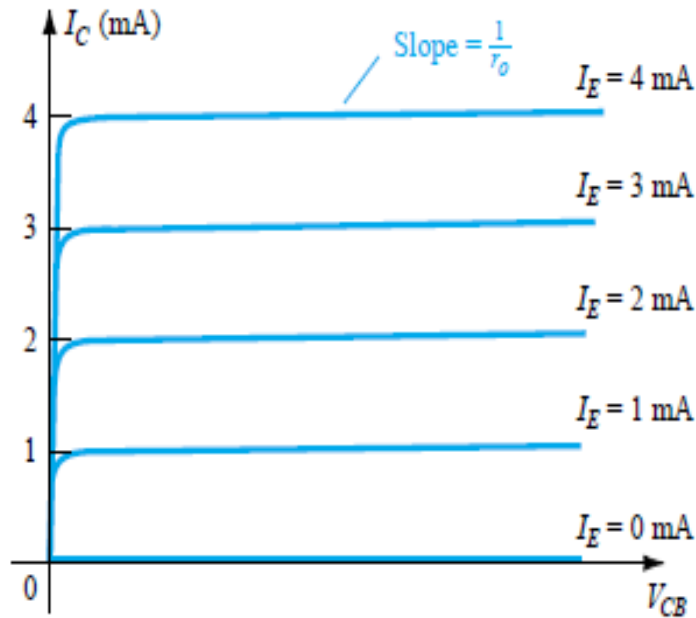


Figure 7.18 Defining  $Z_o$ .

*In general, for the common-base configuration the input impedance is relatively small and the output impedance quite high.*

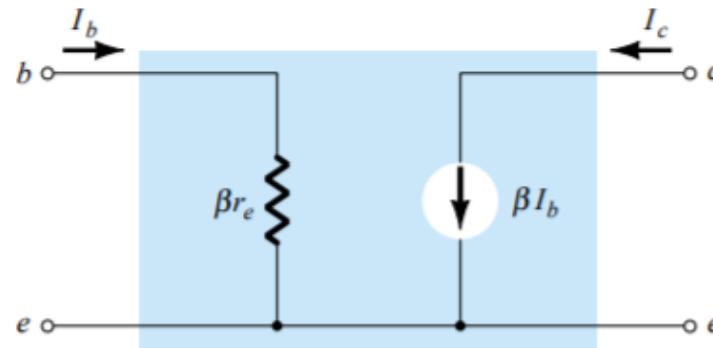
In actuality:

*For the common-base configuration, typical values of  $Z_o$  are in the megohm range.*



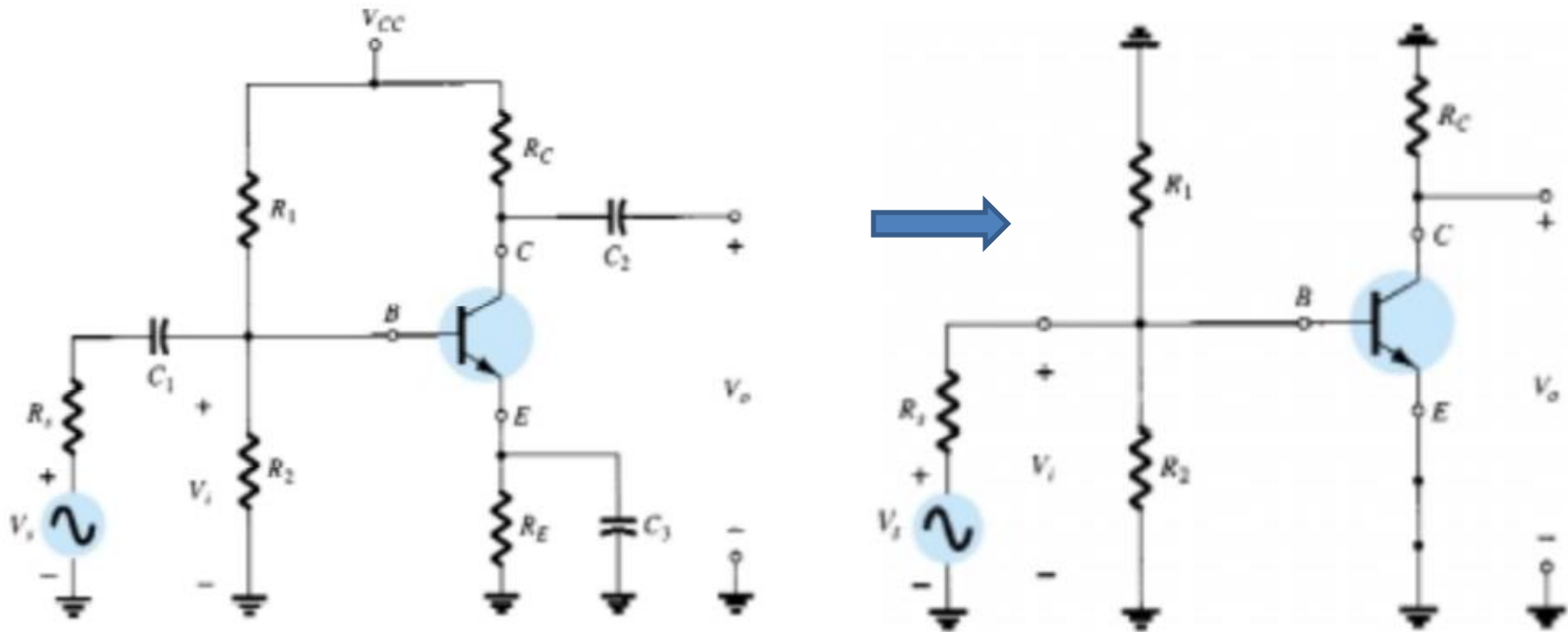
# Ac analysis

1. Deactivate (grounded) dc sources in the circuit.
2. Replace coupling and bypass capacitors by short circuit equivalent.
3. Redraw the circuit (optional),
4. Replace the transistor by its ac model.

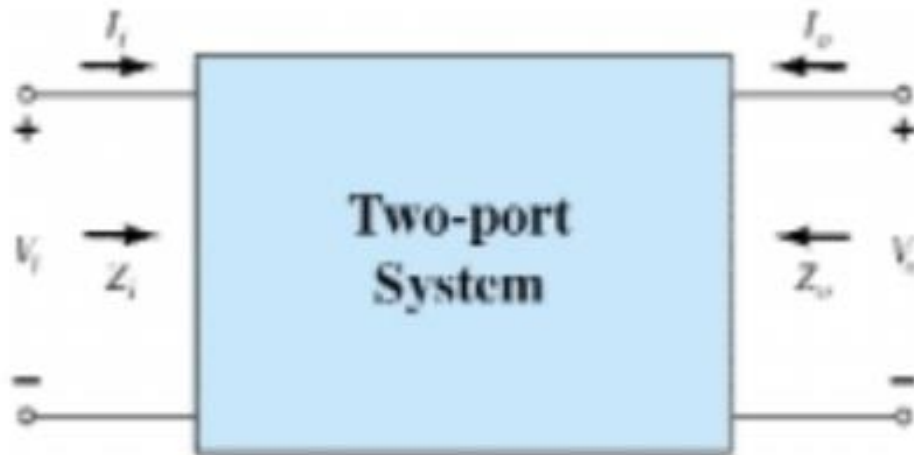


$r_e$  model

# Ac analysis and Transistor models



# Parameters of importance



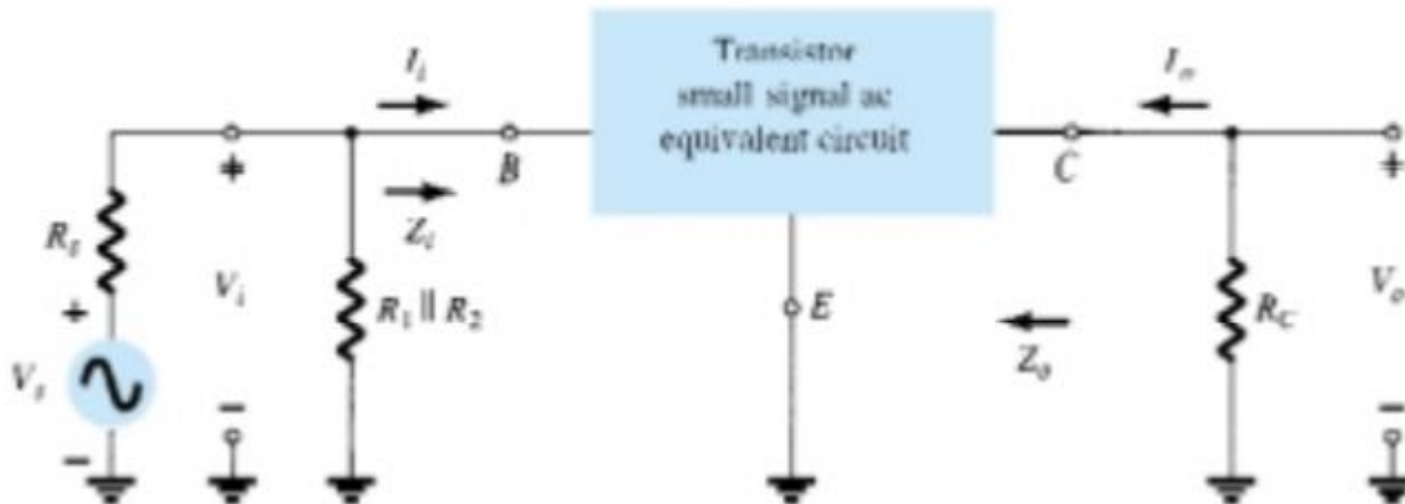
$$Z_i = \frac{V_i}{I_i}$$

$$Z_o = \frac{V_o}{I_o}$$

$$A_v = \frac{V_o}{V_i}$$

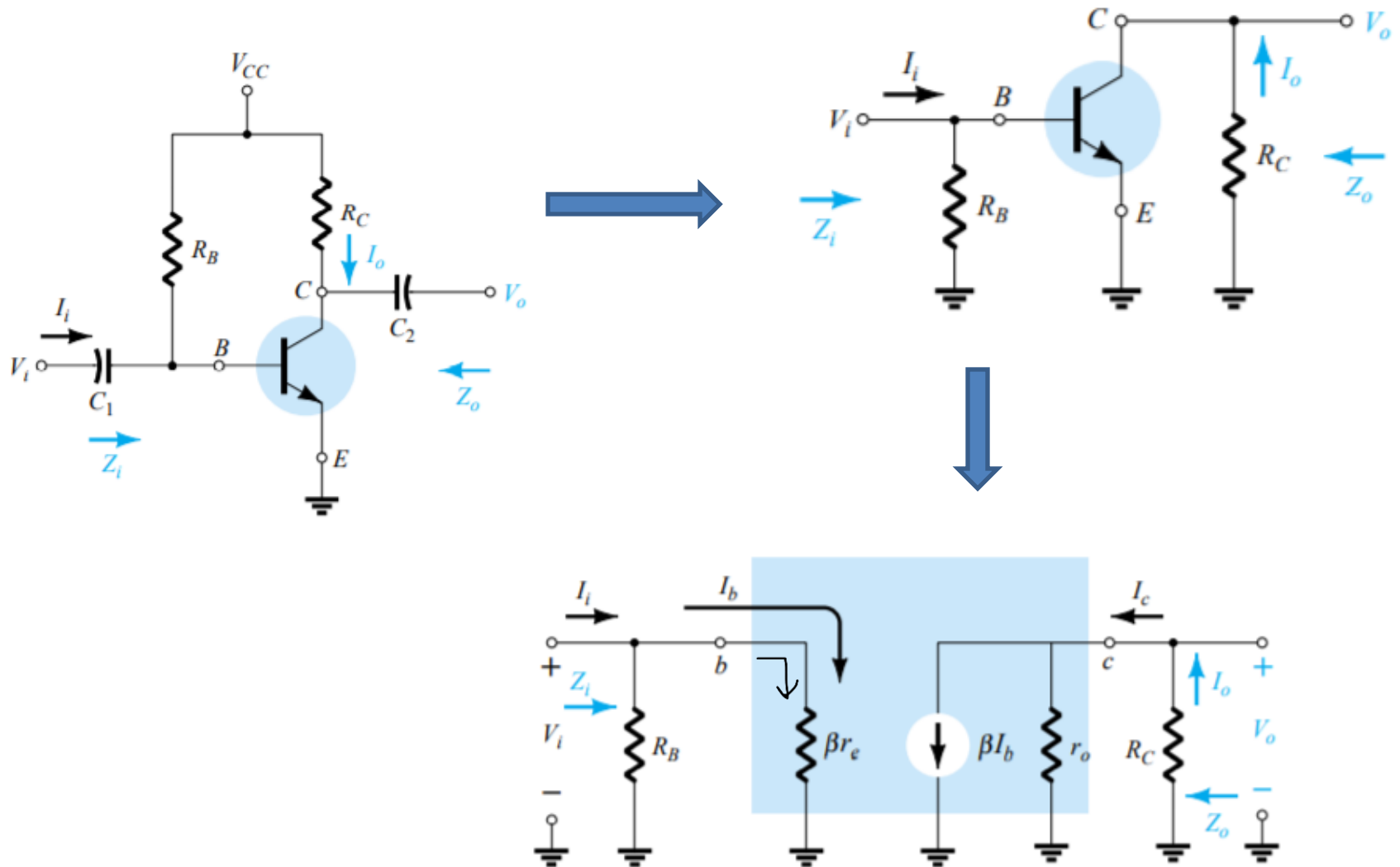
$$A_i = \frac{I_o}{I_i}$$

# Redrawing the circuit



**Figure 7.5** Circuit of Fig. 7.4 redrawn for small-signal ac analysis.

# Fixed bias amplifier



# Ac circuit parameters

Voltage gain:

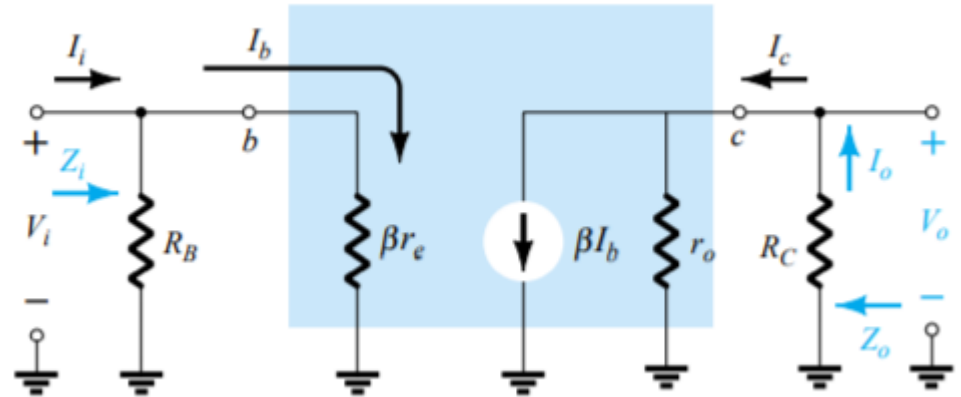
$$V_o = -\beta I_b (R_C \parallel r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \parallel r_o)$$

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \parallel r_o)}{r_e}$$

$$A_v = -\frac{R_C}{r_e} \quad r_o \geq 10R_C$$



Input Impedance,

$$Z_i = R_B \parallel \beta r_e \quad \Omega$$

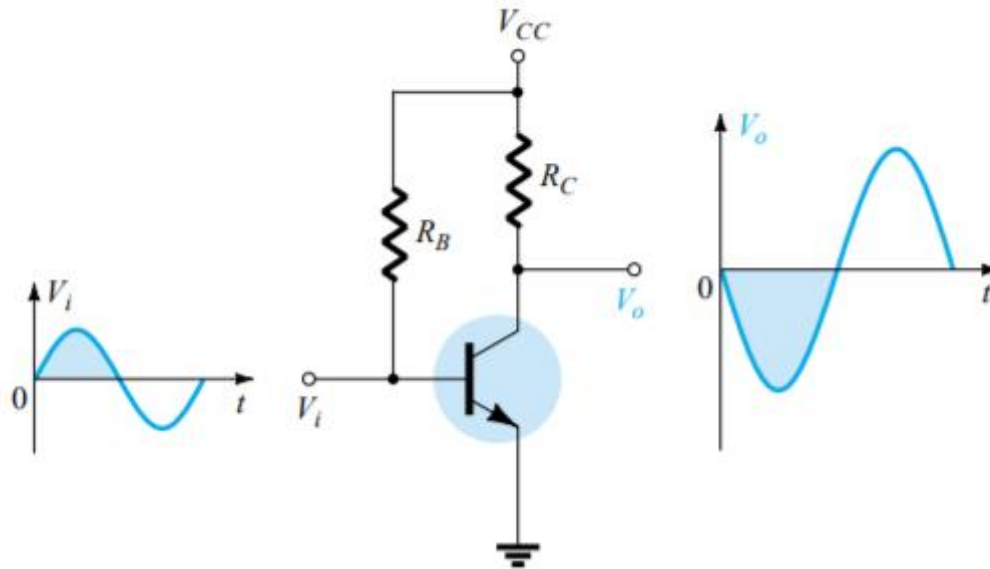
Output Impedance,

$$Z_o = R_C \parallel r_o \approx R_C \quad \Omega$$

Current gain:

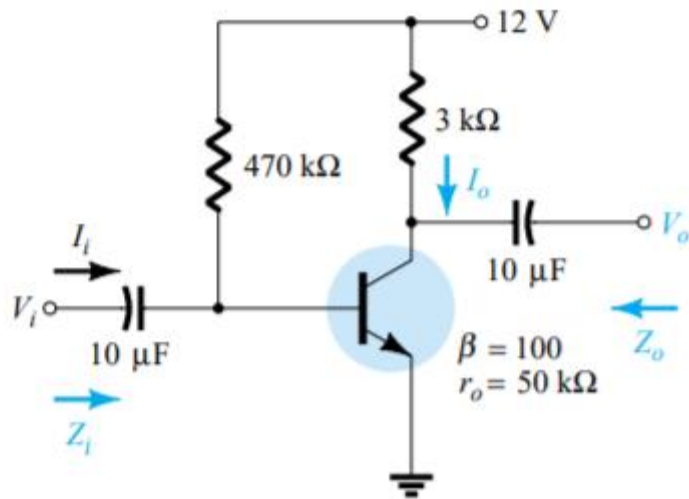
$$A_i = \beta$$

# Output ac signal swing



**Figure 8.5** Demonstrating the  $180^\circ$  phase shift between input and output waveforms.

# Example-1



(a) DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{470 \text{ k}\Omega} = 24.04 \text{ }\mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04 \text{ }\mu\text{A}) = 2.428 \text{ mA}$$

$$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.428 \text{ mA}} = \mathbf{10.71 \text{ }\Omega}$$

(b)  $\beta r_e = (100)(10.71 \text{ }\Omega) = 1.071 \text{ k}\Omega$

$$Z_i = R_B \parallel \beta r_e = 470 \text{ k}\Omega \parallel 1.071 \text{ k}\Omega = \mathbf{1.069 \text{ k}\Omega}$$

(c)  $Z_o = R_C = \mathbf{3 \text{ k}\Omega}$

(d)  $A_v = -\frac{R_C}{r_e} = -\frac{3 \text{ k}\Omega}{10.71 \text{ }\Omega} = \mathbf{-280.11}$

(e) Since  $R_B \geq 10\beta r_e$  ( $470 \text{ k}\Omega > 10.71 \text{ k}\Omega$ )

$$A_i \cong \beta = \mathbf{100}$$



# Voltage divider bias

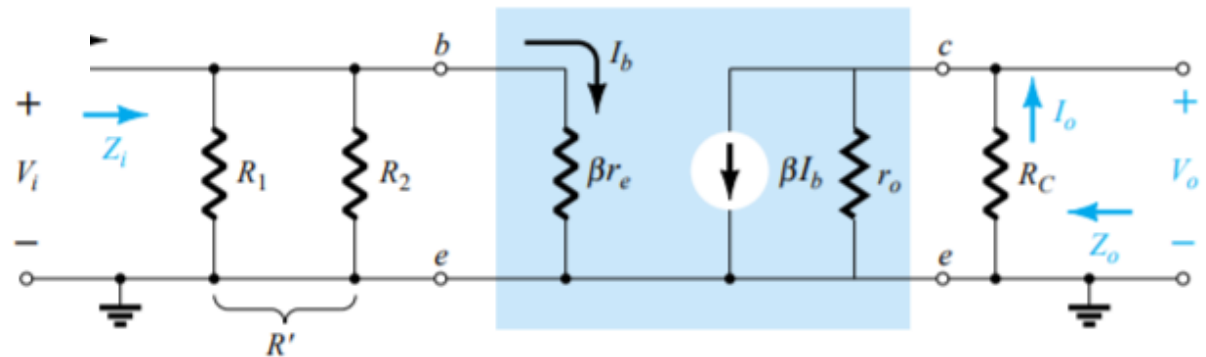
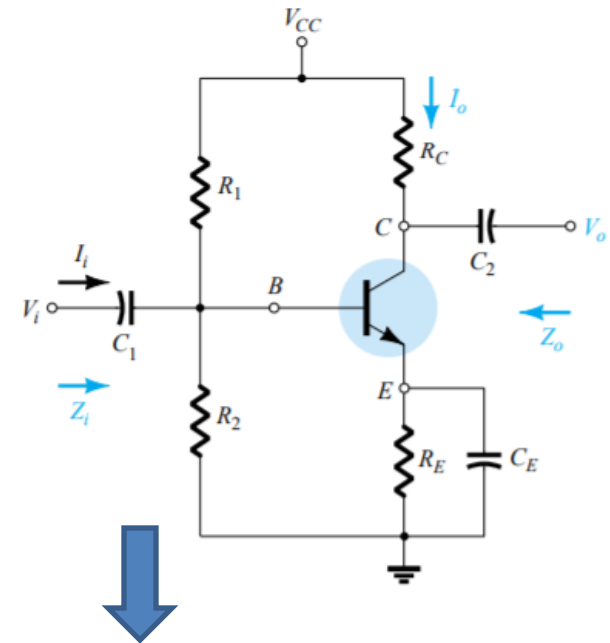
$$R' = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$Z_i = R' \parallel \beta r_e$$

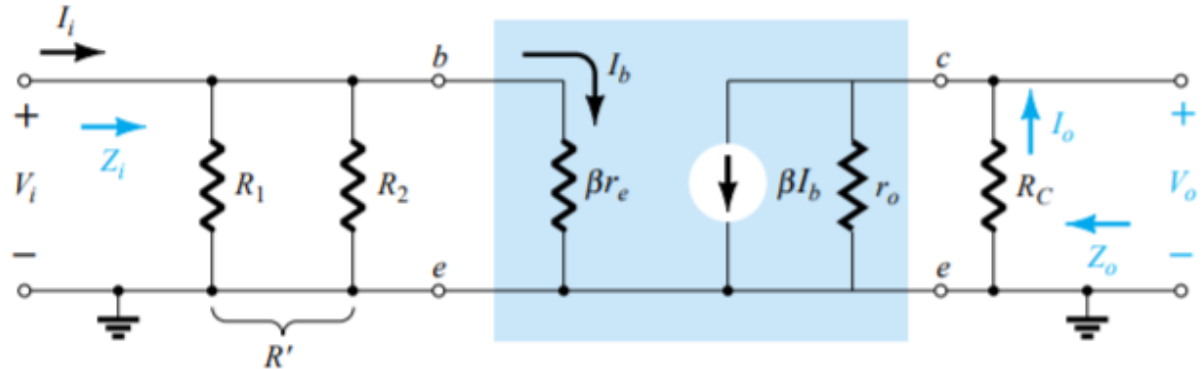
$$Z_o = R_C \parallel r_o$$

$$Z_o \cong R_C$$

$$r_o \geq 10 R_C$$



# Voltage and current gain



$$V_o = -(\beta I_b)(R_C \parallel r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \parallel r_o)$$

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \parallel r_o}{r_e}$$

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e}$$

$$r_o \geq 10R_C$$

Current gain:

$$A_i = \beta$$

**Phase relationship:**

180° phase shift between  $V_o$  and  $V_i$ .

# Example-2

- Find  $Z_i$ ,  $Z_o$ ,  $A_v$  and  $A_i$ , given  $I_{EQ} = 1.41\text{mA}$

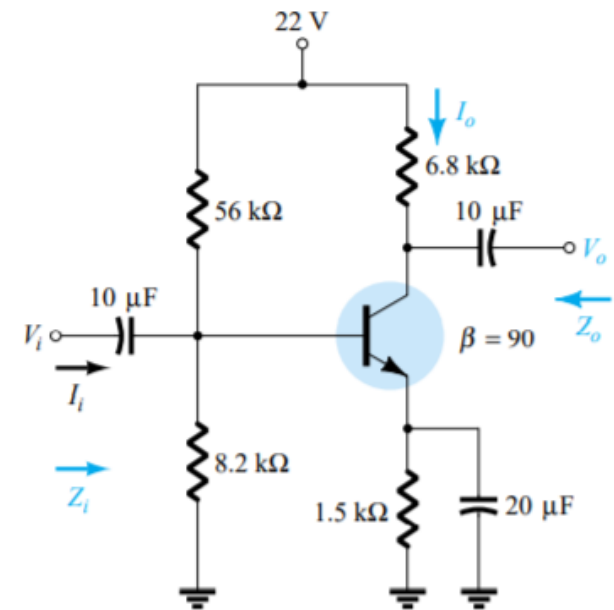
$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.41\text{ mA}} = \mathbf{18.44\ \Omega}$$

$$(b) R' = R_1 \parallel R_2 = (56\text{ k}\Omega) \parallel (8.2\text{ k}\Omega) = 7.15\text{ k}\Omega$$

$$Z_i = R' \parallel \beta r_e = 7.15\text{ k}\Omega \parallel (90)(18.44\ \Omega) = 7.15\text{ k}\Omega \parallel 1.66\text{ k}\Omega = \mathbf{1.35\text{ k}\Omega}$$

$$(c) Z_o = R_C = \mathbf{6.8\text{ k}\Omega}$$

$$(d) A_v = -\frac{R_C}{r_e} = -\frac{6.8\text{ k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$$

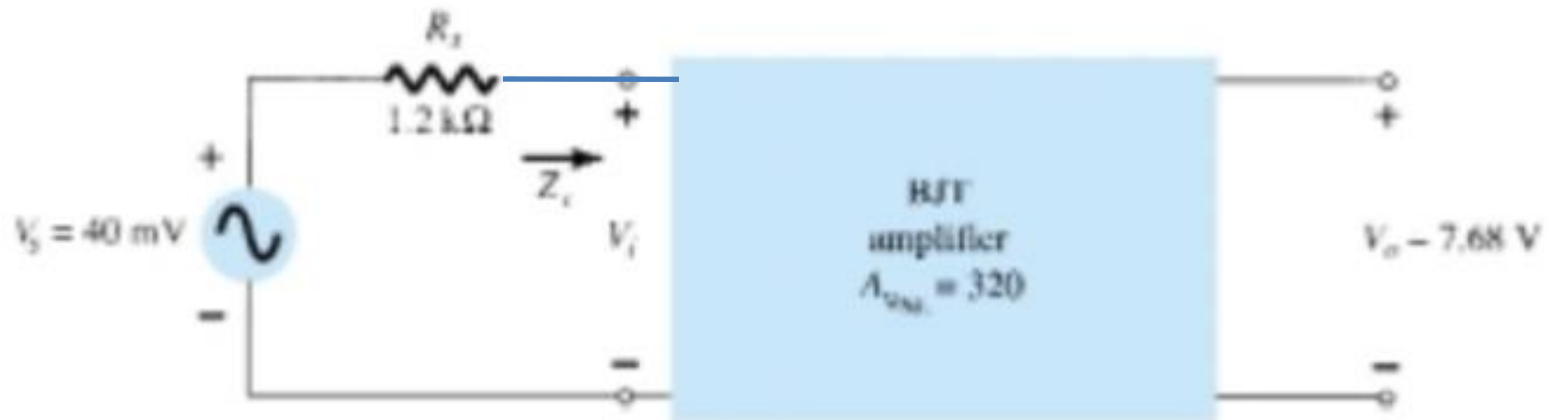


# Example-3

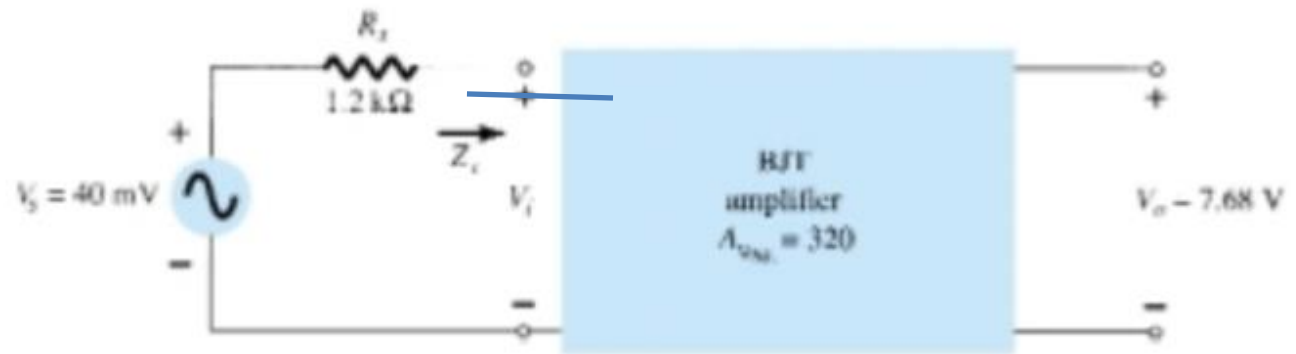
## EXAMPLE 7.3

For the BJT amplifier of Fig. 7.14, determine:

- (a)  $V_i$ .
- (b)  $I_i$ .
- (c)  $Z_i$ .
- (d)  $A_{V_s}$ .



# Solution



## Solution

$$(a) A_{vNL} = \frac{V_o}{V_i} \text{ and } V_i = \frac{V_o}{A_{vNL}} = \frac{7.68 \text{ V}}{320} = \mathbf{24 \text{ mV}}$$

$$(b) I_i = \frac{V_s - V_i}{R_s} = \frac{40 \text{ mV} - 24 \text{ mV}}{1.2 \text{ k}\Omega} = \mathbf{13.33 \text{ }\mu\text{A}}$$

$$(c) Z_i = \frac{V_i}{I_i} = \frac{24 \text{ mV}}{13.33 \text{ }\mu\text{A}} = \mathbf{1.8 \text{ k}\Omega}$$

$$(d) A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{vNL}$$

$$= \frac{1.8 \text{ k}\Omega}{1.8 \text{ k}\Omega + 1.2 \text{ k}\Omega} (320)$$

$$= \mathbf{192}$$

For the system of Fig. 7.13 having a source resistance  $R_s$ , the level of  $V_i$  would first have to be determined using the voltage-divider rule before the gain  $V_o/V_s$  could be calculated. That is,

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

with

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

and

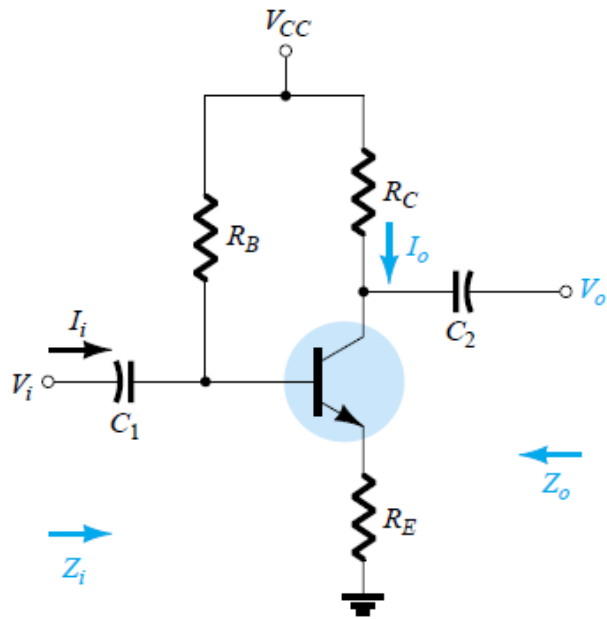
$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i}$$

so that

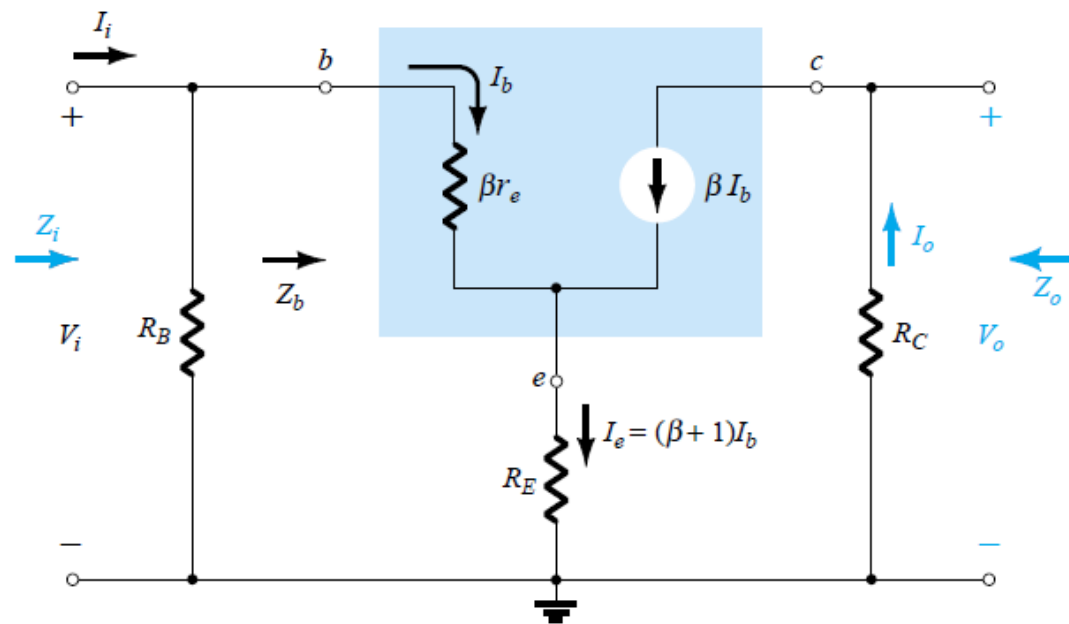
$$A_{v_s} = \frac{V_o}{V_s} = \frac{Z_i}{Z_i + R_s} A_{vNL} \quad (7.8)$$

## CE EMITTER-BIAS CONFIGURATION

### Unbypassed

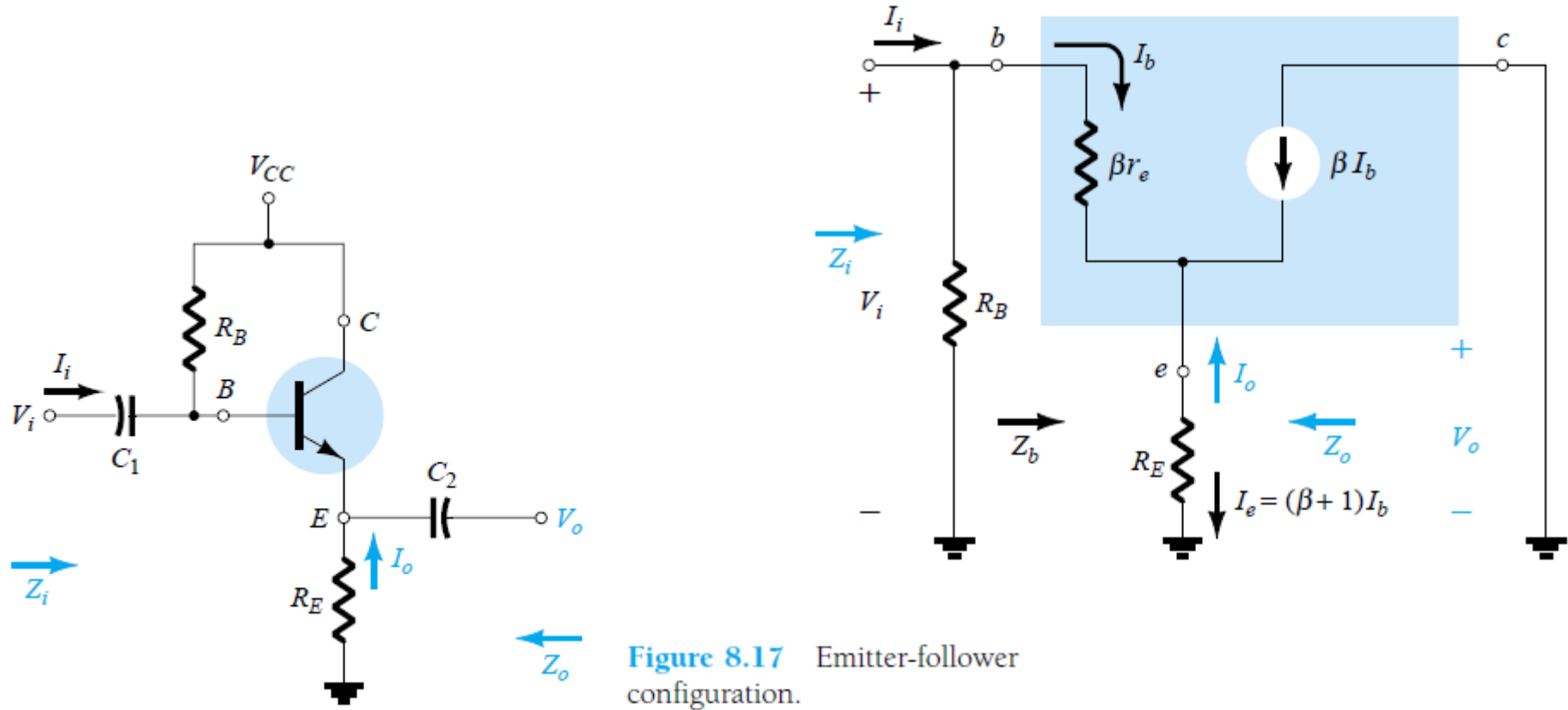


**Figure 8.10** CE emitter-bias configuration.



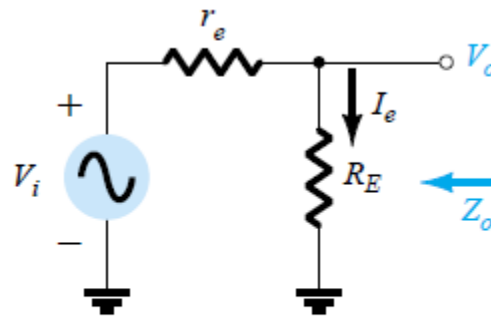
**Figure 8.11** Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 8.10.

## EMITTER-FOLLOWER CONFIGURATION



**Figure 8.17** Emitter-follower configuration.

## EMITTER-FOLLOWER CONFIGURATION



**Figure 8.19** Defining the output impedance for the emitter-follower configuration.

To determine  $Z_o$ ,  $V_i$  is set to zero and

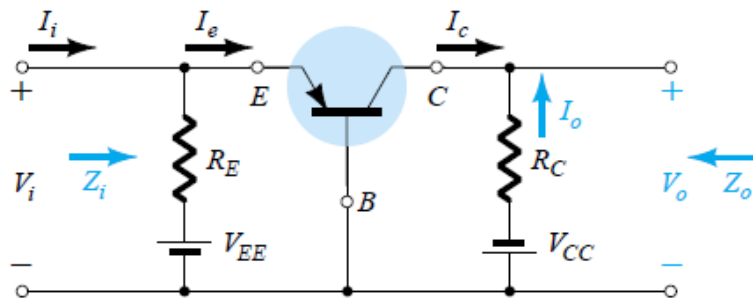
$$Z_o = R_E \parallel r_e \quad (8.42)$$

Since  $R_E$  is typically much greater than  $r_e$ , the following approximation is often applied:

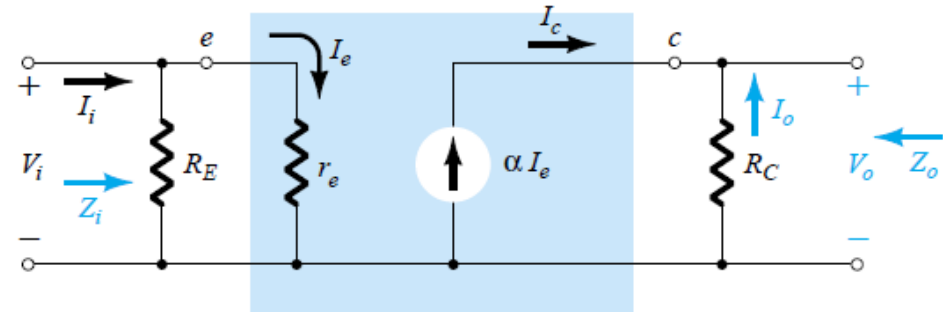
$$Z_o \cong r_e \quad (8.43)$$



## COMMON-BASE CONFIGURATION

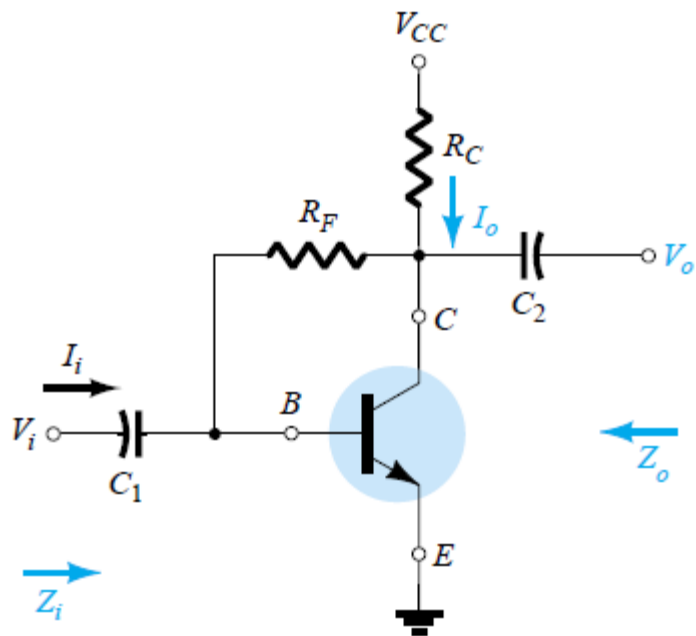


**Figure 8.23** Common-base configuration.

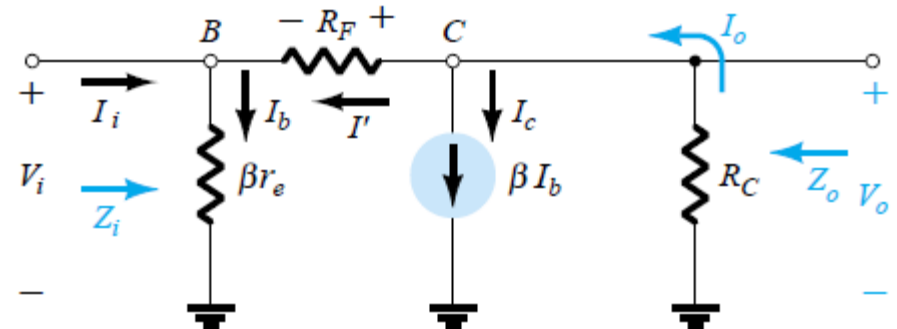


**Figure 8.24** Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 8.23.

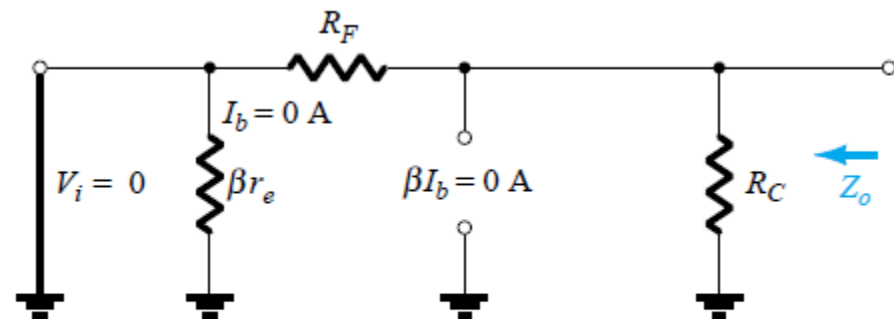
## COLLECTOR FEEDBACK CONFIGURATION



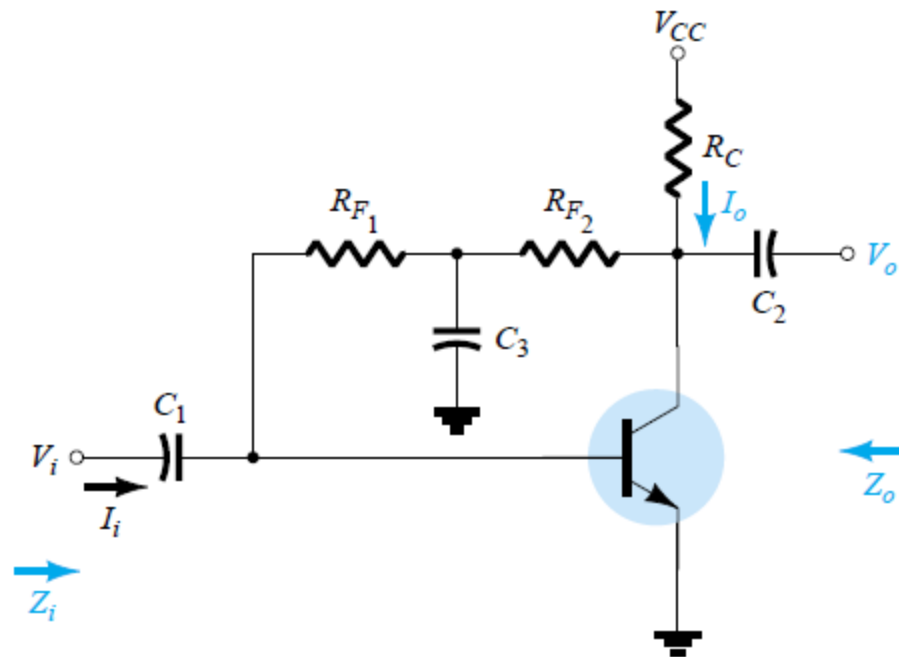
**Figure 8.26** Collector feedback configuration.



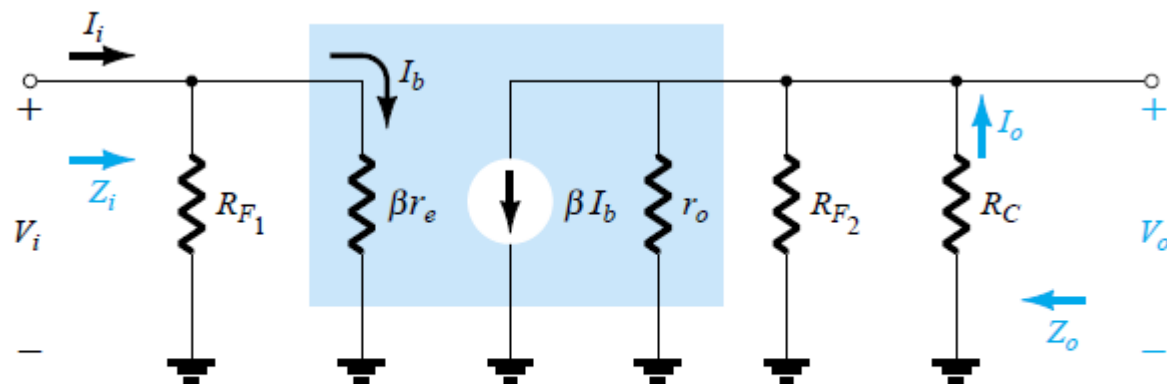
**Figure 8.27** Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 8.26.



**Figure 8.28** Defining  $Z_o$  for the collector feedback configuration.



**Figure 8.31** Collector dc feedback configuration.



**Figure 8.32** Substituting the  $r_e$  equivalent circuit into the ac equivalent network of Fig. 8.31.

Practice yourself and send me  
your feedback, if any.