FET Biasing

Text Book

Electronic Devices and Circuit Theory

by R Boylestad and L Nashelsky

Things to Remember

- ❖ distinct difference between the analysis of BJT and FET transistors is that the input controlling variable for a BJT transistor is a current level, while for the FET a voltage is the controlling variable.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$\boxed{I_G \cong 0\ \text{A}} \tag{6.1}$$

and

$$\boxed{I_D = I_S} \tag{6.2}$$

For JFETS and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2} \tag{6.3}$$

For enhancement-type MOSFETs, the following equation is applicable:

$$\boxed{I_D = k(V_{GS} - V_T)^2} \tag{6.4}$$

Fixed bias circuit

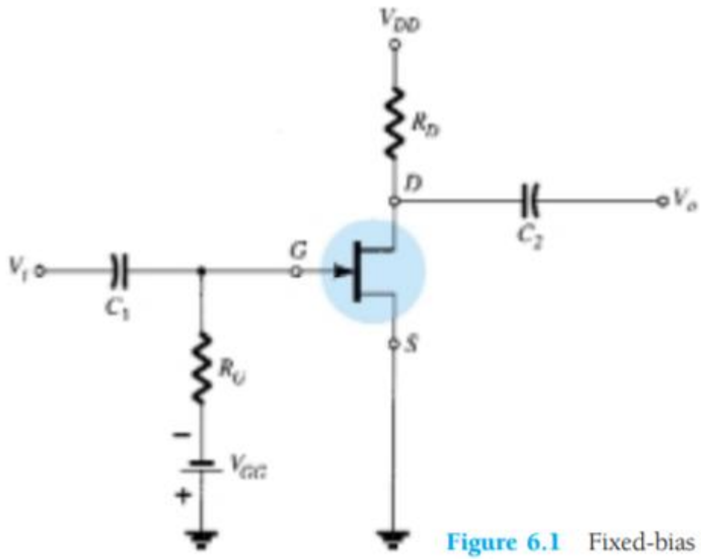


Figure 6.1 Fixed-bias configuration.

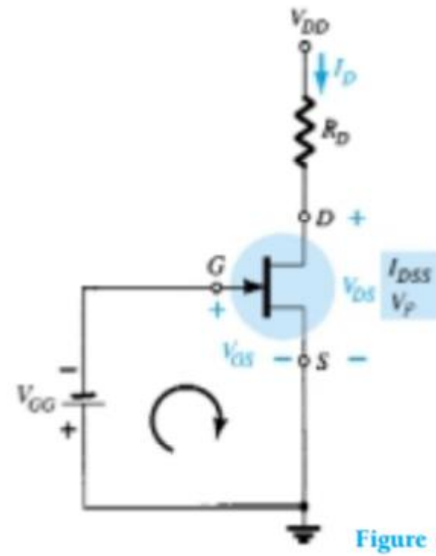
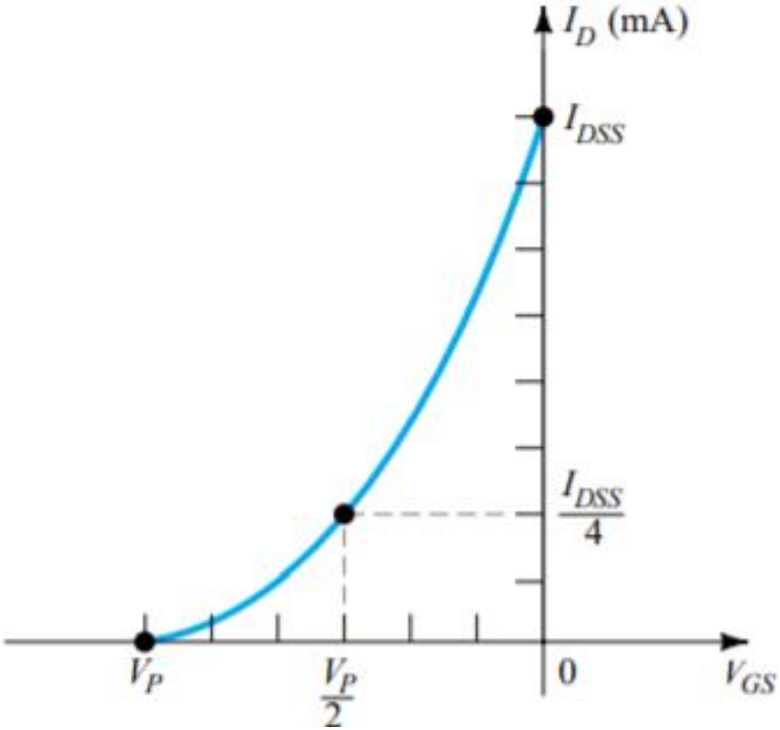


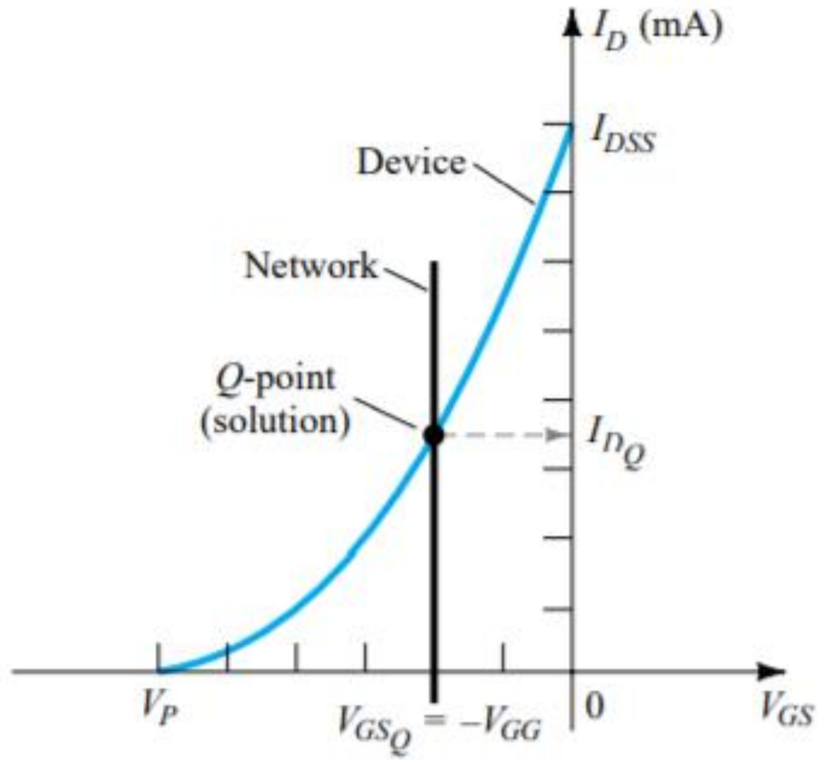
Figure 6.2 Network for dc analysis.

$$-V_{GG} - V_{GS} = 0$$

$$\boxed{V_{GS} = -V_{GG}}$$

Graphical Approach





Output quantities

The drain-to-source voltage of the output section can be detern
Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and $$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

Recall that single-subscript voltages refer to the voltage at a poir
ground. For the configuration of Fig. 6.2,

$$\boxed{V_S = 0 \text{ V}}$$

Using double-subscript notation:

$$V_{DS} = V_D - V_S$$

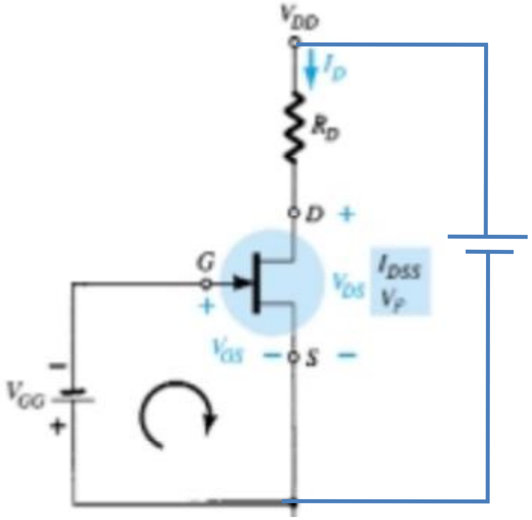
or $$V_D = V_{DS} + V_S = V_{DS} + 0 \text{ V}$$

and $$\boxed{V_D = V_{DS}} \quad (6.8)$$

In addition, $$V_{GS} = V_G - V_S$$

or $$V_G = V_{GS} + V_S = V_{GS} + 0 \text{ V}$$

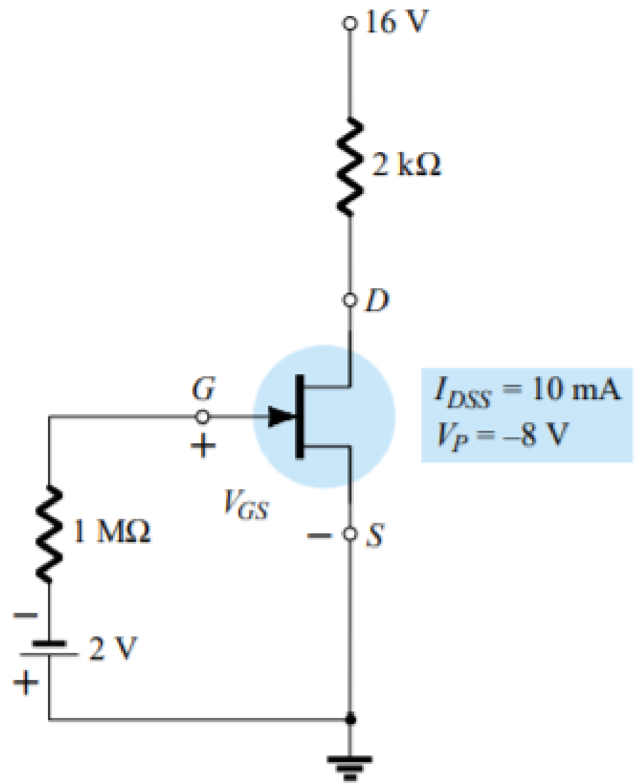
and $$\boxed{V_G = V_{GS}} \quad (6.9)$$



Example-1

Determine the following for the network of Fig. 6.6.

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_D.
(e) V_G.
(f) V_S.



Analytical Approach

Mathematical Approach:

(a) $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

(b) $I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$

$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$

$= \mathbf{5.625\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$

$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$

(d) $V_D = V_{DS} = \mathbf{4.75\ V}$

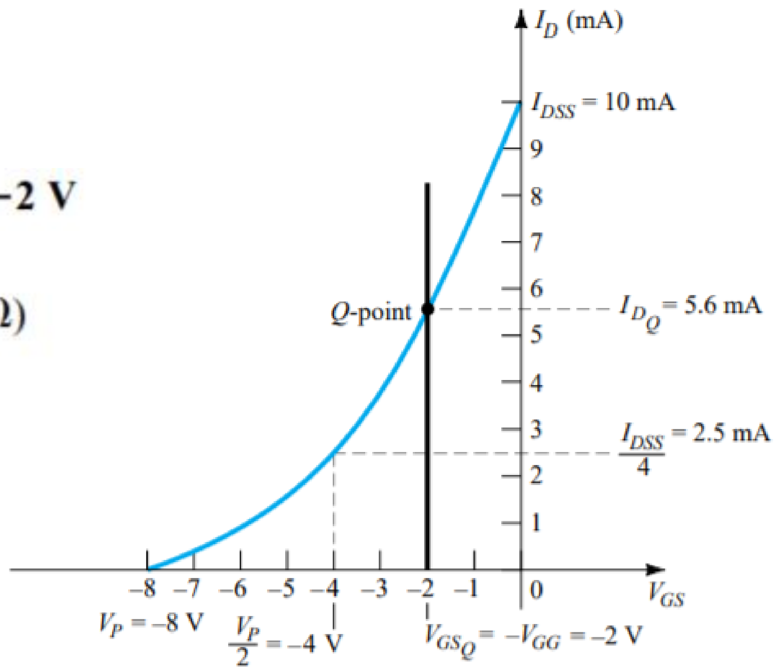
(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

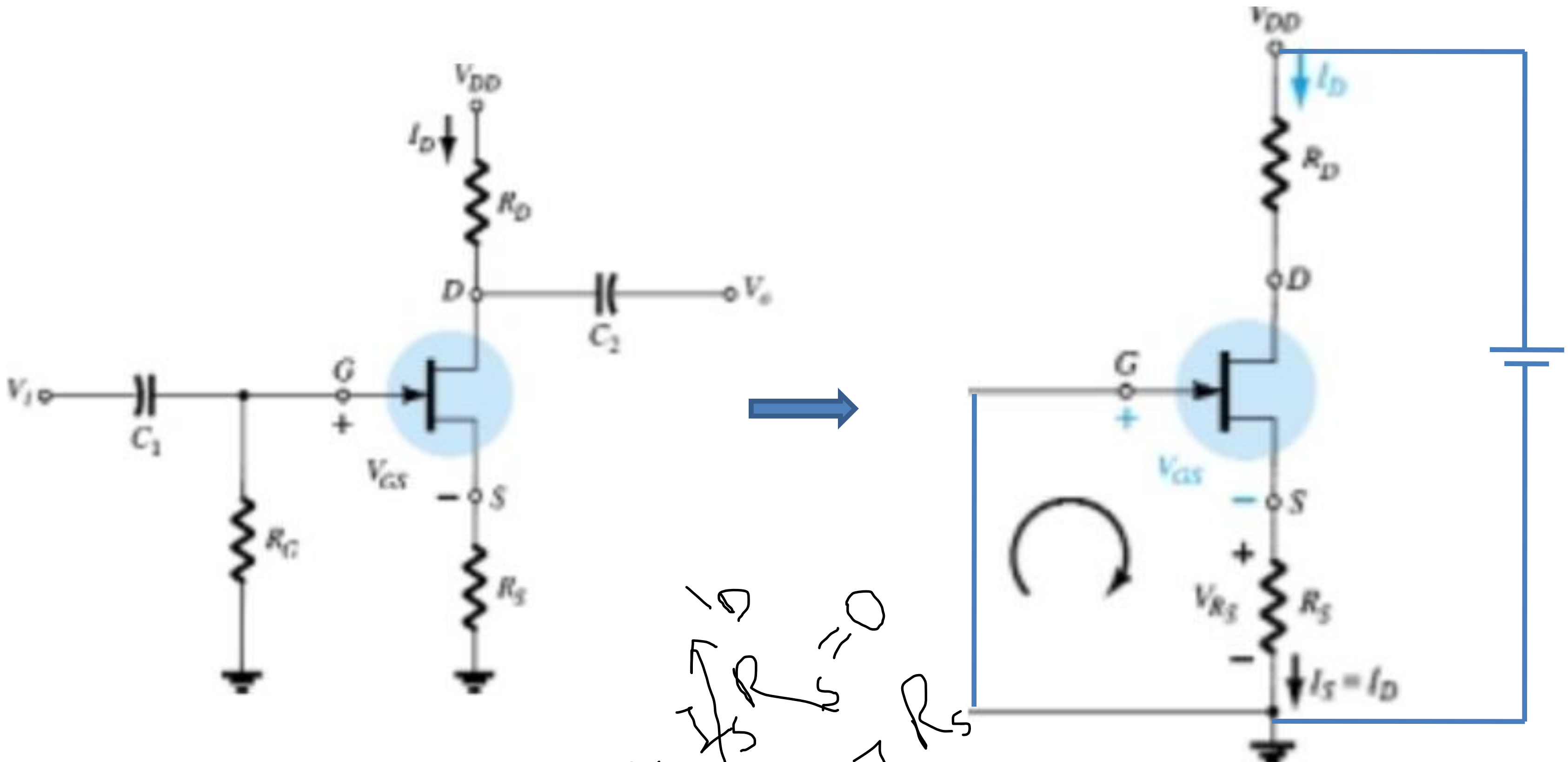
Graphical Approach

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

(b) $I_{D_Q} = \mathbf{5.6\ mA}$
(c) $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.6\ \text{mA})(2\ \text{k}\Omega)$
$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4.8\ V}$
(d) $V_D = V_{DS} = \mathbf{4.8\ V}$
(e) $V_G = V_{GS} = \mathbf{-2\ V}$
(f) $V_S = \mathbf{0\ V}$



Self bias circuit



I_D

$+V_{GS} + I_S R_S = 0$

$V_{GS} = -I_D R_S$

Finding V_{GS}

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 6.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$\boxed{V_{GS} = -I_D R_S}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

or

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, an equation of the following form can be obtained:

$$I_D^2 + K_1 I_D + K_2 = 0$$

Graphical Method

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The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and $$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but $$I_D = I_S$$

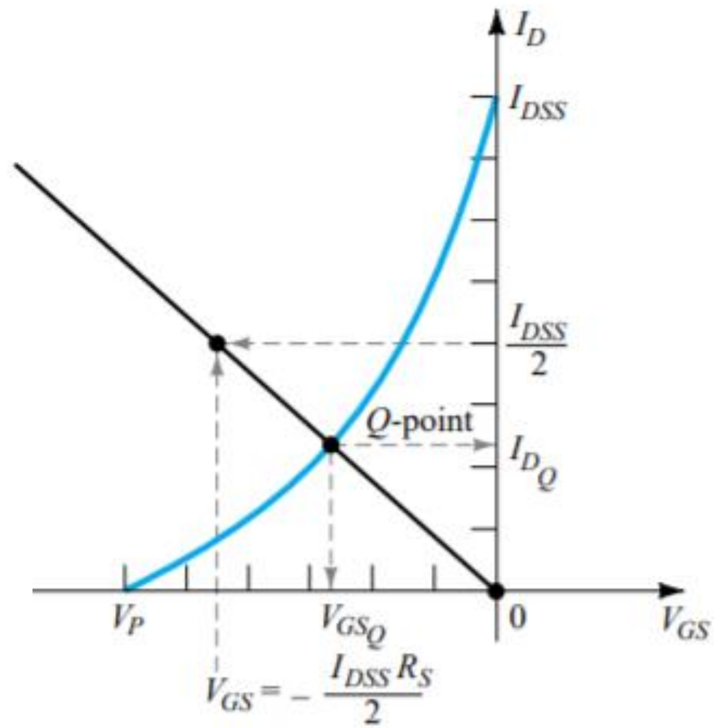
and $$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \qquad (6.11)$$

In addition:

$$\boxed{V_S = I_D R_S} \qquad (6.12)$$

$$\boxed{V_G = 0\ \mathrm{V}} \qquad (6.13)$$

and $$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}} \qquad (6.14)$$

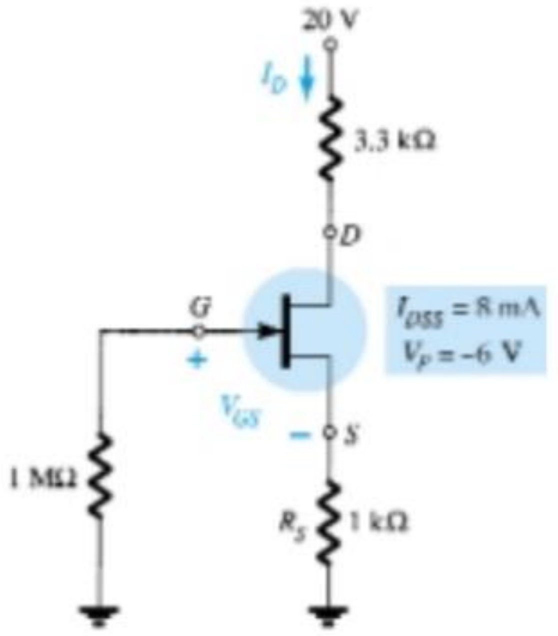


Example-2

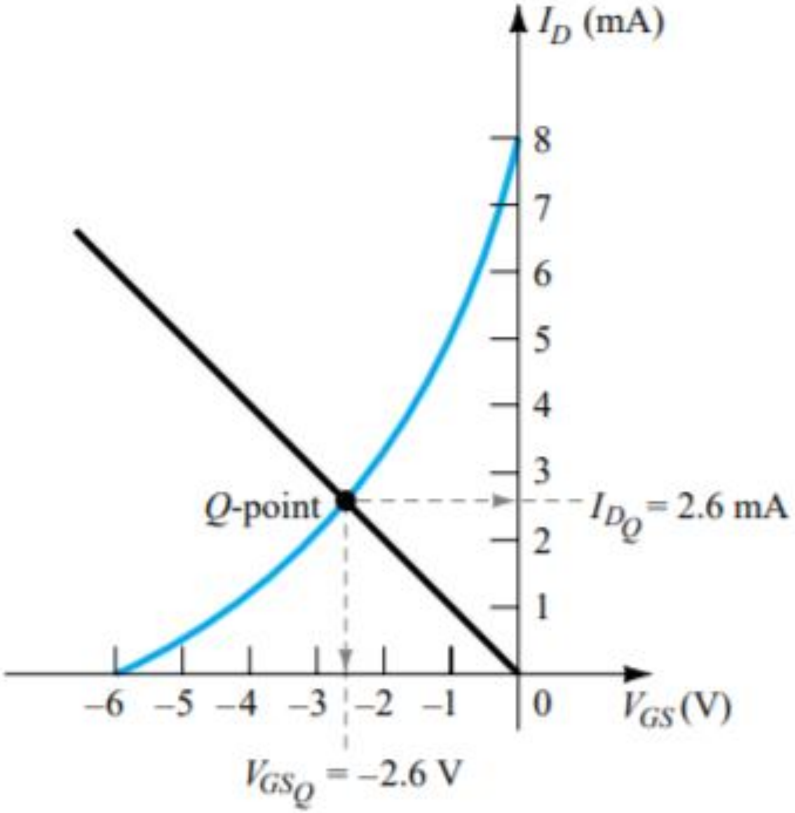
EXAMPLE 6.2

Determine the following for the network of Fig. 6.12.

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_S.
(e) V_G.
(f) V_D.



Solution



(b) At the quiescent point:

$$I_{D_Q} = \mathbf{2.6\ mA}$$

(c) Eq. (6.11): $V_{DS} = V_{DD} - I_D(R_S + R_D)$
$= 20\ \text{V} - (2.6\ \text{mA})(1\ \text{k}\Omega + 3.3\ \text{k}$
$= 20\ \text{V} - 11.18\ \text{V}$
$= \mathbf{8.82\ V}$

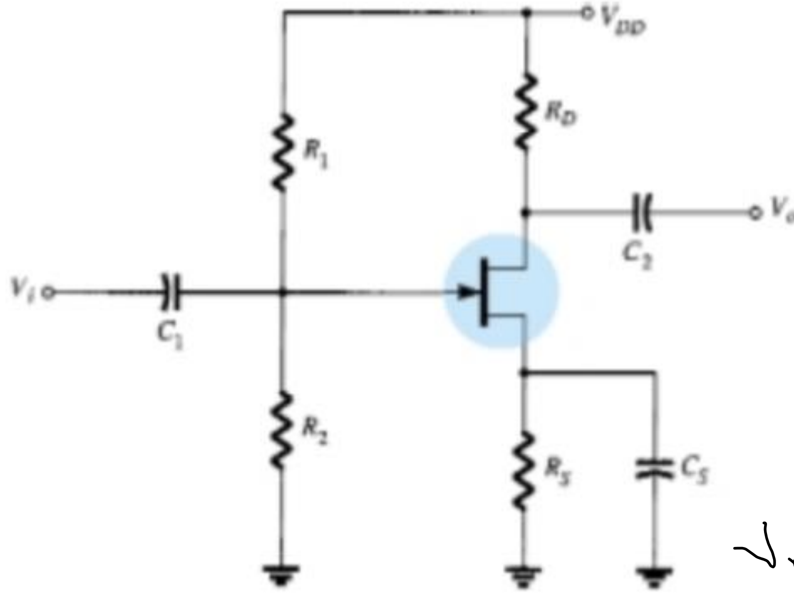
(d) Eq. (6.12): $V_S = I_D R_S$
$= (2.6\ \text{mA})(1\ \text{k}\Omega)$
$= \mathbf{2.6\ V}$

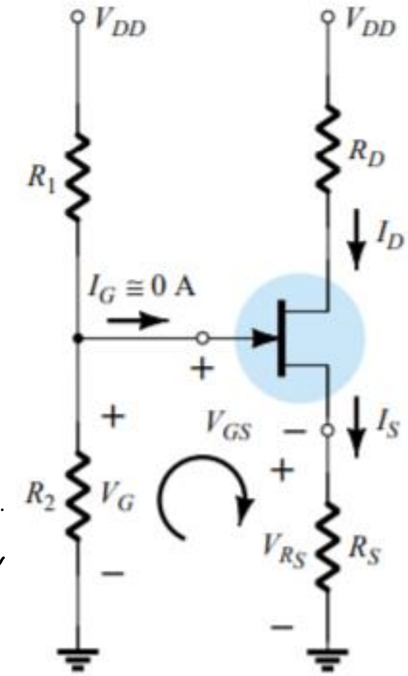
(e) Eq. (6.13): $V_G = \mathbf{0\ V}$

(f) Eq. (6.14): $V_D = V_{DS} + V_S = 8.82\ \text{V} + 2.6\ \text{V} = \mathbf{11.42\ V}$

or $V_D = V_{DD} - I_D R_D = 20\ \text{V} - (2.6\ \text{mA})(3.3\ \text{k}\Omega) = \mathbf{11.42\ V}$

Voltage Divider bias





$$V_G = \frac{V_{DD} * R_2}{R_1 + R_2}$$

Solution

$$\boxed{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}} \qquad (6.15)$$

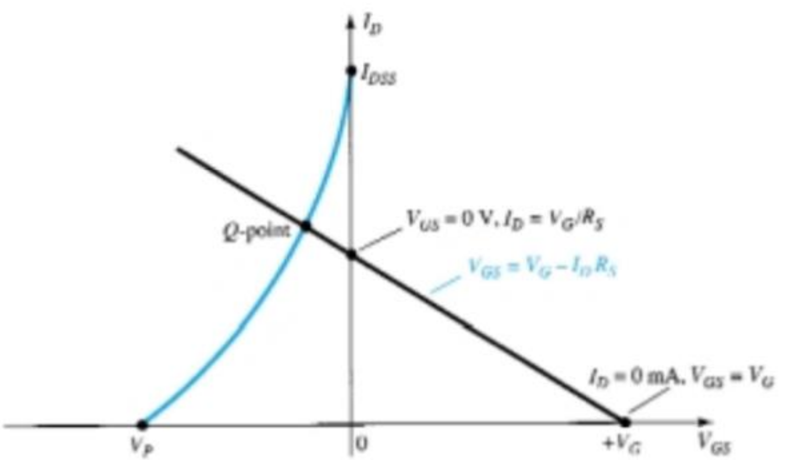
Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 6.21 will result in

$$V_G - V_{GS} - V_{R_S} = 0$$

and
$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

$$\boxed{V_{GS} = V_G - I_D R_S} \qquad (6.16)$$



$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)} \qquad (6.19)$$

$$\boxed{V_D = V_{DD} - I_D R_D} \qquad (6.20)$$

$$\boxed{V_S = I_D R_S} \qquad (6.21)$$

Example-3

Determine the following for the network of Fig. 6.24.

(a) I_{D_Q} and V_{GS_Q}.

(b) V_D.

(c) V_S.

(d) V_{DS}.

(e) V_{DG}.

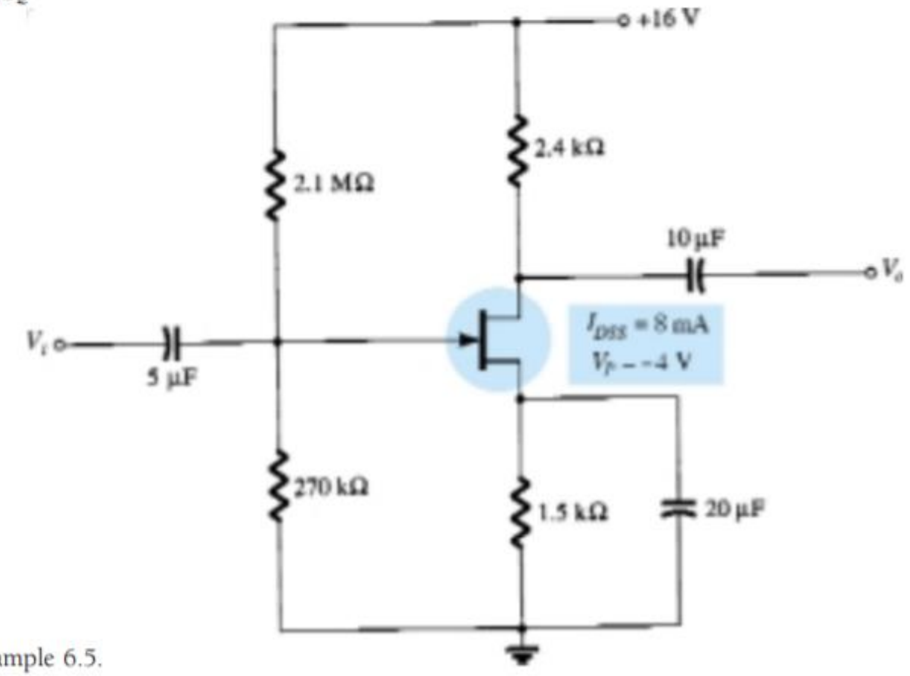


Figure 6.24 Example 6.5.

Solution

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\text{ k}\Omega)(16\text{ V})}{2.1\text{ M}\Omega + 0.27\text{ M}\Omega}$$

$$= 1.82\text{ V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\text{ V} - I_D(1.5\text{ k}\Omega)$$

When $I_D = 0$ mA:

$$V_{GS} = +1.82\text{ V}$$

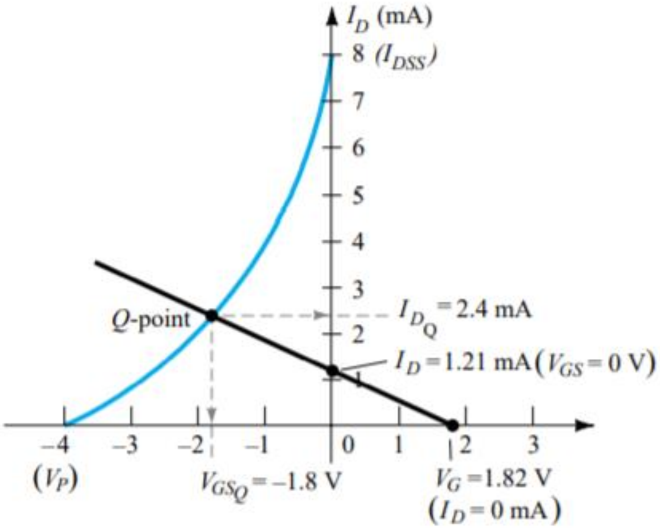


Figure 6.25 Determining the Q-point for the network of Fig. 6.24.

(b) $V_D = V_{DD} - I_D R_D$

$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega)$

$= \mathbf{10.24\text{ V}}$

(c) $V_S = I_D R_S = (2.4\text{ mA})(1.5\text{ k}\Omega)$

$= \mathbf{3.6\text{ V}}$

(d) $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega + 1.5\text{ k}\Omega)$

$= \mathbf{6.64\text{ V}}$

or $V_{DS} = V_D - V_S = 10.24\text{ V} - 3.6\text{ V}$

$= \mathbf{6.64\text{ V}}$

Common Gate Configuration

Practice yourself and send me your feedback, if any.

MOSFET Biasing

DEPLETION-TYPE MOSFETs

The primary difference from JFET is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS}.

EXAMPLE 6.7 For the n-channel depletion-type MOSFET of Fig. 6.29, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS}.

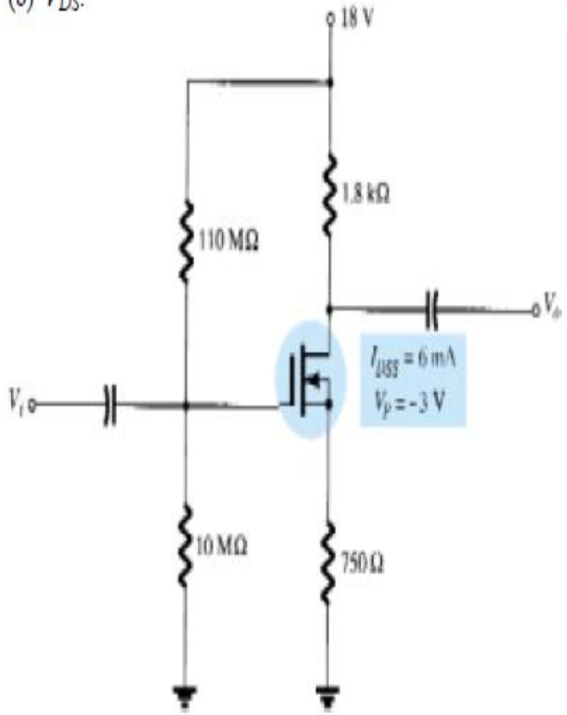


Figure 6.29 Example 6.7

Solution

(a) For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}(1.778)$$

$$= 10.67\text{ mA}$$

The resulting transfer curve appears in Fig. 6.30. Proceeding as described for JFETs, we have:

$$\text{Eq. (6.15):}\quad V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$

$$\text{Eq. (6.16):}\quad V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

MOSFET Biasing

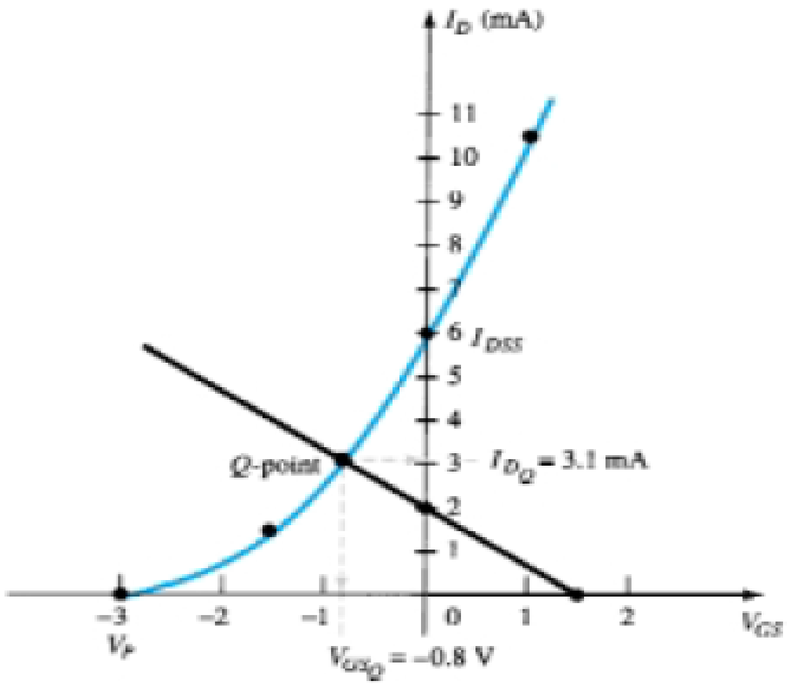


Figure 6.30 Determining the Q-point for the network of Fig. 6.29.

(b) Eq. (6.19): $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$$= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega)$$

$$\cong 10.1\text{ V}$$

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{750\ \Omega} = 2\text{ mA}$$

The plot points and resulting bias line appear in Fig. 6.30. The resulting operating point:

$$I_{D_Q} = \mathbf{3.1\ mA}$$

$$V_{GS_Q} = \mathbf{-0.8\ V}$$

Enhancement type MOSFET biasing

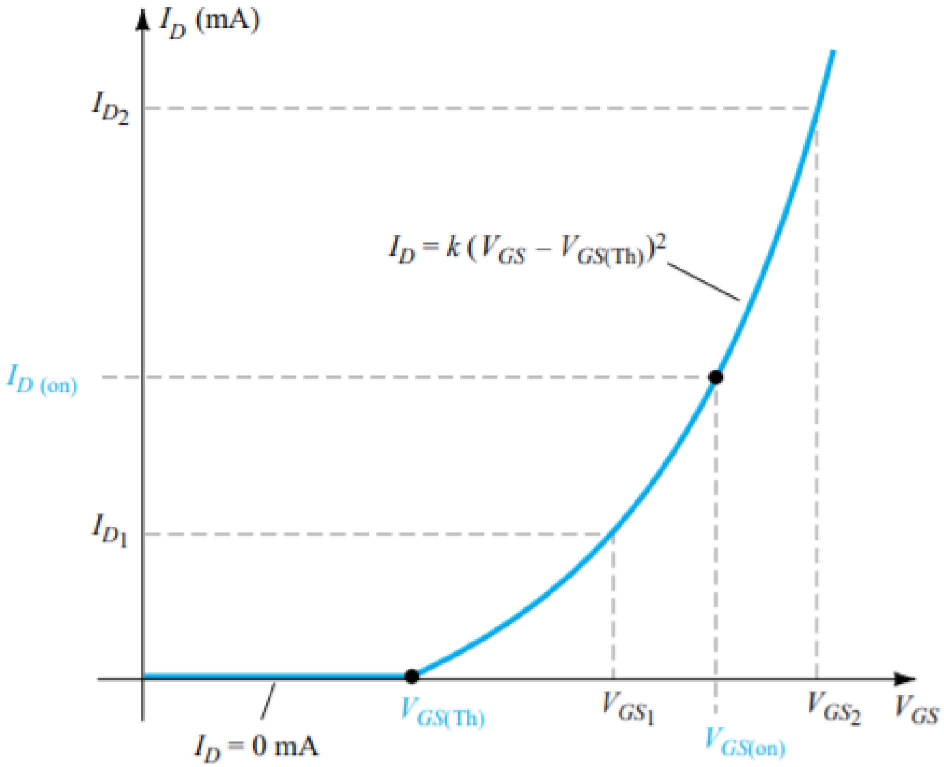


Figure 6.35 Transfer characteristics of an *n*-channel enhancement-type MOSFET.

Feedback biasing

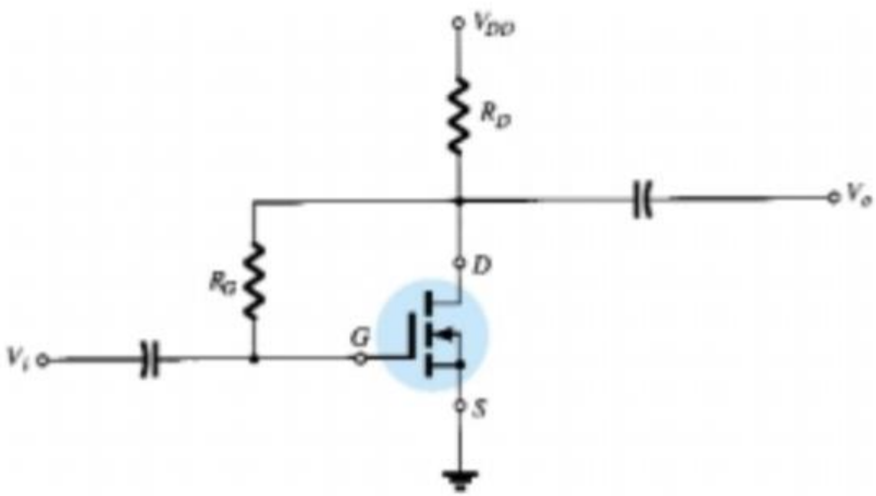


Figure 6.36 Feedback biasing arrangement.

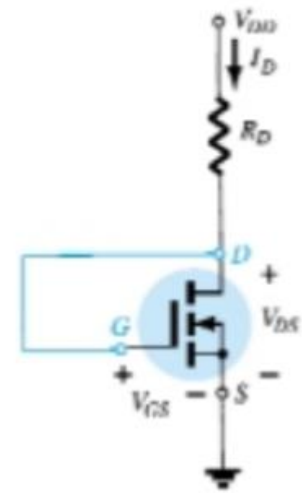
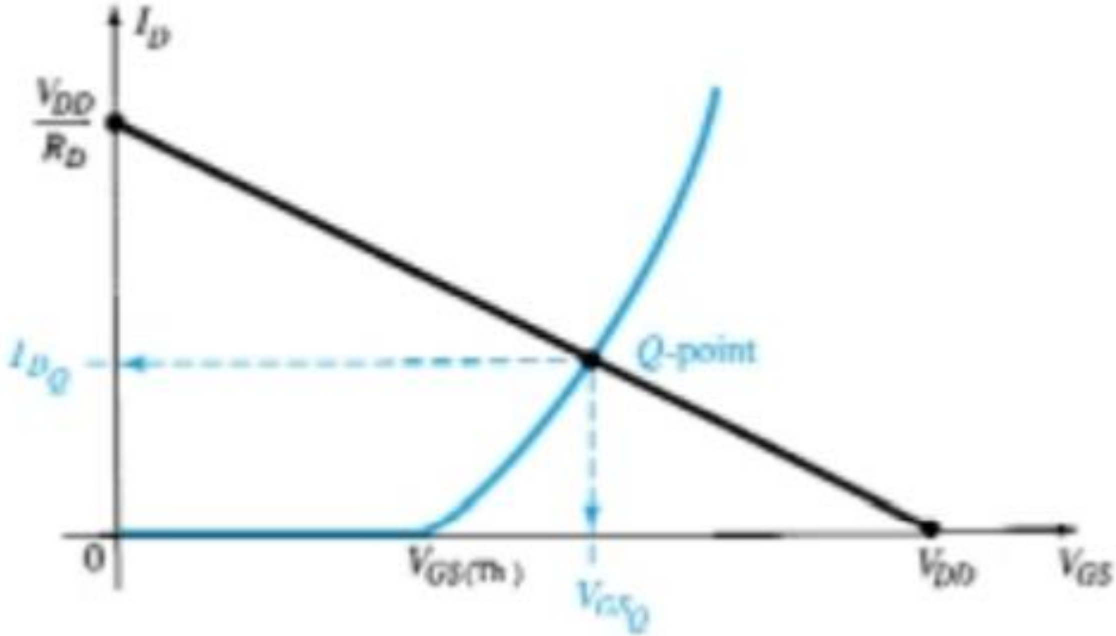


Figure 6.37 DC equivalent of the network of Fig. 6.36.

Analysis

$$V_{GS} = V_{DD} - I_D R_D$$



Example-1

Determine I_{D_Q} and V_{DS_Q} for the enhancement-type MOSFET of Fig. 6.39.

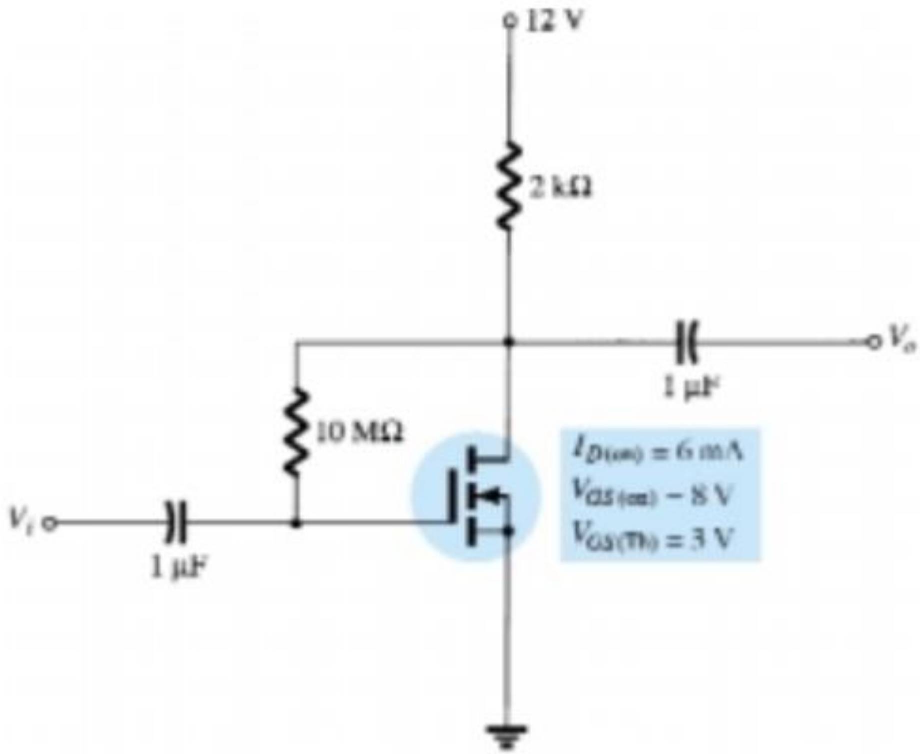
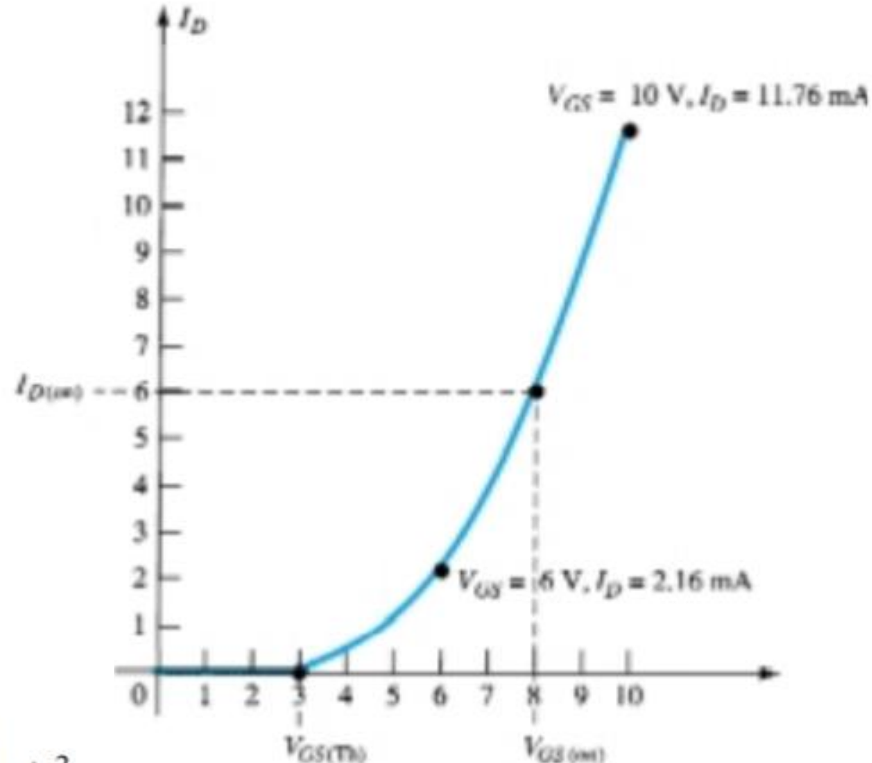


Figure 6.39 Example 6.11.

Solution



Finding k:

$$\text{Eq. (6.26):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{A/v}^2$$

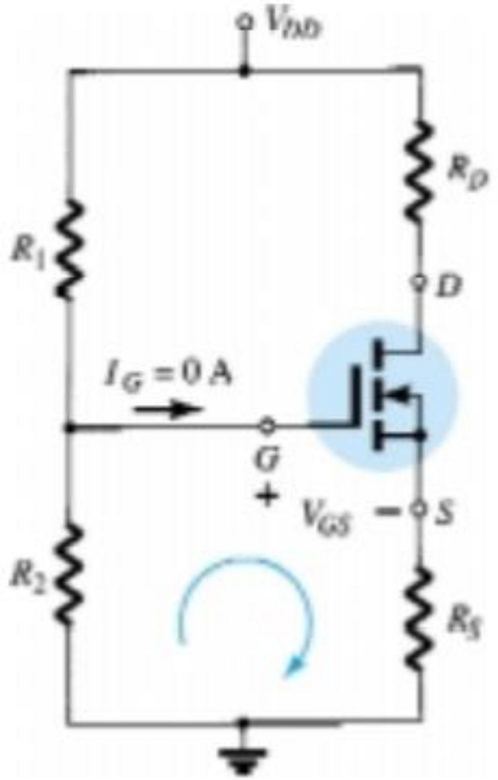
$$= \mathbf{0.24 \times 10^{-3}\ A/V^2}$$

(between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$

$$= 2.16\text{ mA}$$

Voltage divider bias



$$\boxed{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}}$$

$$+V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)}$$

Example-2

Determine I_{DQ}, V_{GSQ}, and V_{DS} for the network of Fig. 6.43.

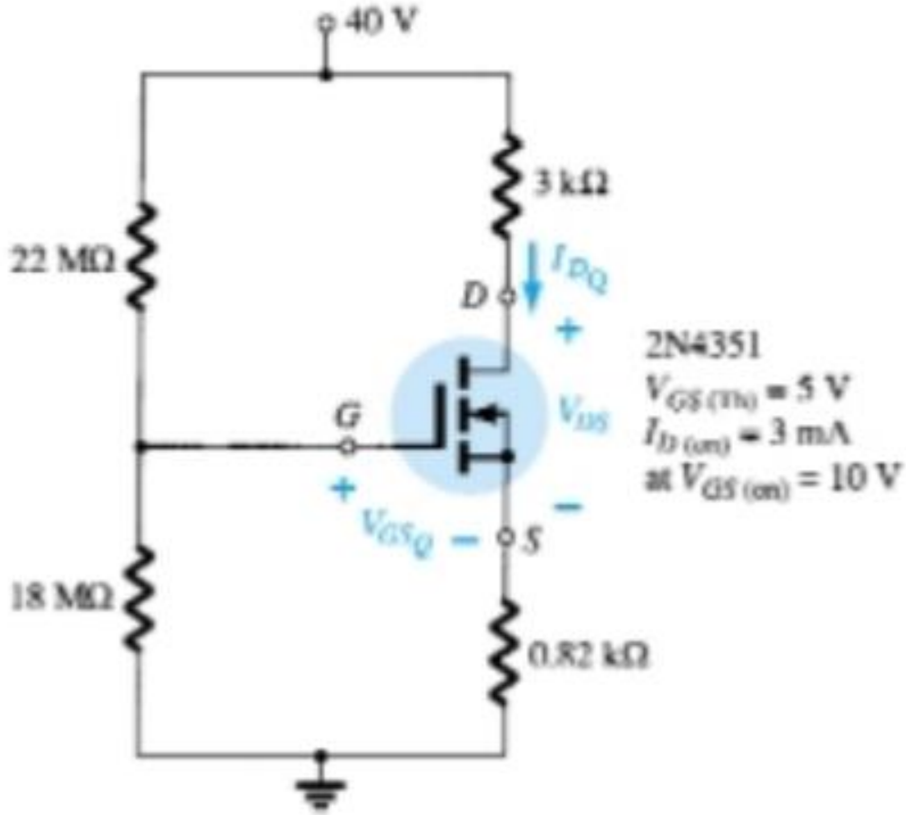


Figure 6.43 Example 6.12.

Solution

$$V_{GS(\text{Th})} = 5\text{ V}, \qquad I_{D(\text{on})} = 3\text{ mA with } V_{GS(\text{on})} = 10\text{ V}$$

$$\text{Eq. (6.26):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\text{ M}\Omega)(40\text{ V})}{22\text{ M}\Omega + 18\text{ M}\Omega} = 18\text{ V}$$

$$V_{GS} = V_G - I_D R_S = 18\text{ V} - I_D(0.82\text{ k}\Omega)$$

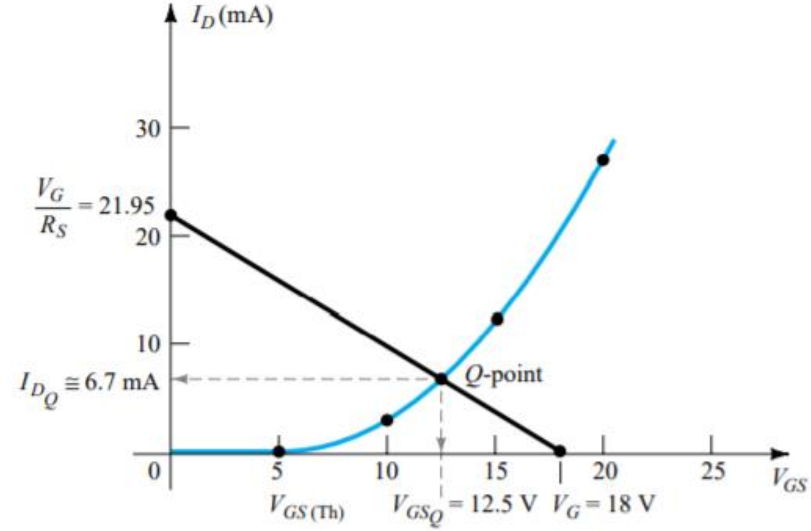


Figure 6.44 Determining the Q-point for the network of Example 6.12.

$$I_{D_Q} \cong \mathbf{6.7\text{ mA}}$$

$$V_{GS_Q} = \mathbf{12.5\text{ V}}$$

$$\text{Eq. (6.33):} \quad V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\text{ V} - (6.7\text{ mA})(0.82\text{ k}\Omega + 3.0\text{ k}\Omega)$$

$$= 40\text{ V} - 25.6\text{ V}$$

$$= \mathbf{14.4\text{ V}}$$

P-Channel FETs

Practice yourself and send me
your feedback, if any.