FET
AC small signal analysis

Text Book

Electronic Devices and Circuit Theory

by R Boylestad and L Nashelsky

Basics on FET Amplifier

- Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance.

- They are also considered low-power consumption configurations with good frequency range and minimal size and weight.

- Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs.

- BJT had an amplification factor β(beta), the FET has a transconductance factor, *gm*.

JFET small signal model

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Graphical Determination of g_m

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}}$$

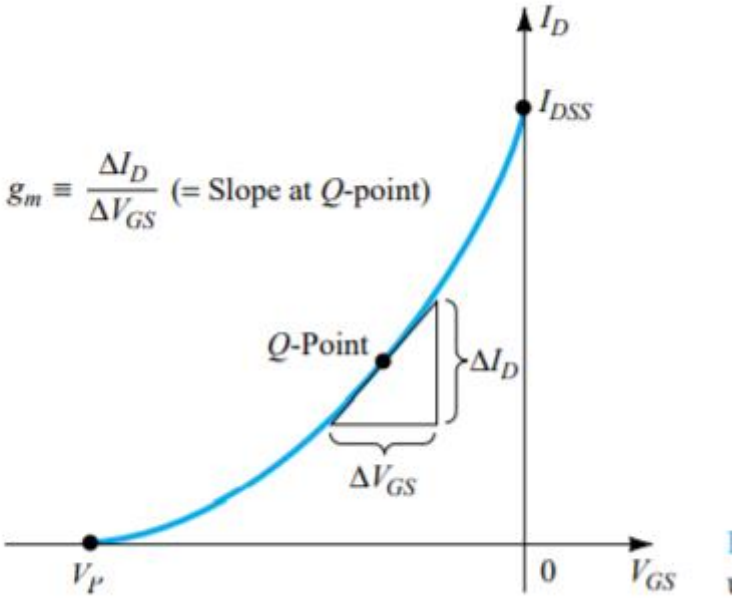


Figure 9.1 Definition of g_m using transfer characteristic.

FET small signal model

Mathematical Definition of g_m

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{Q\text{-pt.}} = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

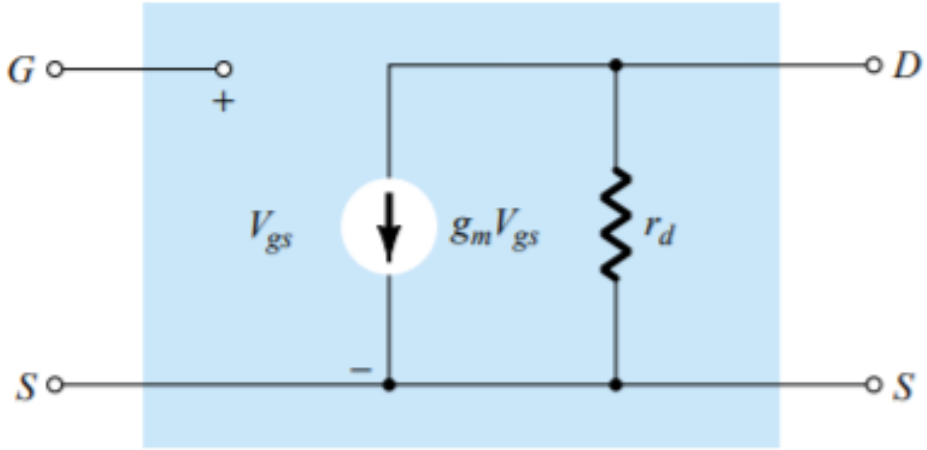
$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

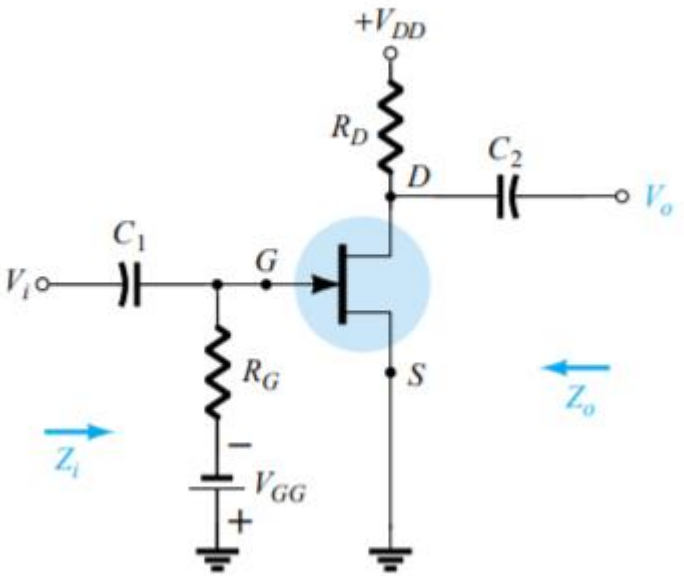
$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}}$$

JFET AC equivalent circuit/model

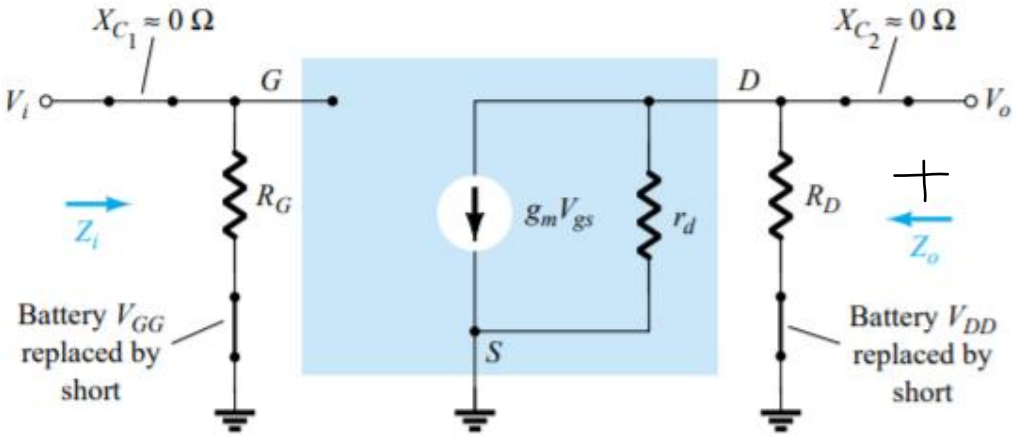


Fixed bias circuit (JFET and D-MOSFET)



$$Z_i = R_G \quad \Omega$$

$$Z_0 = r_d \,\|\, R_D \cong R_D \quad \Omega$$



Voltage gain,

$A_V = -g_m R_D$

Voltage gain

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

$$V_{gs} = V_i$$

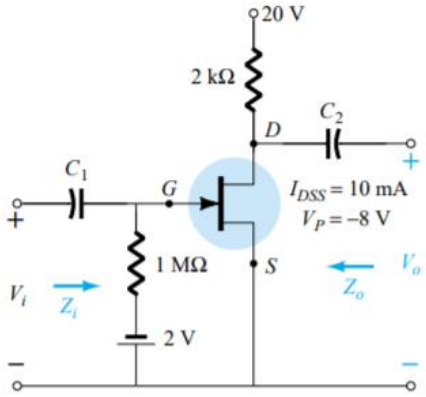
$$V_o = -g_m V_i(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D$$

$r_d \geq 10R_D$

Example-3



(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

(e) $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$

$= \mathbf{-3.48}$

(f) $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

JFET SELF-BIAS CONFIGURATION (Bypassed R_S)

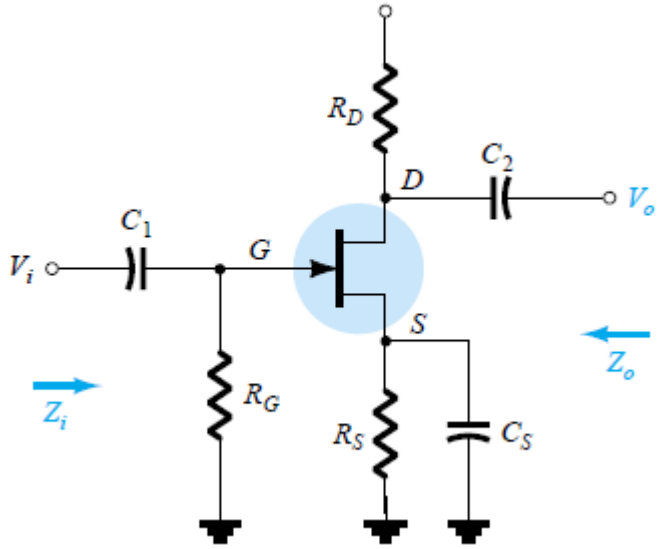
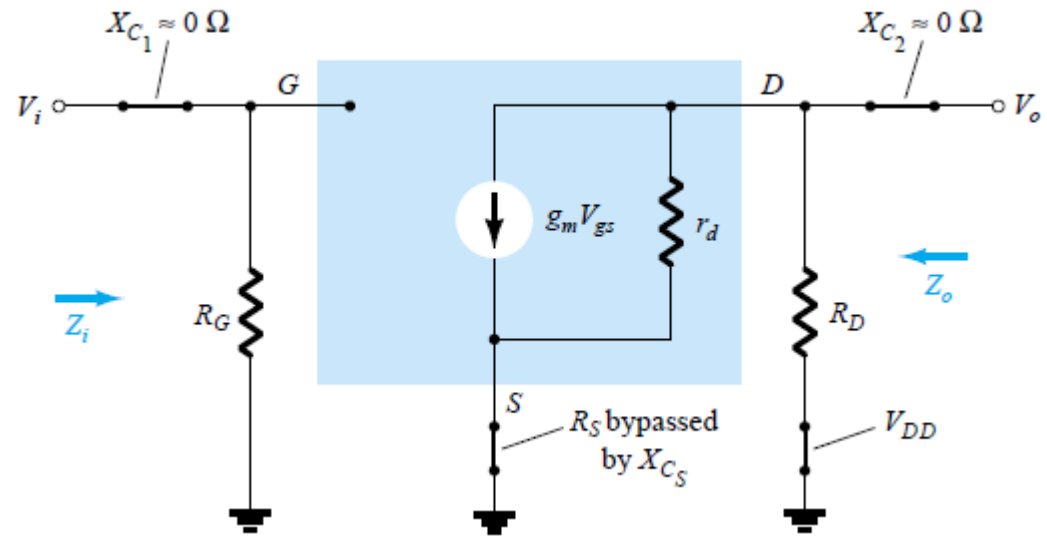


Figure 9.15 Self-bias JFET configuration

JFET SELF-BIAS CONFIGURATION (Bypassed R_S)



$$Z_i = R_G$$

Z_o:

$$Z_o = r_d \| R_D$$

If $r_d \geq 10R_D$,

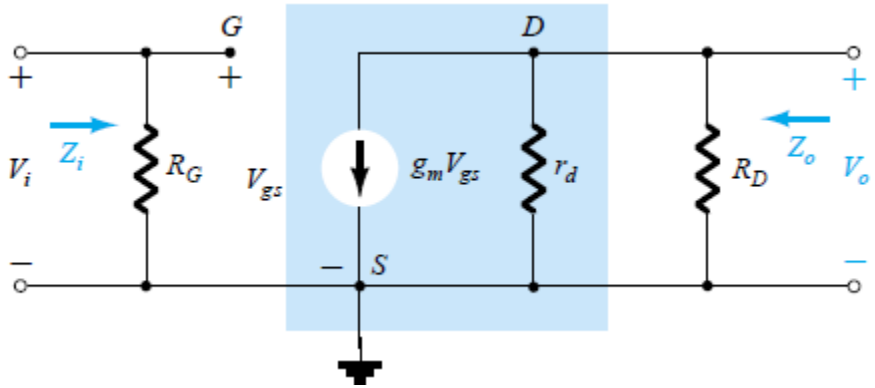
$$Z_o \cong R_D \quad r_d \geq 10R_D$$

A_v:

$$A_v = -g_m(r_d \| R_D)$$

If $r_d \geq 10R_D$,

$$A_v = -g_m R_D \quad r_d \geq 10R_D$$



Voltage divider bias

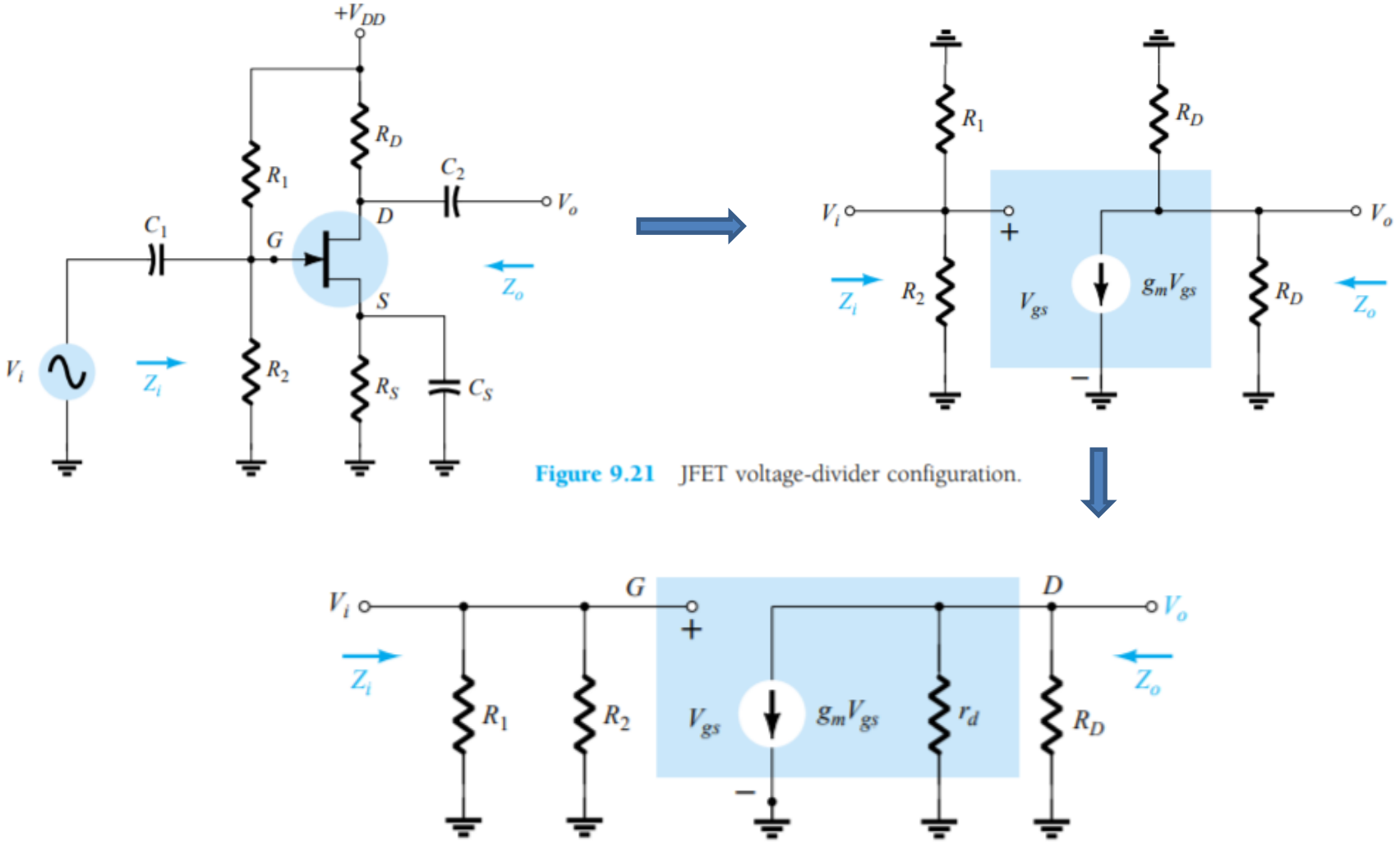


Figure 9.21 JFET voltage-divider configuration.

DEPLETION-TYPE MOSFETs

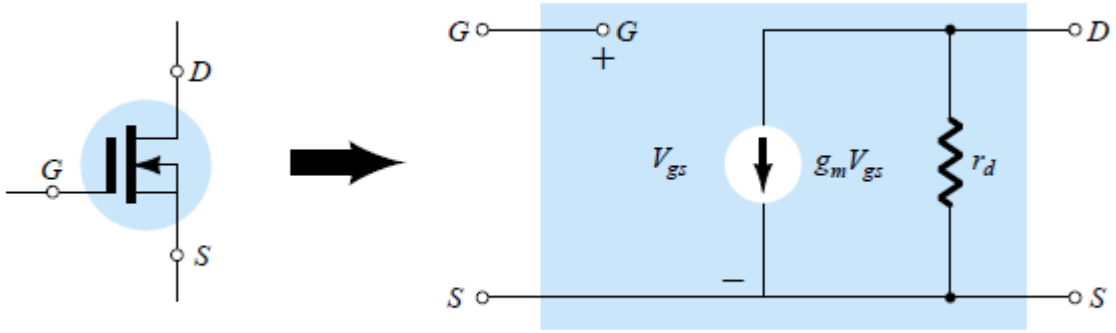


Figure 9.33 D-MOSFET ac equivalent model.

ENHANCEMENT-TYPE MOSFETs

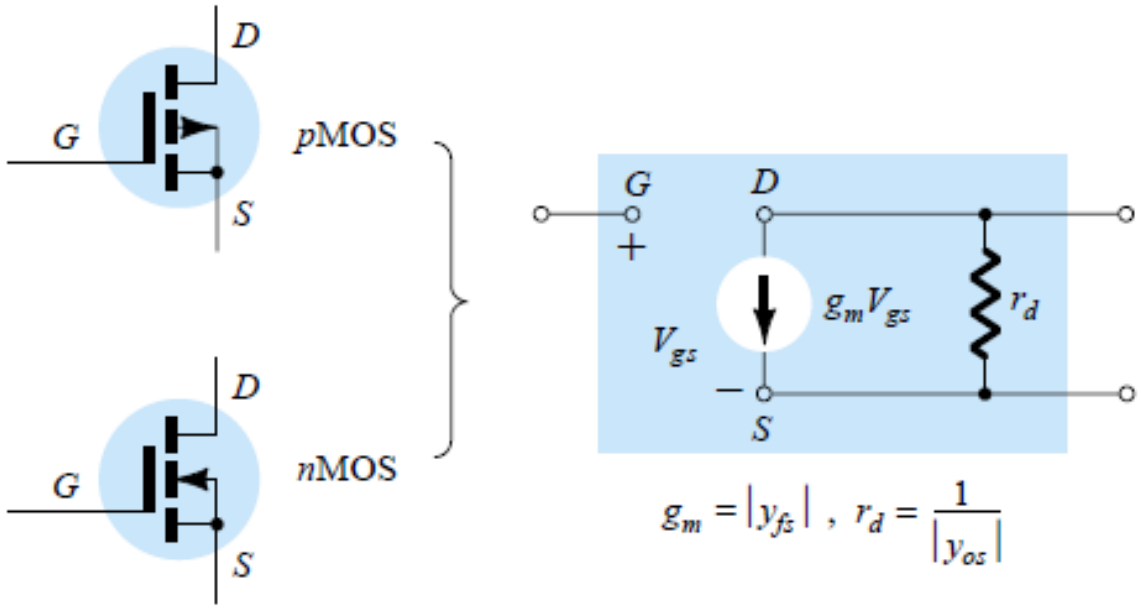


Figure 9.36 Enhancement MOSFET ac small-signal model.

Practice yourself by including other remaining configurations and send me

your feedback, if any.