BJT Biasing-2

Text Book

Electronic Devices and Circuit Theory

by R Boylestad and L Nashelsky

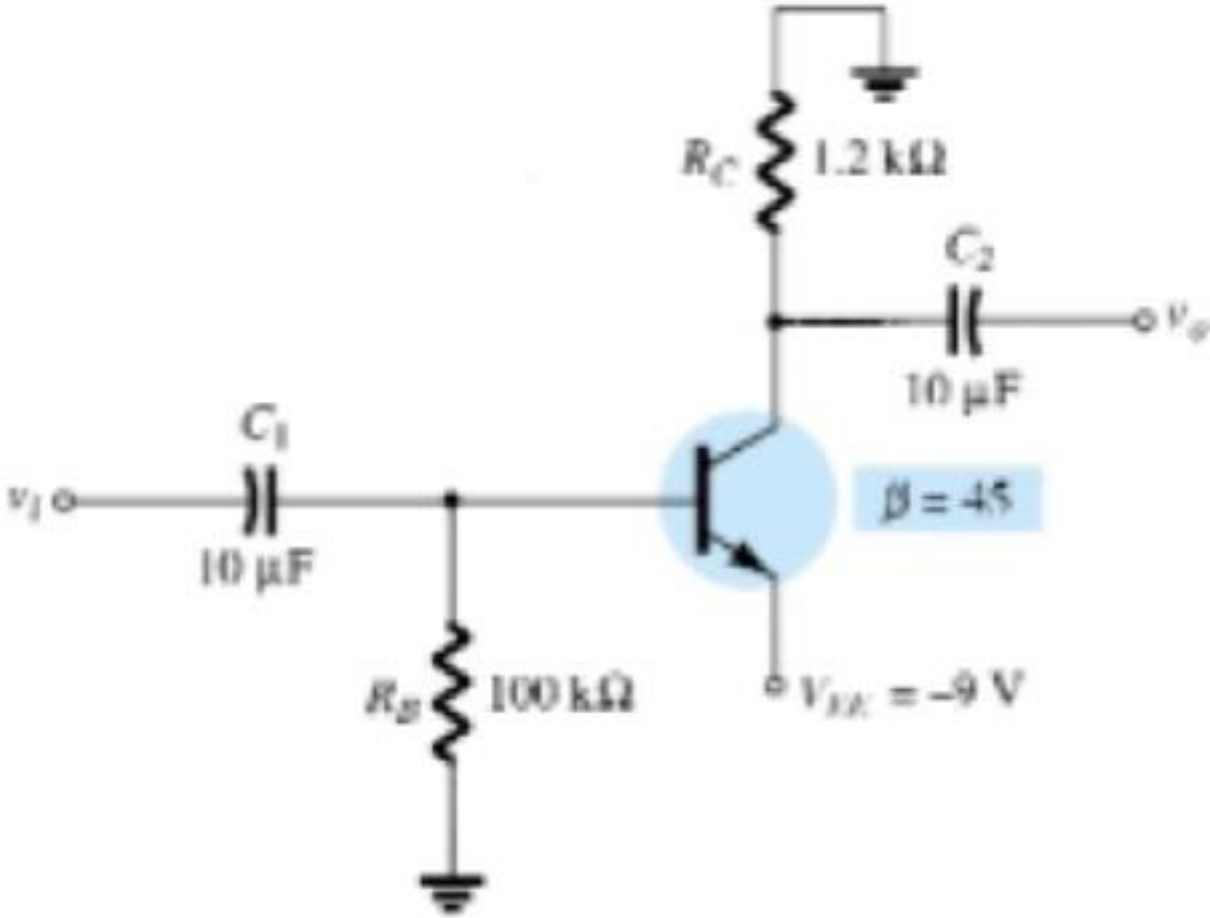
Basic relations

$$\boxed{V_{BE} = 0.7\text{ V}}$$

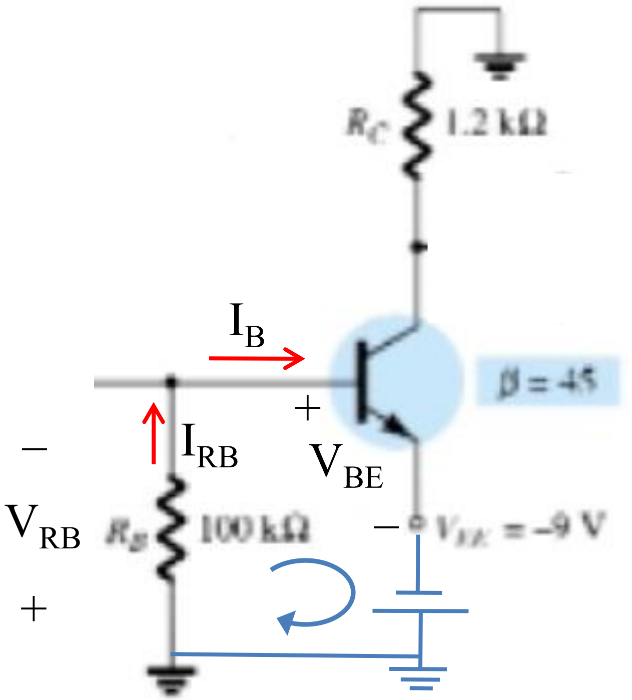
$$\boxed{I_E = (\beta + 1)I_B \cong I_C}$$

$$\boxed{I_C = \beta I_B}$$

Biasing circuit



Analysis



Applying KVL around the input loop:

$$+V_{RB} + V_{BE} - 9 = 0$$

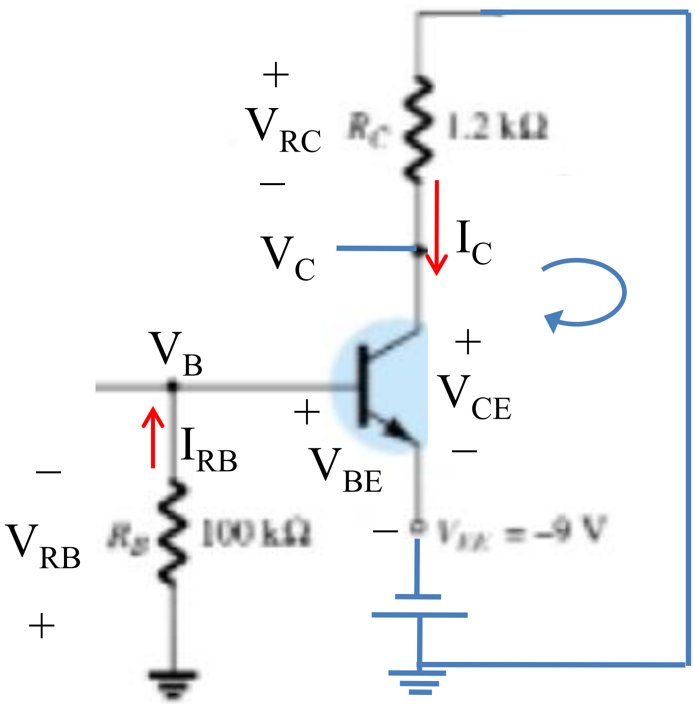
$$I_B R_B + 0.7 - 9 = 0$$

$$I_B = \frac{8.3}{100} mA = 83 \mu A$$

Now,

$$I_C = \beta I_B = 45 \times 83 = 3.735\ mA$$

Analysis (continue..)



Applying KVL around the output loop:

$$V_{RC} + V_{CE} - 9 = 0$$

$$V_{CE} = 9 - I_C R_C = 4.52 \text{ V}$$

Now,

$$V_C = -V_{RC} = -I_C R_C = -4.48\text{V}$$

$$\text{or } V_C = -V_{CE} + V_{EE}$$

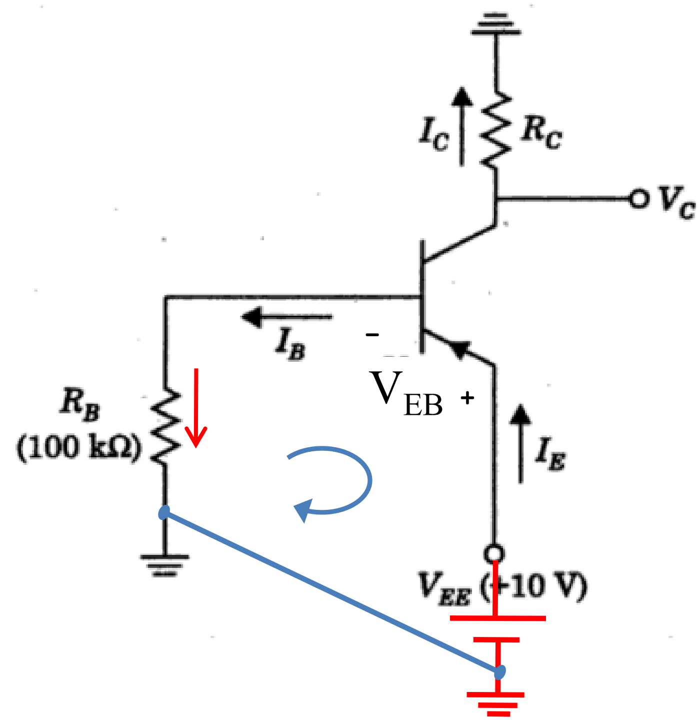
And,

$$V_B = -V_{RB} = -I_B R_B = -8.3\text{V}$$

$$\text{or } V_B = V_{BE} - V_{EE}$$

PNP Transistor

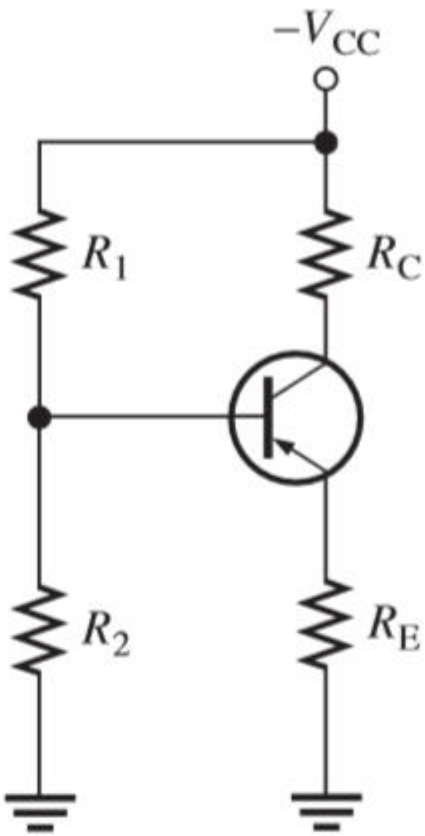
Applying KVL around the input loop:

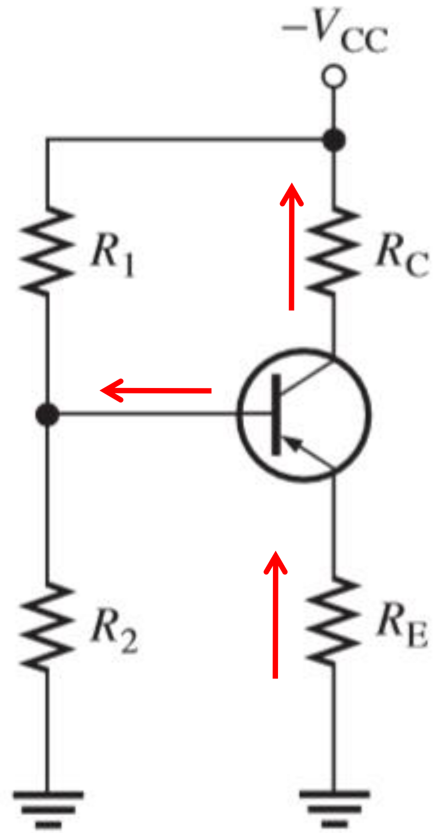


$$V_{EE} - V_{EB} - I_B R_B = 0$$

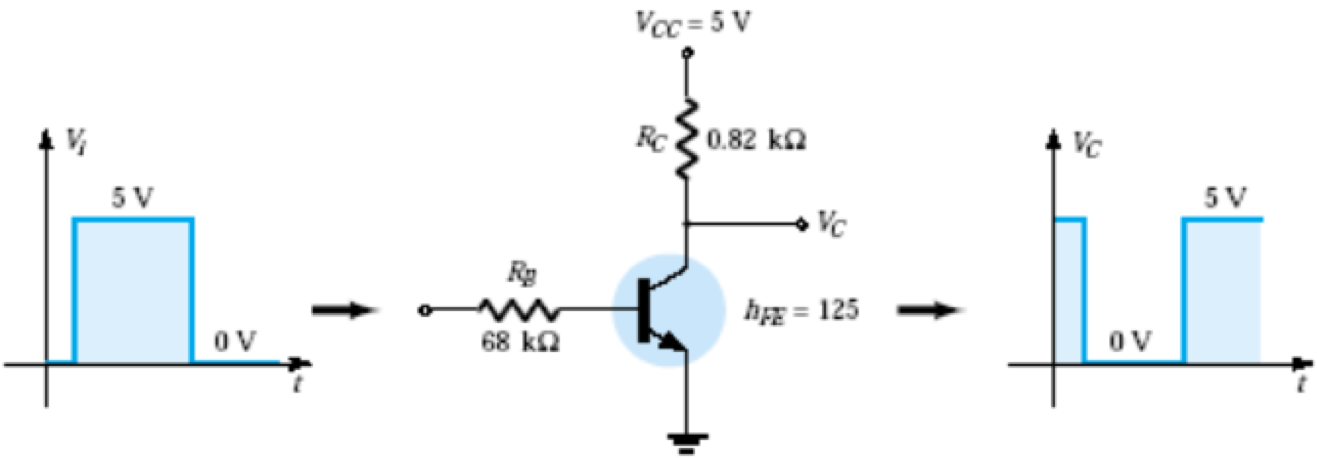
$$I_B = \frac{V_{EE} - V_{EB}}{R_B} = \frac{10 - 0.7}{100k} = 93\mu A$$

Voltage divider bias





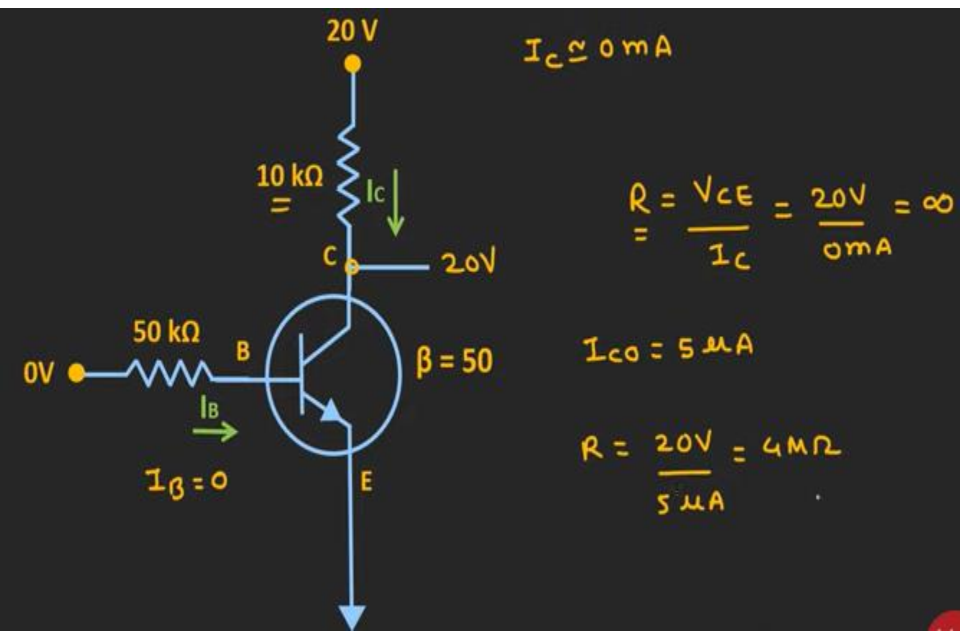
TRANSISTOR SWITCHING NETWORKS



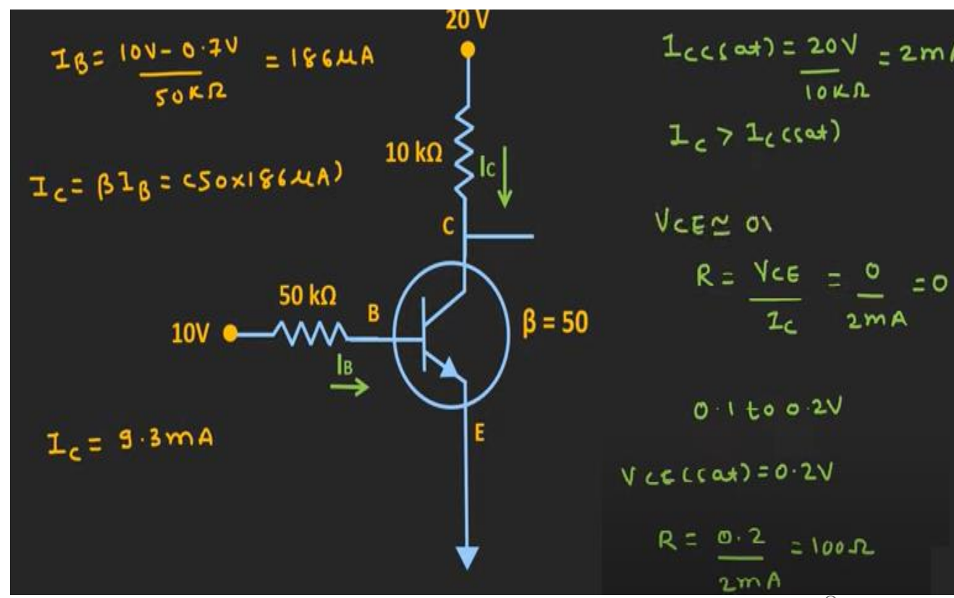
(a)

**hFE refers to the forward current gain in a bipolar junction transistor (BJT) in the common-emitter configuration

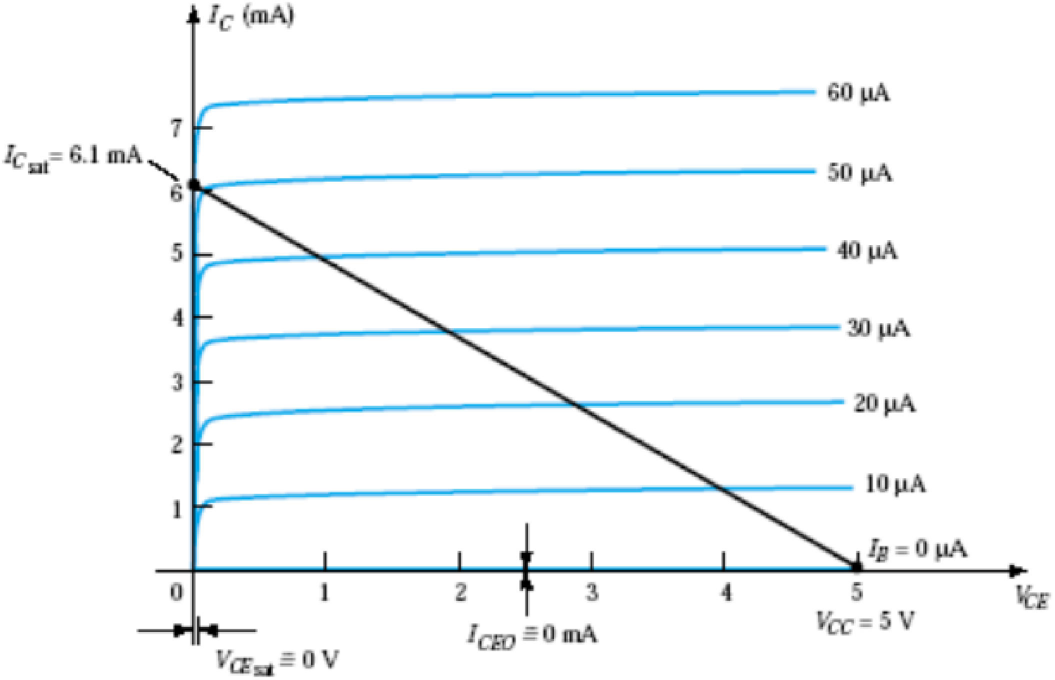
Cutoff region of operation



Saturation region of operation



Confirming operating region



(b)

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = 63\ \mu\text{A}$$

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{5\text{ V}}{0.82\text{ k}\Omega} \cong 6.1\text{ mA}$$

$$I_B = 63\ \mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{6.1\text{ mA}}{125} = 48.8\ \mu\text{A}$$

$$\boxed{I_{C_{sat}} = \frac{V_{CC}}{R_C}}$$

$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

$$\boxed{I_B > \frac{I_{C_{sat}}}{\beta_{dc}}}$$

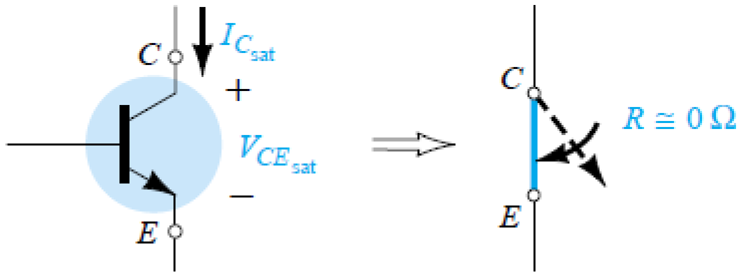


Figure 4.53 Saturation conditions and the resulting terminal resistance.

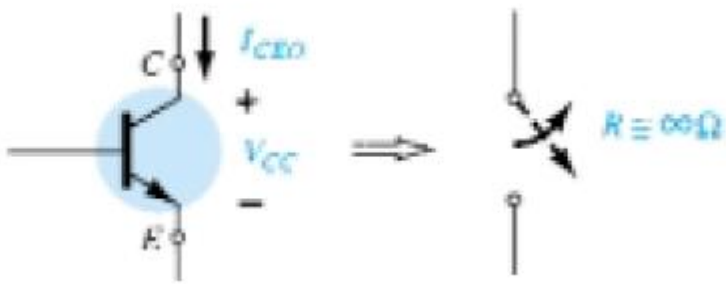


Figure 4.54 Cutoff conditions and the resulting terminal resistance.

Example-4

Determine R_B and R_C for the transistor inverter of Fig. 4.55 if $I_{C_{sat}} = 10$ mA.

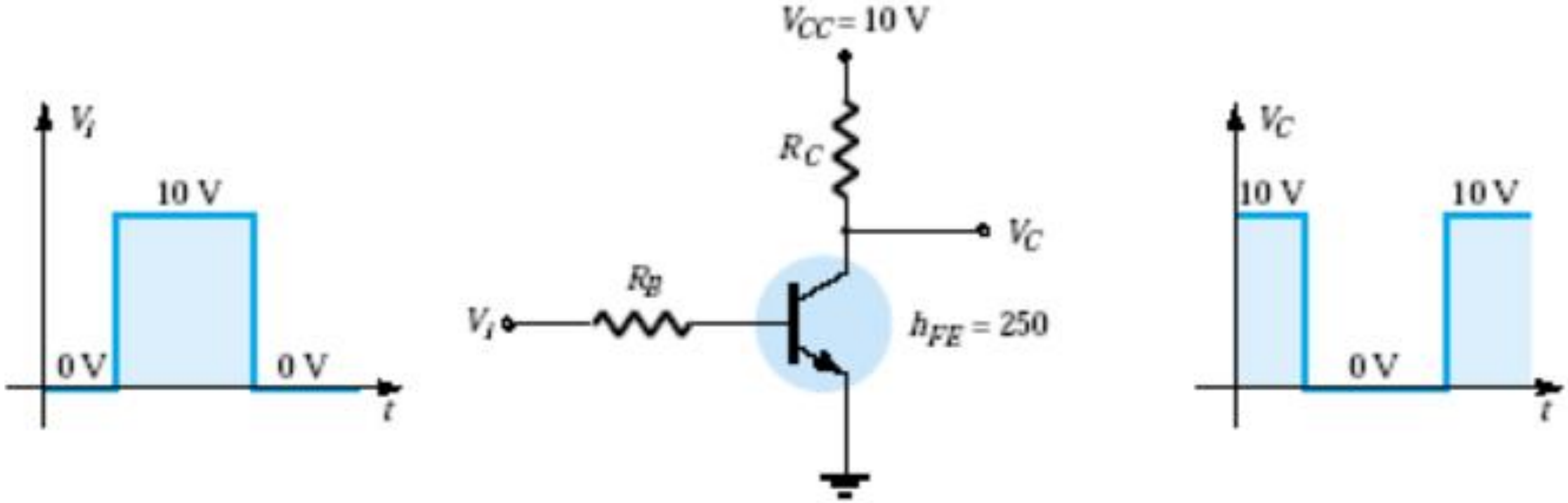


Figure 4.55 Inverter for Example 4.24.

Calculation: To fulfill the inverter design, BJT should operate in saturation mode

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

and

$$10\ \text{mA} = \frac{10\ \text{V}}{R_C}$$

so that

$$R_C = \frac{10\ \text{V}}{10\ \text{mA}} = 1\ \text{k}\Omega$$

At saturation:

$$I_B \cong \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{10\ \text{mA}}{250} = 40\ \mu\text{A}$$

Choosing $I_B = 60\ \mu\text{A}$ to ensure saturation and using

$$I_B = \frac{V_i - 0.7\ \text{V}}{R_B}$$

Calculation (continue..)

we obtain $$R_B = \frac{V_i - 0.7\text{ V}}{I_B} = \frac{10\text{ V} - 0.7\text{ V}}{60\ \mu\text{A}} = 155\text{ k}\Omega$$

Choose $R_B = 150\text{ k}\Omega$, which is a standard value. Then

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{150\text{ k}\Omega} = 62\ \mu\text{A}$$

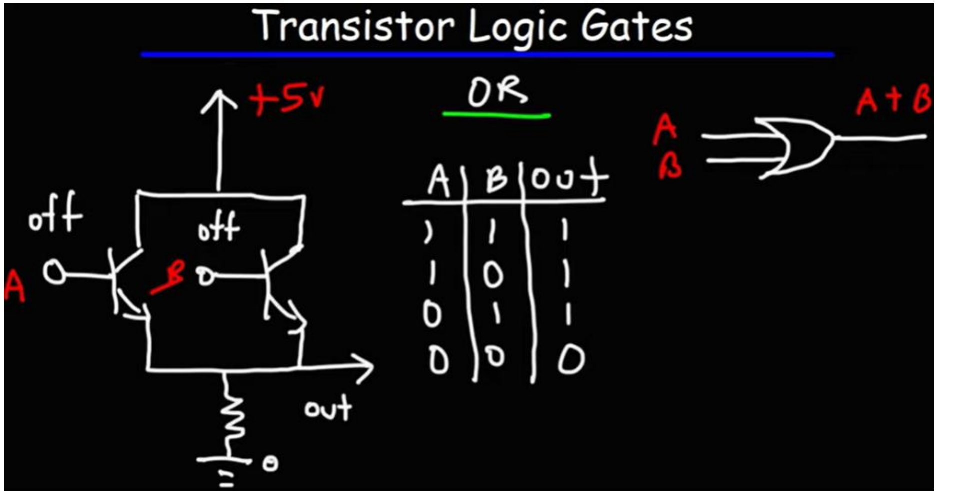
and $$I_B = 62\ \mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = 40\ \mu\text{A}$$

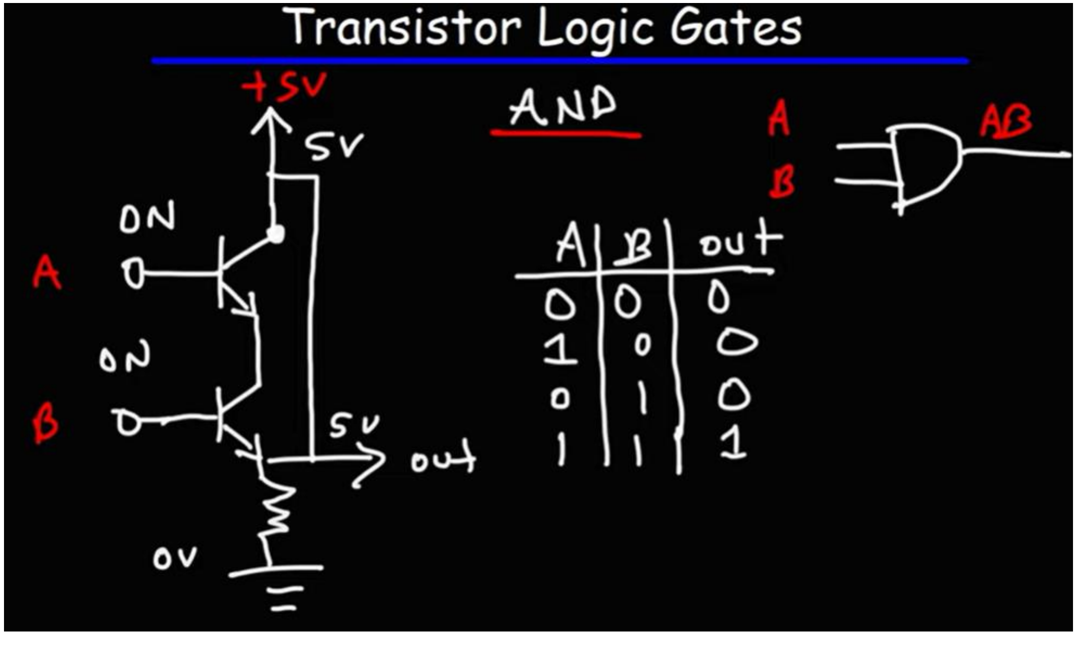
Therefore, use $R_B = \mathbf{150\ k\Omega}$ and $R_C = \mathbf{1\ k\Omega}$.

Transistor Logic Gates - NAND, AND, OR, NOR

Explain how can you design logic gates (AND, OR, NOR,….) by using BJT?????

It is homework??? See the video and learn this.





https://www.youtube.com/watch?v=OWlD7gL9gS0

Bias stability

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

β: increases with increase in temperature

$|V_{BE}|$: decreases about 7.5 mV per degree Celsius (°C) increase in temperature

I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature

Effect of temperature variation

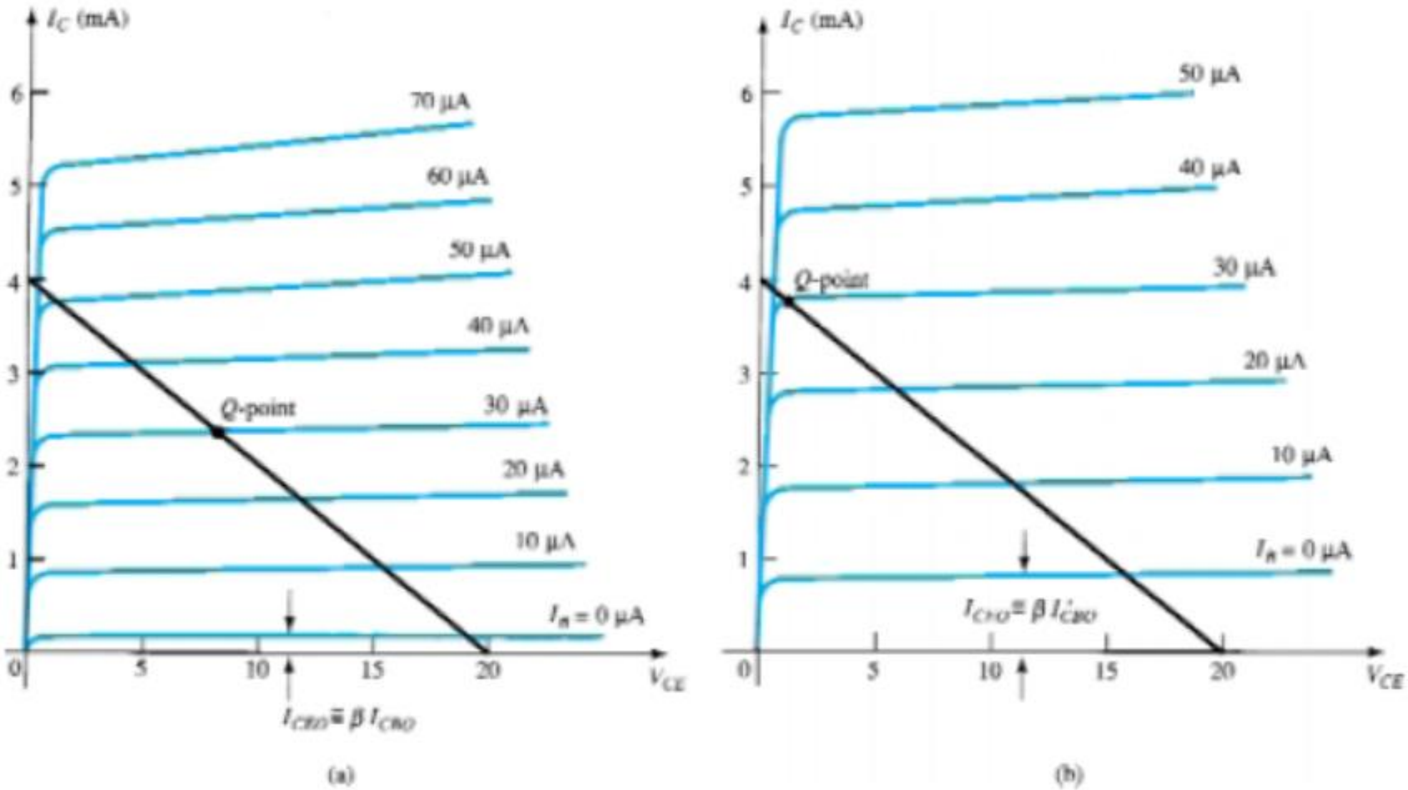


Figure 4.63 Shift in dc bias point (Q-point) due to change in temperature: (a) 25°C; (b) 100°C.

Stability of biasing circuits

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

Fixed bias:

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B}$$

Emitter stabilized bias:

$$I_C = \beta I_B = \beta \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \cong \beta \frac{V_{CC} - V_{BE}}{R_B + \beta R_E}$$

Voltage divider bias:

$$I_C = \beta I_B = \beta \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E} \cong \beta \frac{V_{TH} - V_{BE}}{R_{TH} + \beta R_E}$$

Stability Factor

Bias Stabilization

Stability: It is the measure of the sensitivity of the circuit to the variation in the external parameters

Bias Stabilization

BJT: Collector Current (I_C)

β: Increases with increase in temperature

V_{BE}: Decreases with increase in temperature

I_{CO} (Reverse Saturation Current):
Increases with increase in temperature

Doubles in value with every 10°C increase in temperature

Stability Factor

Stability Factor

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$ V_{BE} and β Constant

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$ I_{CO} and β Constant

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$ I_{CO} and V_{BE} Constant

The above equation could be implemented for all above studied BJT configurations.

Derivation of Stability Factor

Voltage divider Bias for example

Stability Factor

$$\boxed{I_C = \beta I_B + (\beta + 1) I_{CBO}}$$

$$S = \frac{\partial I_C}{\partial I_{CBO}}\bigg|_{V_{BE},\ \beta}$$

$$\frac{\partial I_C}{\partial I_C} = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1)\frac{\partial I_{CBO}}{\partial I_C}$$

$$\Rightarrow 1 - \beta \frac{\partial I_B}{\partial I_C} = (\beta+1) \times \frac{1}{S} \quad \Rightarrow S = \frac{(\beta+1)}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

By using KVL and $I_E = I_C + I_B$

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

$$\Rightarrow V_{TH} - I_B R_{TH} - V_{BE} - (I_C + I_B) R_E = 0$$

$$\Rightarrow I_B (R_{TH} + R_E) = V_{TH} - V_{BE} - I_C R_E$$

$$\Rightarrow I_B = \frac{V_{TH} - V_{BE} - I_C R_E}{R_{TH} + R_E}$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_{TH} + R_E}$$

Derive the stability factor equations for Voltage divider bias, emitter stabilised bias , …………configurations. For example,….

$S(I_{CO})$: EMITTER-BIAS CONFIGURATION

For the emitter-bias configuration, an analysis of the network will result in

$$\boxed{S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{(\beta + 1) + R_B/R_E}} \qquad (4.54)$$

Voltage-Divider Bias Configuration

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_{Th}/R_E}{(\beta + 1) + R_{Th}/R_E} \tag{4.59}$$

Feedback-Bias Configuration (R_E 5 0 Ω)

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_C}{(\beta + 1) + R_B/R_C} \tag{4.60}$$

S(V_{BE})

The stability factor defined by

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

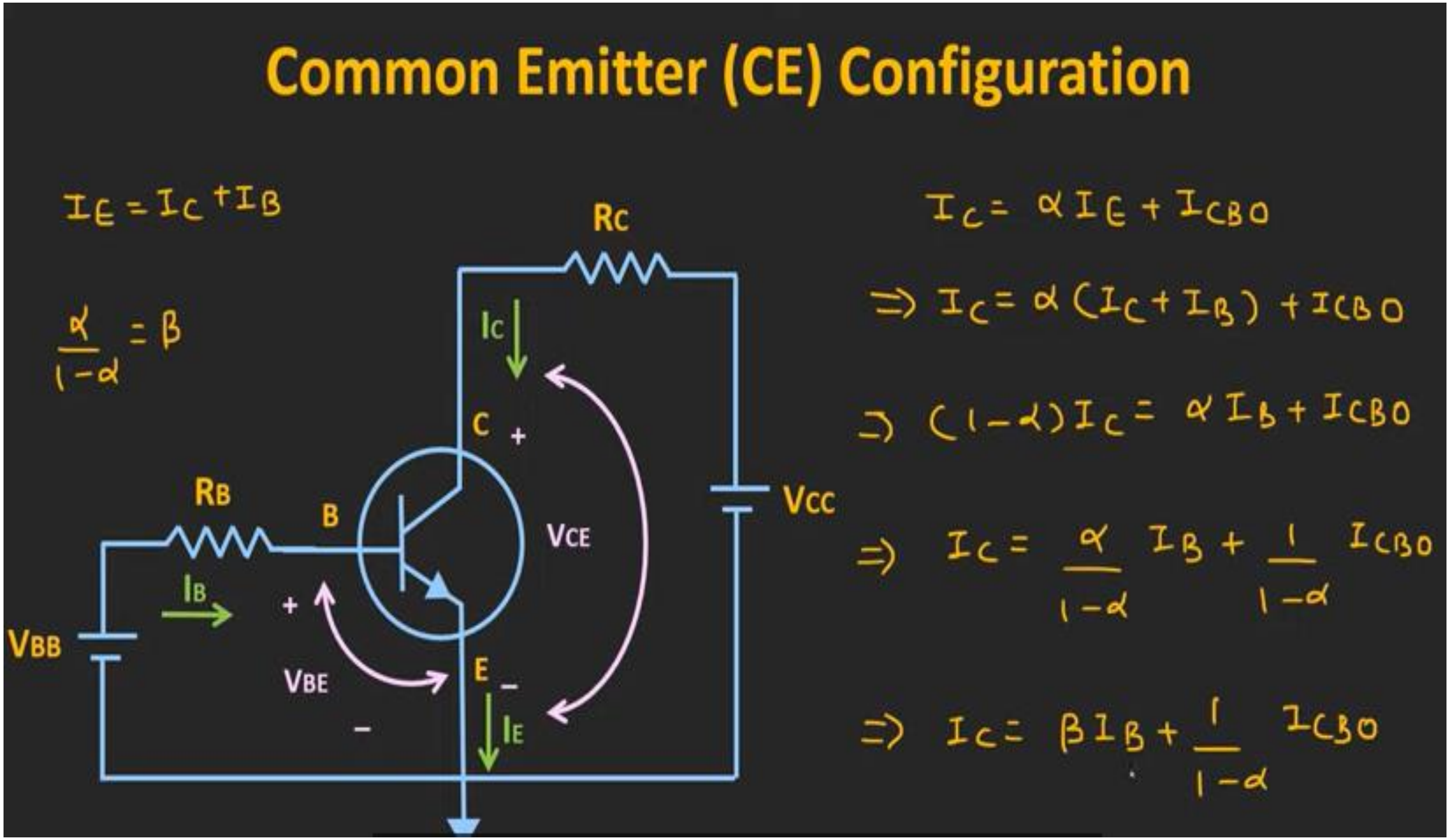
will result in the following equation for the emitter-bias configuration:

$$S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_E} \tag{4.64}$$

Practice yourself and send me your feedback, if any.

ICBO is high in CE configuration, Why ?

When IB = 0, we are getting I_{CBO}



Summary

- Biasing is necessary to fix-up the Q-pt.
- For distortion less maximum amplification, mid-pt biasing is required.
- Thumb rule for mid-pt biasing-

$$V_{CEQ} = \frac{1}{2} V_{CE,cut-off} = \frac{1}{2} V_{CC} \qquad I_{CQ} = \frac{1}{2} I_{C,Sat}$$

- Bias stability is important, dependency to beta variation should be minimized.
- Practice both biasing circuit analysis and design.

Practice yourself and send me your feedback, if any.