Operational Amplifier (Op-Amp)

Text Books

1. Electronic Devices and Circuit Theory

by R Boylestad and L Nashelsky

2. Op-Amps and Linear Integrated Circuits

by Ramakant A. Gayakwad

3. Microelectronic Circuits Analysis and Design

by Muhammad H. Rashid

4. Electronic Principles 7th Edition

by Albert Malvino, David Bates

The Operational Amplifier

An operational amplifier (often op amp or opamp) is a direct-coupled high gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level transistor and an output stage.

It is electronic voltage amplifier with a differential input, a (usually) single-ended output, and an extremely high gain.

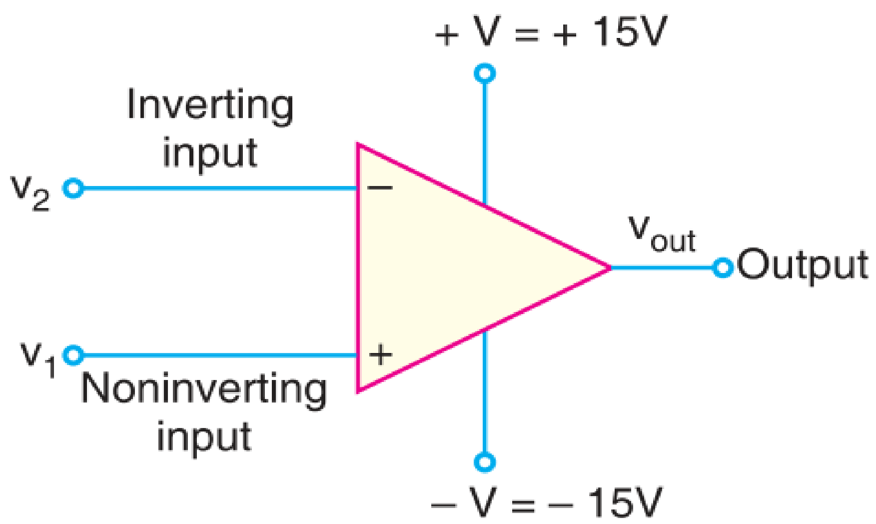
Its name comes from its original use of performing mathematical operations in analog computers.

It is a versatile device used to amplify dc as well as ac signals.

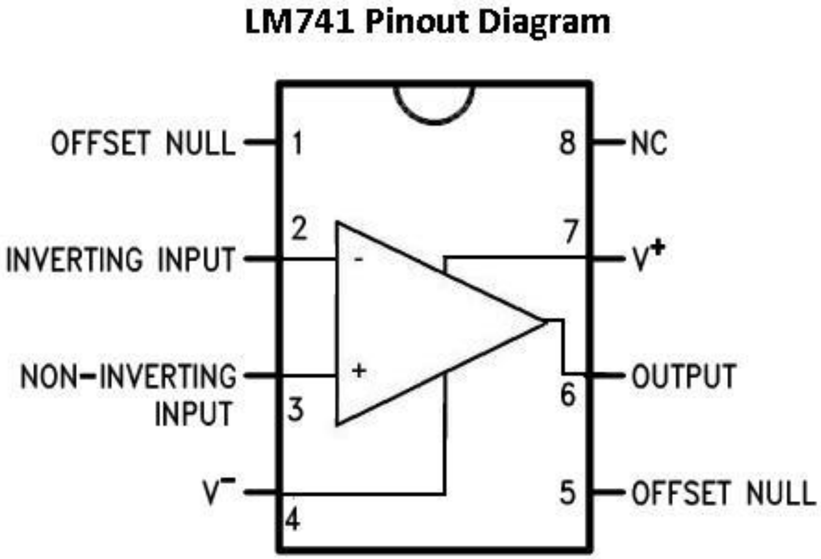
It was originally designed for performing mathematical operations such as addition, subtraction, multiplication, and integration. Thus, the name operational amplifier.

With the addition of suitable external feedback, these are used to build waveform converter,ac and dc signal amplification, comparators, regulators, oscillator, active filter, and so many interesting circuits with other external devices or components.

Schematic Symbol: Operational Amplifier

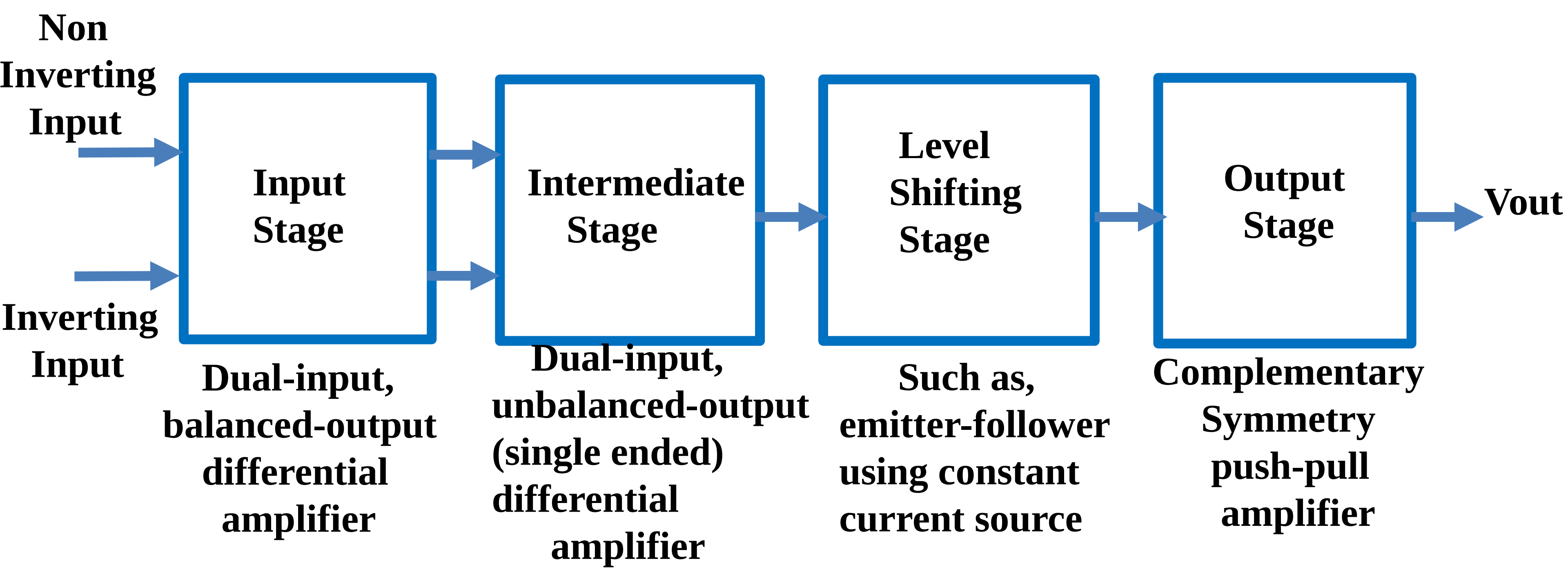


Schematic Symbol of an op-amp



Chapter 8, Paper 662 of Electronic Principles 7th Edition *by Albert Malvino, David Bates*

Block Diagram of an Op-Amp



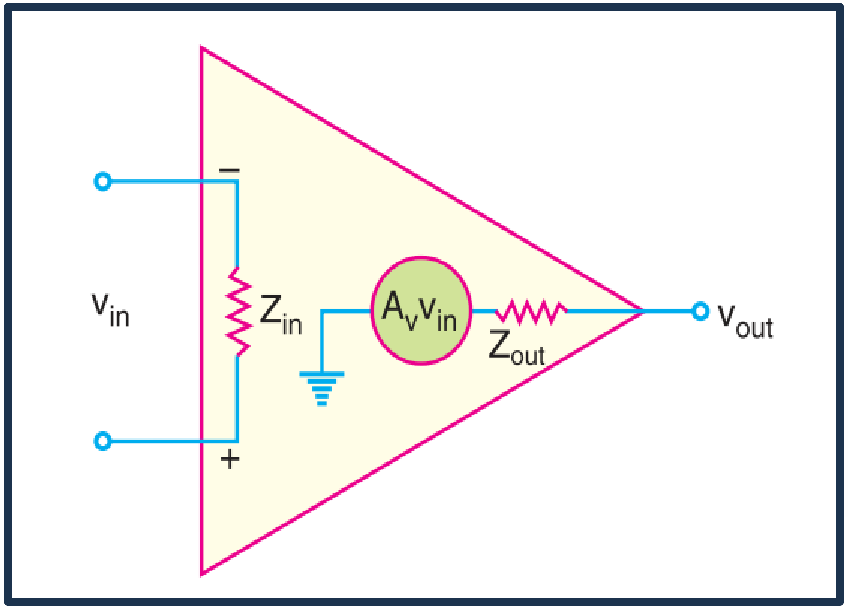
Block Diagram of an op-amp

Chapter 1, Page 18 of Op-Amps and Linear Integrated Circuits *by Ramakant A. Gayakwad*

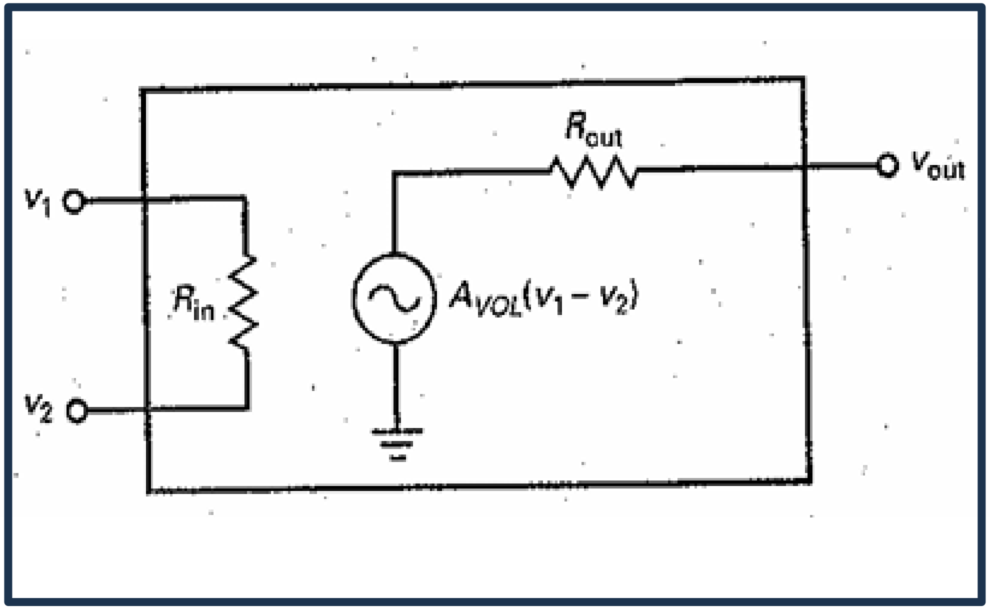
Block Diagram of an Op-Amp

- Op-amp is a multistage amplifier. The input stage is the dual-input, balanced-output differential amplifier. This stage is usually for ensuring most of the voltage gain of the amplifier and establishing the input resistance of the op-amp.
- The next stage is another differential amplifier which takes the output of the first stage. Generally, it is dual input, unbalanced output (single-ended output).
- After that, the shifting stage is there to shift the dc level at the output of the intermediate stage downward to zero volts with respect to ground.
- The final stage is a push-pull complementary amplifier output stage. It increases the output voltage swing and raises the current supplying capability of the op-amp. It can also provide low output resistance if it is well-designed.

Circuit Diagram of Practical Op-Amp



With Single Input (Vin)



With Double Inputs (V1 and V2)

In a practical op-amp, the input impedance is not infinite, output impedance is not zero, and gain is not infinite.

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Parameters & Characteristics of Ideal Op-Amp

1. Infinite open loop voltage gain
2. Infinite unity-gain frequency
3. Infinite input resistance so that almost any signal source can drive it
4. Zero output resistance so that output can drive an infinite number of other devices
5. Zero output voltage when input voltage is zero
6. Zero input bias current
7. Zero input offset current
8. Zero input offset voltage
9. Infinite bandwidth
10. Infinite common mode rejection ratio
11. Infinite slew rate

Practical *OP*-amp	**Ideal *OP*-amp**
$Z_{in} = 2\ \text{M}\Omega$	$Z_{in} \to \infty$ (Open circuit)
$A_v = 1 \times 10^5$	$A_v \to \infty$
$Z_{out} = 100\ \Omega$	$Z_{out} = 0\Omega$

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The Ideal voltage transfer curve

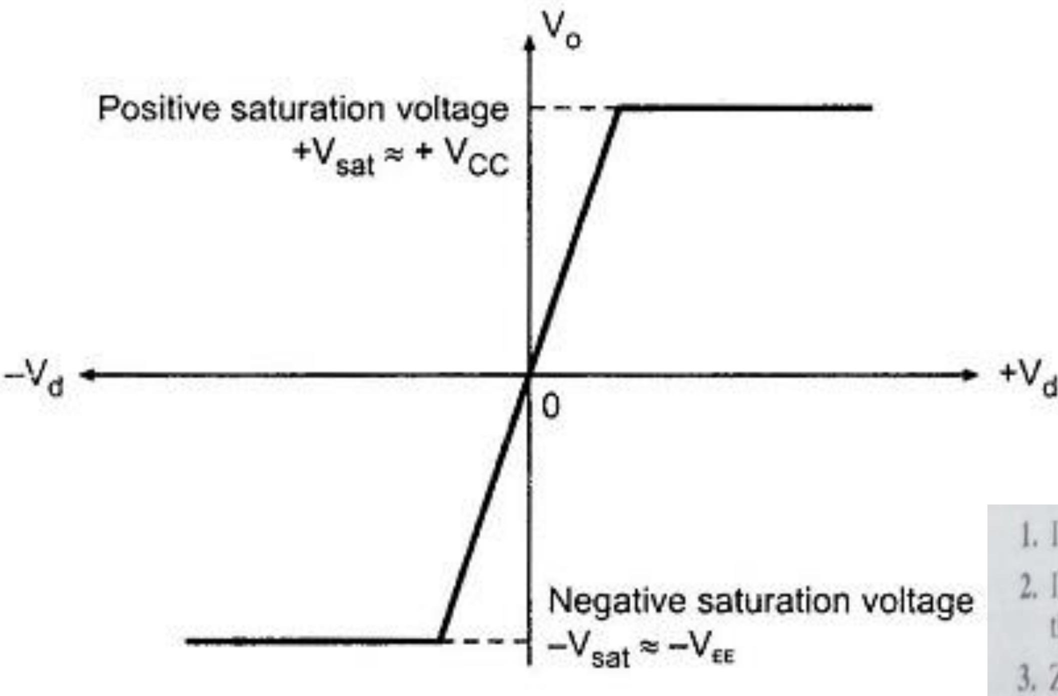
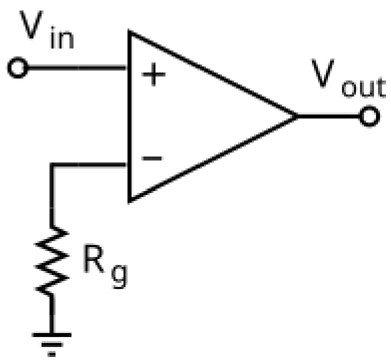


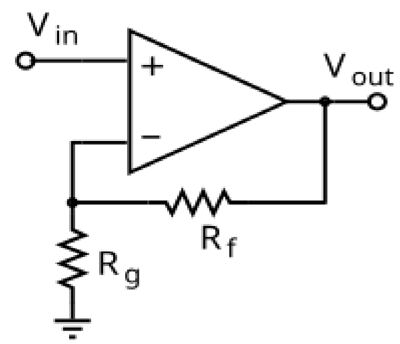
Fig. 2.7 Ideal voltage transfer curve

1. Infinite voltage gain *A*.
2. Infinite input resistance R_i so that almost any signal source can drive it and there is no loading of the preceding stage.
3. Zero output resistance R_o so that the output can drive an infinite numbe of other devices.
4. Zero output voltage when input voltage is zero.
5. Infinite bandwidth so that any frequency signal from 0 to ∞ Hz can b amplified without attenuation.
6. Infinite common-mode rejection ratio so that the output common-mode noise voltage is zero.
7. Infinite slew rate so that output voltage changes occur simultaneously with input voltage changes.

Open loop and Close loop operation



An op amp without negative feedback (a comparator)



An op amp with negative feedback (a non-inverting amplifier)

- The magnitude of AOL is typically very large (100,000 or more for integrated circuit op amps, corresponding to +100 dB).
- Thus, even small microvolts of difference between V+ and V− may drive the amplifier into clipping or saturation.
- The magnitude of AOL is not well controlled by the manufacturing process, and so it is impractical to use an open-loop amplifier as a stand-alone differential amplifier.

- If predictable operation is desired, negative feedback is used, by applying a portion of the output voltage to the inverting input.
- The closed-loop feedback greatly reduces the gain of the circuit.
- When negative feedback is used, the circuit's overall gain and response is determined primarily by the feedback network, rather than by the op-amp characteristics.

Comparison Between Ideal Op-Amp and Typical Op-amps Available

Table 18-1 Typical Op-Amp Characteristics

Quantity	Symbol	Ideal	LM741C	LF157A
Open-loop voltage gain	A_{VOL}	Infinite	100,000	200,000
Unity-gain frequency	f_{unity}	Infinite	1 MHz	20 MHz
Input resistance	R_{in}	Infinite	2 MΩ	10^{12} Ω
Output resistance	R_{out}	Zero	75 Ω	100 Ω
Input bias current	$I_{in(bias)}$	Zero	80 nA	30 pA
Input offset current	$I_{in(off)}$	Zero	20 nA	3 pA
Input offset voltage	$V_{in(off)}$	Zero	2 mV	1 mV
Common-mode rejection ratio	CMRR	Infinite	90 dB	100 dB

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Comparison of Ideal & Practical Op-Amp

Characteristics of Ideal Op-Amp:

1. Infinite open loop voltage gain
2. Infinite unity-gain frequency
3. Infinite input resistance so that almost any signal source can derive it
4. Zero output resistance so that output can derive an infinite number of other devices
5. Zero output voltage when input voltage is zero
6. Zero input bias current
7. Zero input offset current
8. Zero input offset voltage
9. Infinite bandwidth
10. Infinite common mode rejection ratio
11. Infinite slew rate

Op-Amp as integrated circuit

Generally, Op amp is available as integrated circuit (IC)

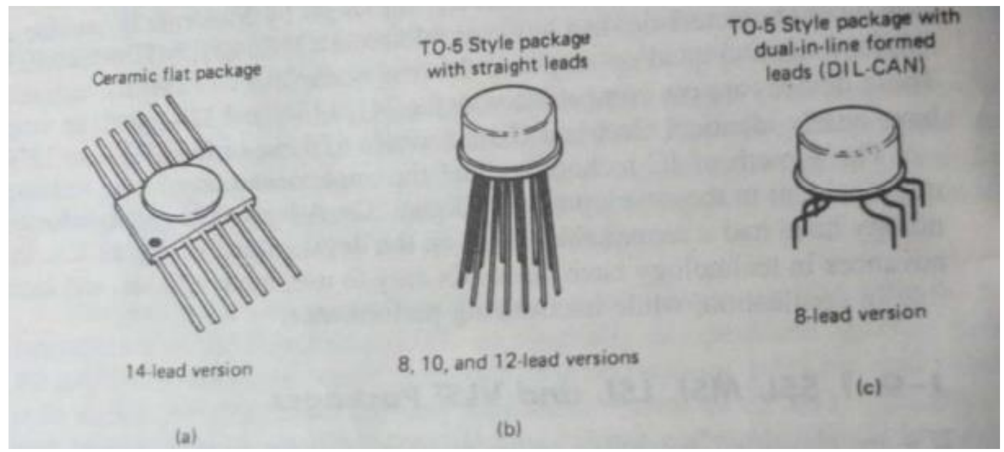
Manufacturer Designation

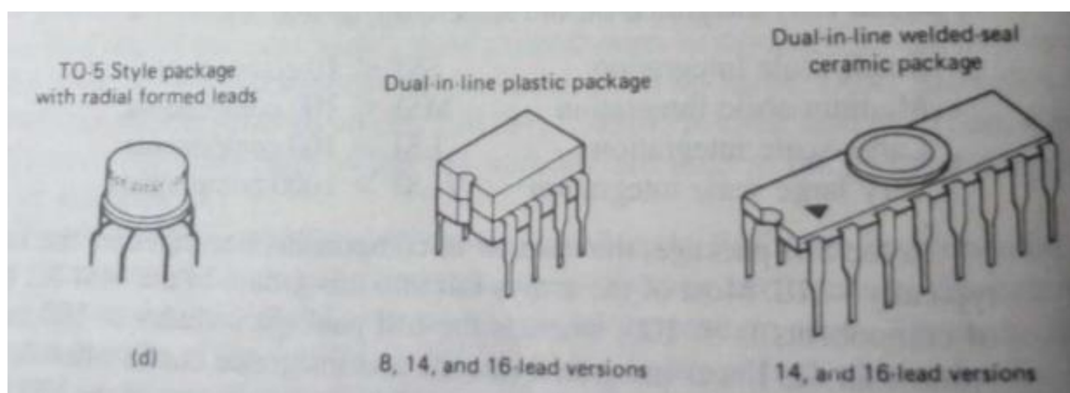
Fairchild	µA
	µAF
National Semiconductor	LM
	LH
	LF
	TBA
Motorola	MC
	MFC
RCA	CA
	CD
Texas Instruments	SN
Signetics	N/S
	NE/SE
	SU
Burr-Brown	BB

National Semiconductor	LM741
Motorola	MC1741
RCA	CA3741
Texas Instruments	SN52741
Signetics	N5741

Package Type

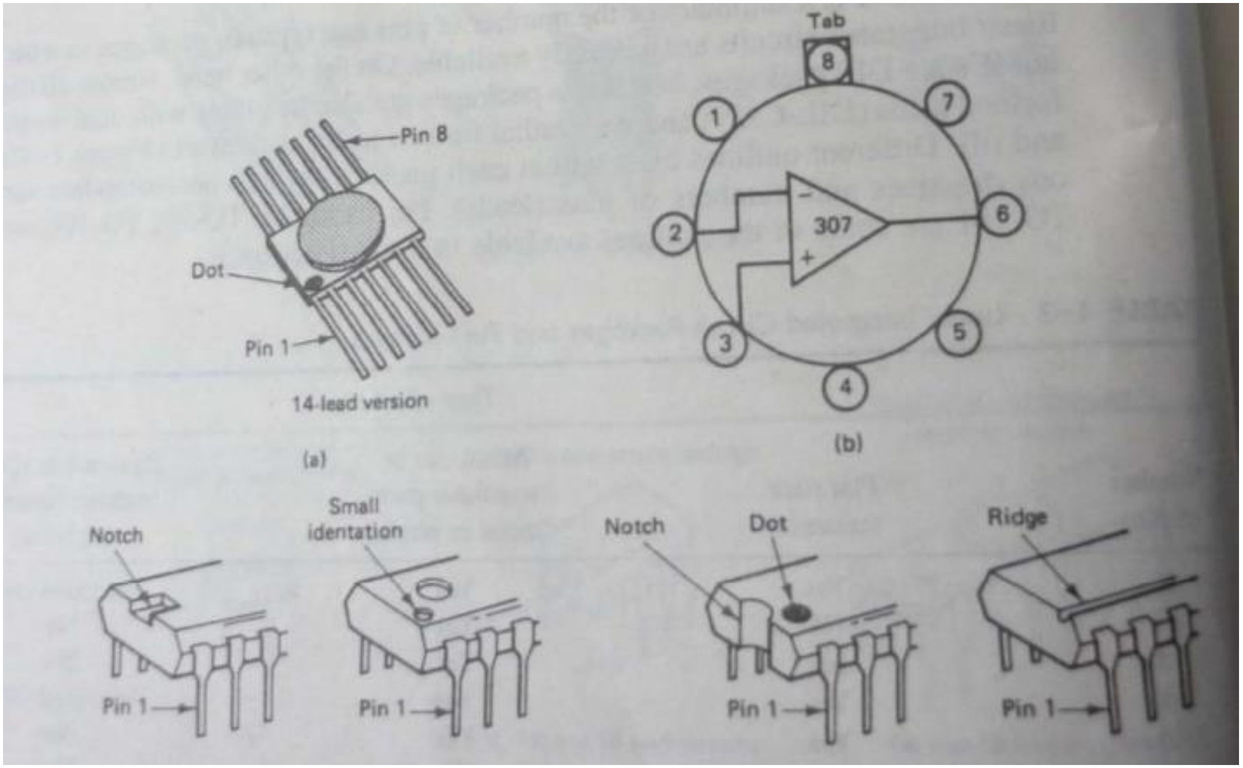
1. The flat pack
2. The metal can or transistor pack
3. The dual-in-line package (for short, DIP)





Op-Amp as integrated circuit

Pin Identification



1–9–1 SSI, MSI, LSI, and VLSI Packages

ICs are classified according to the number of components (or gates, in the case of digital ICs) integrated on the same chip, as follows:

Small-scale integration	SSI $<$ 10 components
Medium-scale integration	MSI $<$ 100 components
Large-scale integration	LSI $>$ 100 components
Very large scale integration	VLSI $>$ 1000 components

Temperature Range

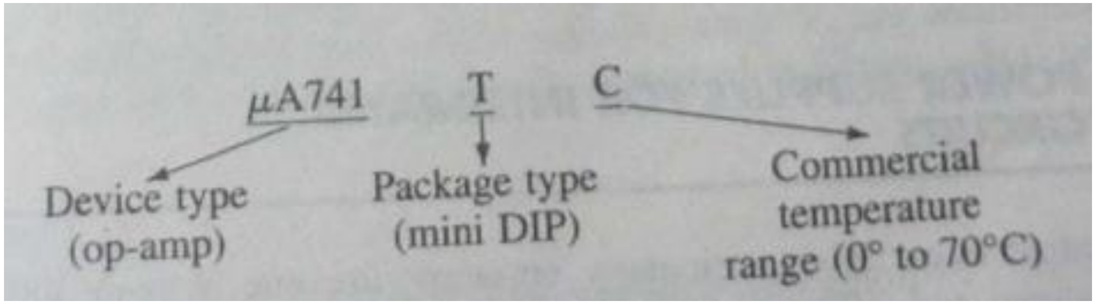
1-10-3 Temperature Ranges

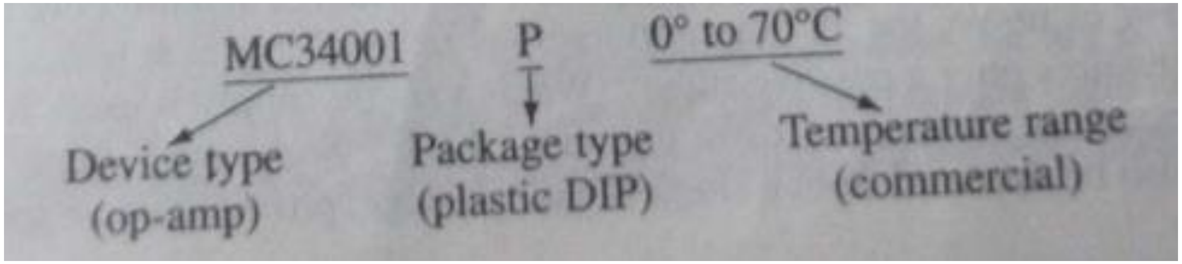
All ICs manufactured fall into one of the three basic temperature grades:

1. Military temperature range: −55° to +125°C (or −55° to +85°C)
2. Industrial temperature range: −20° to +85°C (or −40° to +85°C)
3. Commercial temperature range: 0° to +70°C (or 0° to +75°C)

of the IC parameters and condi-

Ordering Information





SSI	MSI	LSI	VLSI	ULSI
< 100 active devices	100-1000 active devices	1000-100000 active devices	>100000 active devices	Over 1 million active devices
Integrated resistors, diodes & BJT's	BJT's and Enhanced MOSFETS	MOSFETS	8bit, 16bit Microprocessors	Pentium Microprocessors

Disadvantages of first generation Op-amp

1. No short circuit protection: The op-amp is susceptible to burnout if output it accidentally shorted to ground.
2. A possible latch-up problem: Output voltage can be latched up to some value and then fails to respond to changes in input signal applied.
3. Requires an external frequency-compensating network (two capacitors and a resistor) for stable operation.

A **latch-up** is a type of short circuit which can occur in an integrated circuit (IC)

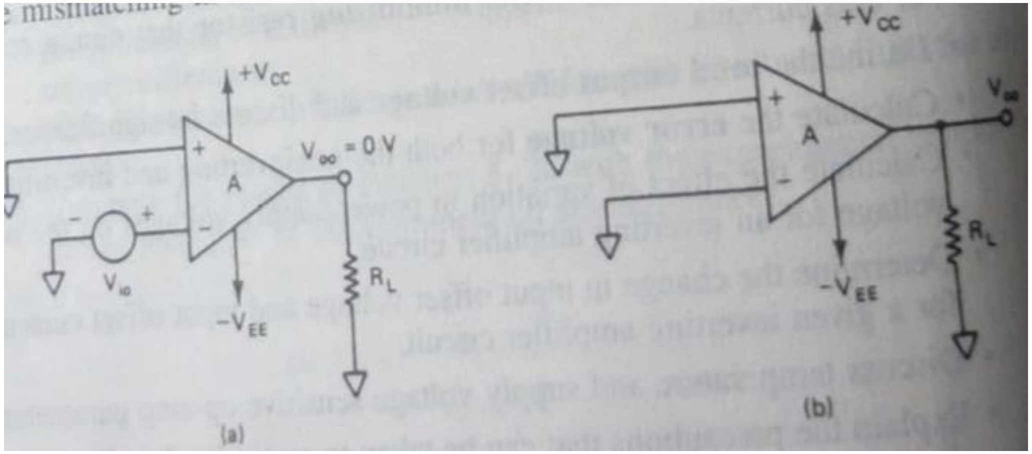
Detailed features of 741

1. No external frequency compensation required
2. Short-circuit protection
3. Offset null capability
4. Large common mode and differential voltage ranges
5. Low power consumption
6. No latch-up problem

Input Offset Voltage

It is the differential input voltage that exists between two input terminals of an op-amp without any inputs applied.

In other words, it is the amount of input voltage that should be applied between two inputs in order to force the output voltage to zero.

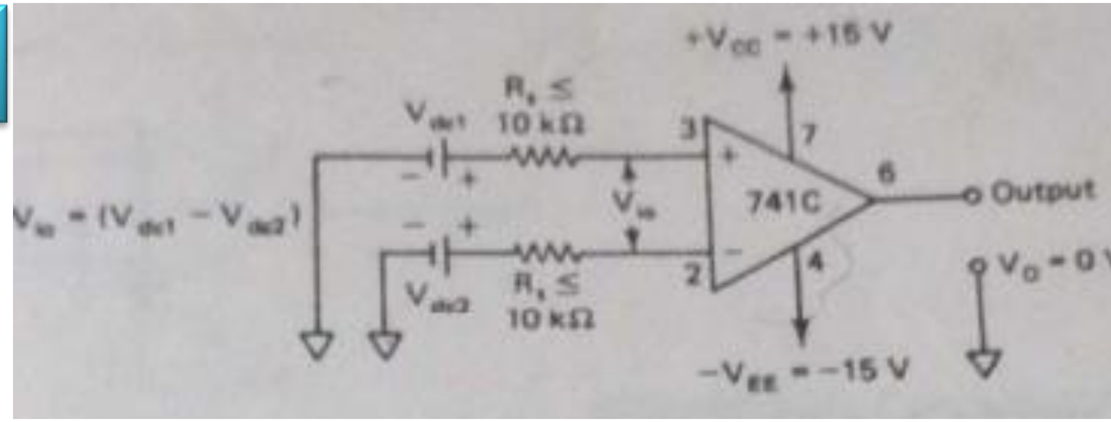


- The output offset voltage V_{00} is caused by mismatching between two input terminals.
- Even though all the components are integrated on the same chip , it is not possible to have two transistors in the input differential amplifier stage with exactly same characteristics.
- This means that the collector currents in these two transistors are not equal, which causes a differential output voltage from the first stage.
- The output of the first stage is amplified by following stage and possibly aggravated by more mismatching in them.
- Thus, the output voltage caused by mismatching between two input terminals is the output offset V_{00}.
- The output offset voltage V_{00} is a dc voltage,
- it may be positive or negative in polarity depending on whether the potential difference between two input terminals is positive or negative.

Chapter 4, Page 126 of **Op-Amps and Linear Integrated Circuits** *by Ramakant A. Gayakwad*

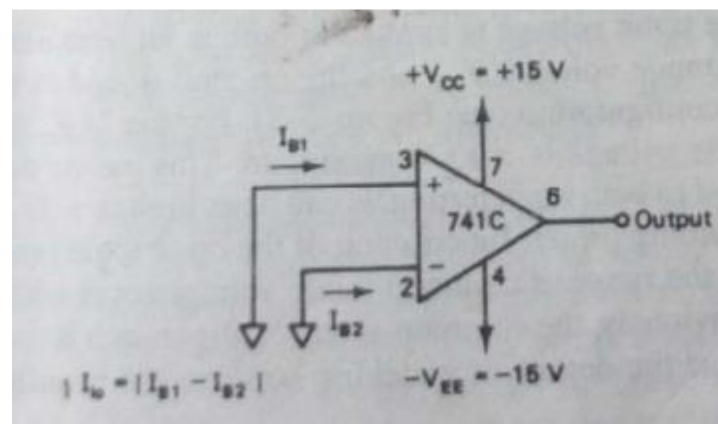
Input Offset voltage

- Absolute value is listed on the data sheet
- For a 741C, the maximum value of Vi0 is 6 mV dc
- For 741C precision op-amp, the maximum value of Vi0 is 150 µV dc



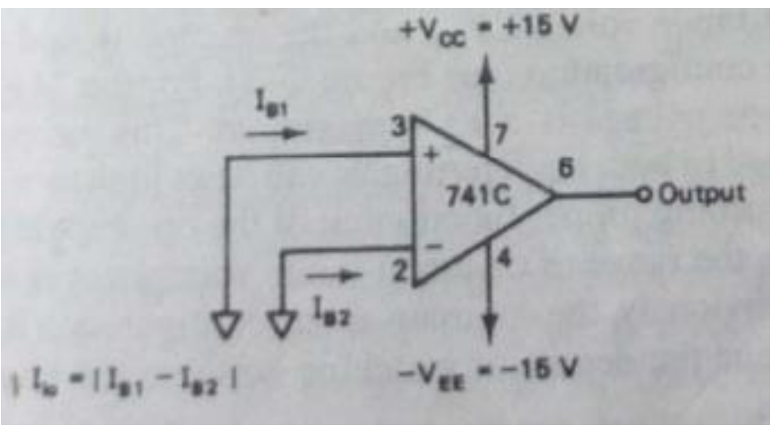
Input Bias current

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$



For a 741C, I_B is 500 nA
For 741C precision op-amp, I_B is ±7 nA

Input Offset current



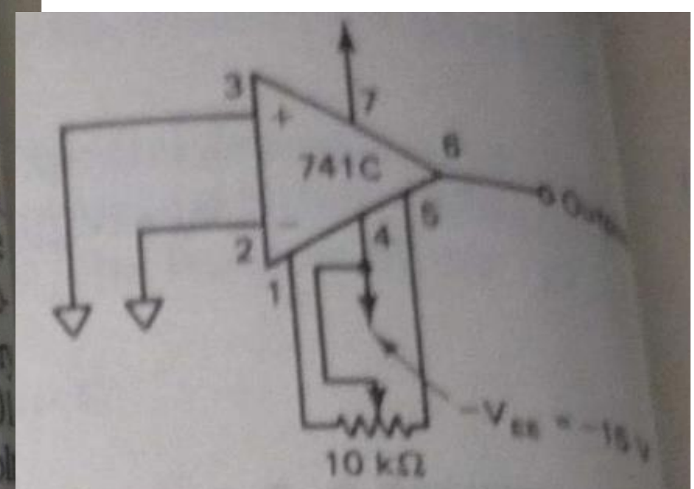
$$I_{io} = |I_{B1} - I_{B2}|$$

For a 741C the maximum value of Ii0 is 200 nA
For 741C precision op-amp, the maximum value of Ii0 is 6 nA

Differential Input Resistance. Differential input resistance, R_i, (often referre to as input resistance) is the equivalent resistance that can be measured at eithe the inverting or noninverting input terminal with the other terminal connected t ground. For the 741C the input resistance is a relatively high 2 MΩ. Howeve for FET input op-amps this value is amazingly large. For example, R_i is 1000 GΩ (10^{12} Ω) for the μAF771 FET input op-amp.

Input Capacitance. Input capacitance C_i is the equivalent capacitance that can be measured at either the inverting or noninverting terminal with the other termina connected to ground. A typical value of C_i is 1.4 pF for the 741C. This parame ... all op-amp data sheets.

Offset Voltage Adjustment Range. One of the features of the 741 family op-amps is an offset voltage null capability. The 741 op-amps have pins 1 and 5 marked as *offset null* for this purpose. As shown in Figure 2–4, a 10-kΩ potentiometer can be connected between offset null pins 1 and 5, and the wiper of the poten- tiometer can be connected to the negative supply $-V_{EE}$. By varying the poten- tiometer, the *output offset voltage* (output voltage without any input applied) can be reduced to zero volts. Thus the offset voltage adjustment range is the range through which the input offset voltage can be adjusted by varying the 10-kΩ po- tentiometer. For the 741C the offset voltage adjustment range is ±15 mV. Very few op-amps have the offset voltage null capability, some of these being the 301, 748, and 777. This means that for most op-amps we have to design an offset voltage compensating network in order to reduce the output offset voltage to zero. The design of such a network is presented in Chapter 4.



DIFFERENTIAL AND COMMON-MODE OPERATION

Differential Inputs

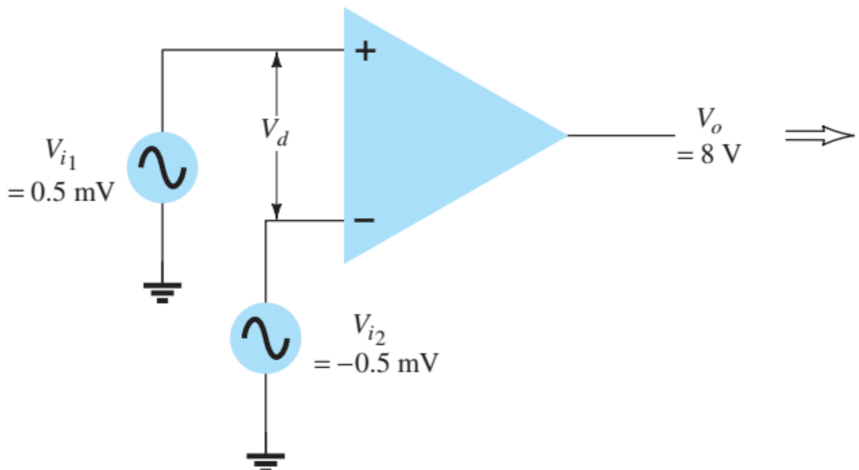
$$V_d = V_{i_1} - V_{i_2}$$

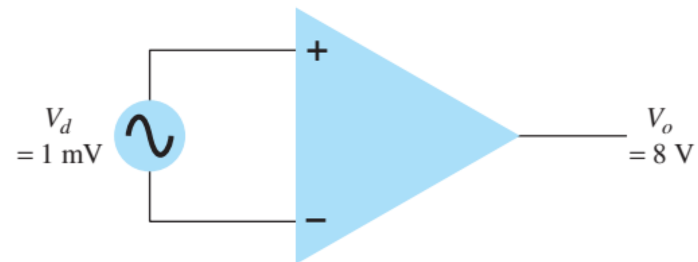
Common Inputs

$$V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2})$$

Output Voltage

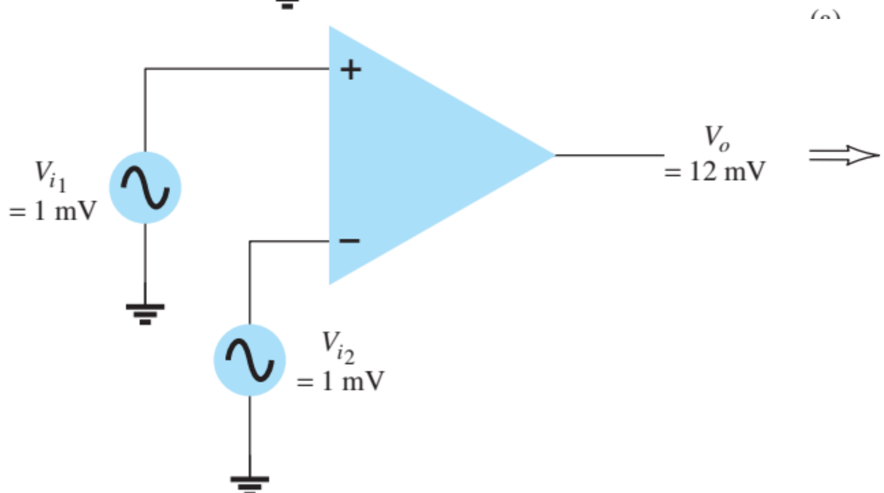
$$V_o = A_d V_d + A_c V_c$$

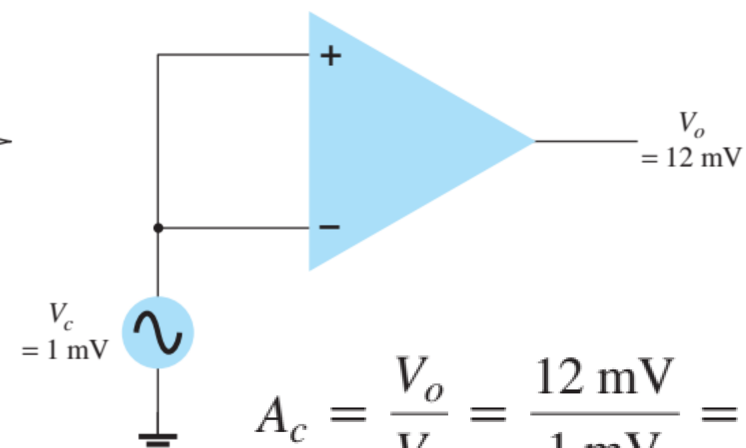




$$A_d = \frac{V_o}{V_d} = \frac{8\text{ V}}{1\text{ mV}} = 8000$$

(a)





$$A_c = \frac{V_o}{V_c} = \frac{12\text{ mV}}{1\text{ mV}} = 12$$

(b)

Common-Mode Rejection Ratio

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{8000}{12} = \mathbf{666.7}$$

$$\text{CMRR} = 20\log_{10}\frac{A_d}{A_c} = 20\log_{10}666.7 = \mathbf{56.48\ dB}$$

$$V_o = A_dV_d + A_cV_c = A_dV_d\left(1 + \frac{A_cV_c}{A_dV_d}\right)$$

$$\boxed{V_o = A_dV_d\left(1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_d}\right)}$$

Supply Voltage Rejection Ratio (SVRR)

The change in the input offset voltage due to the change of the supply voltage is SVRR

$$SVRR = \frac{\Delta V_{i0}}{\Delta V}$$

For a 741C, the SVRR = 150 μV/V
For a 714C, the SVRR = 6.31 μV/V

More few terms for 741 IC

Large signal voltage gain:

Output voltage swing:

Output resistance:

Output short circuit current:

Supply current:

Power consumption:

Transient response:

Slew Rate

- Slew rate is the ability of the output change from one value to another in a given time.

- The slew rate is apparent for large amplitude (on the order of volts) and high frequency signal.

- Large amplitude and high frequency signal lead the compensation capacitor in the op-amp to take finite time to charge and discharge

- Slew rate is cause by the capacitor charging rate. Voltage across the capacitor is the output voltage

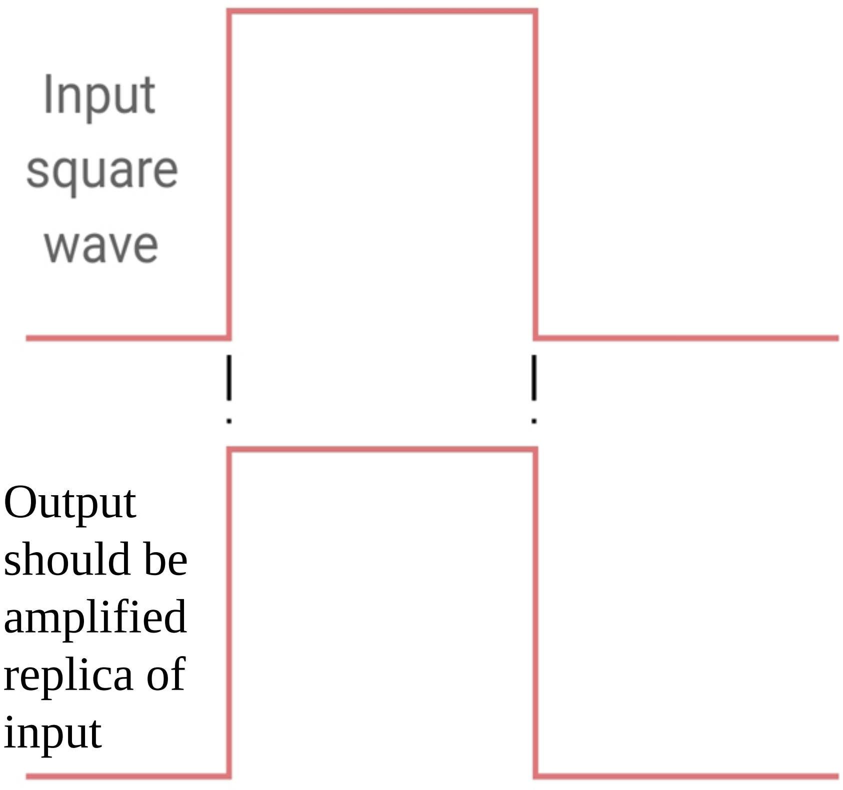
- Slew rate is measured in V/µs

- Slew rate for sine wave is

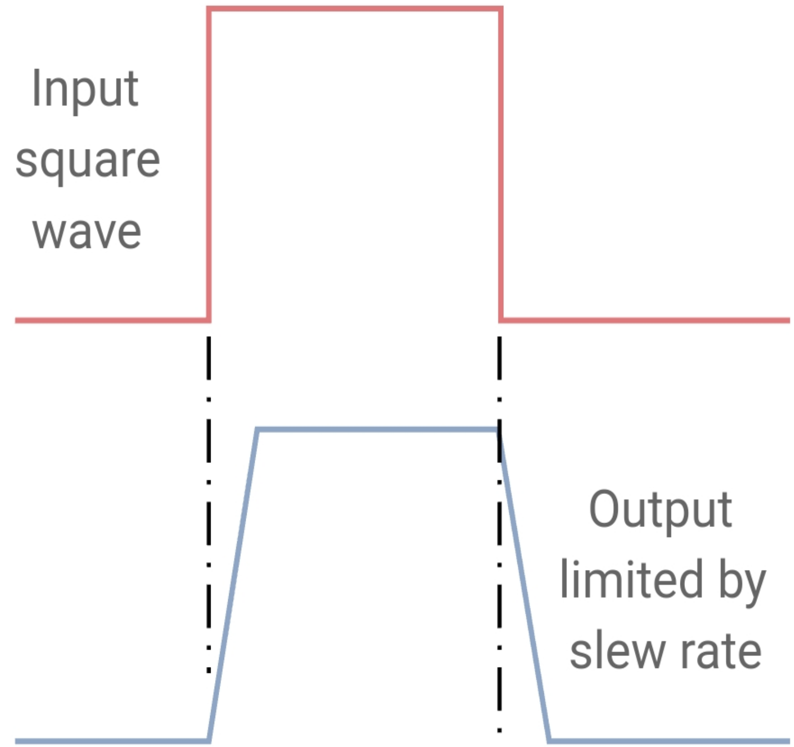
$$SR = \left.\frac{dv_0}{dt}\right|_{\max} = \frac{2\pi f V_p}{10^6} \quad \text{V/µs}$$

Slew Rate

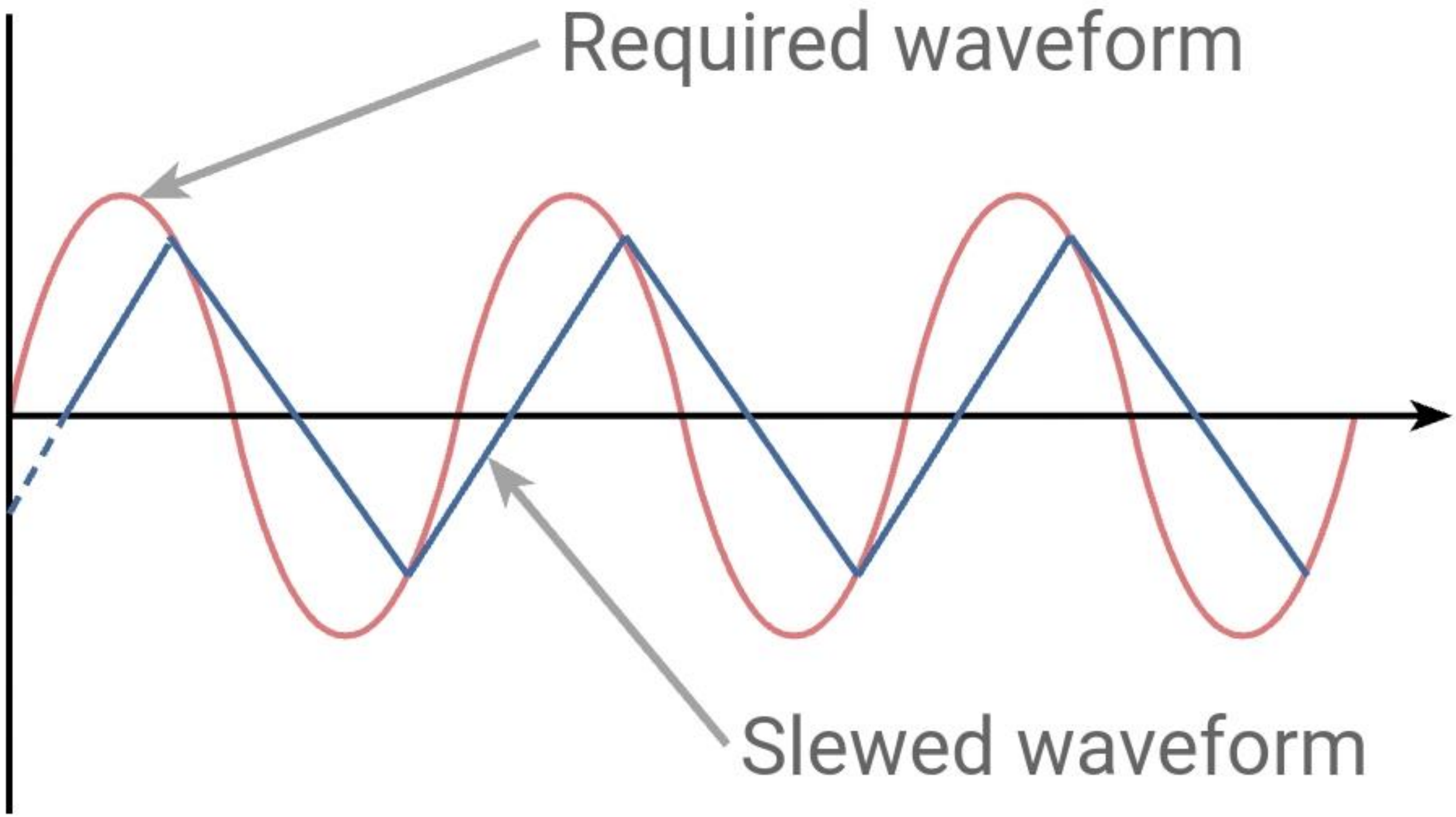
Wanted Response



Actual Response



Slew Rate

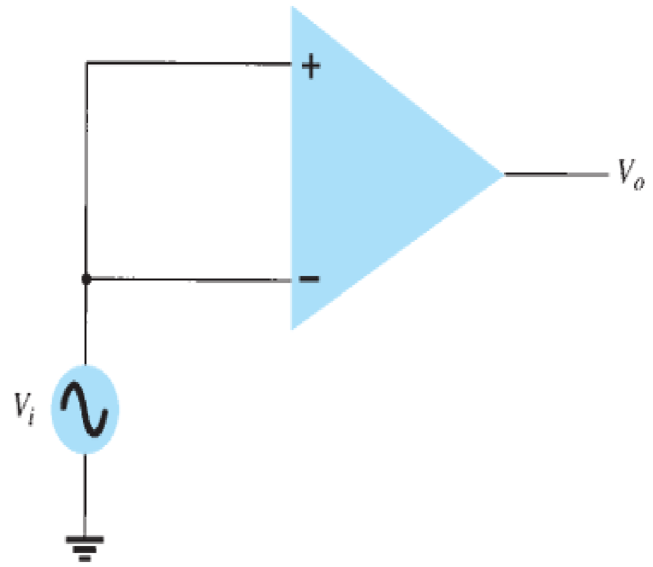


Op amp slewing distortion (limit)

Common-Mode Operation of Op-Amps

Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 10.8. Ideally, the two inputs are equally amplified, and since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.



Chapter 10, Page 609 of Electronic Devices and Circuit Theory *by R Boylestad and L Nashelsky*

Common-Mode Operation of Op-Amps

Common-Mode Rejection

A significant feature of a differential connection is that the signals that are opposite at the inputs are highly amplified, whereas those that are common to the two inputs are only slightly amplified—the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide attenuation of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature is referred to as *common-mode rejection*.

Common-Mode Rejection Ratio

Having obtained A_d and A_c (as in the measurement procedure discussed above), we can now calculate a value for the common-mode rejection ratio (CMRR), which is defined by the following equation:

$$\boxed{\text{CMRR} = \frac{A_d}{A_c}} \tag{10.29}$$

The value of CMRR can also be expressed in logarithmic terms as

$$\boxed{\text{CMRR (log)} = 20 \log_{10} \frac{A_d}{A_c} \quad \text{(dB)}} \tag{10.30}$$

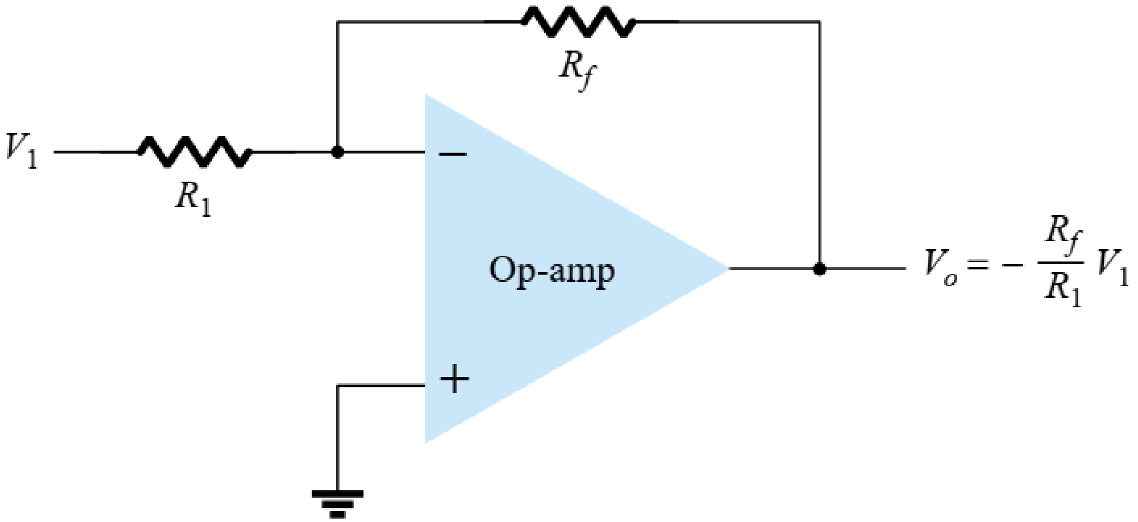
A_d = differential gain of the amplifier

A_c = common-mode gain of the amplifier

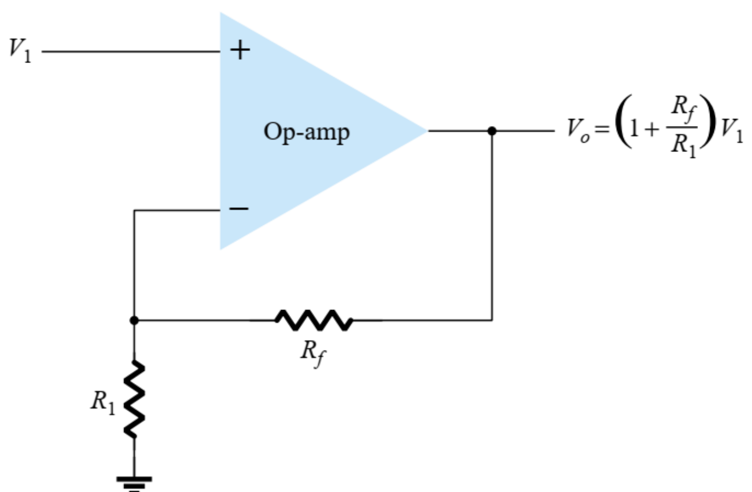
Chapter 10, Page 609-610 of Electronic Devices and Circuit Theory *by R Boylestad and L Nashelsky*

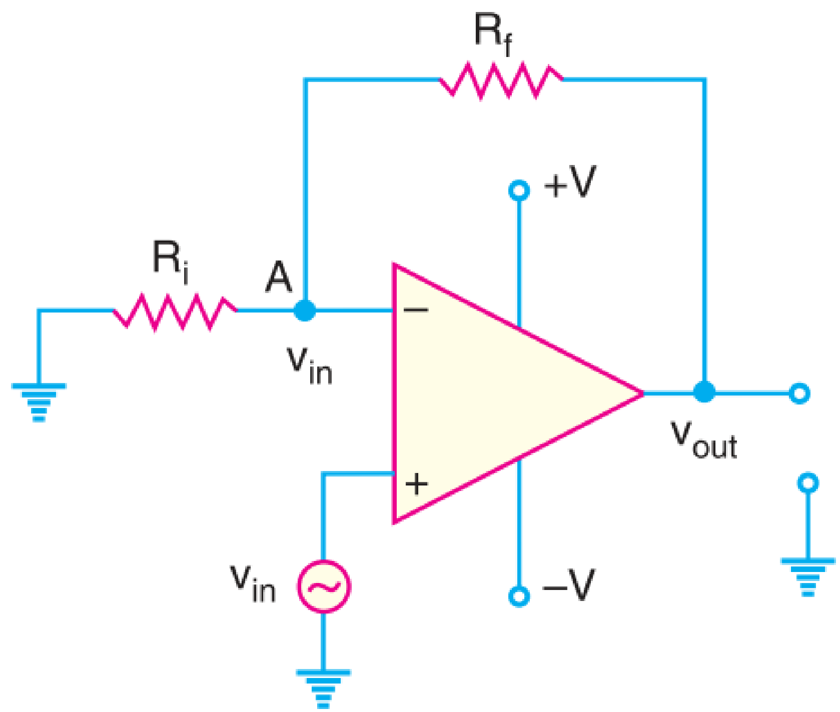
Close loop operation Example

Inverting:



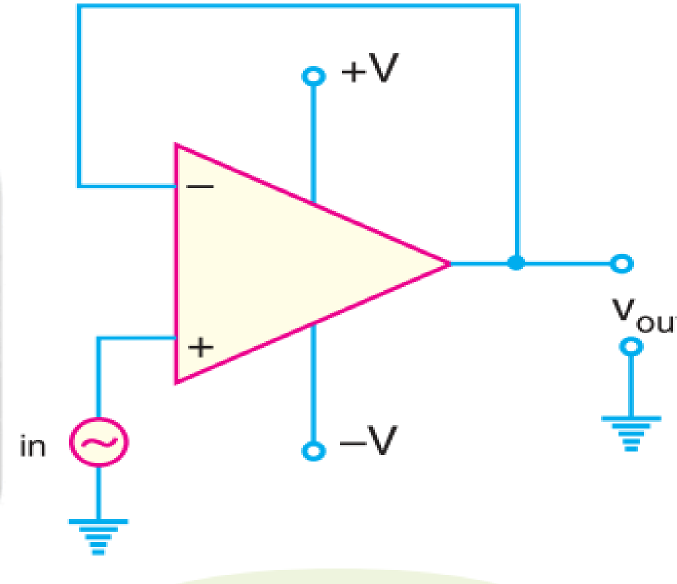
Non-inverting:



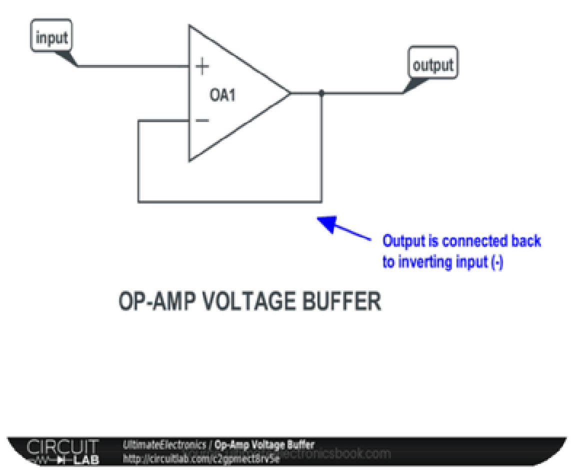


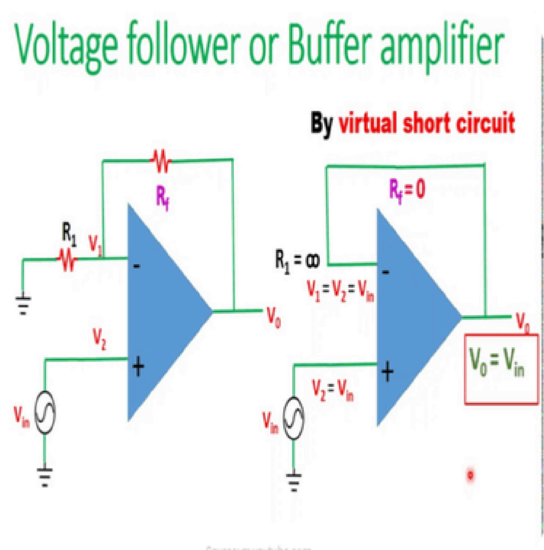
Buffer Amplifier:

- Buffer amplifiers, or voltage buffers, are essential in electronics for transferring signals between circuits of different impedance levels, maintaining signal integrity
- They prevent signal distortion and power loss, especially when connecting a high-impedance source to a low-impedance load
- There are two primary types: voltage buffers with high input and low output impedance and current buffers that ensure steady current flow
- Commonly found in audio systems, data acquisition systems, and RF circuits, they require careful design to mitigate challenges like instability and oscillation



Advantages??? & Applications ???





One of the main advantages of the buffer amplifier is impedance matching between circuits. Its high input impedance and low output impedance ensure that signals are transferred efficiently, no matter the varying impedance levels of circuits.

Multistage Op-Amp Amplifier

Multiple-Stage Gains

When a number of stages are connected in series, the overall gain is the product of the individual stage gains. Figure 11.5 shows a connection of three stages. The first stage is connected to provide noninverting gain as given by Eq. (11.1). The next two stages provide an inverting gain given by Eq. (11.1). The overall circuit gain is then noninverting and is calculated by

$$A = A_1 A_2 A_3$$

where $A_1 = 1 + R_f/R_1$, $A_2 = -R_f/R_2$, and $A_3 = -R_f/R_3$.

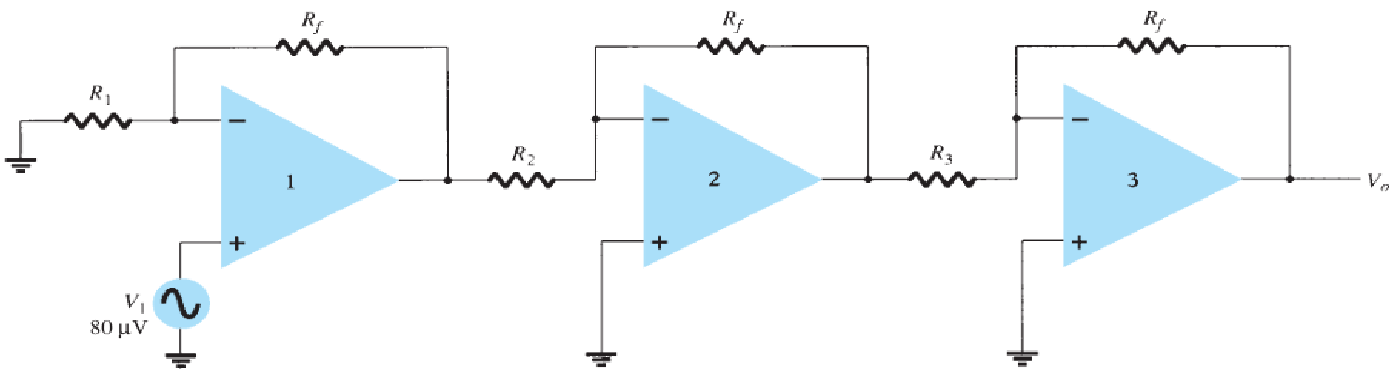


FIG. 11.5
Constant-gain connection with multiple stages.

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Multistage Op-Amp Amplifier

11.2 VOLTAGE SUMMING

Another popular use of an op-amp is as a summing amplifier. Figure 11.8 shows the connection, with the output being the sum of the three inputs, each multiplied by a different gain. The output voltage is

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \tag{11.3}$$

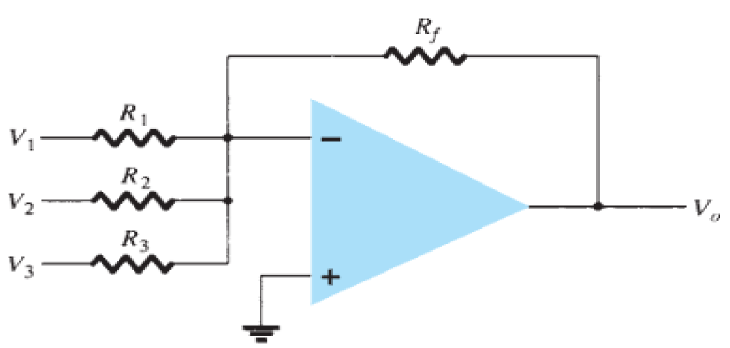

FIG. 11.8
Summing amplifier.

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Multistage Op-Amp Amplifier

Voltage Subtraction

Two signals can be subtracted from one another in a number of ways. Figure 11.10 shows two op-amp stages used to provide subtraction of input signals. The resulting output is given by

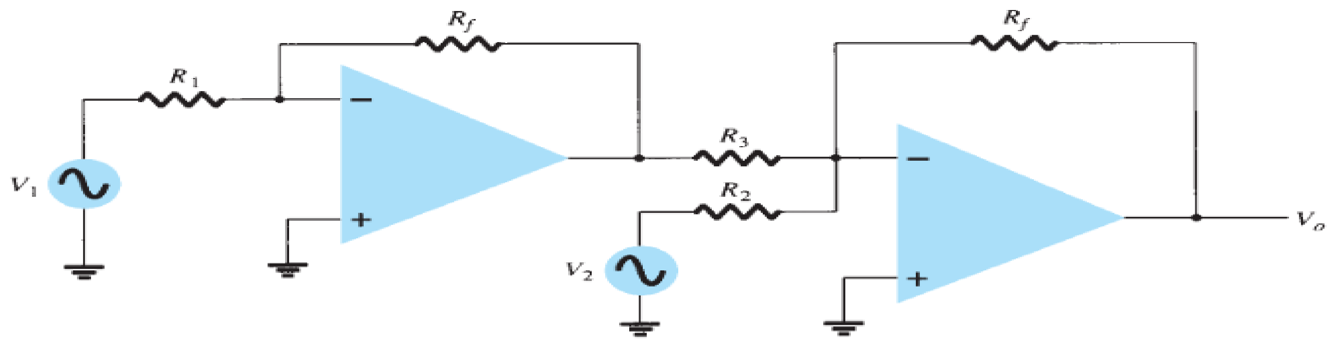


FIG. 11.10
Circuit for subtracting two signals.

$$V_o = -\left[\frac{R_f}{R_3}\left(-\frac{R_f}{R_1}V_1\right) + \frac{R_f}{R_2}V_2\right]$$

$$\boxed{V_o = -\left(\frac{R_f}{R_2}V_2 - \frac{R_f}{R_3}\frac{R_f}{R_1}V_1\right)} \qquad \textbf{(11.4)}$$

Example 11.3 to 11.7 are needed to be solved.

Chapter 11, Page 658-659 of Electronic Devices and Circuit Theory *by R Boylestad and L Nashelsky*

Operational Amplifier Applications

Text Books

1. Electronic Devices and Circuit Theory

by R Boylestad and L Nashelsky

***2.* Op-Amps and Linear Integrated Circuits**

by Ramakant A. Gayakwad

3. Microelectronic Circuits Analysis and Design

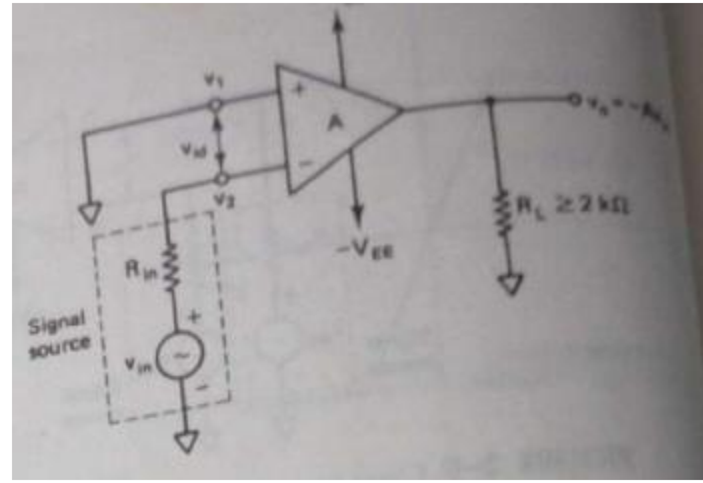
by Muhammad H. Rashid

4. Electronic Principles 7th Edition

by Albert Malvino, David Bates

Open loop op-amp configuration

1. Differential amplifier
2. Inverting amplifier
3. Noninverting amplifier



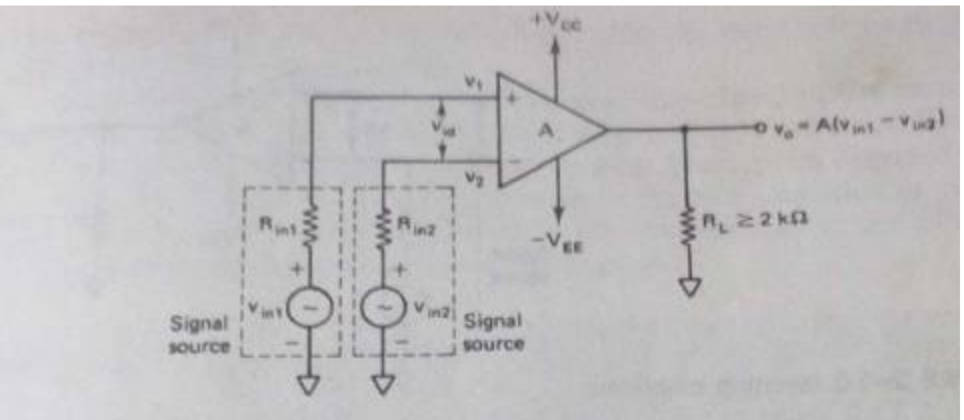
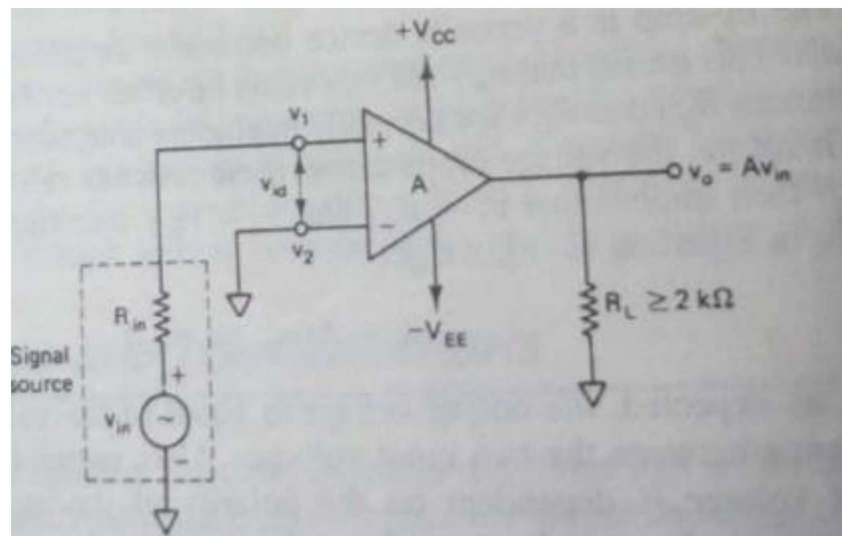
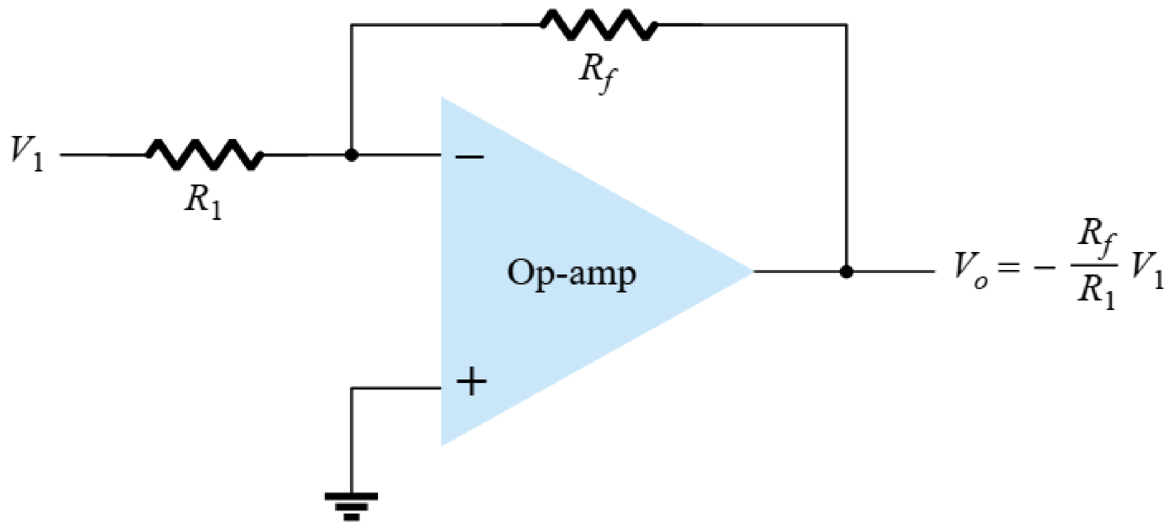


FIGURE 2–9 Open-loop differential amplifier.



Inverting Amplifier

Closed Loop Inverting Amplifier



Closed Loop Inverting Amplifier

Inverting Amplifier

Output Voltage of Closed-Loop Inverting Amplifier

Inverting Amplifier

The most widely used constant-gain amplifier circuit is the inverting amplifier, as shown in Fig. 10.34. The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor (R_1) and feedback resistor (R_f)—this output also being inverted from the input. Using Eq. (10.8), we can write

$$V_o = -\frac{R_f}{R_1} V_1$$

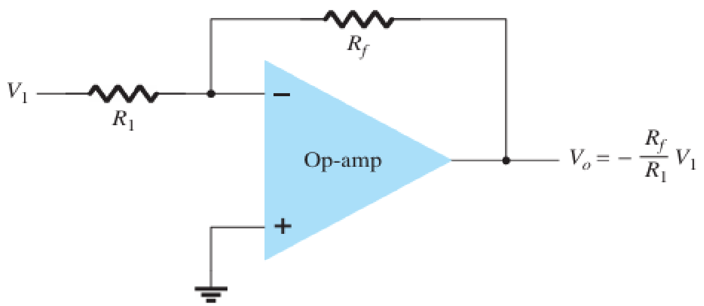


FIG. 10.34
Inverting constant-gain multiplier.

EXAMPLE 10.5 If the circuit of Fig. 10.34 has $R_1 = 100\ \text{k}\Omega$ and $R_f = 500\ \text{k}\Omega$, what output voltage results for an input of $V_1 = 2$ V?

Solution:

$$\text{Eq. (10.8):} \quad V_o = -\frac{R_f}{R_1} V_1 = -\frac{500\ \text{k}\Omega}{100\ \text{k}\Omega}(2\ \text{V}) = \mathbf{-10\ V}$$

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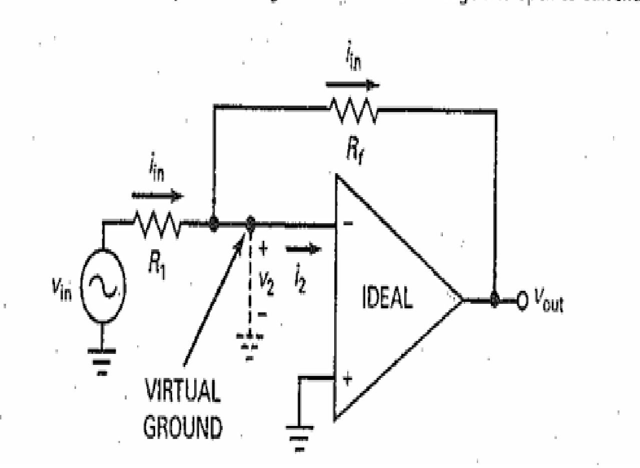
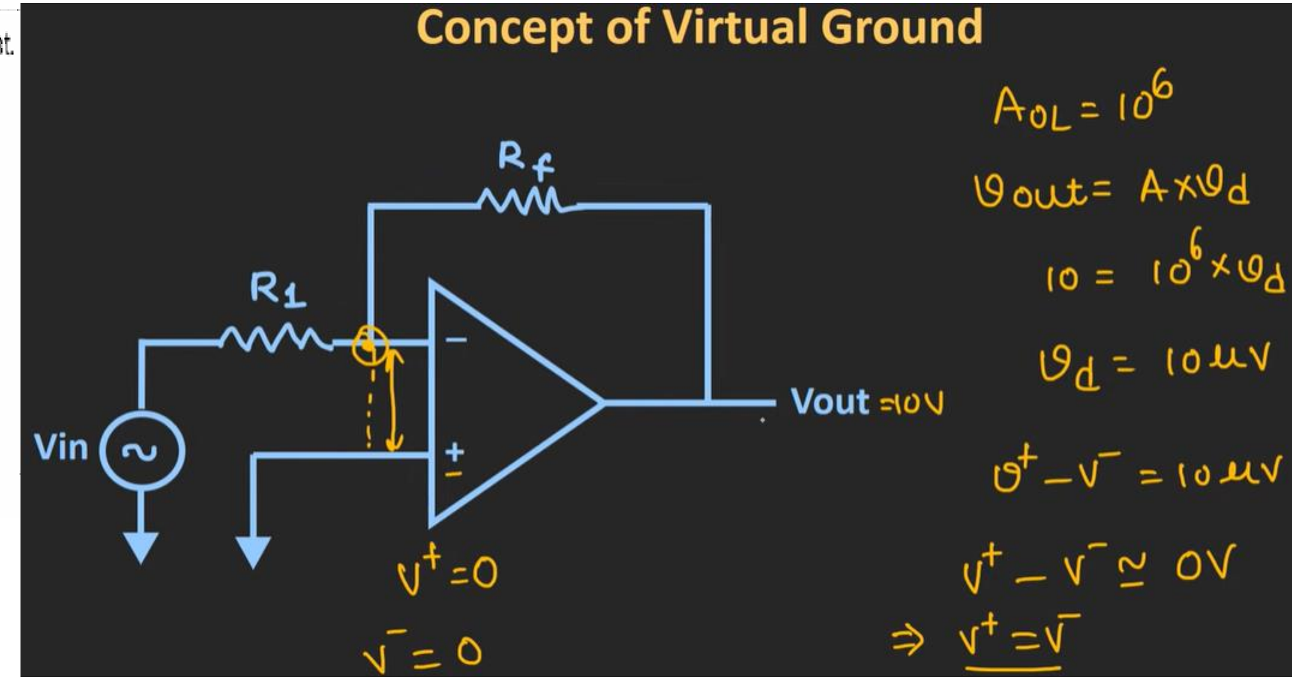
Inverting Amplifier

Concept of Virtual Ground in Closed-Loop Inverting Amplifier

e 18-13 The concept of virtual ground: shorted to voltage and open to current.





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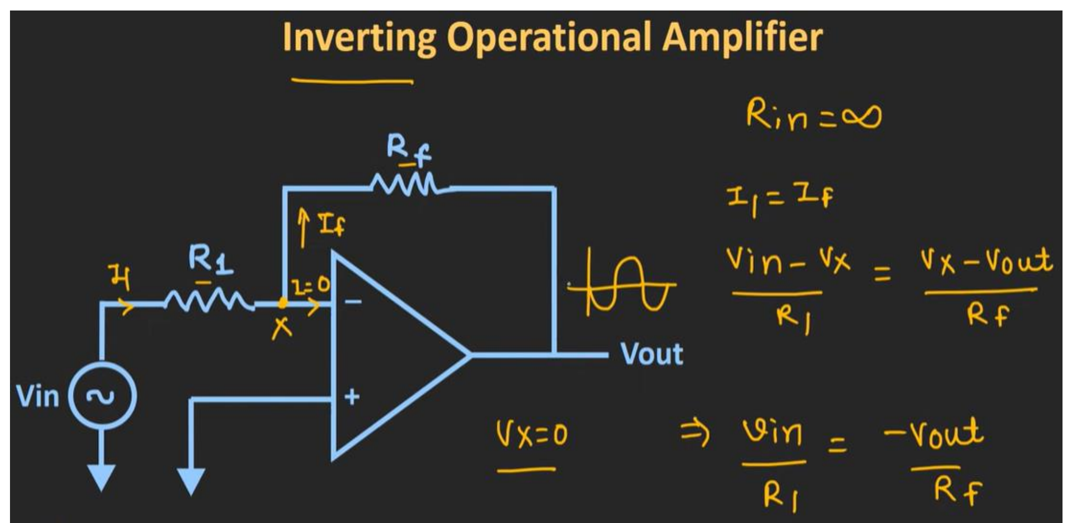


Inverting Amplifier

Voltage Gain of Closed Loop Inverting Amplifier

Voltage Gain

In Fig. 18-14, visualize a virtual ground on the inverting input. Then, the right end of R_1 is a voltage ground, so we can write:

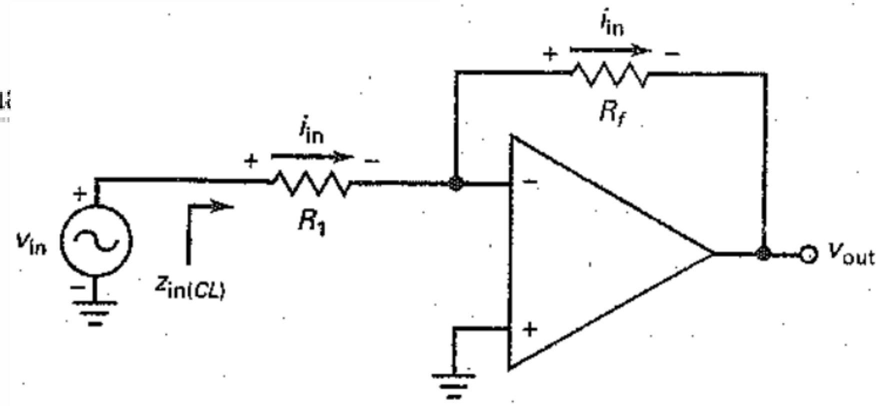
$$v_{in} = i_{in} R_1$$

Similarly, the left end of R_f is a voltage ground, so the m age is:

$$v_{out} = -i_{in} R_f$$

Divide v_{out} by v_{in} to get the voltage gain:

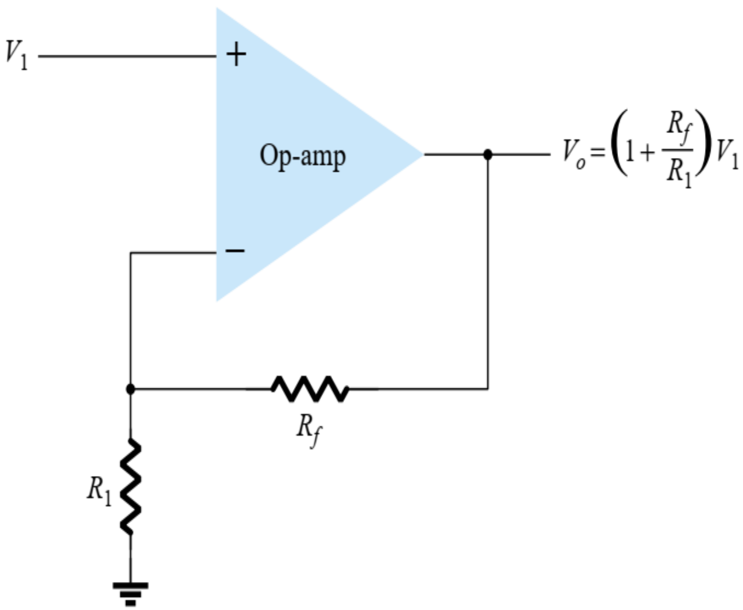
$$A_{v(CL)} = \frac{-R_f}{R_1}$$

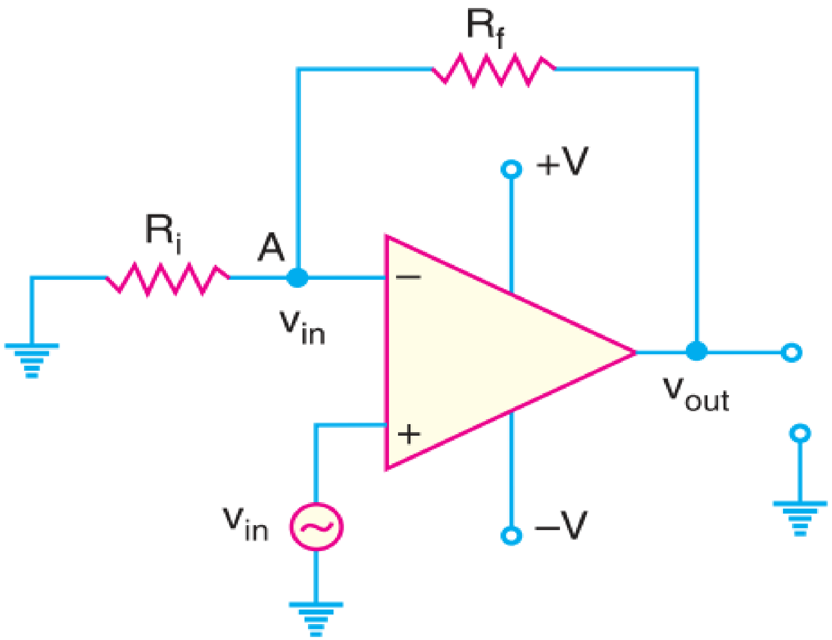


where $A_{v(CL)}$ is the closed-loop voltage gain. This is called the **closed-loop voltage gain** because it is the voltage when there is a feedback path between the output and the input. Because of the negative feedback, the closed-loop voltage gain $A_{v(CL)}$ is always smaller than the open-loop voltage gain A_{VOL}.

Example 18.7 is needed to be solved.

Closed Loop Non-Inverting Amplifier





Closed Loop Non-Inverting Amplifier

Non-Inverting Amplifier

Output Voltage of Closed-Loop Non-Inverting Amplifier

Noninverting Amplifier

The connection of Fig. 10.35a shows an op-amp circuit that works as a noninverting amplifier or constant-gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability (discussed later). To determine the voltage gain of the circuit, we can use the equivalent representation shown in Fig. 10.35b. Note that the voltage across R_1 is V_1 since $V_i \approx 0$ V. This must be equal to the output voltage, through a voltage divider of R_1 and R_f, so that

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

which results in

$$\boxed{\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}} \qquad \textbf{(10.9)}$$

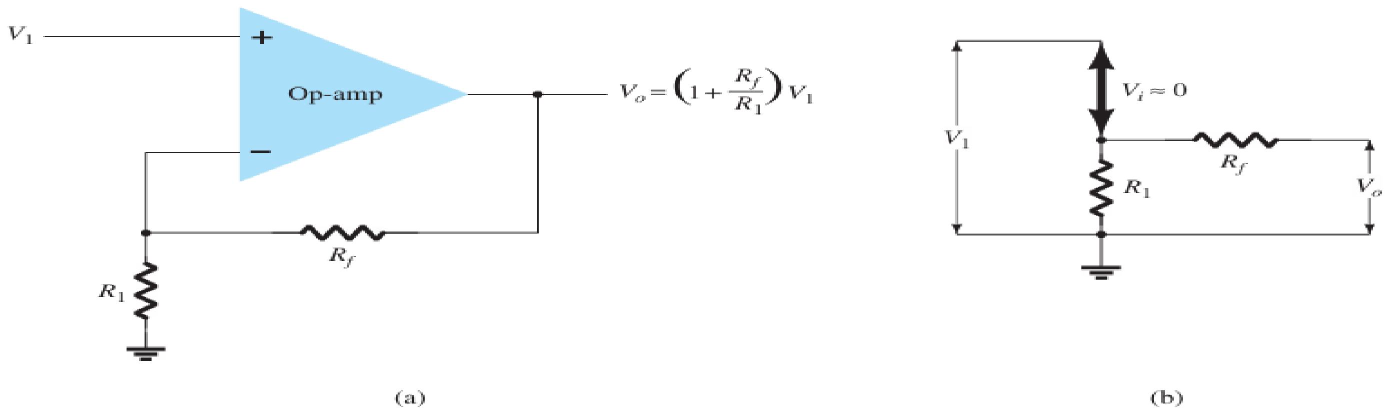
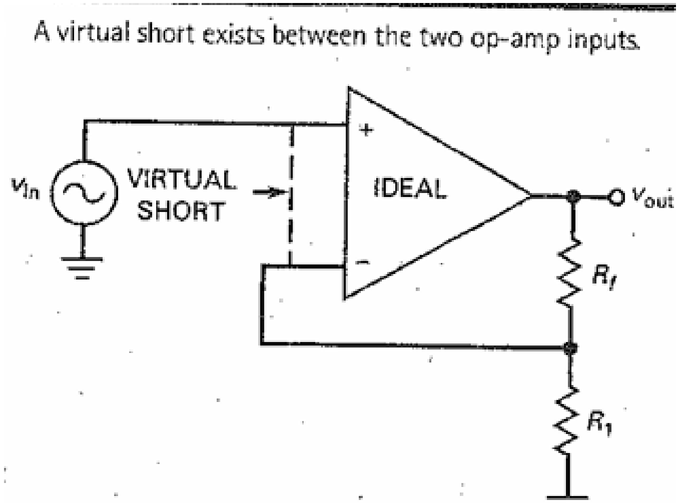


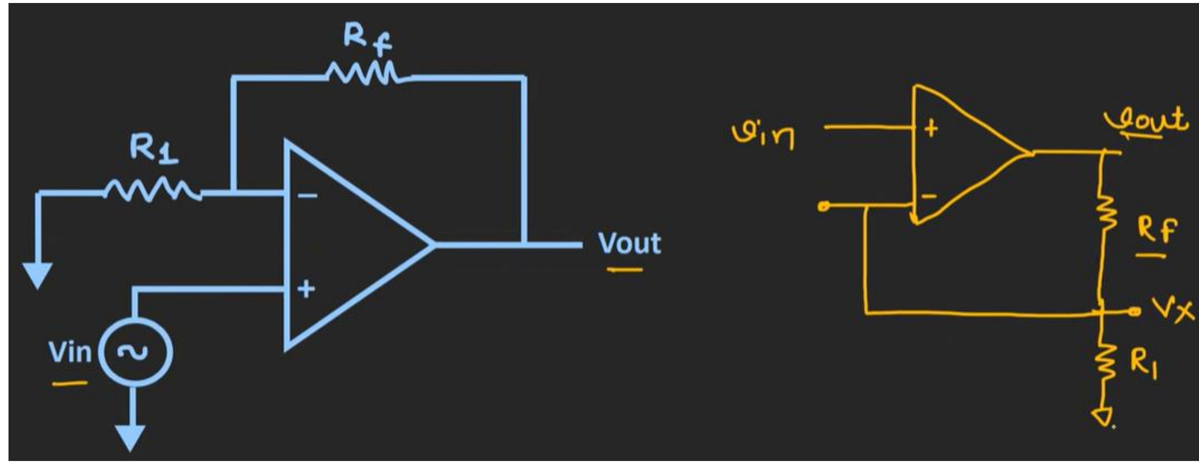
FIG. 10.35
Noninverting constant-gain multiplier.

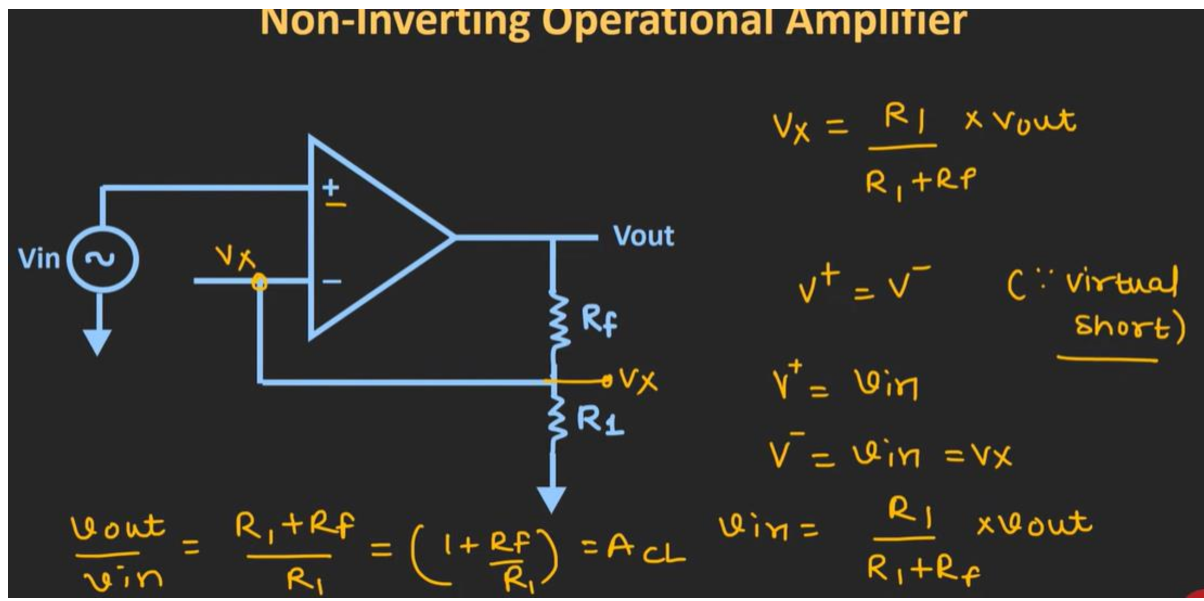
Example 10.6 is needed to be solved

Non-Inverting Amplifier

Concept of Virtual Ground in Closed-Loop Non-Inverting Amplifier







Example 18.10 is needed to be solved

Chapter 18, Page 681 of **Electronic Principles 7th Edition** *by Albert Malvino, David Bates*

Non-Inverting Amplifier

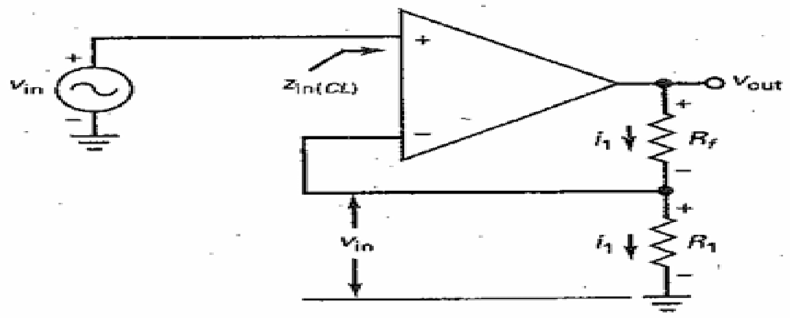
Voltage Gain of Closed Loop Non-Inverting Amplifier

Voltage Gain

In Fig. 18-20, visualize a virtual short between the input terminals of the op amp. Then, the virtual short means that the input voltage appears across R_1, as shown. So, we can write:

$$v_{in} = i_1 R_1$$

Figure 18–20 Input voltage appears across R_1 and same current flows through resistors.



Since no current can flow through a virtual short, the same i_1 current must flow through R_f, which means that the output voltage is given by:

$$v_{out} = i_1(R_f + R_1)$$

Divide v_{out} by v_{in} to get the voltage gain:

$$A_{v(CL)} = \frac{R_f + R_1}{R_1}$$

or

$$A_{v(CL)} = \frac{R_f}{R_1} + 1 \qquad (18\text{-}12)$$

This is easy to remember because it is the same as the equation for an inverting amplifier, except that we add 1 to the ratio of resistances. Also note that the output is in phase with the input. Therefore, no (−) sign is used in the voltage gain equation.

Chapter 18, Page 681-682 of **Electronic Principles 7th Edition** *by Albert Malvino, David Bates*

Summing Amplifier

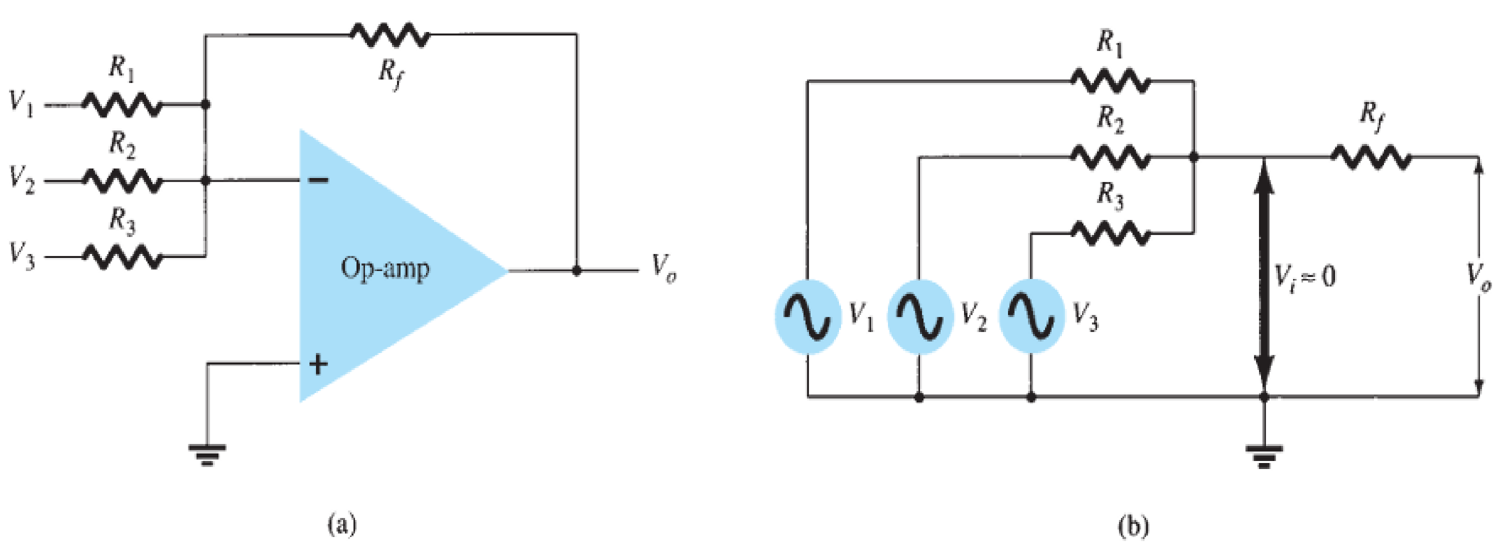


FIG. 10.37

(a) Summing amplifier; (b) virtual-ground equivalent circuit.

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Summing Amplifier and the Equation of its Output Voltage

Example 10.7 is needed to be solved

Summing Amplifier

The Summing Amplifier

Whenever we need to combine two or more analog signals into a single output, the **summing amplifier** of Fig. 18-23*a* is a natural choice. For simplicity, the circuit shows only two inputs, but we can have as many inputs as needed for the application. A circuit like this amplifies each input signal. The gain for each *channel* or input is given by the ratio of the feedback resistance to the appropriate input resistance. For instance, the closed-loop voltage gains of Fig. 18-23*a* are:

$$A_{v1(CL)} = \frac{-R_f}{R_1} \quad \text{and} \quad A_{v2(CL)} = \frac{-R_f}{R_2}$$

The summing circuit combines all the amplified input signals into a single output, given by:

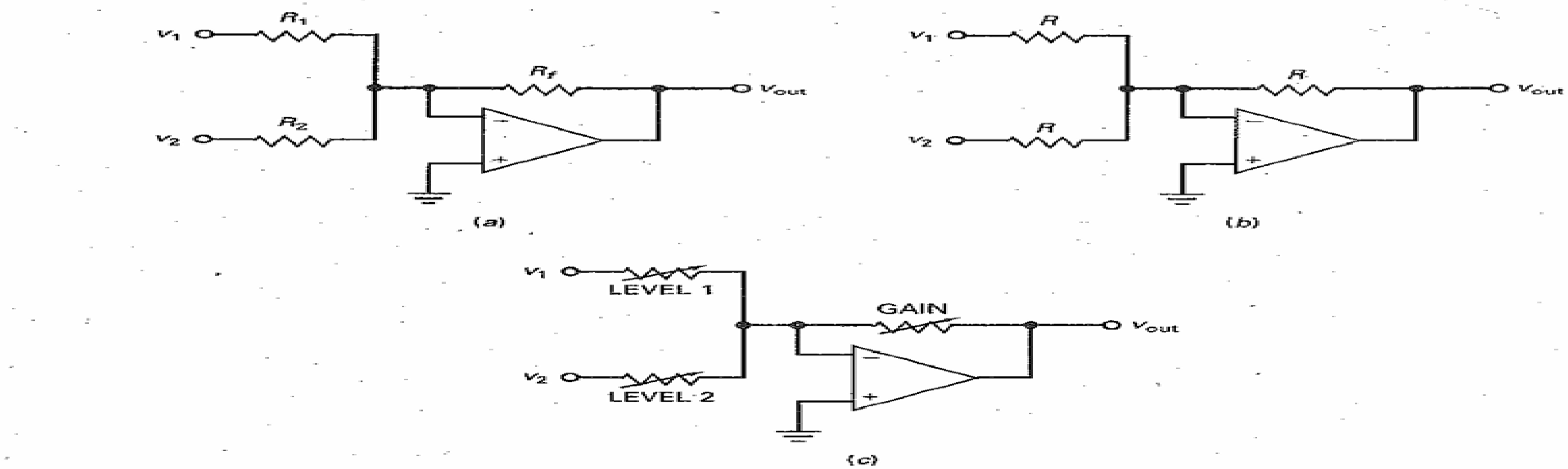
$$v_{out} = A_{v1(CL)}v_1 + A_{v2(CL)}v_2 \tag{18-13}$$

It is easy to prove Eq. (18-13). Since the inverting input is a virtual ground, the total input current is:

$$i_{in} = i_1 + i_2 = \frac{v_1}{R_1} + \frac{v_2}{R_2}$$

Summing Amplifier

Figure 18–23 Summing amplifier.



Because of the virtual ground, all this current flows through the feedback resistor, producing an output voltage with a magnitude of:

$$v_{out} = (i_1 + i_2)R_f = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2\right)$$

Here you see that each input voltage is multiplied by its channel gain and added to produce the total output. The same result applies to any number of inputs.

In some applications, all resistances are equal, as shown in Fig. 18-23*b*. In this case, each channel has a closed-loop voltage gain of unity (1) and the output is given by:

$$v_{out} = -(v_1 + v_2 + \ldots + v_n)$$

Example 18.12 is needed to be solved

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Differentiator

Differentiator

A differentiator circuit is shown in Fig. 10.41. Although it is not as useful as the circuit forms covered above, the differentiator does provide a useful operation, the resulting relation for the circuit being

$$\boxed{v_o(t) = -RC\frac{dv_1(t)}{dt}} \qquad \textbf{(10.15)}$$

where the scale factor is $-RC$.

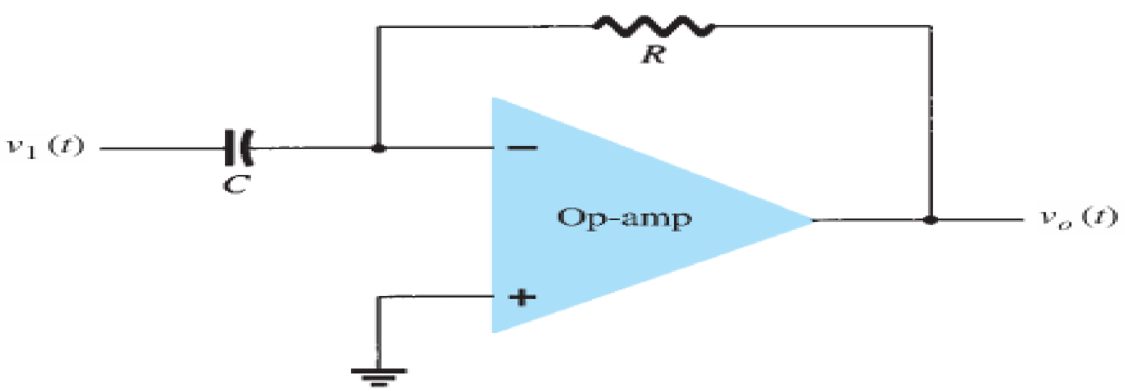

FIG. 10.41
Differentiator circuit.

Derivation of the output voltage is needed.

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Integrator

Integrator

So far, the input and feedback components have been resistors. If the feedback component used is a capacitor, as shown in Fig. 10.38a, the resulting connection is called an *integrator*. The virtual-ground equivalent circuit (Fig. 10.38b) shows that an expression for the voltage between input and output can be derived in terms of the current I from input to output. Recall that virtual ground means that we can consider the voltage at the junction of R and X_C to be ground (since $V_i \approx 0$ V) but that no current goes into ground at that point. The capacitive impedance can be expressed as

$$X_C = \frac{1}{j\omega C} = \frac{1}{sC}$$

where $s = j\omega$ is in the Laplace notation.* Solving for V_o/V_1 yields

$$I = \frac{V_1}{R} = -\frac{V_o}{X_C} = \frac{-V_o}{1/sC} = -sCV_o$$

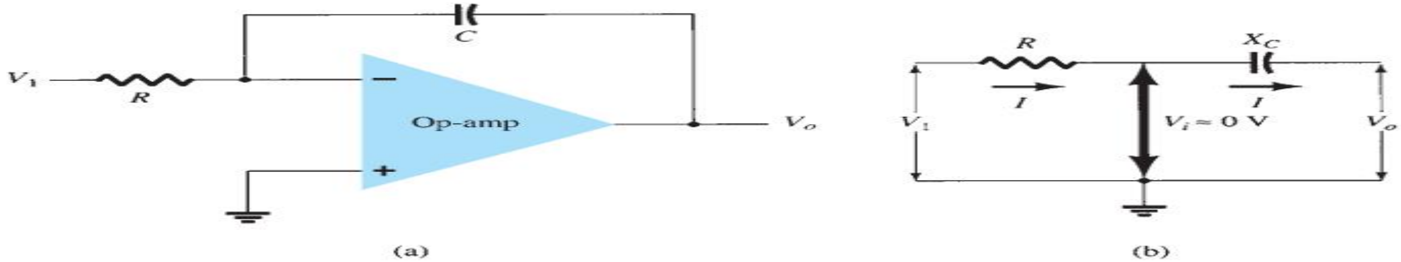

FIG. 10.38
Integrator.

$$\frac{V_o}{V_1} = \frac{-1}{sCR} \quad (10.12)$$

This expression can be rewritten in the time domain as

$$\boxed{v_o(t) = -\frac{1}{RC}\int v_1(t)\,dt} \quad (10.13)$$

Derivation of the output voltage is needed.

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Voltage Follower

Unity Follower

The unity-follower circuit, as shown in Fig. 10.36a, provides a gain of unity (1) with no polarity or phase reversal. From the equivalent circuit (see Fig. 10.36b) it is clear that

$$\boxed{V_o = V_1} \qquad \textbf{(10.10)}$$

and that the output is the same polarity and magnitude as the input. The circuit operates like an emitter- or source-follower circuit except that the gain is exactly unity.

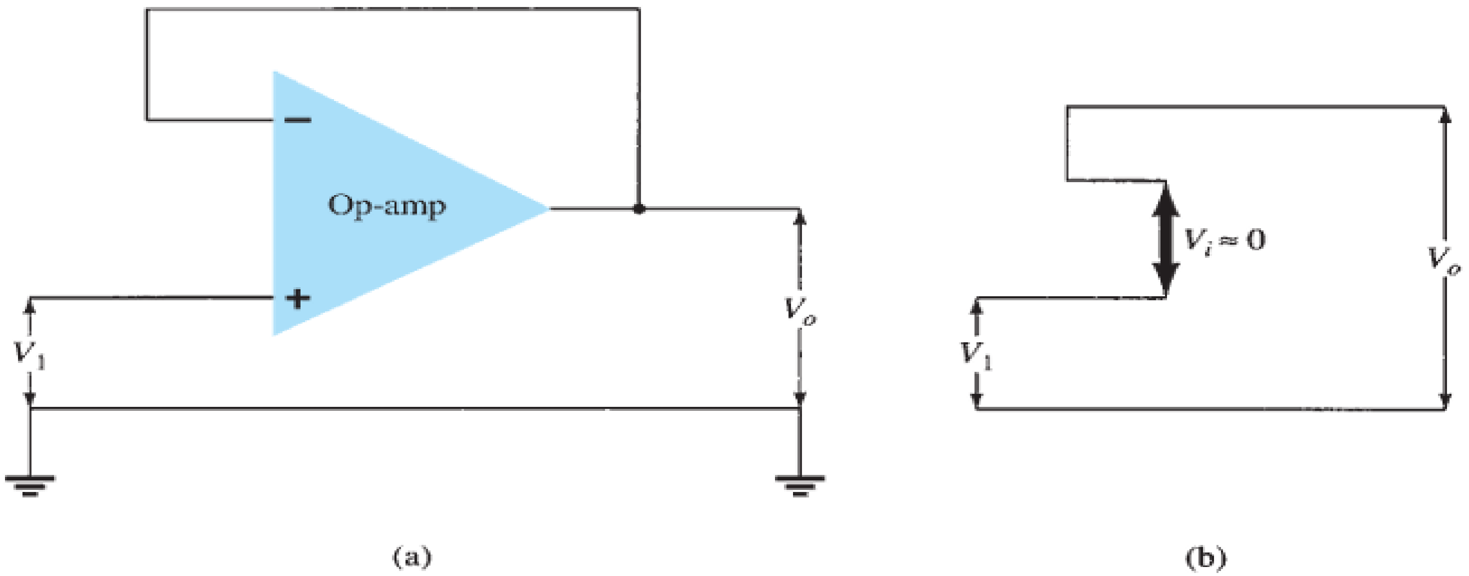

FIG. 10.36
(a) Unity follower; (b) virtual-ground equivalent circuit.

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Please solve Examples and Exercise problems of related topics

Practice yourself and send me your feedback, if any.