Power Electronic Devices

Text Books

1. Electronic Devices and Circuit Theory

by R Boylestad and L Nashelsky

Silicon Controlled Rectifier (SCR)

- Within the family of *pnpn* devices, the silicon-controlled rectifier (SCR) is unquestionably of the greatest interest today.
- It was first introduced in 1956 by Bell Telephone Laboratories.
- A few of the more common areas of application for SCRs include relay controls, time-delay circuits, regulated power suppliers, static switches, motor controls, choppers, inverters, cycloconverters, battery chargers, protective circuits, heater controls, and phase controls.

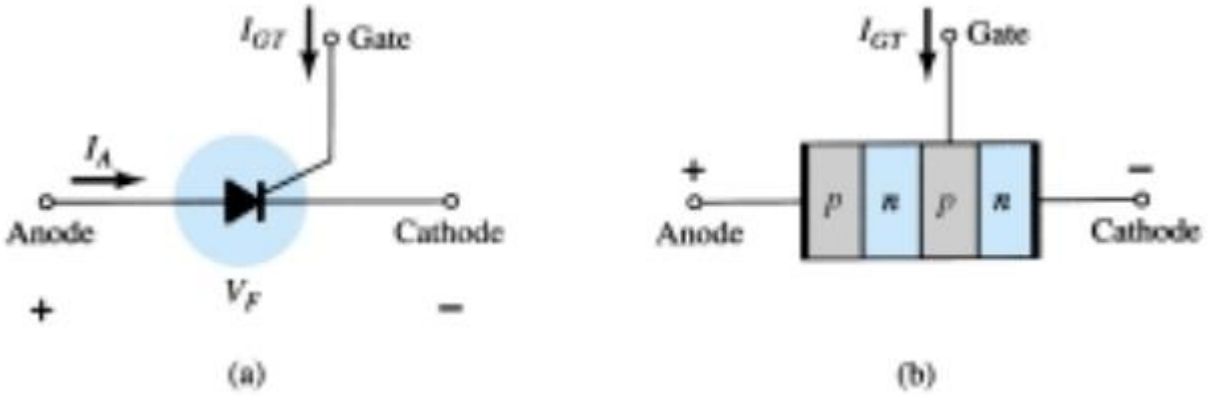


Figure 21.1 (a) SCR symbol; (b) basic construction.

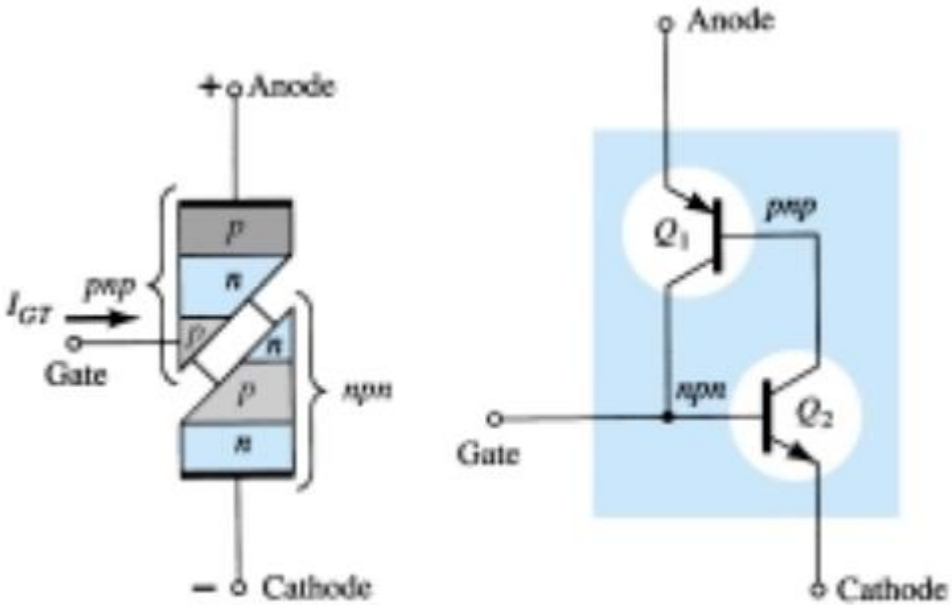
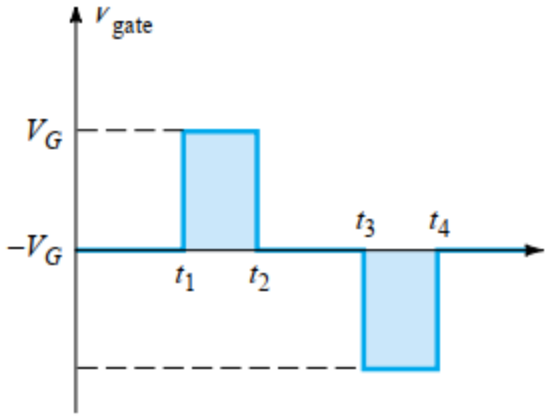


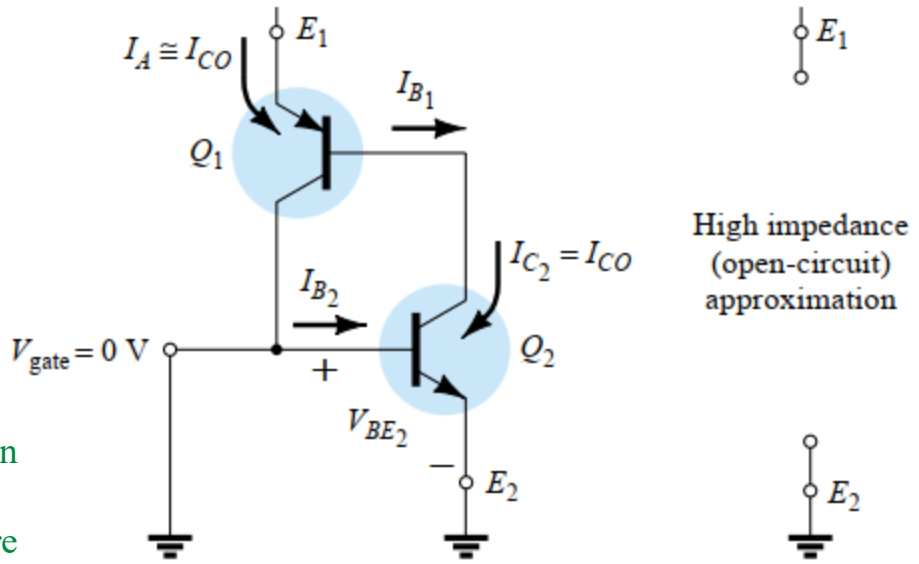
Figure 21.2 SCR two-transistor equivalent circuit.

Silicon Controlled Rectifiers (SCR)



(a)

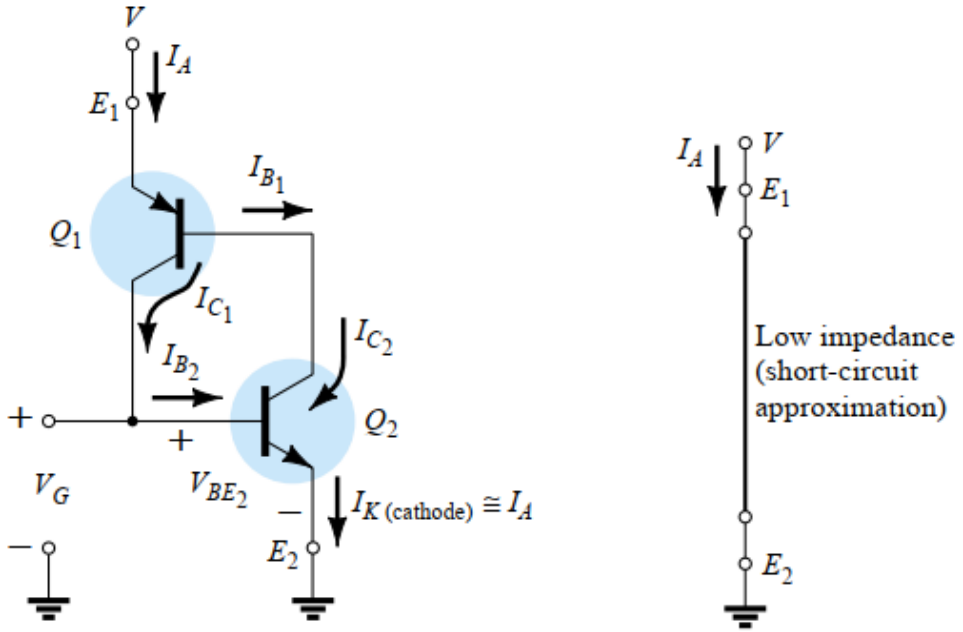
- The SCR is a rectifier constructed of silicon material with a third terminal for control purposes.
- Silicon was chosen because of its high temperature and power capabilities.



(b) (c)

Figure 21.3 "Off" state of the SCR.

❖ In addition to gate triggering, SCRs can also be turned on by significantly raising the temperature of the device or raising the anode-to-cathode voltage to the breakover value.

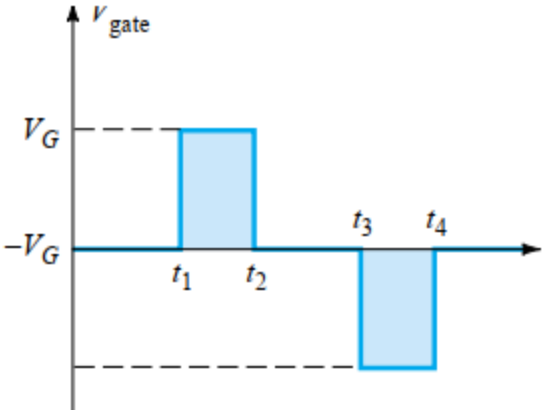


(a) (b)

Figure 21.4 "On" state of the SCR.

Silicon Controlled Rectifiers (SCR)

An SCR *cannot* be turned off by simply removing the gate signal, and only a special few can be turned off by applying a negative pulse to the gate terminal as shown in Fig. t = t_3.



The two general methods for turning off an SCR are categorized as the anode current interruption and the forced-commutation technique.

The two possibilities for current interruption are shown in Fig. 21.5. In Fig. 21.5a, I_A is zero when the switch is opened (series interruption), while in Fig. 21.5b, the same condition is established when the switch is closed (shunt interruption).

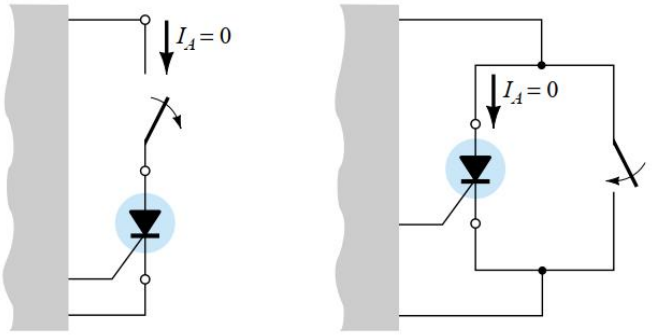


Figure 21.5 Anode current interruption.

- Forced commutation is the "forcing" of current through the SCR in the direction opposite to forward conduction. There are a wide variety of circuits for performing this function

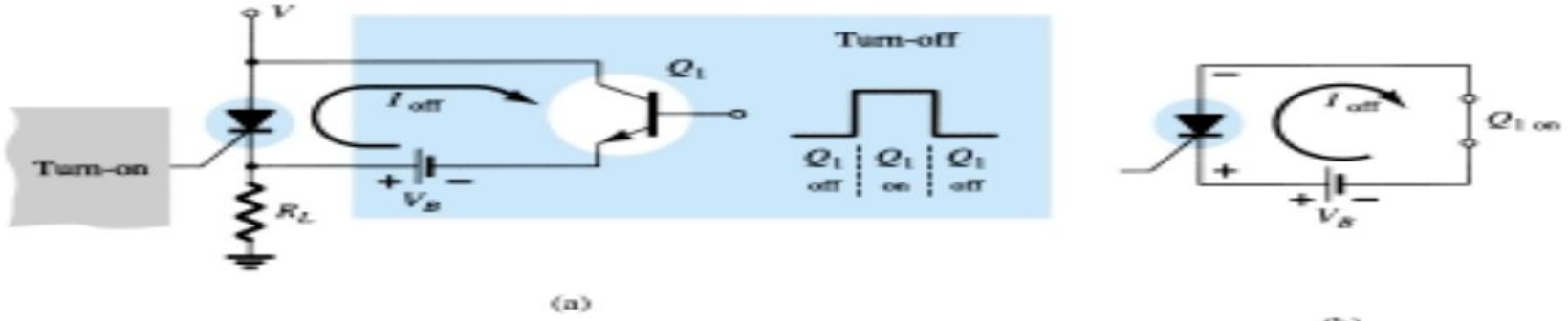


Figure 21.6 Forced-commutation technique.

SCR CHARACTERISTICS AND RATINGS

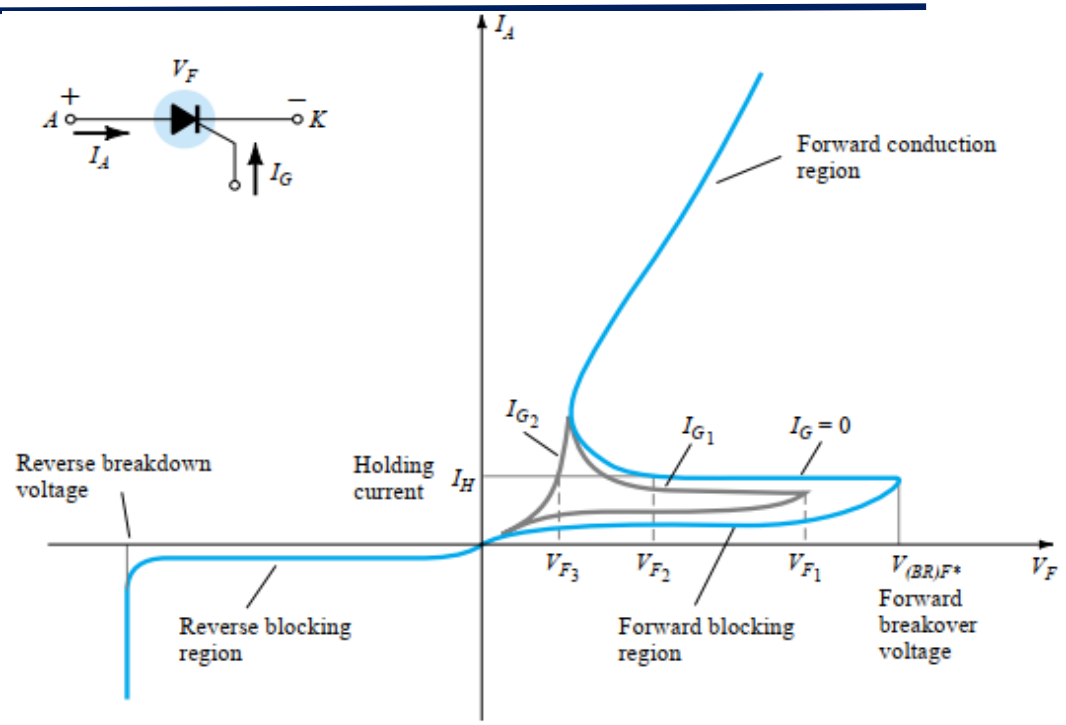


Figure 21.7 SCR characteristics.

1. *Forward breakover voltage* $V_{(BR)F*}$ is that voltage above which the SCR enters the conduction region. The asterisk (*) is a letter to be added that is dependent on the condition of the gate terminal as follows:

   O = open circuit from G to K

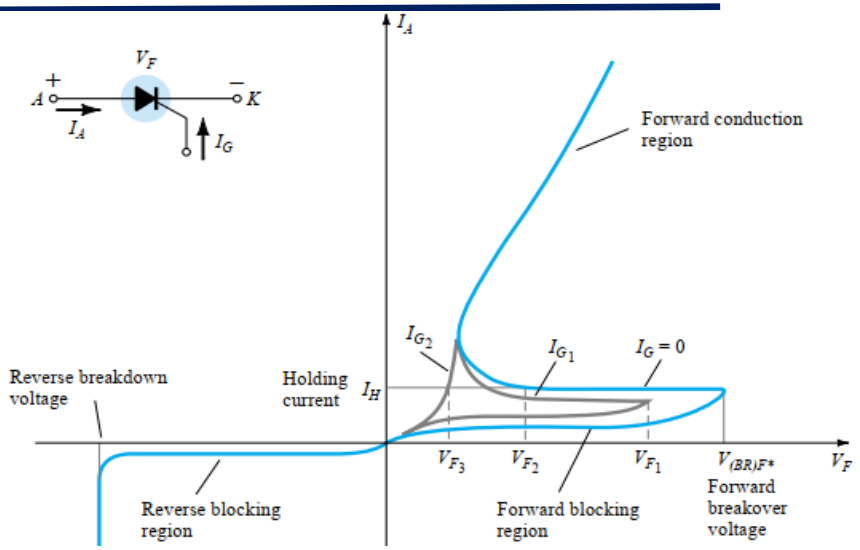
   S = short circuit from G to K

   R = resistor from G to K

   V = fixed bias (voltage) from G to K

2. *Holding current* (I_H) is that value of current below which the SCR switches from the conduction state to the forward blocking region under stated conditions.
3. *Forward and reverse blocking regions* are the regions corresponding to the open-circuit condition for the controlled rectifier which *block* the flow of charge (current) from anode to cathode.
4. *Reverse breakdown voltage* is equivalent to the Zener or avalanche region of the fundamental two-layer semiconductor diode.

SCR CHARACTERISTICS AND RATINGS



It should be immediately obvious that the SCR characteristics of Fig. 21.7 are very similar to those of the basic two-layer semiconductor diode except for the horizontal offshoot before entering the conduction region. It is this horizontal jutting region that gives the gate control over the response of the SCR. For the characteristic having the solid blue line in Fig. 21.7 ($I_G = 0$), V_F must reach the largest required breakover voltage ($V_{(BR)F^*}$) before the "collapsing" effect will result and the SCR can enter the conduction region corresponding to the *on* state. If the gate current is increased to I_{G_1}, as shown in the same figure by applying a bias voltage to the gate terminal, the value of V_F required for the conduction (V_{F_1}) is considerably less. Note also that I_H drops with increase in I_G. If increased to I_{G_2}, the SCR will fire at very low values of voltage (V_{F_3}) and the characteristics begin to approach those of the basic *p-n* junction diode. Looking at the characteristics in a completely different sense, for a particular V_F voltage, say V_{F_2} (Fig. 21.7), if the gate current is increased from $I_G = 0$ to I_{G1} or more, the SCR will fire.

Silicon Controlled Rectifiers (SCR)

21.6 SCR APPLICATIONS

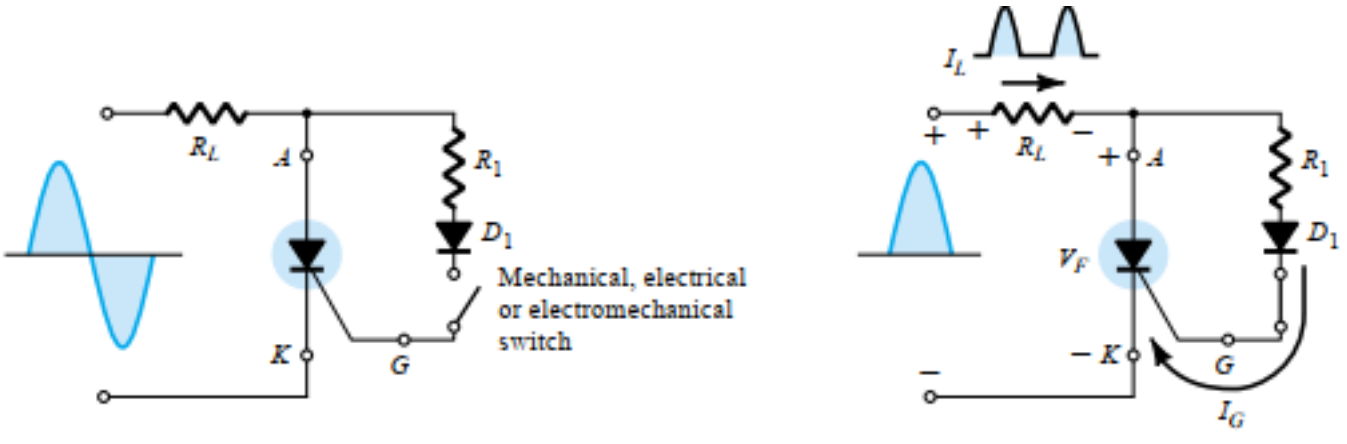


Figure 21.11 Half-wave series static switch.

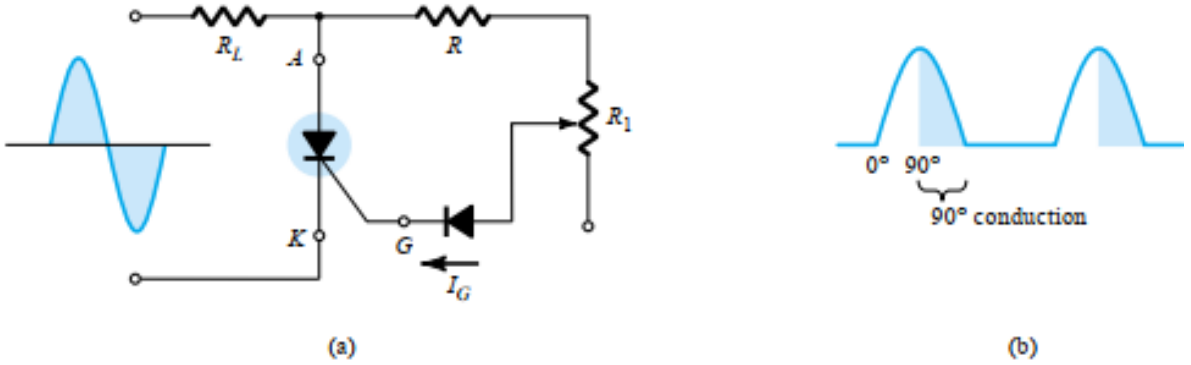
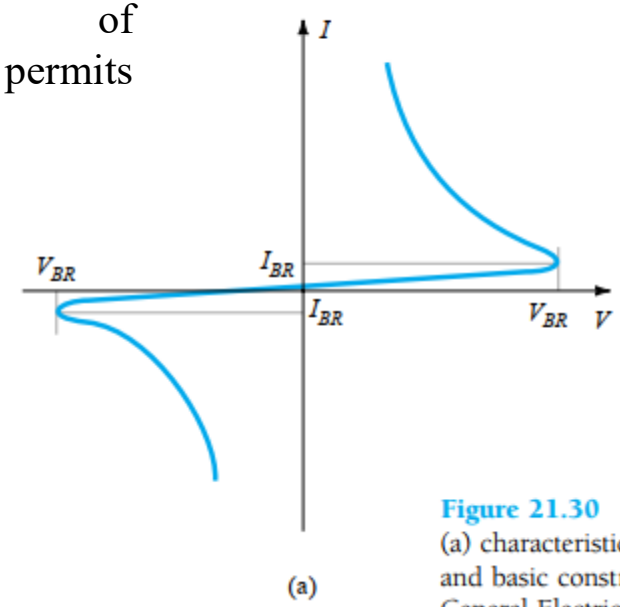


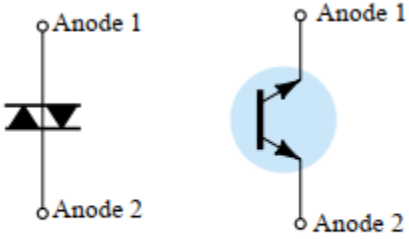
Figure 21.12 Half-wave variable-resistance phase control.

21.11 DIAC

- ✓ The diac is basically a two-terminal parallel-inverse combination of semiconductor layers that permits triggering in either direction.

- ✓ The characteristics of the device clearly demonstrate that there is a breakover voltage in either direction. This possibility of an *on* condition in either direction can be used to its fullest advantage in ac applications.





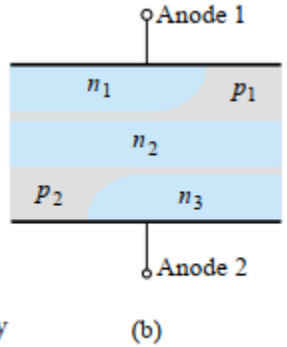


Figure 21.30 Diac: (a) characteristics; (b) symbols and basic construction. (Courtesy General Electric Company.)

- ✓ The use of the Diac in a proximity detector

The basic arrangement of the semiconductor layers of the diac is shown in Fig. 21.30b, along with its graphical symbol. Note that neither terminal is referred to as the cathode. Instead, there is an anode 1 (or electrode 1) and an anode 2 (or electrode 2). When anode 1 is positive with respect to anode 2, the semiconductor layers of particular interest are $p_1n_2p_2$ and n_3. For anode 2 positive with respect to anode 1, the applicable layers are $p_2n_2p_1$ and n_1.

For the unit appearing in Fig. 21.30, the breakdown voltages are very close in magnitude but may vary from a minimum of 28 V to a maximum of 42 V. They are related by the following equation provided in the specification sheet:

21.12 TRIAC

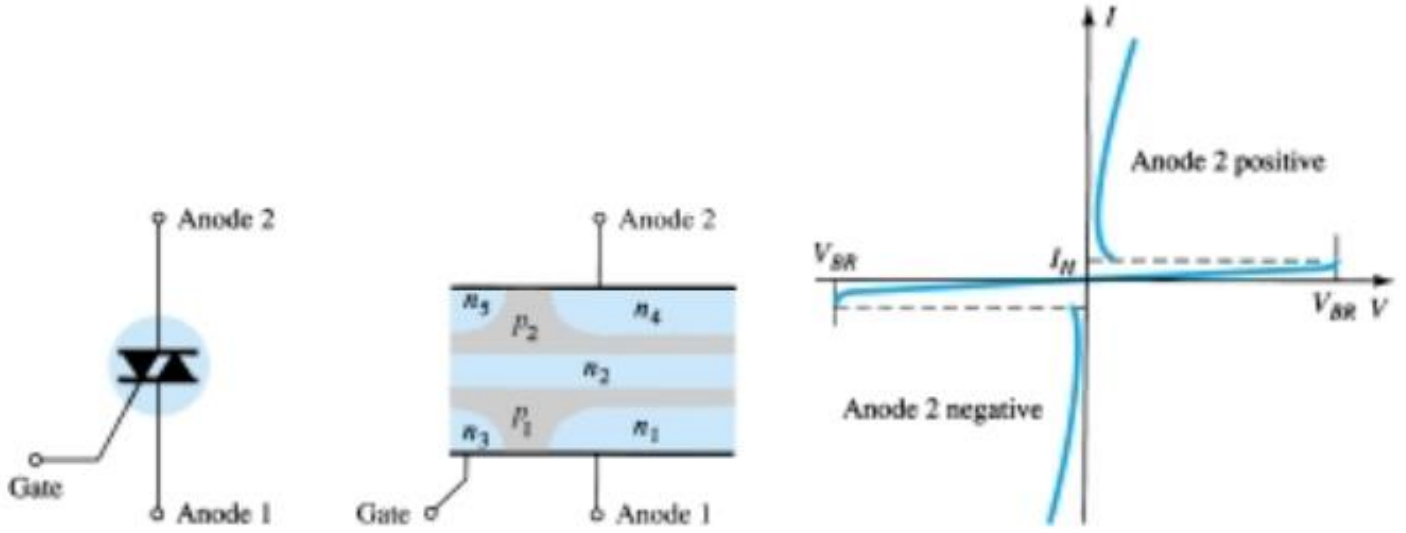


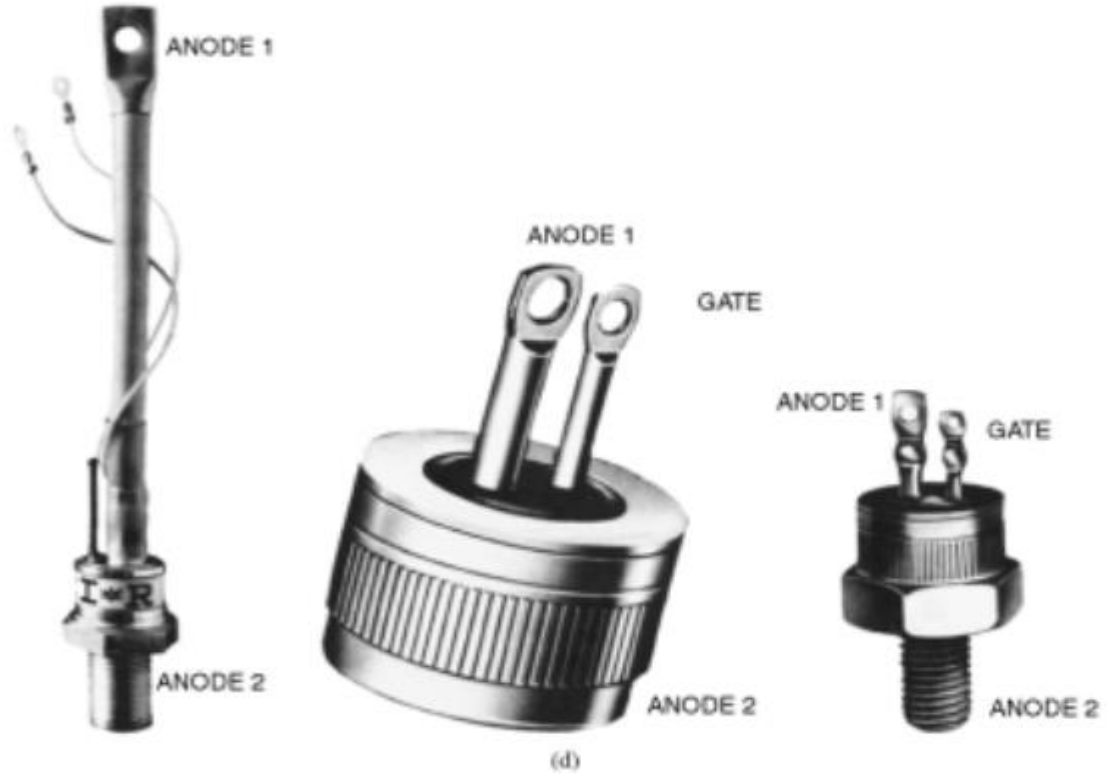
Figure 21.33 Triac: (a) symbol; (b) basic construction; (c) characteristics; (d) photographs.

- The triac is fundamentally a diac with a gate terminal for controlling the turn-on conditions of the bilateral device in either direction.
- In other words, for either direction the gate current can control the action of the device in a manner very similar to that demonstrated for an SCR.
- The characteristics, however, of the triac in the first and third quadrants are somewhat different from those of the diac, as shown in Fig. 21.33c.
- Note the holding current in each direction not present in the characteristics of the diac.

For each possible direction of conduction, there is a combination of semiconductor layers whose state will be controlled by the signal applied to the gate terminal.

21.12 TRIAC

- In this capacity, it is controlling the ac power to the load by switching on and off during the positive and negative regions of input sinusoidal signal.
- The advantage of this configuration is that during the negative portion of the input signal, the same type of response will result since both the diac and triac can fire in the reverse direction.
- By varying the resistor *R*, the conduction angle can be controlled.



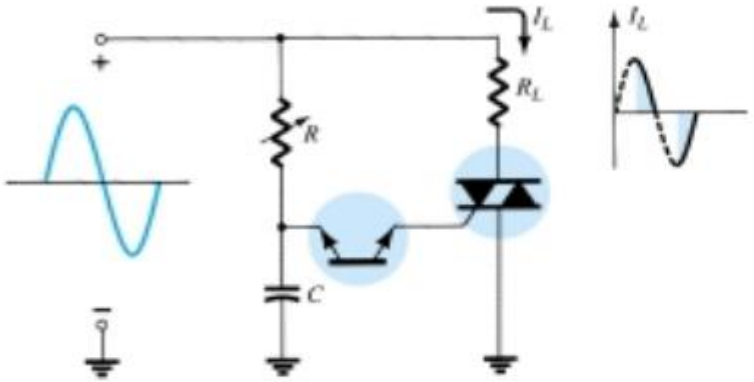


Figure 21.34 Triac application: phase (power) control.

21.13 UNIJUNCTION TRANSISTOR

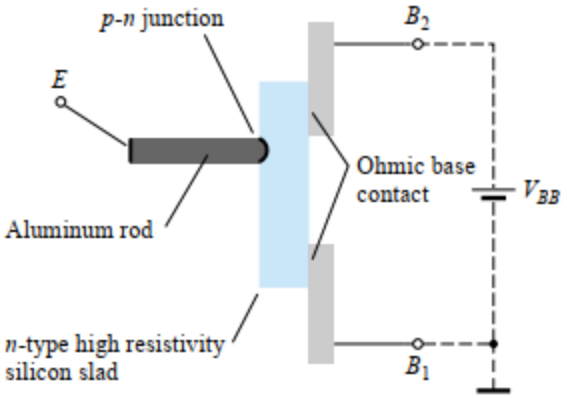


Figure 21.35 Unijunction transistor (UJT): basic construction.

The UJT is a three-terminal device having the basic construction of Fig.

→ One PN junction.
→ Three terminal device.
→ Emitter, Base 1, Base 2 } Terminals.

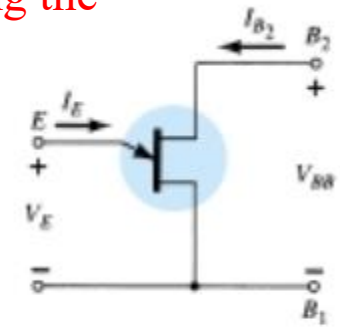


Figure 21.36 Symbol and basic biasing arrangement for the unijunction transistor.

- A slab of lightly doped (increased resistance characteristic) *n*-type silicon material has two base contacts attached to both ends of one surface and an aluminum rod alloyed to the opposite surface.
- The *p-n* junction of the device is formed at the boundary of the aluminum rod and the *n*-type silicon slab. The single *p-n* junction accounts for the terminology *unijunction.*
- It was originally called a duo (double) base diode due to the presence of two base contacts.
- Note in Fig. 21.35 that the aluminum rod is alloyed to the silicon slab at a point closer to the base 2 contact than the base 1 contact and that the base 2 terminal is made positive with respect to the base 1 terminal by V_{BB} volts. The effect of each will become evident in the paragraphs to follow.

In symbol, the emitter leg is drawn at an angle to the vertical line representing the slab of *n*-type material. The arrowhead is pointing in the direction of conventional current (hole) flow when the device is in the forward-biased, active, or conducting state.

$$R_{BB} = (R_{B_1} + R_{B_2})|_{I_E} = 0$$

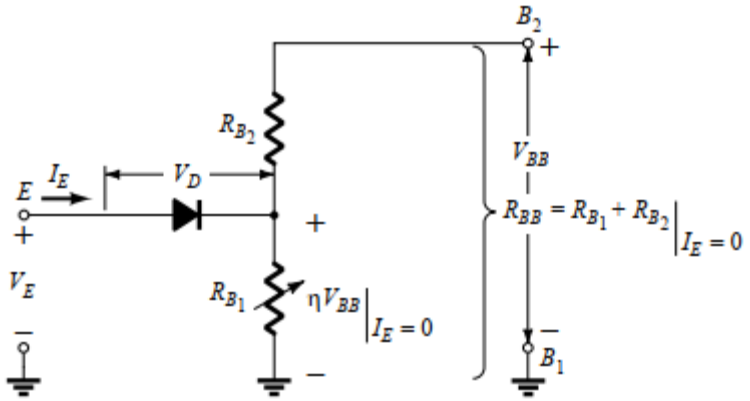


Figure 21.37 UJT equivalent circuit.

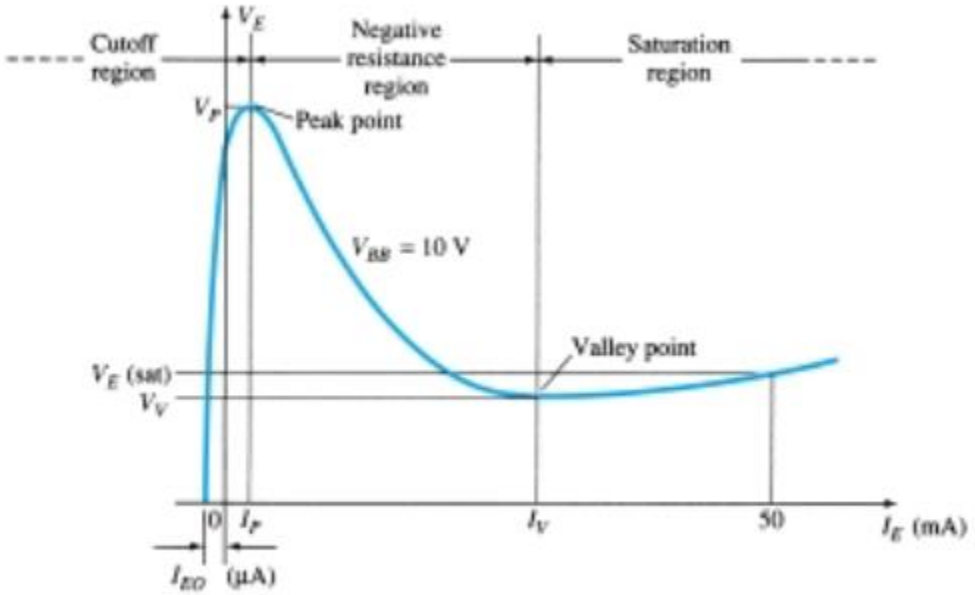


Figure 21.38 UJT static emitter-characteristic curve.

- Cutoff: when V_E is less (up to peak point, V_p) than the other side voltage of the diode (V_D+eta*V_{BB}), diode is in reverse bias
- Negative resistance: when V_E increases I_E increases, majority of holes pass from p type to n type region, conductivity increases hence, R_{B1} decreases. V decreases as well, reaches a valley voltage.
- Saturation: Increasing V_E does not decreases the resistance , gets saturated actually

21.13 UNIJUNCTION TRANSISTOR

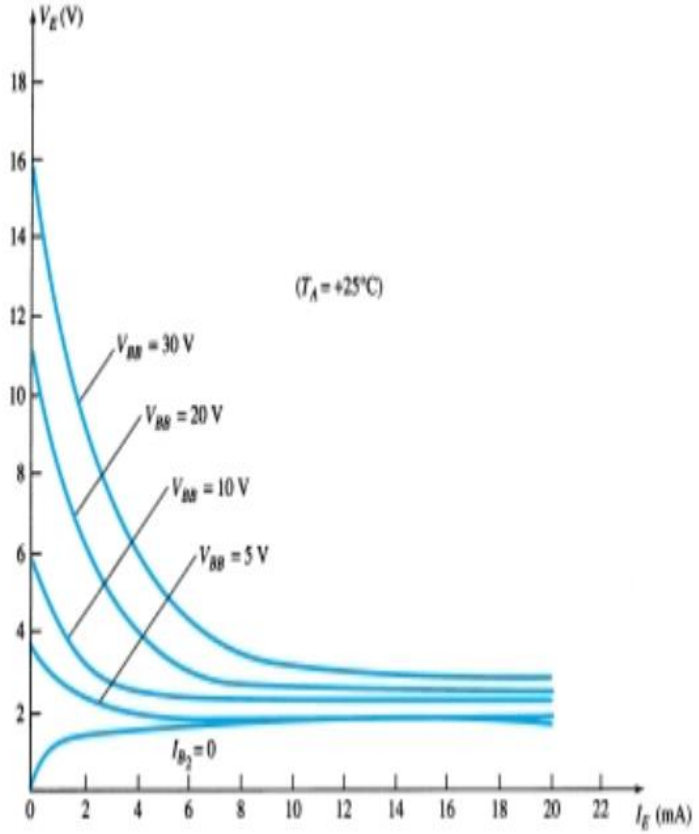


Figure 21.39 Typical static emitter-characteristic curves for a UJT.

(a)

Absolute maximum ratings (25°C):

Power dissipation	300 mW
RMS emitter current	50 mA
Peak emitter current	2 A
Emitter reverse voltage	30 V
Interbase voltage	35 V
Operating temperature range	−65°C to +125°C
Storage temperature range	−65°C to +150°C

Electrical characteristics (25°C):

		Min.	Typ.	Max.
Intrinsic standoff ratio		0.56	0.65	
(V_{BB} = 10 V)	η	0.56	0.65	0.75
Interbase resistance (kΩ)				
(V_{BB} = 3 V, I_E = 0)	R_{BB}	4.7	7	9.1
Emitter saturation voltage				
(V_{BB} = 10 V, I_E = 50 mA)	$V_{E(sat)}$		2	
Emitter reverse current				
(V_{BB} = 3 V, I_{B1} = 0)	I_{EO}		0.05	12
Peak point emitter current	I_P (μA)		0.04	5
(V_{BB} = 25 V)				
Valley point current				
(V_{BB} = 20 V)	I_V (mA)	4	6	

(b)

(c)

Figure 21.40 UJT: (a) appearance; (b) specification sheet; (c) terminal identification. (Courtesy General Electric Company.)

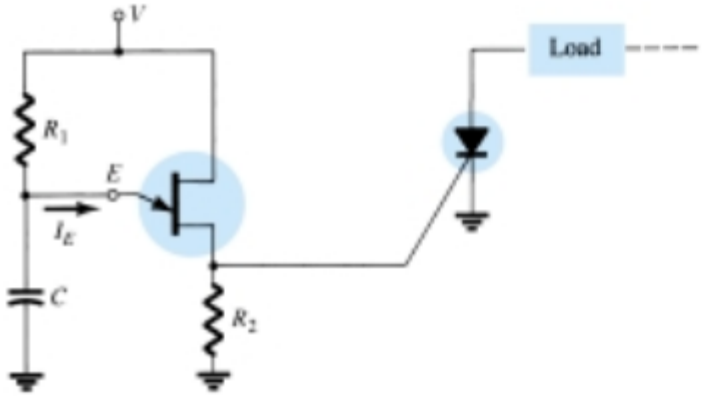


Figure 21.41 UJT triggering of an SCR.

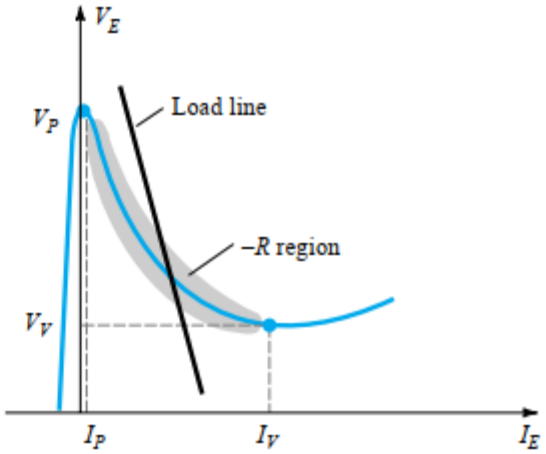


Figure 21.42 Load line for a triggering application.

Applications: oscillators, trigger circuits, sawtooth generators, phase control, timing circuits, bistable networks, and voltage- or current-regulated supplies.

The fact that this device is, in general, a low-power-absorbing device under normal operating conditions is a tremendous aid in the continual effort to design relatively efficient systems.

Definitions: Power Amplifier

An amplifier receives a signal from some pickup transducer or other input source and provides a larger version of the signal to some output device or to another amplifier stage.

An input transducer signal is generally small (a few millivolts from a cassette or CD input, or a few microvolts from an antenna) and needs to be amplified sufficiently to operate an output device (speaker or other power-handling device).

Amplifier Types

Small signal amplifiers:

- the main factors are usually amplification linearity and magnitude of gain.
- Since signal voltage and current are small in a small-signal amplifier, the amount of power-handling capacity and power efficiency are of little concern.

Large-signal or power amplifiers:

Primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts.

Amplifier Types

One method used to categorize amplifiers is by class.

What is class?

Amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal.

Class A (Operating cycle 360^0)

Class B (Operating cycle 180^0)

Class AB (Operating cycle 180^0 to 360^0)

Class C (Less than 180^0)

Class D (Pulse operation)

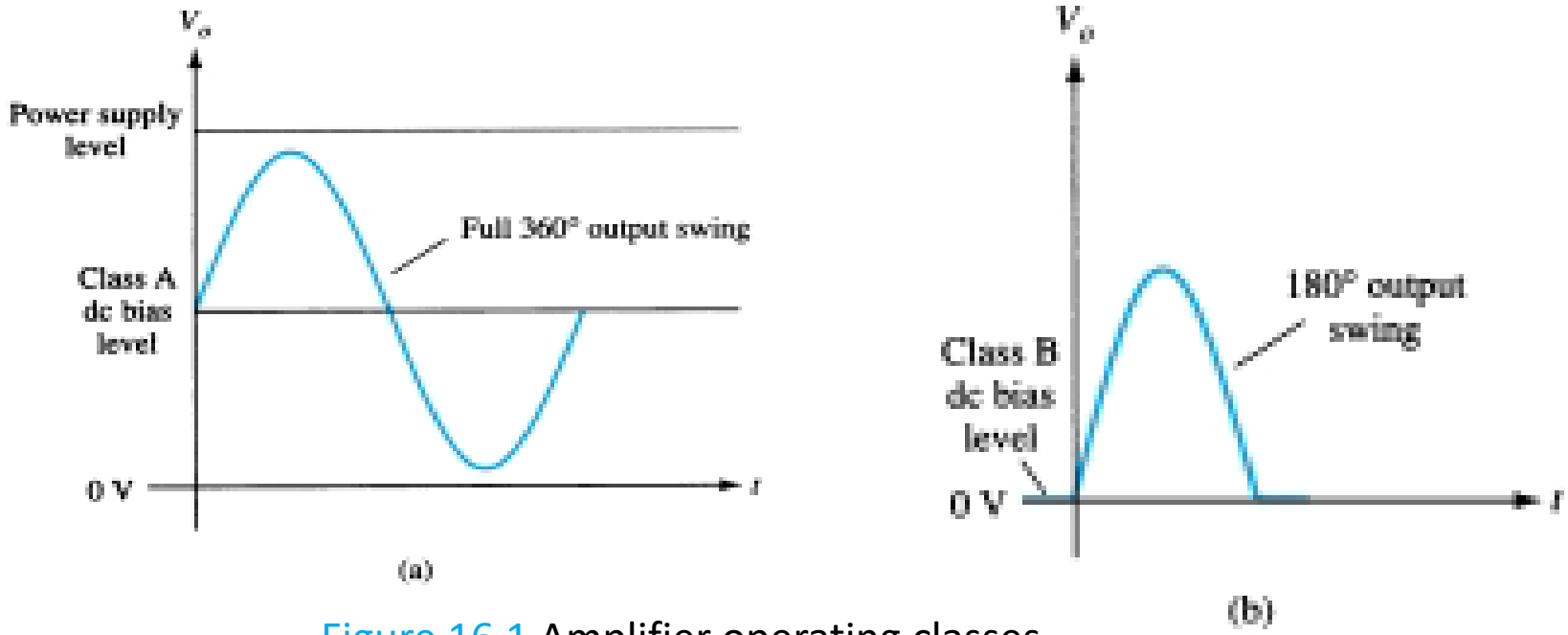


Figure 16.1 Amplifier operating classes.

TABLE 16.1 Comparison of Amplifier Classes

	Class A	Class AB	Class B	Class C*	Class D
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

**Class C is usually not used for delivering large amounts of power, thus the efficiency is not given here.*

Amplifier Efficiency

The power efficiency of an amplifier, defined as the ratio of power output to power input, improves (gets higher) going from class A to class D.

Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%	Typically over 90%

**Class C is usually not used for delivering large amounts of power, thus the efficiency is not given here.*

SERIES-FED CLASS A AMPLIFIER

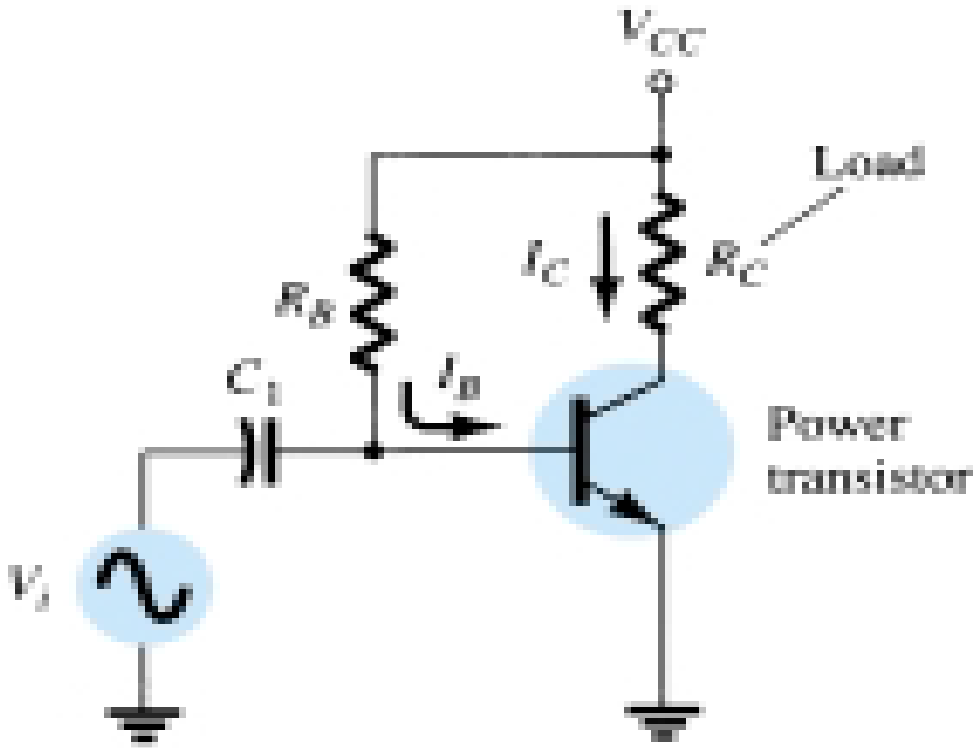


Figure 16.2 Series-fed class A large-signal amplifier.

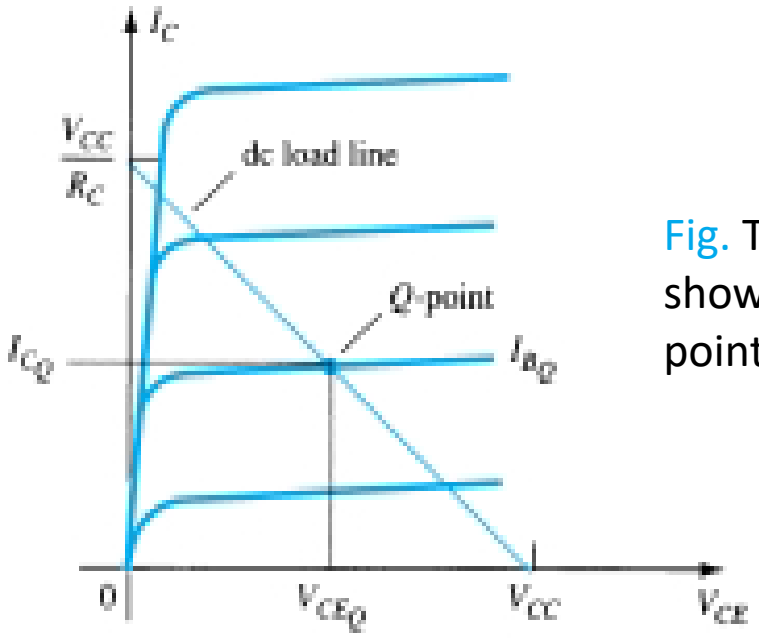


Fig. Transistor characteristic showing load line and Q point.

DC Bias Operation

The dc bias set by V_{CC} and R_B fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7\ \text{V}}{R_B}$$

with the collector current then being

$$I_C = \beta I_B$$

with the collector–emitter voltage then

$$V_{CE} = V_{CC} - I_C R_C$$

AC Operation

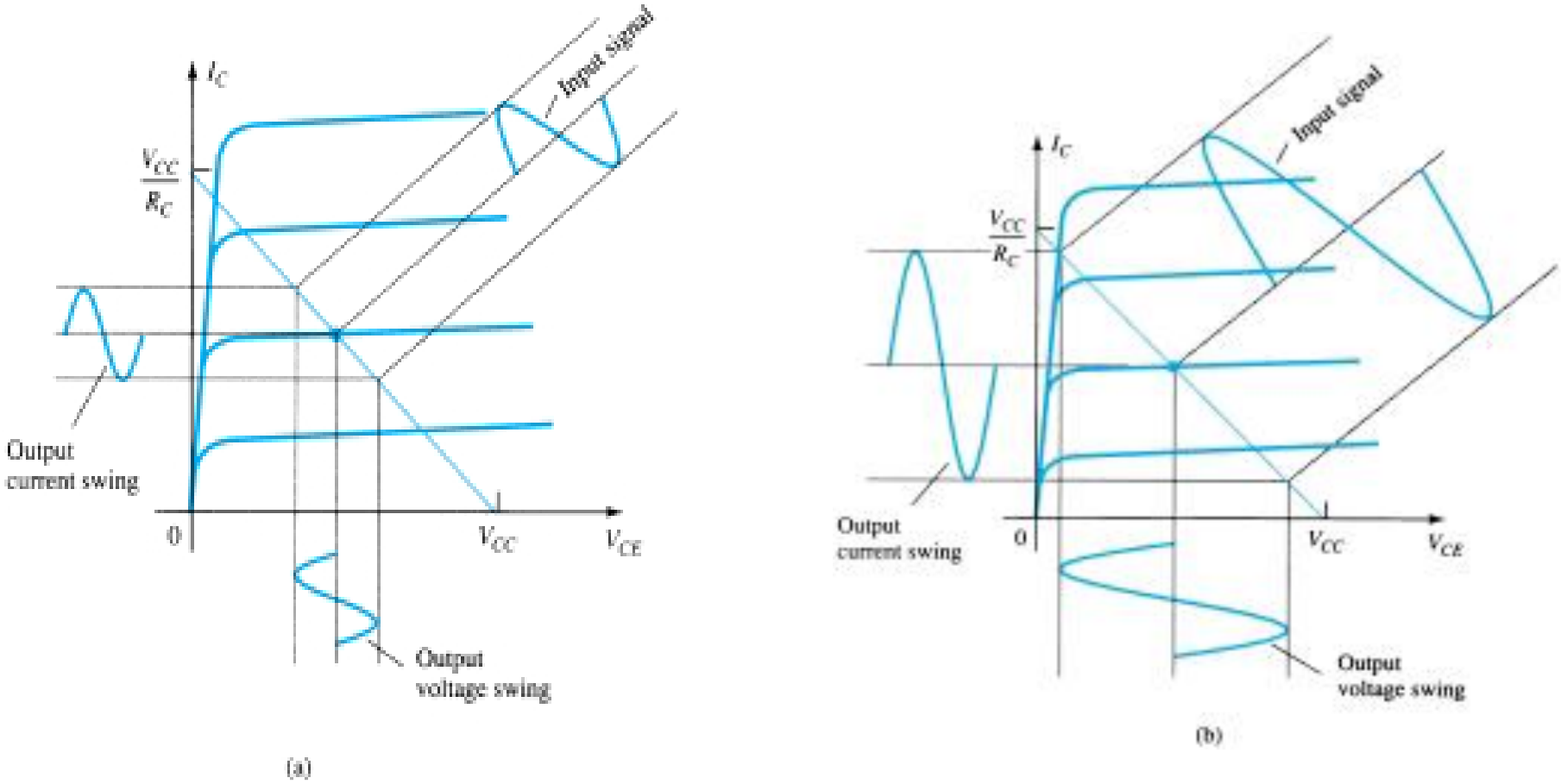


Figure 16.4 Amplifier input and output signal variation

Power Considerations

$$P_i(\text{dc}) = V_{CC}I_{C_Q}$$

OUTPUT POWER

Using rms signals: The ac power delivered to the load (R_C) may be expressed using

$$P_o(\text{ac}) = V_{CE}(\text{rms})I_C(\text{rms})$$

$$P_o(\text{ac}) = I_C^2(\text{rms})R_C$$

$$P_o(\text{ac}) = \frac{V_C^2(\text{rms})}{R_C}$$

Using peak signals: The ac power delivered to the load may be expressed using

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p})I_C(\text{p})}{2}$$

$$P_o(\text{ac}) = \frac{I_C^2(\text{p})}{2R_C}$$

$$P_o(\text{ac}) = \frac{V_{CE}^2(\text{p})}{2R_C}$$

Using peak-to-peak signals: The ac power delivered to the load may be expressed using

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p-p})I_C(\text{p-p})}{8}$$

$$P_o(\text{ac}) = \frac{I_C^2(\text{p-p})}{8}R_C$$

$$P_o(\text{ac}) = \frac{V_{CE}^2(\text{p-p})}{8R_C}$$

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\% \ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

MAXIMUM EFFICIENCY

For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is

$$\text{maximum } V_{CE}(\text{p-p}) = V_{CC}$$

For the current swing it is

$$\text{maximum } I_C(\text{p-p}) = \frac{V_{CC}}{R_C}$$

Using the maximum voltage swing in Eq. (16.7a) yields

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}(V_{CC}/R_C)}{8}$$

$$= \frac{V_{CC}^2}{8R_C}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_C) = V_{CC}\frac{V_{CC}/R_C}{2}$$

$$= \frac{V_{CC}^2}{2R_C}$$

the maximum efficiency:

$$\text{maximum \% } \eta = \frac{\text{maximum } P_o(\text{ac})}{\text{maximum } P_i(\text{dc})} \times 100\%$$

$$= \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100\%$$

$$= 25\%$$

The maximum efficiency of a class A series-fed amplifier is thus seen to be 25%.

16.3 TRANSFORMER-COUPLED CLASS A AMPLIFIER

A form of class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load as shown in Fig. 16.6. This is a simple circuit form to use in presenting a few basic concepts. More practical circuit versions are covered later. Since the circuit uses a transformer to step voltage or current, a review of voltage and current step-up and step-down is presented next.

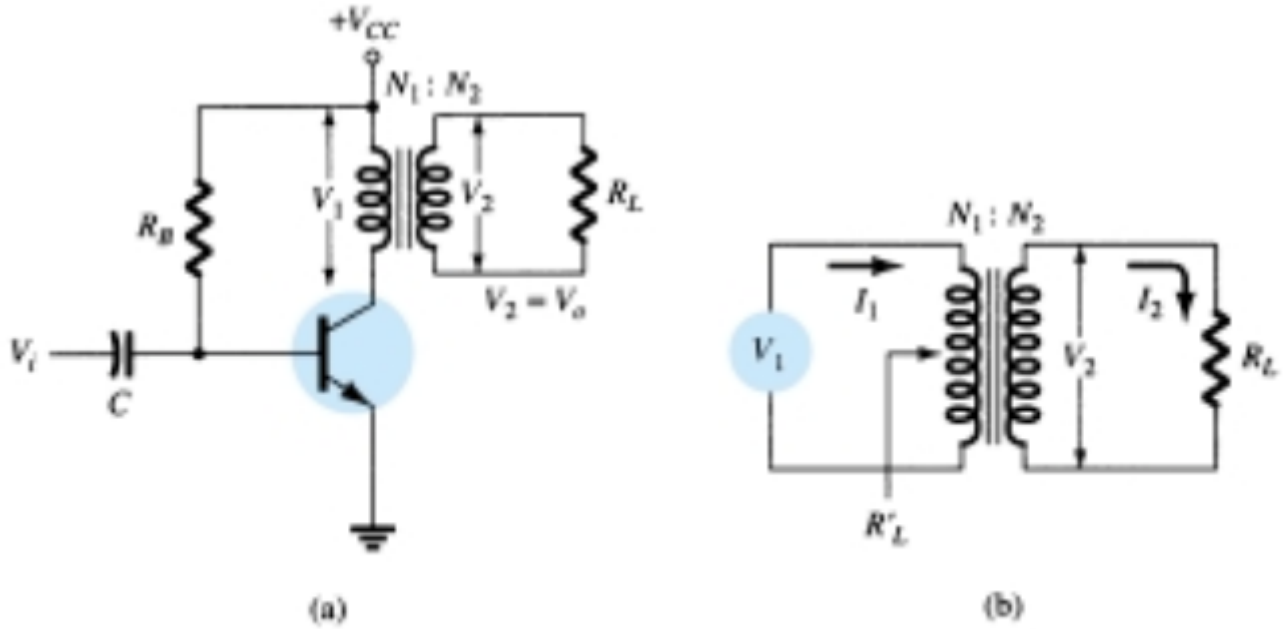
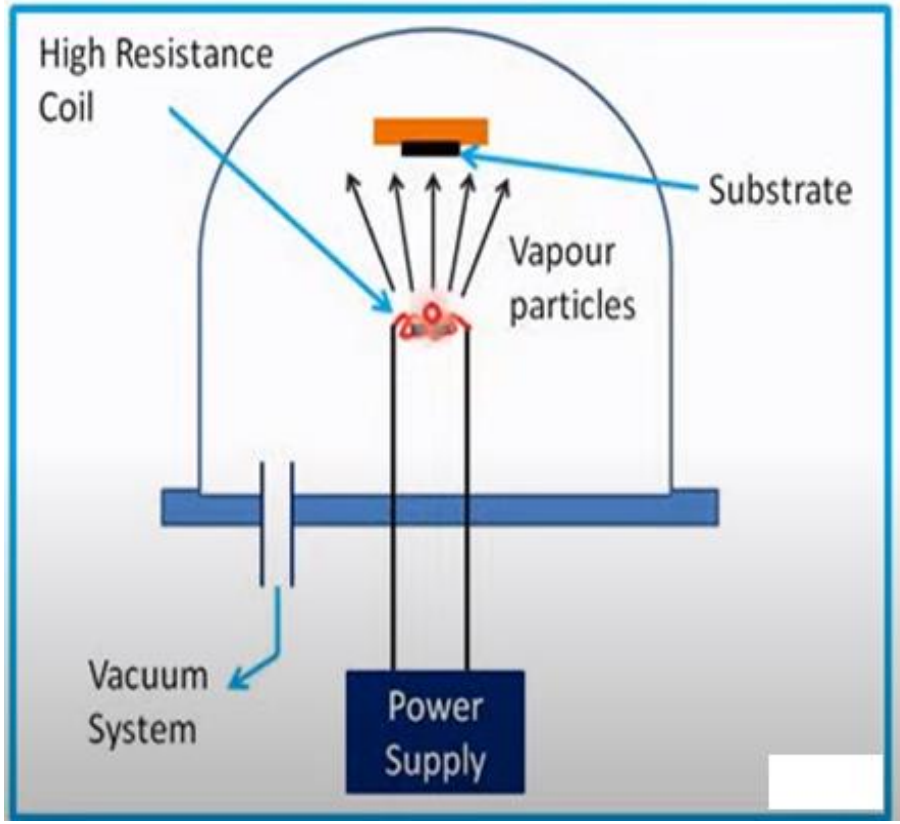


Figure 16.6 Transformer-coupled audio power amplifier.

Physical Vapour Deposition Method (Resistive Method)



- Bottom-up Approach.
- The material is evaporated in a vacuum.
- Vapour particles travel towards the cold target (substrate) Deposited and condense back to a solid state.
- Resistance evaporators

heat is generated to evaporate the material by passing current through a high resistance coil.

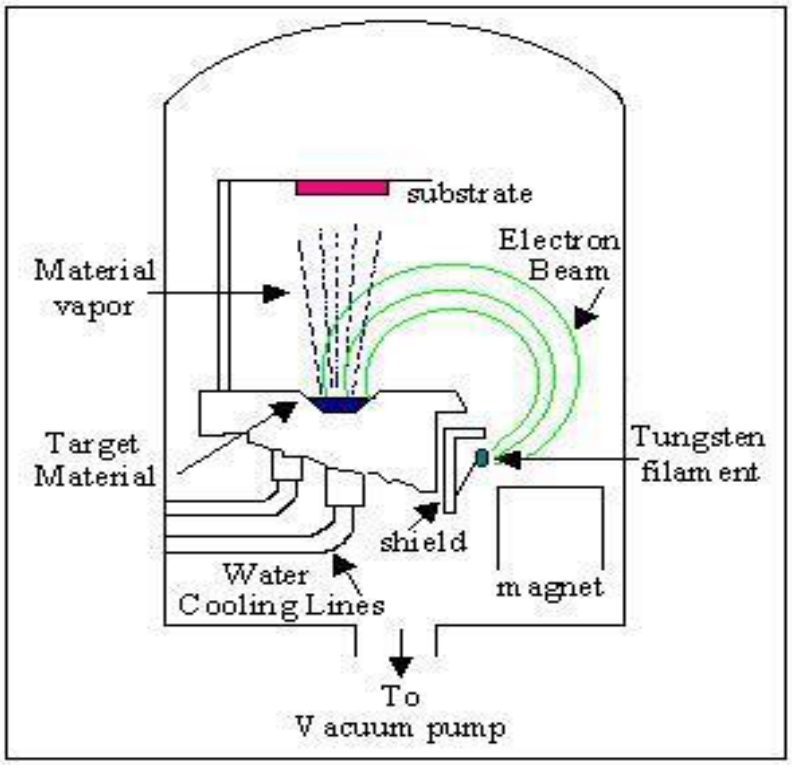
A. Evaporation:

- conventional vacuum evaporation (thermal)
- electron-beam evaporation
- pulsed laser evaporation
- molecular-beam epitaxy
- Others

B. Sputtering:

- DC sputtering
- radio frequency (RF) sputtering
- magnetron sputtering
- reactive sputtering
- Others

Physical Vapour Depositions : electron beam evaporation



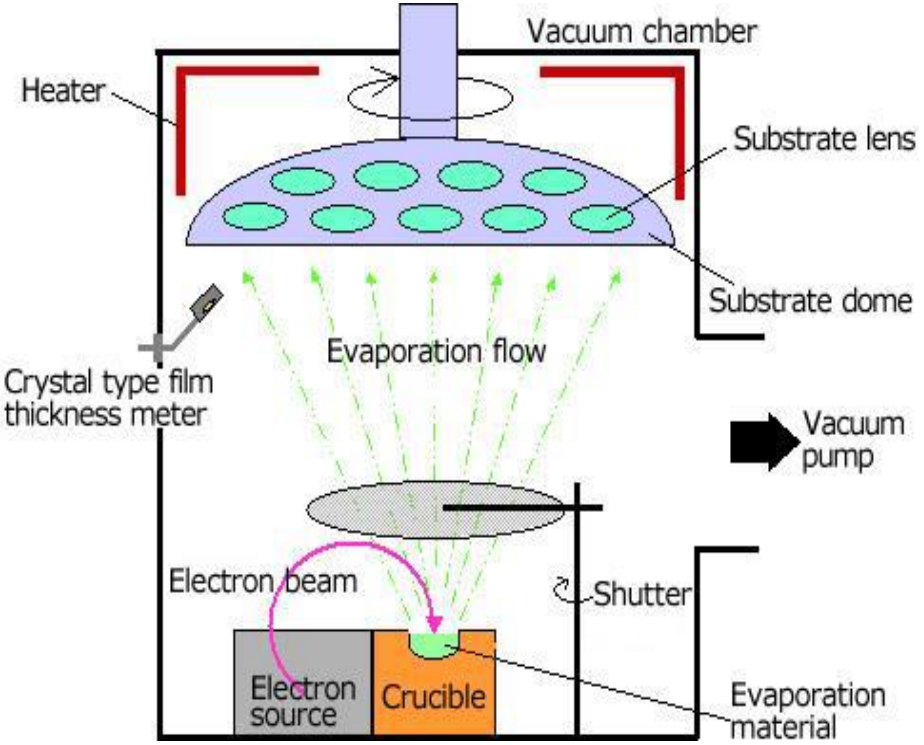


Figure 4: Schematic of electron beam evaporation system.

- ✓ In electron beam evaporation (EBE), a stream of electrons is accelerated through fields of typically 5–10 kV and focused onto the surface of the material for evaporation.
- ✓ The electrons lose their energy very rapidly upon striking the surface and the material melts at the surface and evaporates.
- ✓ That is, the surface is directly heated by impinging electrons, in contrast to conventional heating modes.
- ✓ Direct heating allows the evaporation of materials from water-cooled crucibles.

Patterning Nano-patterning

The 3D microstructures are created with a process called *patterning*.

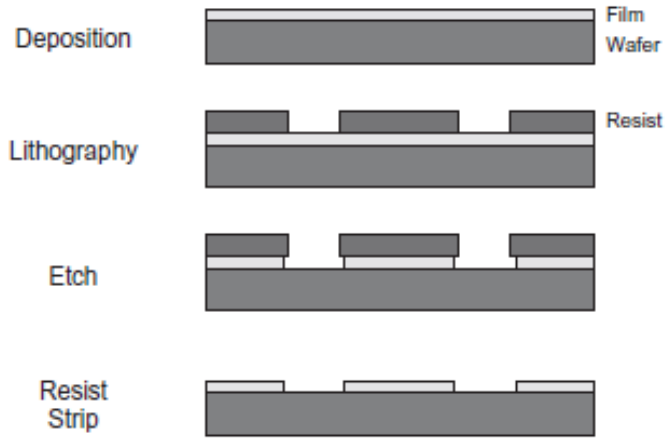


Figure 1.1 *A simple subtractive patterning process*

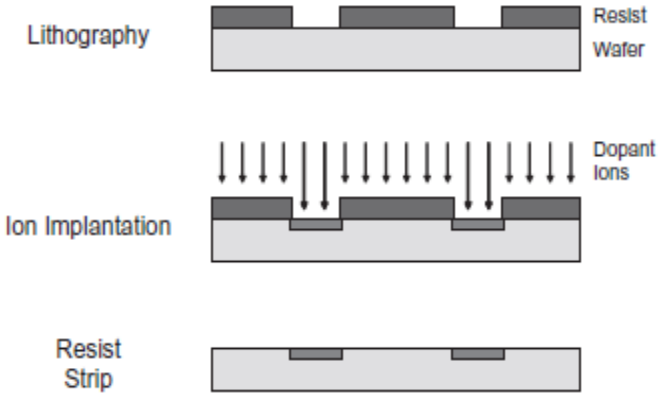
Subtractive patterning :

The common *subtractive* patterning process (Figure 1.1) involves three steps:

(1) deposition of a uniform film of material on the wafer;

(2) lithography to create a positive image of the pattern that is desired in the film; and

(3) etch to transfer that pattern into the wafer.



Patterning as a means of selective doping using ion implantation

Additive process :

An *additive* process (such as electroplating) changes the order of these steps:

(1) lithography to create negative image of the pattern that is desired; and

(2) selective deposition of material into the areas not protected by the lithographically produced pattern.

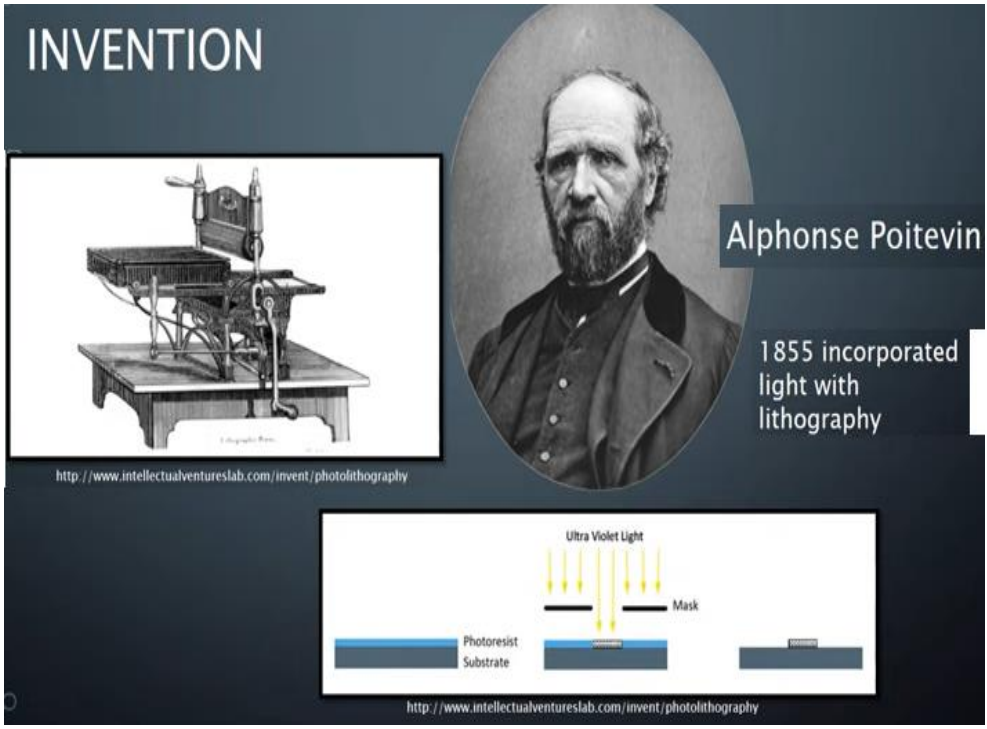
Copper is often patterned additively.

Nano-patterning: Photo-Lithography

- **Photolithography** or **optical lithography (**a subclass of microlithography**)** is a general term used for techniques that use light to produce minutely patterned thin films of suitable materials over a substrate, such as a silicon wafer, to protect selected areas of it during subsequent etching, deposition, or implantation operations.

- Photolithography is the most common method for semiconductor fabrication of integrated circuits ("ICs" or "chips"), such as solid-state memories and microprocessors. It can create extremely small patterns, down to a few tens of nanometers in size.

- It provides precise control of the shape and size of the objects it creates and can create patterns over an entire wafer in a single step, quickly and with relatively low cost.



Nano-patterning: Photo-Lithography

- Typically, ultraviolet light is used to transfer a geometric design from an optical mask to a light-sensitive chemical (photoresist) coated on the substrate.
- The photoresist either breaks down or hardens where it is exposed to light. The patterned film is then created by removing the softer parts of the coating with appropriate solvents.
- Conventional photoresists typically consists of three components: resin, sensitizer, and solvent.
- Photolithography processes can be classified according to the type of light used, such as ultraviolet, deep ultraviolet, extreme ultraviolet, or X-ray.
- The wavelength of light used determines the minimum feature size that can be formed in the photoresist.
- However, photolithography cannot be used to produce masks on surfaces that are not perfectly flat; and, like all chip manufacturing processes, it requires extremely clean operating conditions.

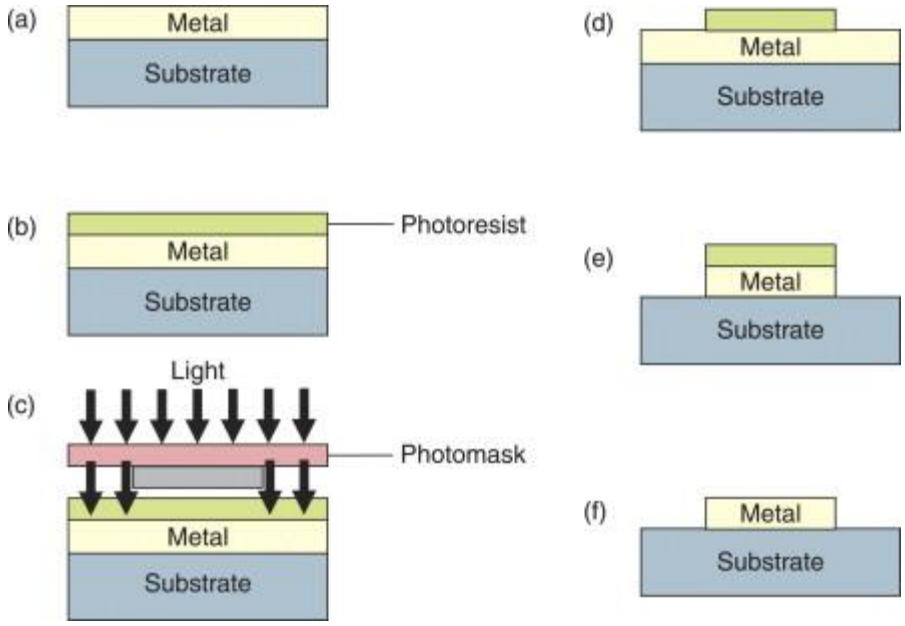
Cleaning Wafer

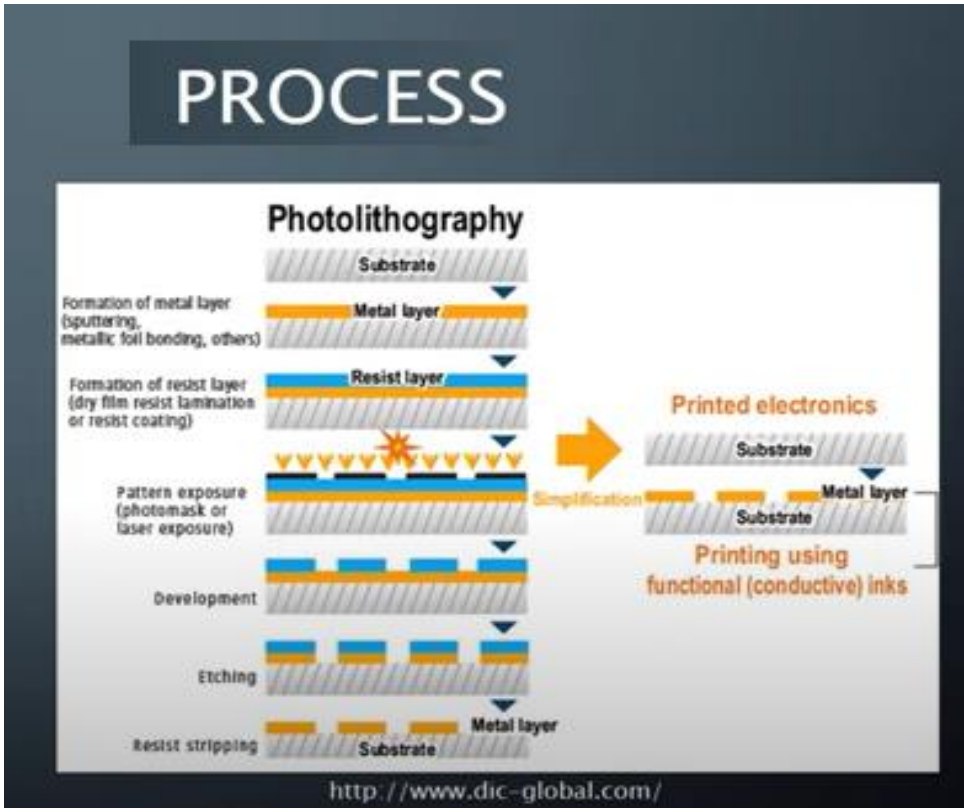
If organic or inorganic contaminations are present on the wafer surface, they are usually removed by wet chemical treatment, e.g. the RCA clean procedure based on solutions containing hydrogen peroxide.

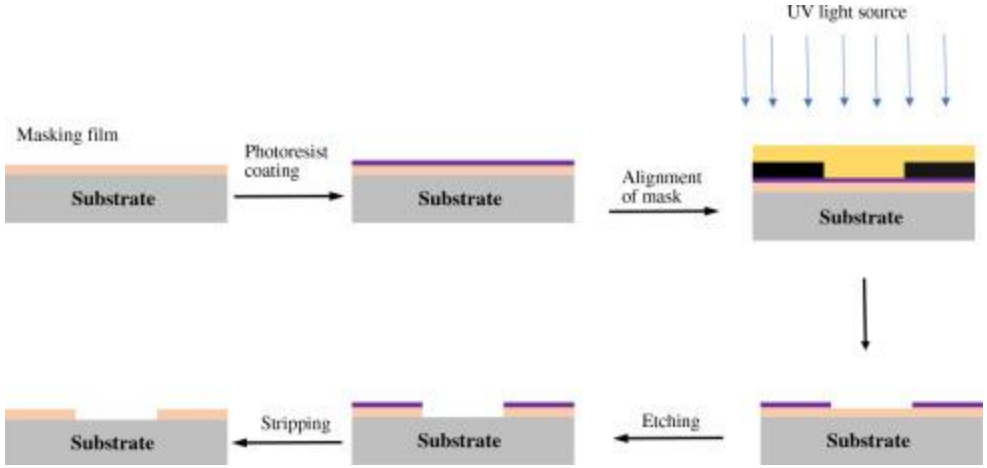
RCA cleaning (Radio Corporation of America) was a cleaning method developed in order to remove both organic and ionic contaminants from wafers.

Other solutions made with trichloroethylene, acetone or methanol can also be used to clean.

Nano-patterning: Photo-Lithography







Please solve Examples and Exercise problems of related topics

Practice yourself and send me your feedback, if any.