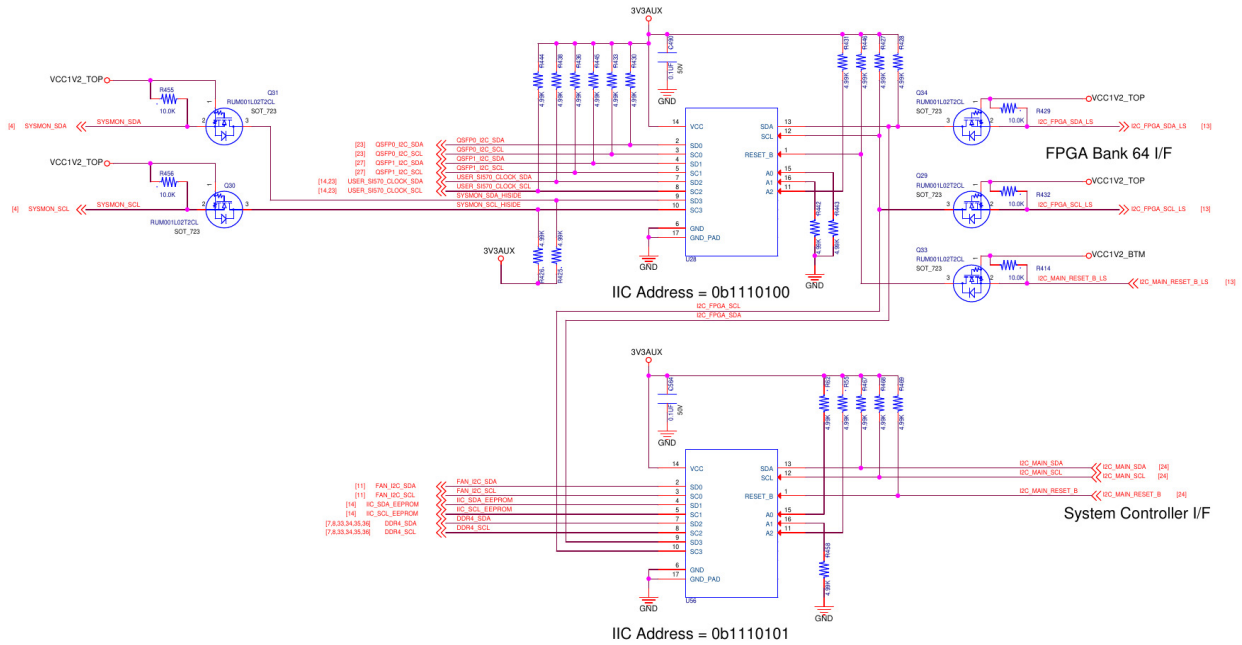
Overview

The BCU1525's peripherals are all connected via I2C. The best way to envision this as there being two main I2C "areas" - one being inside the other. The FPGA has been deliberately isolated from some devices, such that it cannot access them directly. The TI MSP432 microcontroller (or "BMC/Board Management Controller") on the BCU1525 is capable of not only accessing the onboard devices which the FPGA cannot, but additionally may access all of the I2C devices the FPGA can. The only exception to this basic layout is that the VRM controller, the LTC3884, has its PMBus interface on its own seperate I2C bus - different from the "I2C_MAIN*" lines shown below. The overall I2C topology (from the released Xilinx VCU1525 schematics, before they were suddenly pulled, and the user guide for it (UG1268) was suddenly gutted of information with no entry in the revision history of the document) is pictured below, with a link to the full image here.



The FPGA Walled Garden

On the FPGA-accessible TCA9548A I2C switch, or mux (it states that a PCA9546 was used in the old VCU1525 documentation; this is incorrect/outdated, at the very least for the BCU1525 variant), we have the two QSFP28 ports - I believe all of their I2C slave endpoints are connected. One is on switch position #0, the other on switch position #1. There is a user-programmable Si570 oscillator with its I2C, as well as an M24C08 8Kb EEPROM on the #2 switch position, with the #3 switch position populated by the XCVU9P FPGA's own SYSMON I2C lines.

Outside the Walled Garden

As from the FPGA, we cannot access anything outside our "walled garden" directly, we need to communicate with the MSP432 microcontroller (aka "BMC/Board Management Controller") in order to access them. It will communicate on both the "main" I2C bus, as well as the special I2C bus where the LTC3884's PMBus interface resides. To get it to do this, we will have to use an undocumented protocol (which is likely how the proprietary Minerator provides most of the features it does) which will cause it to send/receive I2C/SMBus/PMBus transactions on your behalf. The specifics are detailed on a page dedicated to the MSP432 BMC.

The devices present on the outside of the I2C walled garden include the I2C slave interface of the fan controller, a quite nice LM96063, on switch position #0. There is another M24C08 8Kb EEPROM along with three SE98ATP temperature sensors scattered across the PCB, and a port expander (we will get back to this later when describing the individual peripherals) on switch position #1. All four DDR4 DIMM slots' I2C lines (for SPD - Serial Presence Detect, and additional things, on some DIMMs), are on switch position #2, and the FPGA-accessible TCA9548A I2C switch is on switch position #3.