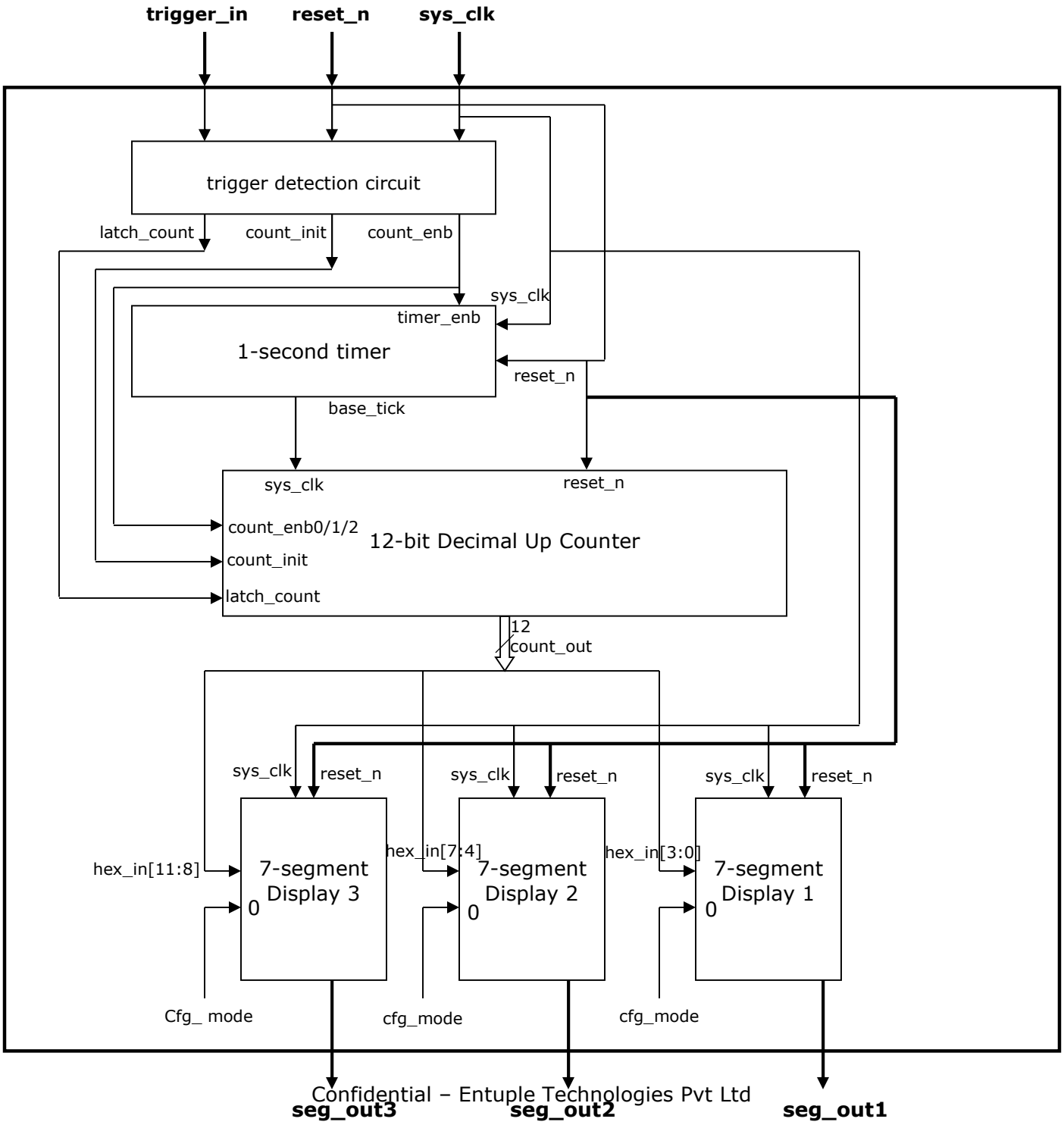
Stopwatch or RTC Design

Design a top module which instantiates 12-bit decimal up counter, trigger detection circuit, hexadecimal to 7-segment display converter and one-second pulse timer circuits and write the testbench and apply the stimulus. Implement the same design on Nexys A7 board.



Module Description:

The block diagram of stopwatch is as shown above. When trigger-in is triggered, stopwatch starts counting. This stopwatch can count from 0 to 999.

Signal Description:

Stopwatch implementation design consists of three external inputs and three external outputs. The external inputs/outputs are :

- sys_clk is the system clock which is operating at 100 MHz frequency. This design uses 100 MHz system clock.
- rst_n is the synchronous active low reset signal. When reset_n is low, the stopwatch system will be reset to 0. This signal is required to reset the internal blocks of the stopwatch design.
- trigger_in is another external input which triggers when start/stop toggle switch is operated by the user.
- Stopwatch starts counting from the time of triggering of start toggle switch till the stop toggle switch is triggered. The current value of the stopwatch is displayed by using 7-segment display which is available on Nexys A7 board.
- Three outputs seg1_out, seg2_out, seg3_out are used to display each digit starting from 000 to 999.

Signal Name	Size	I/O	Description
sys_clk	1	I	System Clock 100 MHz.
reset_n	1	I	Active low system reset. This reset is internally synchronized to the sys_clk.
trigger-in	1	I	trigger_in is the stopwatch trigger input. When this input is high, clock starts counting till the next time this input goes high.
seg1_hex0	1	O	Stopwatch can count from 0 to 999 secs. So output is displayed using three 7-segment display from Nexys A7 board. This signal is LSB which can display from 0 to 9
seg2_hex1	1	O	This signal displays from 0 to 9
seg3_hex2	1	O	This signal is MSB which can display from 0 to 9.

Note: Write the code of the stopwatch by instantiating the modules namely, trigger_det, timer, counter, seg_display. Name the design file as stopwatch_top.vhd, module as stopwatch_top.vhd and the testbench as tb_stopwatch_top.vhd