ANALYSIS OF THE HYBRID MILLER CASCODE COMPENSATION FOR TWO STAGE OPERATIONAL AMPLIFIERS AND ITS COMPARISON WITH CCNSP

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***Abstract*—This paper includes the analysis of Hybrid Miller Cascode Compensation(HMCC) in the two stage Opamps and at last compares it with CCNSP The analysis helps to analyse the settling time and looks to solve the gain peaking at fugb for Open loop transfer function seen in other compensation techniques.**

***Index Terms*—Two stage opamp, settling time, HMCC, CCNSP, CMFB, Pole, Zero**

I. INTRODUCTION

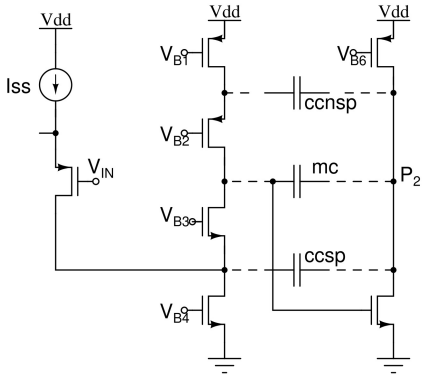

Fig. 1. Capacitor connections for Miller, CCNSP and CCSP compensation

Operational amplifiers are the voltage controlled voltage sources that are vital in circuit design as when used with negative feedback the gain becomes independent of transistor parameters when the open loop gain of opamp is large. Moreover, they are used for calculations like integration, differentiation etc. With the use of negative feedback the bandwidth also increases. but there is a problem with the feedback, the phase lag that results in instability. To take this phase lag under control various techniques are there. The one that will be discussed here is the frequency compensation. There are various compensation techniques Miller compensation, cascode compensation on signal or non signal path, Hybrid cascode compensation etc. The cascode compensations are improvement on the miller compensation as they provide a higher second pole locations and there is no RHP zero. but due to large compensation capacitance there is gain peaking near the fugb which makes the system unstable and because it reduces the gain margin.The Hybrid compensation also comes with the same issue of gain peaking. A new compensaton technique that uses cascode compensation and miller compensation is analysed in this paper. The important thing about these compensations is that where to connect the compensation capacitors. The Miller capacitor is connected to high impedance node and the cascode compensation using non signal path(CCNSP) is connected to low impedance node. This compensation technique works by dividing the capacitor into two paths thereby reducing the gain peaking near fugb. Also this technique shifts the LHP zero generated by CCNSP to higher frequency thereby reducing its effect on the transfer function. This results in fast settling in this compensation technique.

II. OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

OTA's are the part of the opamp circuits that have very high gain, high output impedance which is a drawback of OTA as when a resistive load is applied to it there is a drastic drop in the gain of the OTA. That's why a voltage buffer state is applied to reduce the output resistance. The first stage of the OTA is a differential amplifier because of the excessive use of feedback in the applications. Second stage of a two stage OTA is a high gain state to improve the gain. That's why a Common Source amplifier is used. This amplifier can not be implemented by NMOS transistor with load because due to the presence of a Nmos one of the nmos of differential amplifier

will never be in saturation. To remove such a problem we use a PMOS Current Source.

III. HMCC

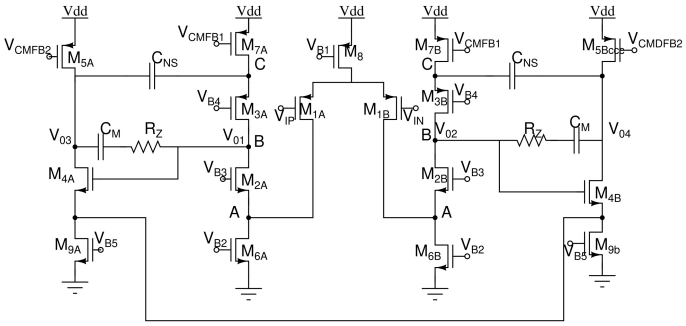

Fig. 2. Circuit Diagram of proposed circuit

The first stage of the two stage OTA is a folded cascode used in the circuit for increased gain and the second stage is a differential pair as it results in large swings in the circuit. WIth this there is one more Common mode feedback circuit used which takes the input from Vcmfb1 and Vcmfb2. and gives us a output that is average of both the voltages. This circuit is used so as to stabilize the input voltages. The proposed circuit requires two CMFb circuits.

A. *Common mode feedback*

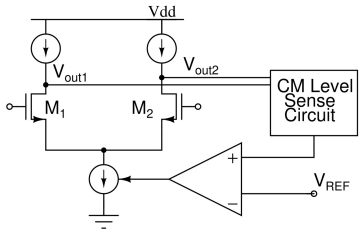

Fig. 3. Common mode feedback

Why we need a Common mode feedback circuit? If the resistive loads of circuit are replaced by PMOS current sources for increasing differential voltage gain of the circuit, then the common mode voltage depends on the closeness of pmos currents to Iss/2. In practical situations these differences result in errors between pmos current and the Iss/2 which forces a change in the node voltages causing transistors to change their region of operation. These high impedance nodes force the node voltage to go to 0V or Vdd. So if CMFb is not used in the circuits then it will result in the failure of opamp.

B. *Folded cascode OPamp*

The folded cascode opamp is used in the proposed circuit. The major benefit of this circuit is the large swing and gain. How to make folded cascode from the differential amplifiers? The basic method is to change the pmos input to nmos or vice versa. The major difference that comes in this circuit is that there is need for extra bias current for the input differential pair. Hence the power consumption of this circuit is larger. One more interesting property is that this circuit can be easily solved using the half circuit analysis. The gain can be easily calculated using the intuition as

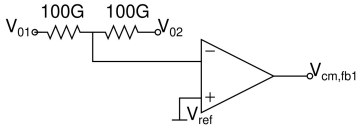

Fig. 4. sensing ckt in Common mode feedback

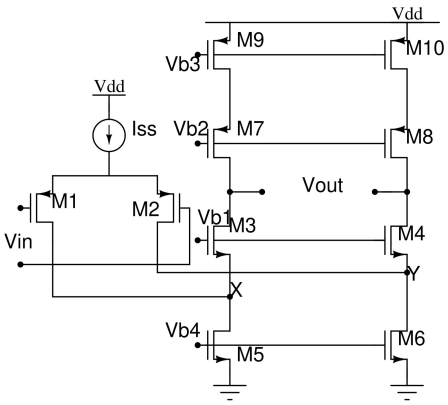

Fig. 5. Folded Cascode opamp

$$|Av| = gm1gm_3ro_3(ro_1||ro_5)||gm_7ro_7ro_9 \quad (1)$$

where

$$G_m = gm_1 \quad (2)$$

and

$$Rout = gm_3ro_3(ro_1||ro_5)||gm_7ro_7ro_9 \quad (3)$$

C. *Three pole one zero system and settling time*

Settling time has a very peculiar relationship with damping factor of the system. It is quite tricky to plot the settling time with respect to damping factor because as damping factor is reduced from 1 the value of settling time falls but as soon as the damping factor is 0.68 there is a sudden increase in the settling time because then the first overshoot touches the tolerance band and Hence the settling time increases. this incresase continues for sometime and then it again jumps to high value of settling time this time because of touching of undershoot to the tolerance band. For practical purposes the value of ζ is taken in between 0.4 to 0.7. [5]

The settling time is based on the poles and zeroes for different type of compensations. It contains two parts, the slew time and after slew time. Slew time is the time taken for transition from original voltage value to the vicinity of new value. This time is non linear in nature. The second time is that time at which the voltage is near final value. The circuit is behaving in quasilinear state. It is observed that for fast

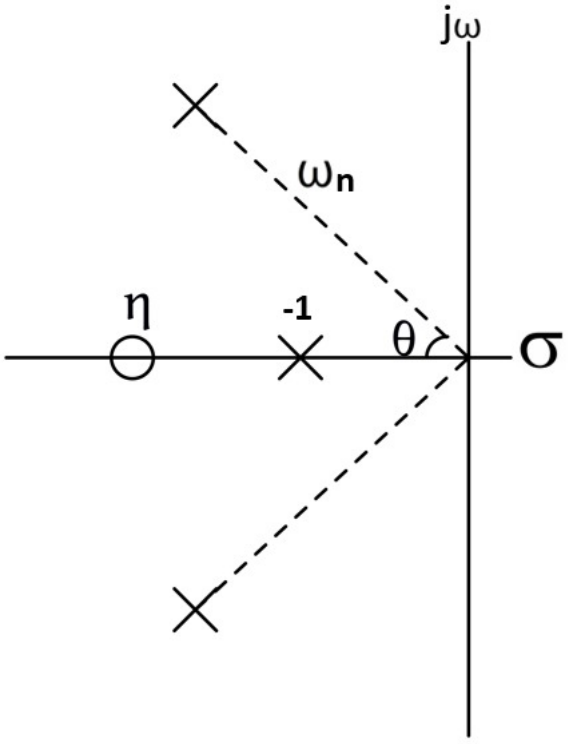

Fig. 6. Three pole one zero system

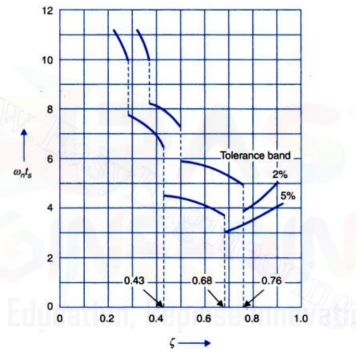

Fig. 7. Normalized settling time with damping factor ref Ij Nagrath M Gopal

opamps slew time is very small but the quasilinear behaviour determines the settling time of the operational amplifier. For analysing the system normalisation concept is used. What can be the normalizing quantity? The dominant pole is taken as the normalising quantity implying that the normalized dominant pole becomes -1 rad/s. This method of normalisation is based on the scaling of the Laplace Transform. The scaling has no effect on the relative settling time as the angle of complex poles remains unvaried. The natural frequency after normalisation is given by

$$w_n = \frac{|P2|}{P1} \tag{4}$$

where P1 is the dominant pole. The zero is given by :

$$n = \frac{Z}{P1}$$

Doublet formation can take place if a side of active load at higher frequency is bypassed or by using a feedforward capacitor. Why Doublet formation is important? This is because the After slew time period is largely dependent on Pole and Zeroes of the Transfer function.

$$doubletspacing = \frac{1}{settlingtime} \tag{5}$$

D. Mathematical analysis of circuit

The impedances and capacitances at different nodes can be calculated in a simple way just by using intuitive understanding. The circuit can be divided into half circuit for analysis because of its symmetry.

1) Finding Resistance: As observed from point 'A' three resistances can be seen parallel to one another. Resistance of M6a, cascode of M2a,M3a,M7a and the third is the thevenin equivalent observed for M1a.

$$R_{M6a} = r_{o6};$$

$$\text{Cascode resistance is } \frac{gm3ro3ro7}{1+gm2ro2}$$

$$\text{Thevenivn resistance } R = r_{o1}$$

This is because the Vip =0 and the tail current source is also at ac ground for differential mode operation. Hence,

$$Ra = r_{o1}||r_{o6}||\frac{gm_3r_{o3}r_{o7}}{1+gm_2r_{o2}} \tag{6}$$

Resistance at point B The resistance here can be calculated very easily as from point b one part is the cascode resistance of M2a is in cascode with parallel of resistance of M6a and M1a and the second part is the cascode of two Pmos. The resistance calculated here is approximate. Otherwise the actual value is

$$[ro2+(ro1||ro6)+gm2ro2(ro1||ro6)]||[ro3+ro7+gm3ro3ro7] \tag{7}$$

but ro3 is small hence neglected.

$$Rb = gm_2r_{o2}(r_{o1}||r_{o6})||gm_3r_{o3}r_{o7} \tag{8}$$

Resistance at point C Resistance at point C is calculated as ro7 will be parallel to the other impedances which is equal to $\frac{ro3+gm2ro2(ro1||ro6)}{1+gm3ro3}$

$$Rc = r_{o7}||\frac{gm_2r_{o2}(r_{o1}||r_{o6})}{1+gm_3r_{o3}} \tag{9}$$

2) Calculating capacitances: Finding Capacitance at A

$$C_a = C_{db1} + C_{gs2} + C_{sb2} + C_{db6} \tag{10}$$

If we assume that bulk and source are short then Cdb becomes Cds. Finding Capacitance at B

$$C_b = C_{db2} + C_{db3} + C_{gs4} + C_{gd2} + C_{gd3} \tag{11}$$

Similarly for this also assume drain and bulk are shorted.

$$C_b = C_{ds2} + C_{ds3} + C_{gs4} + C_{gs2} + C_{gs3} \tag{12}$$

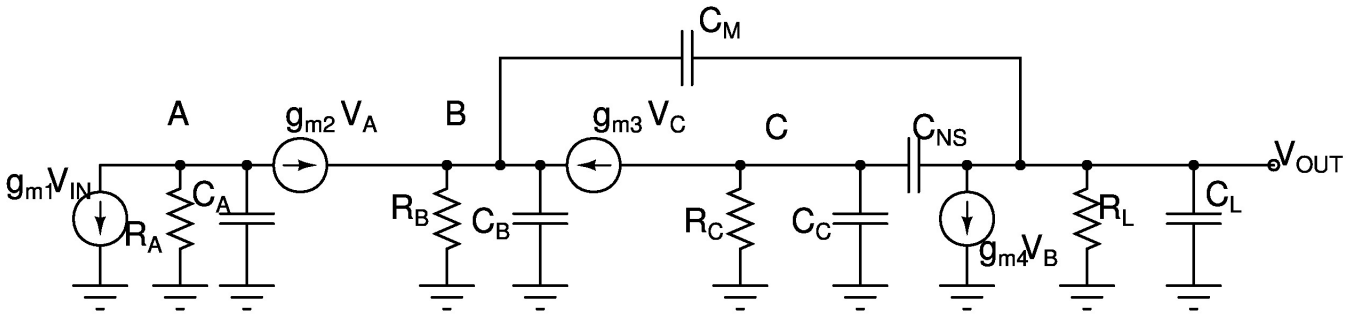

Fig. 8. Small signal model of proposed system

At C taking g and b connected Csb3 =0

$$C_c = C_{gs3} + C_{sb3} + C_{gd7} + c_{db7} \tag{13}$$

or

$$C_c = C_{gs3} + C_{gs7} + C_{gs5} \tag{14}$$

3) Transfer function calculation: Now making the small signal model of the circuit using the parameters that are derived above. Considering node A and Applying Kcl

$$gm_1 V_i n + \frac{V_a}{R_a} + sC_a V_a + gm_2 V_a = 0 \tag{15}$$

Considering node b and applying KCl

$$\frac{V_b}{R_b} + sC_b V_b - gm_2 V_a - gm_3 V_c + sC_m(V_b - V_{out}) \tag{16}$$

Applying Kcl at node C

$$\frac{V_c}{R_c} + sC_c V_c + gm_3 V_c + sC_{ns}(V_c - V_{out}) = 0 \tag{17}$$

Kcl at output node

$$gm_4 V_b + sC_{ns}(V_{out} - V_c) + \frac{V_{out}}{R_l} + sC_l V_{out} + sC_m(V_{out} - V_b) = 0 \tag{18}$$

here the Cns, Cm used are cascode, miller capacitance respectively.

Solving (15),(16),(17) and (18) simultaneously, we get

$$A_{vs} = \frac{K(gm_4 - sC_m)(1 + gm_3 R_c + s(C_m + C_{ns})R_c)}{(1 + gm_2 R_a + sC_a R_a)(s^3 A + S^2 b + sC + D)} \tag{19}$$

where

$$K = gm_1 gm_2 R_a R_b R_l,$$

$$A = R_b R_c R_l (C_{ns} C_b C_c + C_{ns} C_b C_l + C_b C_c C_l + C_{ns} C_b C_m + C_{ns} C_c C_m + C_b C_c C_m + C_{ns} C_l C_m + C_c C_l C_m),$$

$$b = R_b R_c R_l (gm_3 (C_{ns} C_b + C_b C_l + C_b C_m + C_l C_m) + gm_4 C_m (C_{ns} + C_c)),$$

$$C = gm_3 gm_4 R_b R_c R_l (C_{ns} + C_m),$$

$$D = gm_3 R_c,$$

These are the approximated values of A,b,C,D considering transconductances large compared to $\frac{1}{Ra}$, $\frac{1}{Rb}$, $\frac{1}{Rc}$.

4) Zero calculations: A zero gives us the point where the transfer function becomes 0. From the Avs equation equate it to zero $\implies$

$$Avs = \frac{K(gm4 - sCm)(1 + gm3Rc + s(Cm + Cns)Rc)}{(1 + gm2Ra + sCaRa)(s^3 A + S^2 b + sC + D)} = 0 \tag{20}$$

$\implies$ gm4-sCm = 0 or 1+gm3Rc+s(Cm+Cns)Rc =0 From above equations s = $\frac{gm4}{Cm}$ and s= $\frac{-gm3}{Cns+Cc}$ These two zeroes are created. To remove the right half zero the design involves use of Rz or we can use a blocking feedforward path. All this is done to improve stability of system or we can say that the range of values of K for which the system is stable are increased.

5) Pole Calculations: Pole calculations are intuitive. we know that the w=$\frac{1}{RC}$ will give us a pole. Also we can calculate the pole by putting the denominator of (15) equal to zero. i.e.

$$1 + gm2Ra + sCaRa = 0 \tag{21}$$

assuming gm2Ra >> 1

Pole at node A = $\frac{-gm2}{Ca}$ (approx) This is a high frequency pole. For finding other poles

$$s^3 A + s^2 b + sC + D = 0 \tag{22}$$

Using the concepts of polynomial the poles can be given by

$$P1 = \frac{D}{C}(approx) = \frac{-1}{gm_4 R_b R_l (C_{ns} + C_m)} \tag{23}$$

This is the dominant pole and the other two poles will be complex conjugate poles given by s^2A + sb + C = 0 Using Sri dharacharya method of solving quadratic equation

$$P2 = \frac{-b + sqrt(b^2 - 4AC)}{2A} \tag{24}$$

$$Re(P2) = \frac{((-gm_3 Cnum^2 - gm_4 C_m(C_{ns} + C_c))}{2C_{den}^3} \tag{25}$$

Imaginary part is given by

$$0.5j\sqrt{\frac{4gm_3 gm_4 (C_{ns} + C_m)}{C_{denH}^3} - \frac{gm_3 C_{numH} + gm4 C_m (C_{ns} + C_c)^2}{C_{denH}^6}} \tag{26}$$

Similarly we can have P3.

$$C^2_{num} = C_{ns}C_b + C_bC_l + C_bC_m + C_lC_m$$

and

$C^3_{den} = C_{ns}C_bC_c + C_{ns}C_bC_l + C_bC_cC_l + C_{ns}C_bC_m + C_{ns}C_cC_m + C_bC_cC_m + C_{ns}C_lC_m + C_cC_lC_m$

6) Calculating wn and θHmcc:

$$wn = |P2|or|P3| \tag{27}$$

$$wn = sqrt(RE^2 + Im^2) \tag{28}$$

or

$$w_n = sqrt[\frac{gm_3gm_4(C_{ns} + C_m)}{C^3_{den,Hmcc}}] \tag{29}$$

similarly we can calculate the θ of the HMCC system by taking the arctan of $\frac{Im}{Re}$

$$\theta_{HMCC} = tan^{-1}\sqrt{\frac{4gm_3gm_4C^3_{denH}(C_{ns} + C_m)}{(gm_3C^2_{numH} + gm_4C_m(C_{ns} + C_c))^2} - 1} \tag{30}$$

To compare first we will make the compensation capacitances as equal and look at the poes and zeroes.

IV. Comparison of HMCC with CCNSP

TABLE I
COMPARISON OF HMCC AND CCNSP PERFORMANCE PARAMETERS

[1]

S.No	Compensation capacitance = 1.4pF		
	Parameters	***HMCC***	***CCNSP***
1	DC LOOP GAIN(db)	68	68
2	Slew rate	142.8V/μ s	142.8V/μ s
3	Settling Time	12.1ns	16ns
4	PM	55.4^o	89.2^o
5	GM	12.1db	13.4db

As there are two components of the settling time i.e. the slew time and after slew time. When a high step input is applied the slew time component is only dependent on the tail current source and compensation capacitance. It does not depend on the compensation scheme.

$$\text{SR} = \frac{I}{Cc}$$

For Comparing if the compensation capacitances are same then the first pole the dominant one will be same and the settling time depends on the complex conjugate poles and zeroes or doublets.

In HMCC there is a miller capacitance added in the CCNSP hence wn will be changed but the impact will not be large.

$$w_{n,HMCC} = \sqrt{\frac{gm_3gm_4(C_{ns} + C_m)}{(C^3_{denH})}} \tag{31}$$

and, [1]

$$w_{n,CCNSP} = \sqrt{\frac{gm_3gm_4C_{ns}}{C_b(C^2_{denC})}} \tag{32}$$

Comparing these two we get that as the denominator of wn of CCNSP is small the wn of CCNSP is greater than that of HMCC. The numerator value are very little different and that's why the numerators are taken to be the same. The denominator difference is there because of which there is a difference in the wn value but the effect is not very large. But what about the angle of conjugate poles?

$$\theta_{HMCC} = tan^{-1}\sqrt{\frac{4gm_3gm_4C^3_{denH}(C_{ns} + C_m)}{(gm_3C^2_{numH} + gm_4C_m(C_{ns} + C_c))^2} - 1} \tag{33}$$

$$\theta_{CCNSP} = tan^-1[\sqrt{-1 + \frac{4gm_4C_{ns}C^2_{denC}}{gm_3(C_{ns} + C_l)^2C_b}}] \tag{34}$$

[1] As θ Hmcc is lower than θ Ccnsp because of gm4, this is the reason for gain peaking near fugb in case of CCNSP. AS θ is greater than 70^o and ζ =0.7 there are increased oscillations during the settling time which increase the settling time of the circuit in CCNSP. Hence the settling time for HMCC is better than that of CCNSP.

Due to the presence of a Left half zero near fugb in case of CCNSP its phase margin gets improved but this results in very poor settling time. but in case of HMCC the compensation capacitance is divided into two paths which results in the shifting of left half zero to higher frequency that causes the low settling time that we are looking for.

V. Conclusion

The paper gave a deep analysis of HMCC which is a combination of both Miller and CCNSP Compensations. It works to solve the gain peaking problem near fugb by breaking the Compensation capacitances into paths. HMCC also moves LHP zero to high frequency value resulting in faster settling. The phase margin is also improved because of the LHP zero. It shows that the proposed compensation scheme is better than the previous schemes like CCNSP.

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