EE663: Frequency Synthesizers, Clock and Data Recovery Circuits

Course Project

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Objective: Design a phase-locked loop (PLL) that meets the given criteria, including all sub-blocks (phase frequency detector, voltage-controlled oscillator, loop filters, and divider) using Verilog models and transistor level in Cadence design suit.

1 Introduction to the PLL

A Phase locked loop is a circuit designed with the negative feedback to synchronize frequency and phase of a reference system to the given system.

2 Calculations for the given specifications

Given:

$C_{total} < 25pF$
Power dissipated <15mW
$I_{cp} < 100\mu A$
Reference Frequency = 1.5×10^8Hz
Output Frequency = 2.4×10^9Hz
Divider(N) = Divide by 16

$$b = 2[tan^2\phi_m + tan\phi_m sec\phi_m] \tag{1}$$

Assuming phase margin $\phi_m = 65^o$
b = 19.345

$$w_{p3} = w_z(1+b) \tag{2}$$

$$w_{uloop} = \sqrt{b+1}w_z \tag{3}$$

Finding the value of K_{VCO} from the simulations, we get,
$K_{VCO} = 7.23GHz/V$
From the Gardner's constraint

$$w_{uloop} = \frac{w_{ref}}{20} \tag{4}$$

This can be simply converted into the frequency as:

$$f_{uloop} = \frac{f_{ref}}{20} \tag{5}$$

So, $f_{uloop} = 7.5 \times 10^6$Hz
Similarly, for f_z

$$f_{uloop} = \sqrt{b+1}f_z \tag{6}$$

Here the f_z comes out to be 1.66×10^6Hz

$$f_{p3} = (b+1)f_z \tag{7}$$

or $f_{p3} = 33.77MHz$

$$\frac{K_{VCO}I_o}{N} = \frac{(b+1)^{\frac{3}{2}}}{b}C_1{w_z}^2 \tag{8}$$

Putting the values of K_{VCO}, N, b, w_z we get,

$$7.76 \times 10^{-7}I_o = C_1 \tag{9}$$

assuming the current to be around 25μ A we get C_1 = 19.4pF and from b $=\frac{C_1}{C_2}$ we get C_2 =1.001pF.

Now the resistance value is given by $\frac{1}{2\pi f_z C_1}$ = 4.94KΩ

3 Blocks of the PLL

3.1 Voltage Controlled Oscillator

Voltage controlled oscillator is required to generate a frequency which PLL needs to clean. The frequency is given by:

$$f = f_c + K_{VCO}V_c \tag{10}$$

The f_c is observed to be 789MHz. The calculated value of the K_{VCO} comes around to be 7.2GHz.

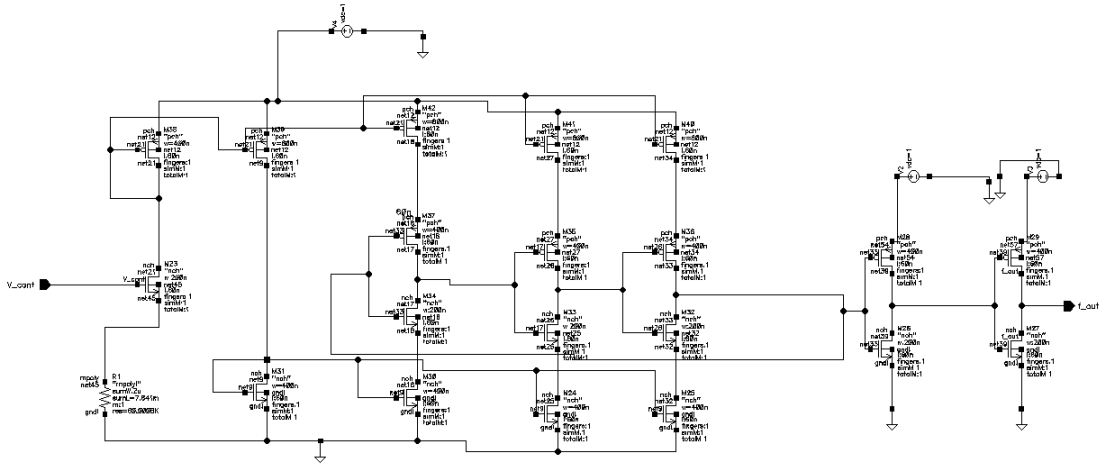

Figure 1: Voltage controlled Oscillator

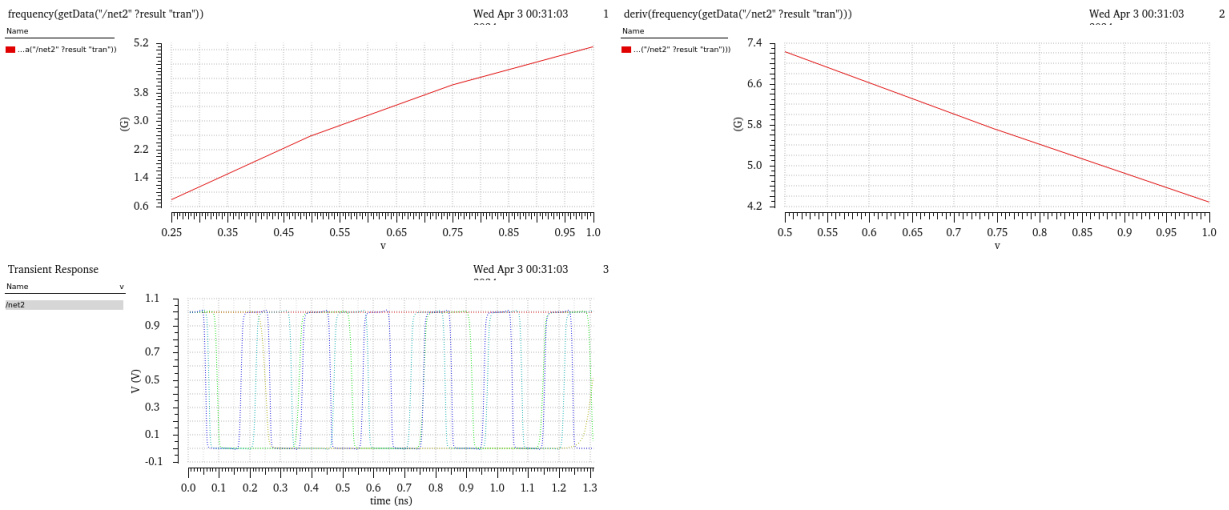

Figure 2: (a)Output Frequency of the VCO vs control voltage(b)Derivative of freq vs control volatge (c) VCO outputs

3.2 Designing Phase and Frequency Detector circuit

PFD circuit is implemented using two DFF with reset pins and as these pins are active low we can say a nand gate is required to reset these pins when Q_a and Q_b is 1. The PFD compares the phases of reference and feedback signals.

The output of the pfd is shown combined with the Charge pump and Loop filter output figure 8.

It shows that when a pulse and a delayed pulse is given in the Data and clk input of the PFD

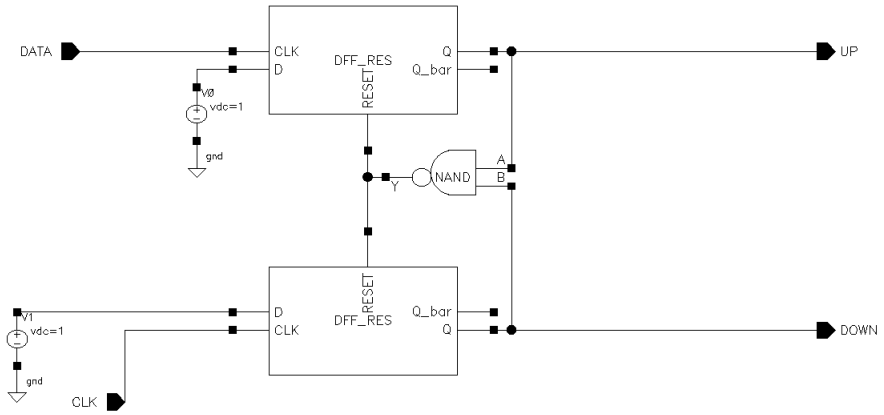

Figure 3: Circuit diagram of the PFD

3.2.1 D-filp flop with reset pin

D-flip flop is implemented using the master slave configuration. It acts as a negative edge triggered flip flop. The two types of nand used are 2 input and 3 input nand gates.

When reset pin is 0 the D-flip flop acts as a proper divider circuit and when reset pin is 1 the output gives spikes only.

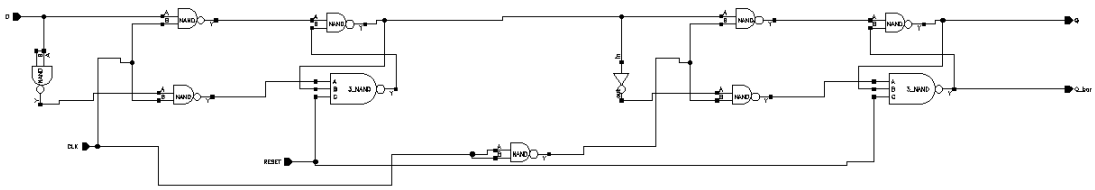

Figure 4: Dff circuit with Reset pin

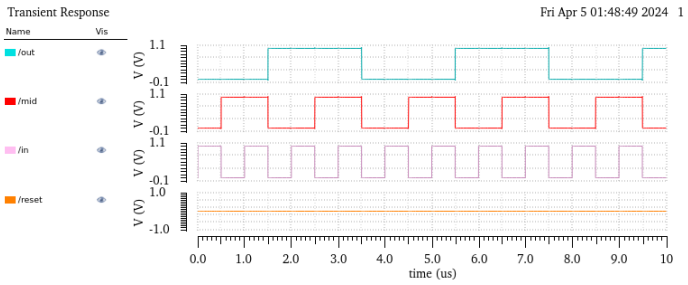

Figure 5: Output when reset pin 0

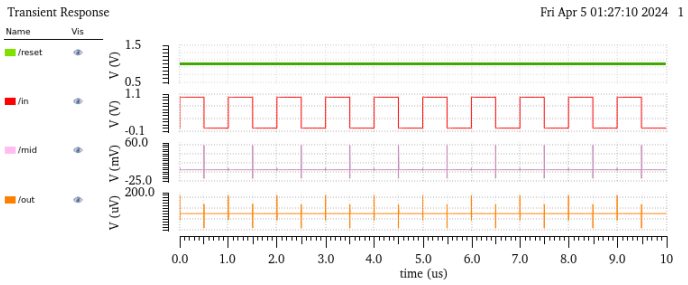

Figure 6: Output when reset pin 1

3.3 Designing Charge Pump and Loop Filter

Charge pump and loop filter are implemented together in the circuit with two current sources two inverters and a buffer. The loop filter comprises of a resistor and two capacitors. The two current sources charge and discharge the capacitors as per the requirement. The output of charge pump,PFD and the Loop filter is shown in the diagram. The output shows that the capacitor charges when Q_a is 1 and Q_b is 0 and vice versa.

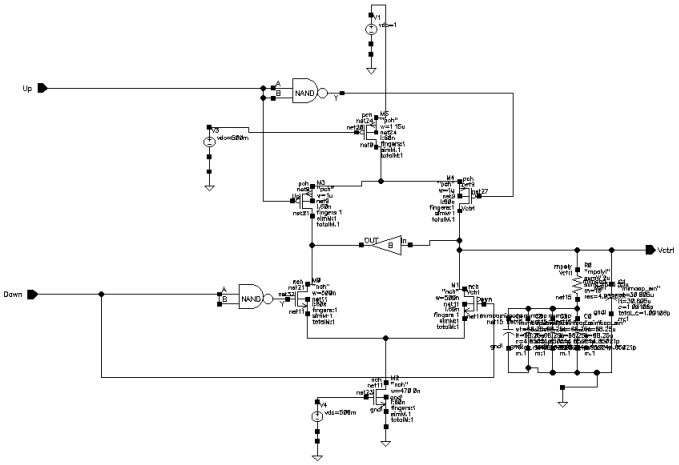

Figure 7: Charge pump and loop filter circuit diagram

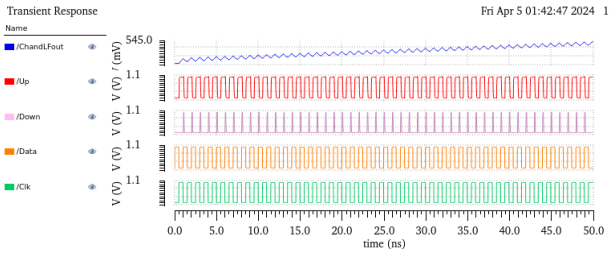

Figure 8: Output characteristics of the charge pump and Loop filter circuit combined with the phase and frequency detector circuit

3.3.1 Buffer

Buffer circuit is implemented using a differential amplifier with active load and the negative input terminal is shorted with the output to make it work like a buffer. On applying 500mV to the input of this circuit output of 504mV was observed.

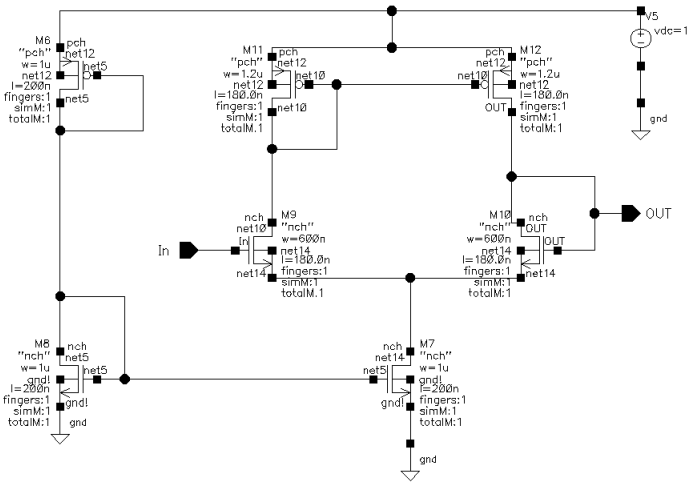

Figure 9: Buffer implementation using 5T OTA

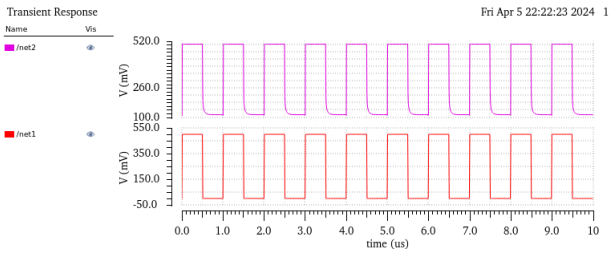

Figure 10: Output of the buffer

3.4 Designing Divide by 16 Divider

Divide by 16 is implemented using 4 D flip flops in the toggle mode. One D flip flop works as a divide by 2 circuit and when 4 are there in cascade, a divide by 16 circuit is implemented. On applying a frequency of 1MHz, an output frequency of 62.5KHz was observed.

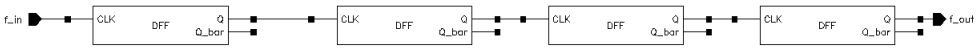

Figure 11: Divide by 16 implementation using edge triggered D flip flops

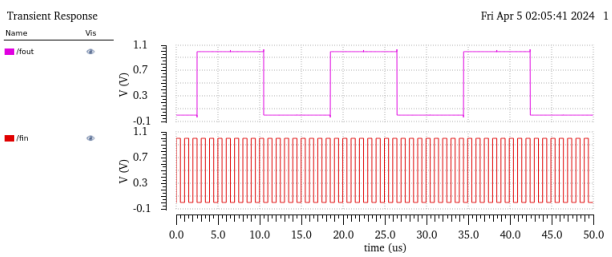

Figure 12: Output and input plot on dividing by 16

3.5 D flip flop implementation

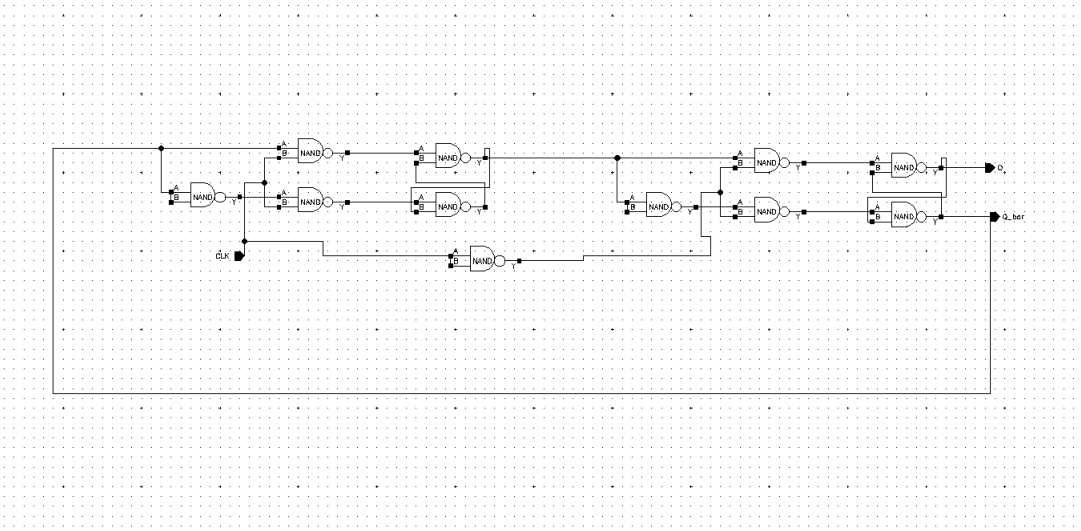

Figure 13: Master Slave D-flip flop

Again a D flip flop is implemented in the master slave configuration which is working as a negative edge triggered circuit. Here reset pin is not used as it is not required so only two input nand are used.

3.5.1 2-input Nand implementation

A nand circuit is implemented using the CMOS implementation technique which consists of two nmos in the series and two pmos in the parallel configuration.

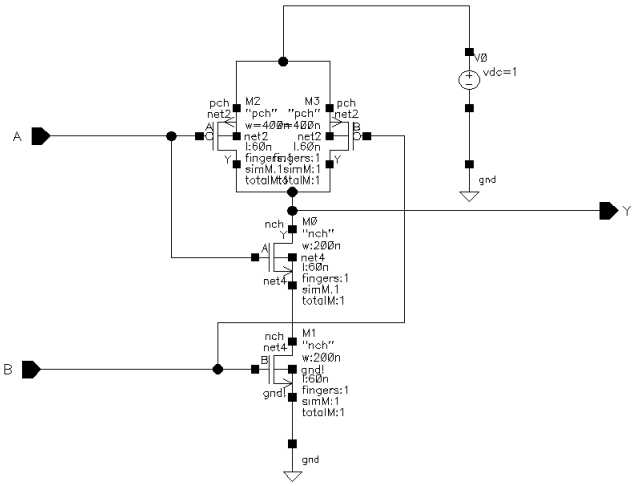

Figure 14: CMOS implementation of Nand gate

3.5.2 3-input Nand implementation

A nand circuit is implemented using the CMOS implementation technique which consists of three nmos in the series and three pmos in the parallel configuration.

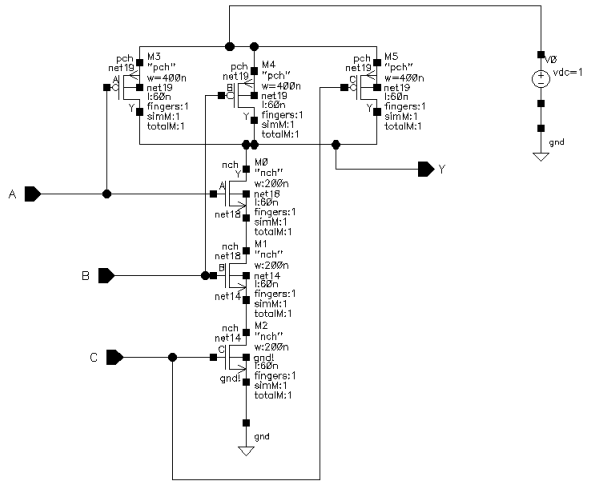

Figure 15: CMOS implementation of Nand gate

3.5.3 Inverter implementation

An inverter circuit is implemented using the CMOS implementation technique which consists of one nmos and pmos. They are cascoded to improve the input output response.

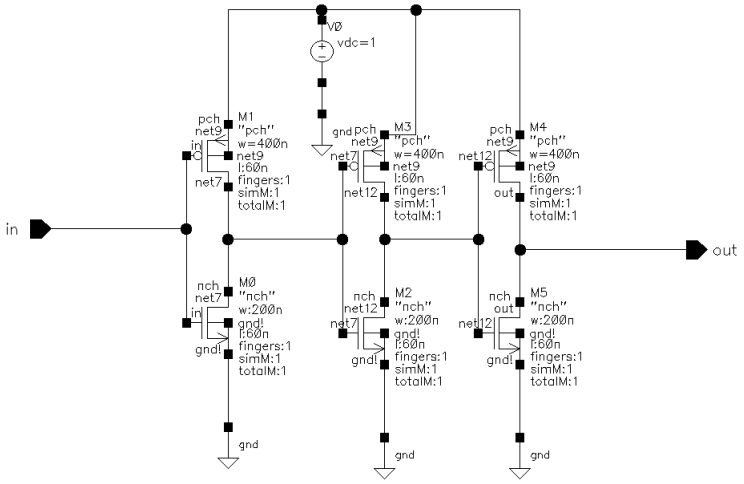

Figure 16: CMOS implementation of Not gate

4 Full PLL Implementation

When all the blocks that are created above are combined together in the shown form, a PLL is formed. It is required to check the regions of the current sources using the DC operating points as the current sources may become resistors when mos goes to the linear region.

The output wave forms are shown. The frequency vs time plot shows how frequency varies with the time when the PLL is trying to lock and as it gets locked the frequency becomes constant. In this case the locked frequency is 2.399GHz

Control voltage vs time also shows how the control voltage of the oscillator varies when the PLL is trying to lock and the constant value of 469mV shows that the PLL is locked.

Up and Down of the PFD shows how the values of phase are changing with respect to time and the phase difference becomes constant when PLL is locked. The last two plots shows the input

and output variations with respect to time. The input pulse frequency is 150MHz and the output frequency is 2.399GHZ

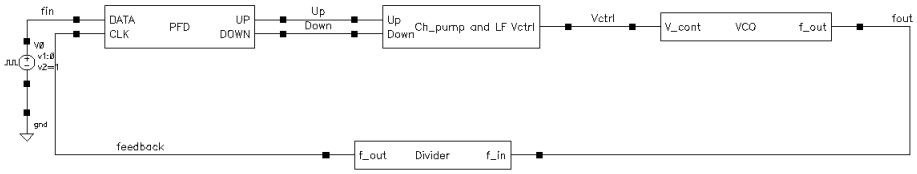

Figure 17: Full block diagram of the Phase locked loop

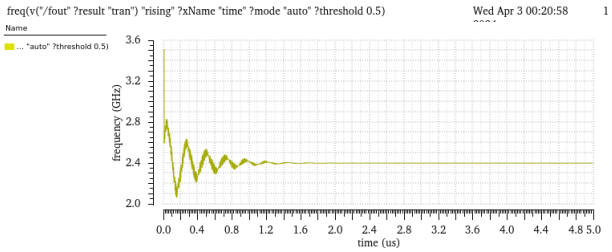

Figure 18: Frequency vs time plot

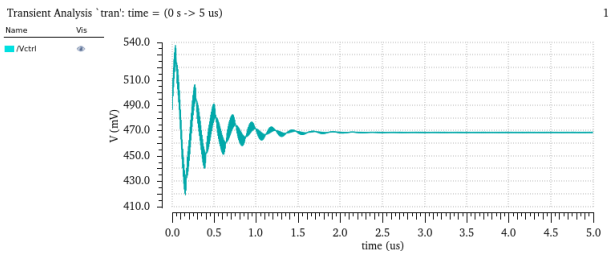

Figure 19: Control volatge vs time

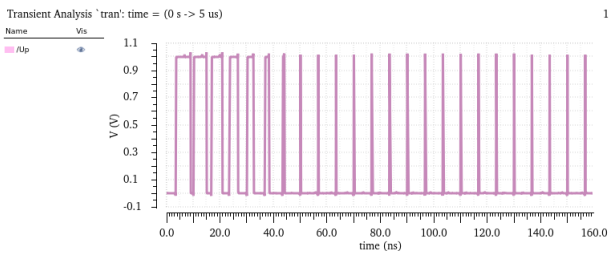

Figure 20: Up of the PFD

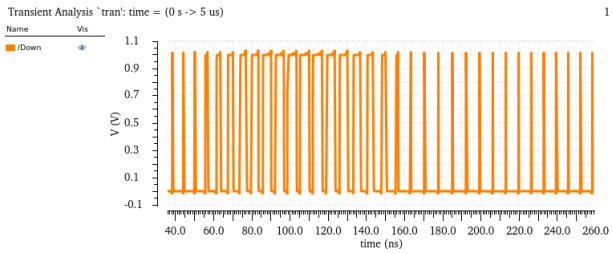

Figure 21: Down of the PFD

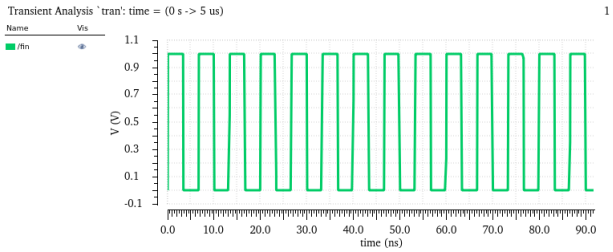

Figure 22: Input frequency vs time

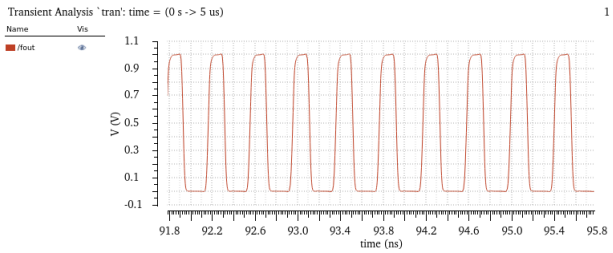

Figure 23: Output frequency vs time

5 Conclusion

In this project we have implemented the phase locked loop with reference frequency of 150MHz and output frequency of 2.4GHz. The current through the charge pump is 35μA. The total capacitance used comes out to be 19.84p + 1.001p = 20.841pF. The total power dissipated comes out to be 606μW.

6 References

[1] P. K. Hanumolu, M. Brownlee, K. Mayaram and Un-Ku Moon, "Analysis of charge-pump phase-locked loops," in IEEE Trans. on Circuits and Syst. I: Regular Papers, vol. 51, no. 9, pp. 1665-1674, Sept. 2004.

[2] H. R. Rategh, H. Samavati and T. H. Lee, "A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver," in IEEE J. of Solid-State Circuits, vol. 35, no. 5, pp. 780-787, May 2000.

[3] Behzad Razavi, "Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level" , Cambridge University Press, 2020.