EE537 Circuit Simulation Lab

Experiment 6B

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1 Design of differential amplifier with resistive load

Design a differential amplifier with resistive load, tail current source of 23*(10) μ A. The ICMR should be 1.2 V, f3,db < 1 MHz and maximize the voltage gain and minimize the common mode gain. Use a load capacitor at the output to band limit the amplifier. Bias the tail current source by using the available reference current of IREF = 10 μ A.

1.1 Hand Calculations

Given tail current source to be 23*(10) = 230μA

1.1.1 Calculating W/L for Input transistors

Calculating the W/L values for the input transistors As we know that as per symmetry considerations I1 + I2 = 230μA I1 = I2 hence I1= I2= 115μA For the input transistors assuming the overdrive to be 100mV

$$Id = \frac{\mu Cox W (Vgs - Vt)^2}{2L} \tag{1}$$

putting the values we get,

$$115\mu = 300\mu * 0.01 * W/L * 0.5 \tag{2}$$

or W/L = 76.66 Similar value will be taken for input transistor 2.

1.1.2 Calculating the W/L for M3 and M4

Now for the tail current source the value of the W/L is given from (1) as

$$230\mu = 300\mu * 0.01 * W/L * 0.5 \tag{3}$$

From these we get W/L = 153.32 Also the reference current source is given to be 10μA. The current will be mirrored from the reference current source. For this we can say, The ratios of W/L of the transistors 3 and 4 should be 23 to get the tail current source as 230μA.

1.1.3 Calculating Vin,cm

The value of Vin,cm; Given that ICMR =1200mV Icmr is given by

$$Vdd - IdRs + Vth1 - Vgs1 - Vov3 = ICMR \tag{4}$$

Vov3 = 100mV, Vgs1-Vth1=100mV, Vth1=500mV, so Vgs1 = 600mV, Vin,cm = Vgs1 + Vov3, or Vin,cm = 600mV+100mV =700mV.

1.1.4 Calculating Rd

Calculating the value of Rd; The maximum value that the ICMR can take is 1.8V so equating this to the Vdd-IdRs+Vth we can get Rd value i.e. 1.8-115μRd+0.5 = 1.8 or Rd = 4.34kΩ Calculation of Capacitance f,3dB < 1MHz

$$\frac{1}{2\pi RC} < 1M \tag{5}$$

R=4.34kΩ Hence putting the values we get

$$C > 37pF \tag{6}$$

Calculating the swing the maximum theoretical swing that is possible is Vdd-Vin,cm+Vth which is equal to 1.5V

Hence the amplitude value is taken to be 100mV

1.2 Show the plots verifying obtained swing, ICMR, differential gain and common mode gain.

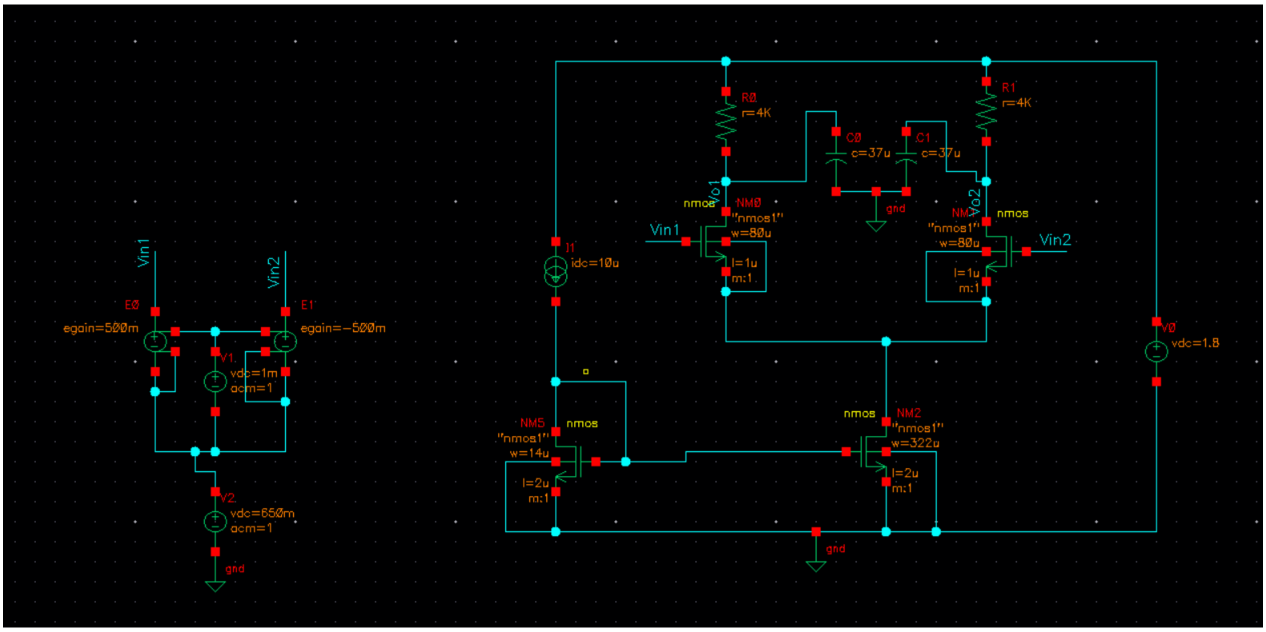

Figure 1: Ckt diagram for icmr calculation

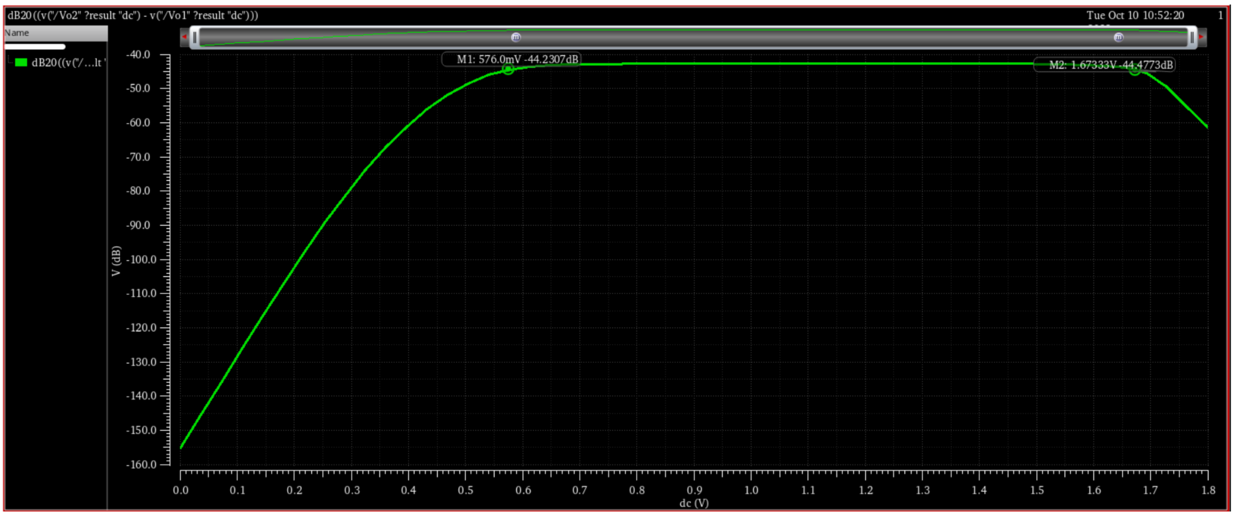

Figure 2: Plot of ICMR

The ICMR can be calculated as
min(Vdd- IdRs + Vth, Vdd) - Vin,cm which is given as
Vdd- Vincm as,
Vdd< Vdd-IdRs +Vth
Hence the value of ICMR is 1150mV. The Observed value is 1094mV

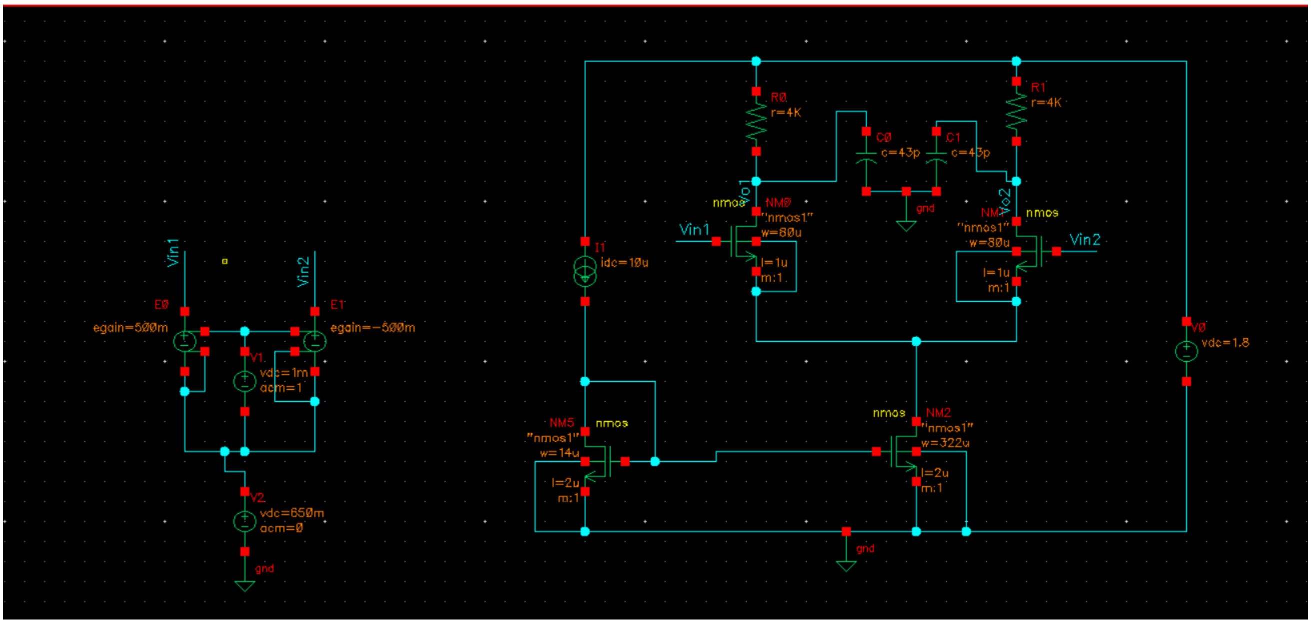

Figure 3: Ckt diagram for differential gain

The Avdm is given by -gmRd
Avdm = -gmRd = -1.85m*4k

Avdm = -7.4 which is approximately equal to 17dB.

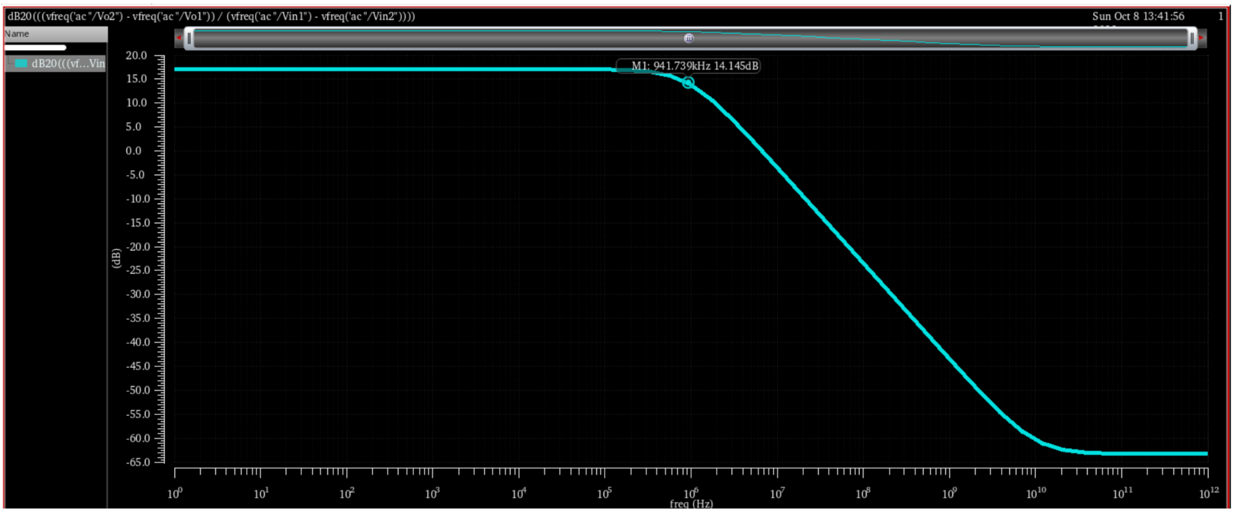

Figure 4: Differential gain wrt frequency

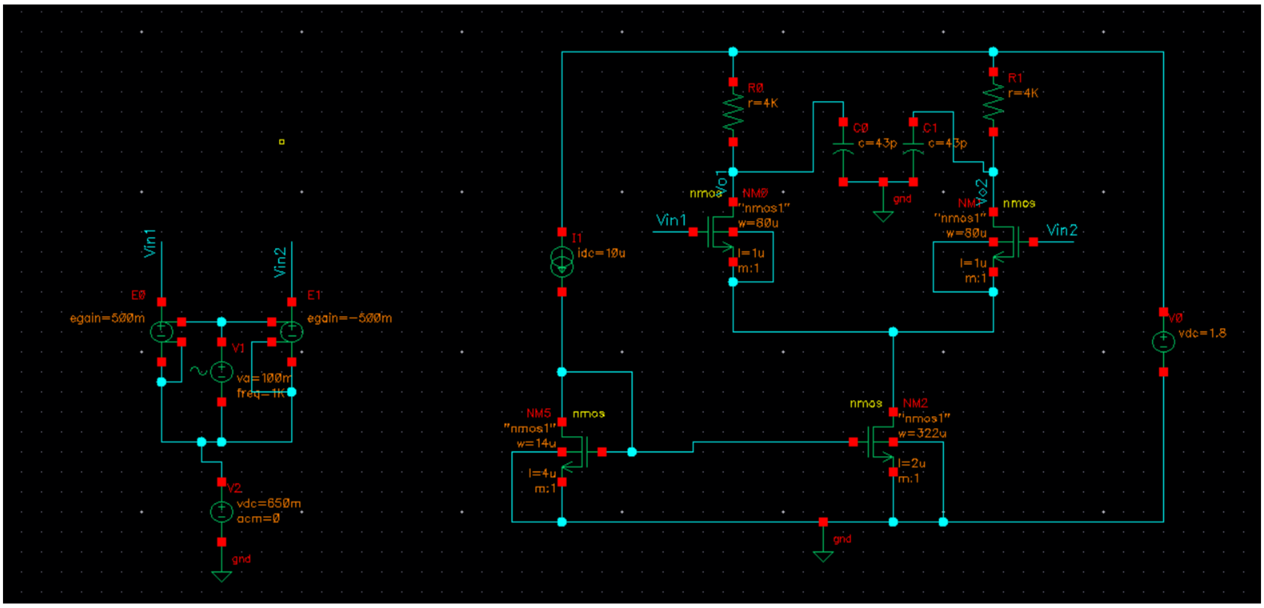

Figure 5: Ckt diagram for swing calculation

The swing can be given as gain*amplitude

The amplitude given is 100mV and the gain calculated is -7.4 the swing comes out to be 740mV and the observed swing is 850mV.

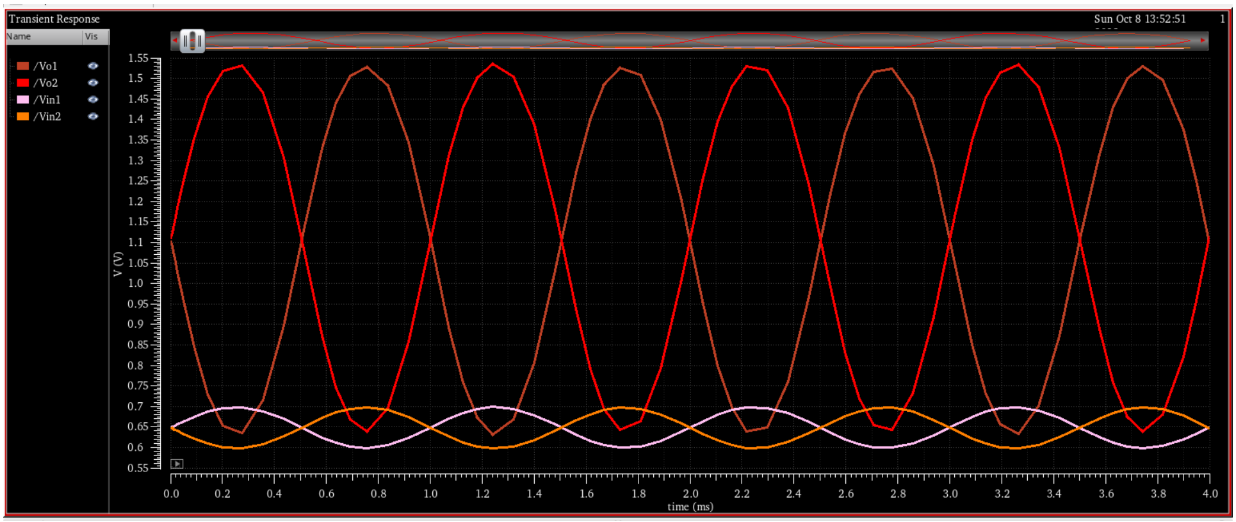

Figure 6: Swings wrt time

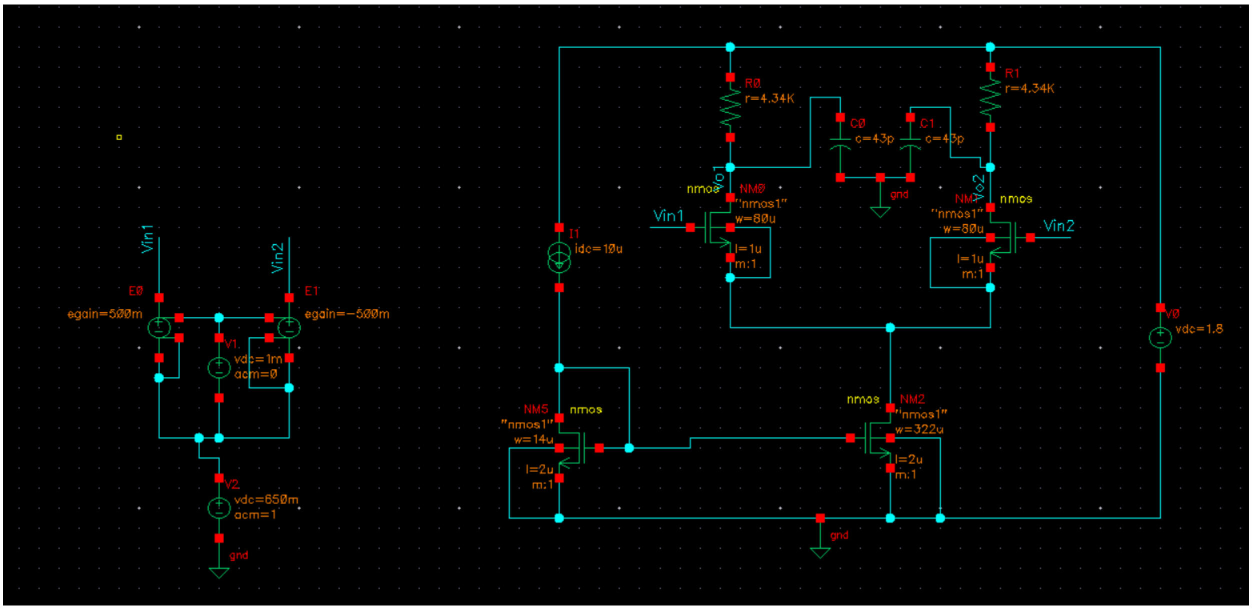

Figure 7: Ckt diagram for common mode gain

The common mode gain is given by

$$Avcm = \frac{\frac{-Rd}{2}}{\frac{1}{2gm} + Rss} \tag{7}$$

$$Avcm = \frac{\frac{-4.34k}{2}}{\frac{1}{2*1.85m} + 4.1k} \tag{8}$$

$$Avcm = 0.49 \tag{9}$$

The value of Avcm in dB is around -6dB.

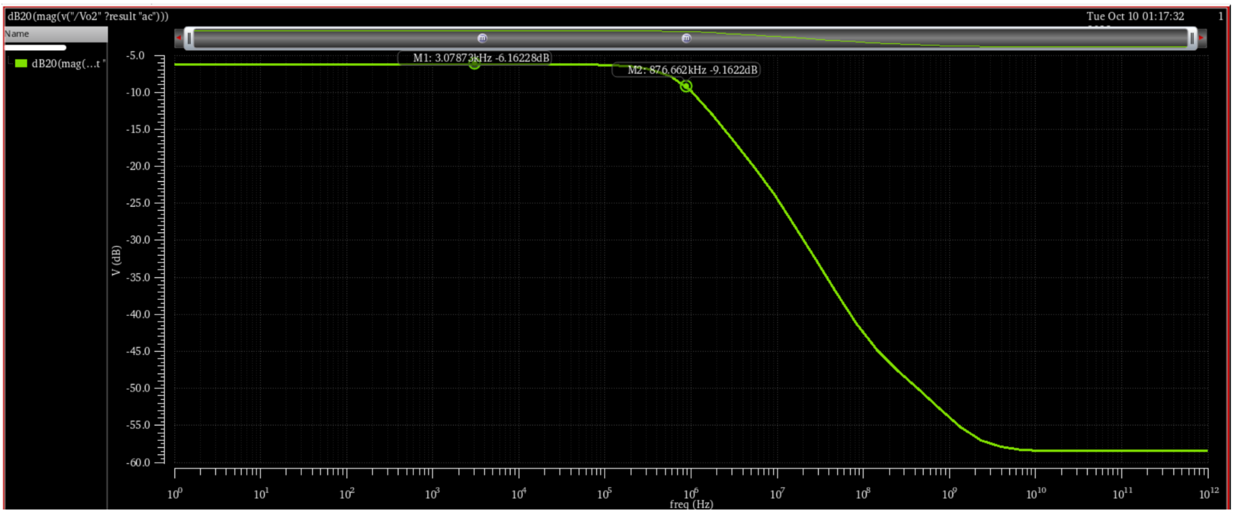

Figure 8: Common mode gain wrt frequency

1.3 Compare the PSD of input referred noise with the PSD of noise observed in previous question. What is the effect of power on PSD?

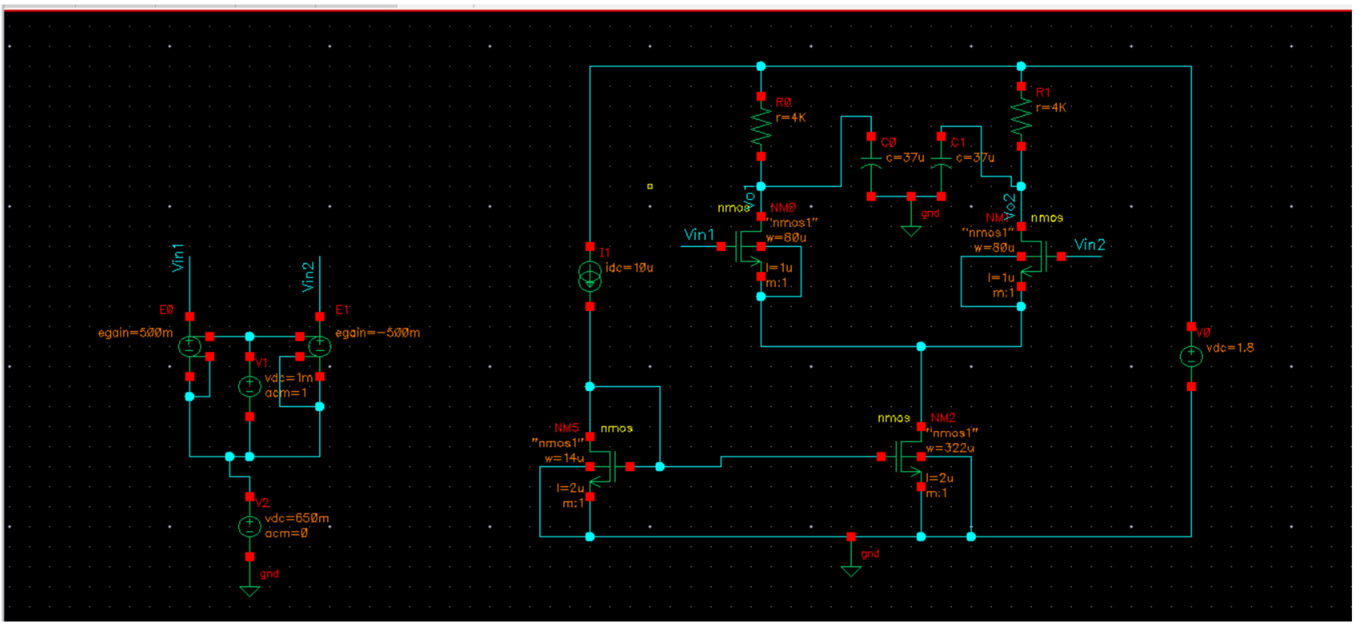

Figure 9: Circuit diagram for noise calculations

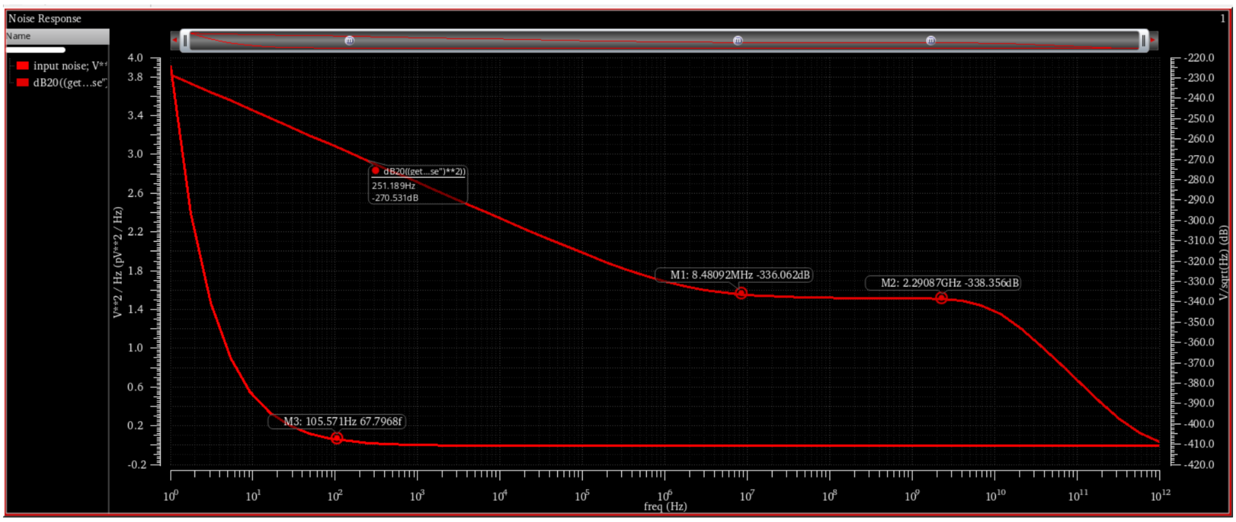

Figure 10: Input noise plot in dB and magnitude

Device	Param	Noise Contribution	% Of Total
/NM0	fn	1.9657e-16	50.03
/NM1	fn	1.95396e-16	49.73
/NM1	id	3.74458e-19	0.10

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 3.92922e-16
Total Input Referred Noise = 5.7701e-11
The above noise summary info is for noise data

Figure 11: Noise summary

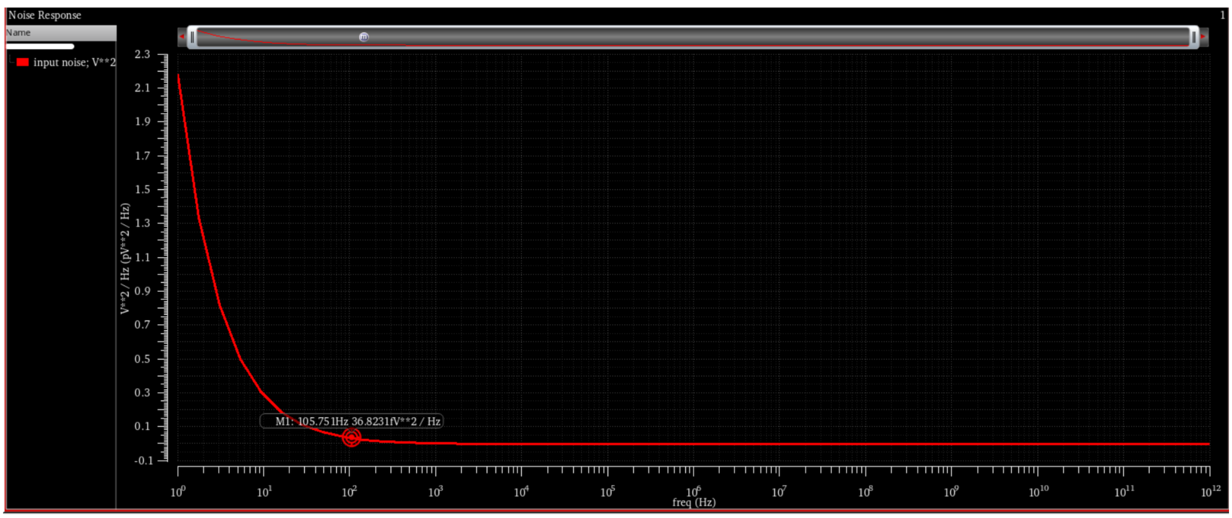

Figure 12: Input noise plot previous case

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Device    Param    Noise Contribution    % Of Total

/NM0      id       7.73733e-07           44.07
/NM1      id       7.59546e-07           43.27
/R0       rn       1.04638e-07           5.96
/R1       rn       1.03792e-07           5.91
/NM0      fn       6.75705e-09           0.38

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 1.7555e-06
Total Input Referred Noise = 2.7529e-08
The above noise summary info is for noise data


Device    Param    Noise Contribution    % Of Total
/NM0      id       7.73733e-07           44.07
/NM1      id       7.59546e-07           43.27
/R0       rn       1.04638e-07           5.96
/R1       rn       1.03792e-07           5.91
/NM0      fn       6.75705e-09           0.38

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 1.7555e-06
Total Input Referred Noise = 2.7529e-08
The above noise summary info is for noise data
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Figure 13: Noise summary for previous case

It is observed that when current increase noise decreases as current in previous case was 10μA and in this case it is 230μA and the input referred noise is 5.7701e-11 and 2.7529e-8 respectively.

The effect of power on PSD. The 3-dB reduction in noise occurs at a cost of doubling the power consumption, which is called "Linear Scaling".We can also say that the widths of the transistors and the resistor are doubled.

2 Design of differential amplifier with current mirror load

Design a differential amplifier with current mirror load, tail current source of 23*(10) μA. The ICMR should be 0.8 V, fugb,db < 40MHz and maximize the voltage gain and minimize the common mode gain. The gm/Id ratio of input transistors should be less than 10. Bias the tail current source by using the available reference current of IREF = 10 μA.

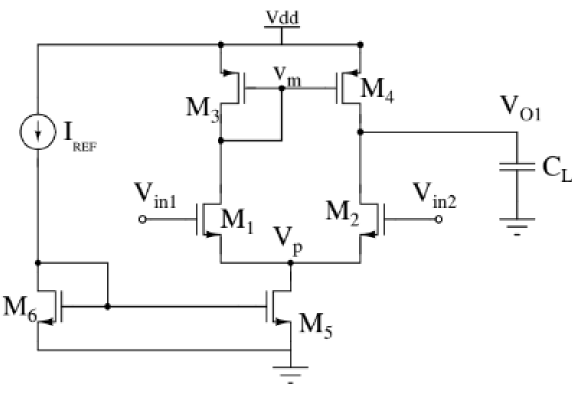

Figure 14: Differential amplifier with current mirror load

2.1 Hand calculations

Given gm/Id < 10, for input transistors, ICMR = 0.8V, fugb¡40MHz, Iref =10μA The tail current source =230μA First we can calculate the ratio of W/L ratio of M3 and M4 which can be easily calculated to be equal to 23.

2.1.1 Calculating W/L for M3 and M4

For M3 transistor the value of W/L is calcualted as follows;
Id= 230μA

$$Id = \frac{\mu CoxW(Vgs - Vt)^2}{2L} \tag{10}$$

Taking the Vgs-Vt for M3 =100mV we can find W/L=153.32. the value of the W/L of M4 can be calculated by dividing the above by 23 which comes out to be 6.665.

2.1.2 Calculating the values of W/L of input Transistors

Here also the current can be said to be divisible by 2 because of the symmetry of the transistors. gm/Id< 10 for input transistors

$$\frac{2Id}{Id(Vgs1 - Vt)} < 10 \tag{11}$$

or Vgs1 - Vt >200mV or Vgs1>700mV Also from these analysis we can say that gm<2.3mS
From (7)
115μ = 300μ(.04)W/L*0.5 or W/L = 19.16.
For the pmos transistors the value of W/L. similarly we can say
115μ =150μ(0.01)(W/L)*0.5 or W/L = 153.32

2.1.3 Calculating Cl

fugb <40MHz or

$$\frac{gm}{2\pi Cl} < 40MHz \tag{12}$$

Put gm = 2.3mS and calculating we get Cl >9.15pF

2.1.4 Calculating Vin,cm

Vin,cm = Vgs1+ Vgs3 -Vth3 Vin,cm > 700+100 = 800mV

2.2 Show the plots verifying obtained swing, ICMR, differential gain and common mode gain.

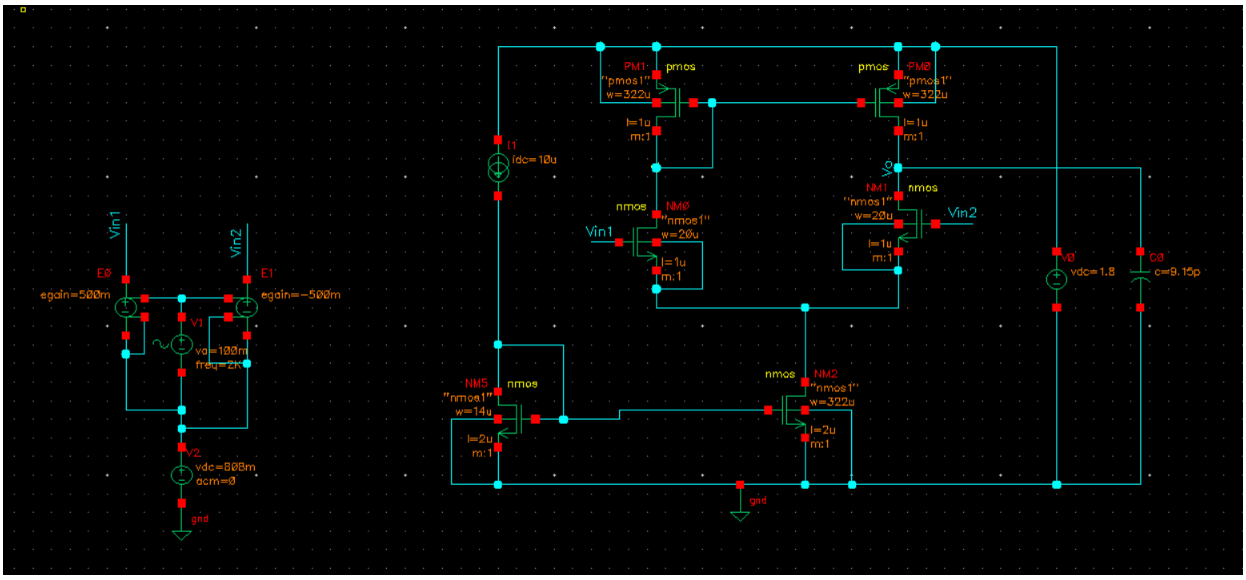

Figure 15: Ckt for ICMR calculations

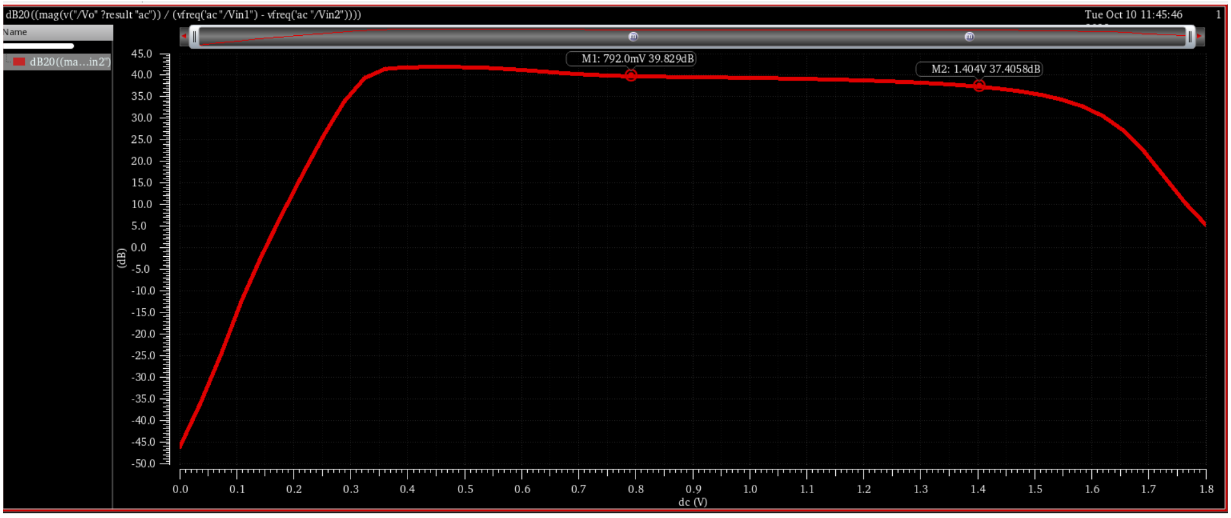

Figure 16: ICMR plot

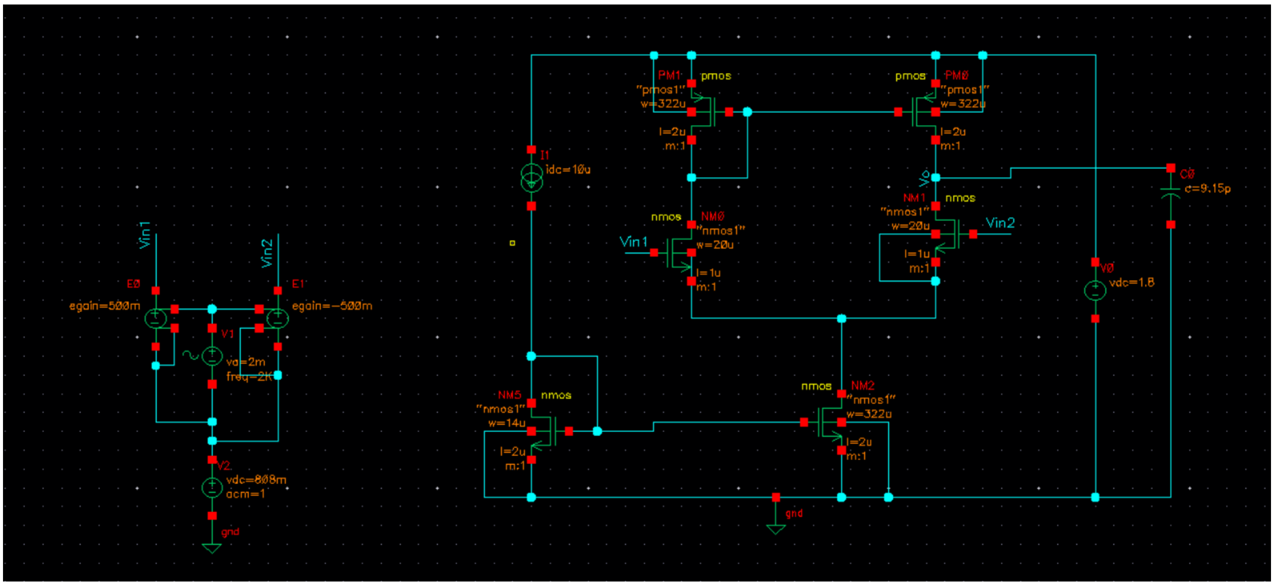

Figure 17: Ckt diagram for calculating different swings

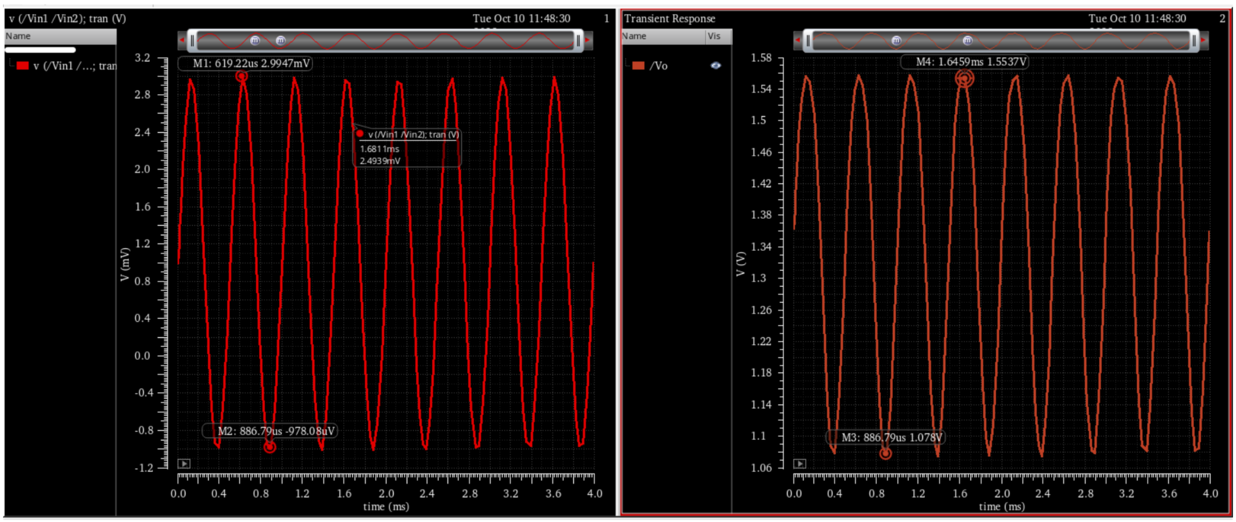

Figure 18: Transient response of the circuit

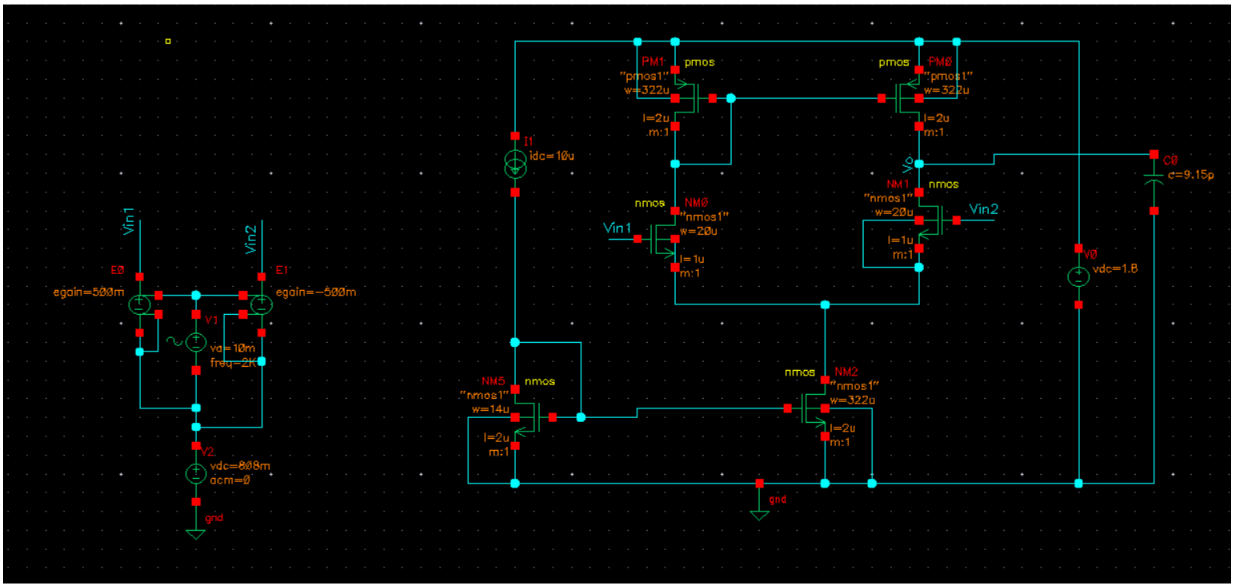

Figure 19: Ckt diagram for frequency analysis of Avdm

$$Avdm = g_{m1}(r_{o1}||r_{o4}) * \frac{2g_{m4}r_{o4}+1}{2(g_{m4}r_{o4}+1)} \tag{13}$$

gm1 = 1.09 m
ro1= 257.377 kΩ
gm4 = 1.32mS
ro4 = 226 kΩ

$$Avdm = 1.09m * (257.377Kohm||226Kohm) * \frac{2*1.32m*226Kohm+1}{2(1.32m*226Kohm+1)} \tag{14}$$

Avdm(in dB) = 20log(Avdm) = 42dB
fugb < 40 MHz

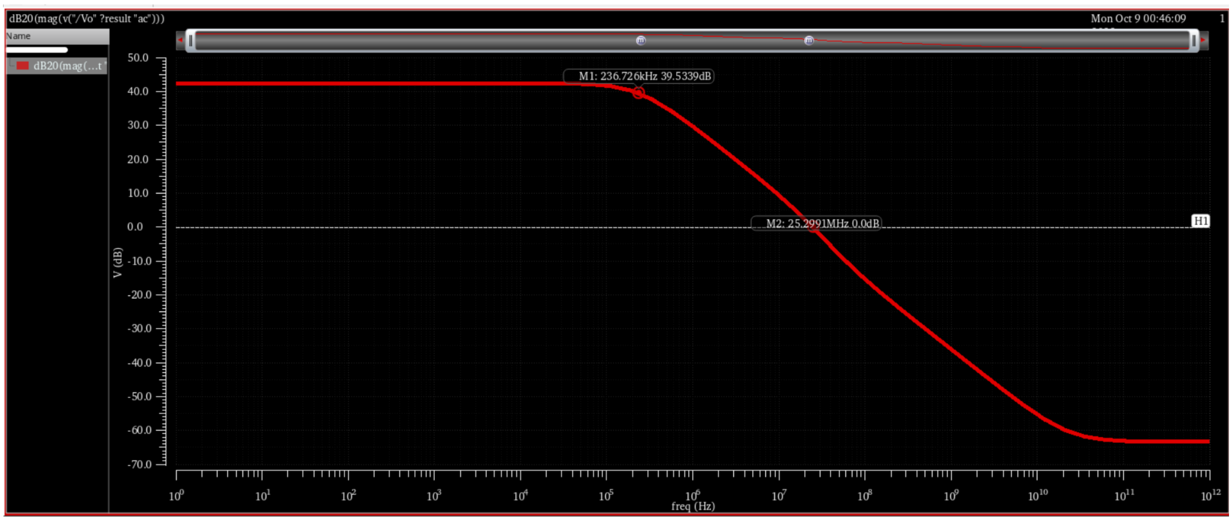

Figure 20: Differential gain wrt frequency

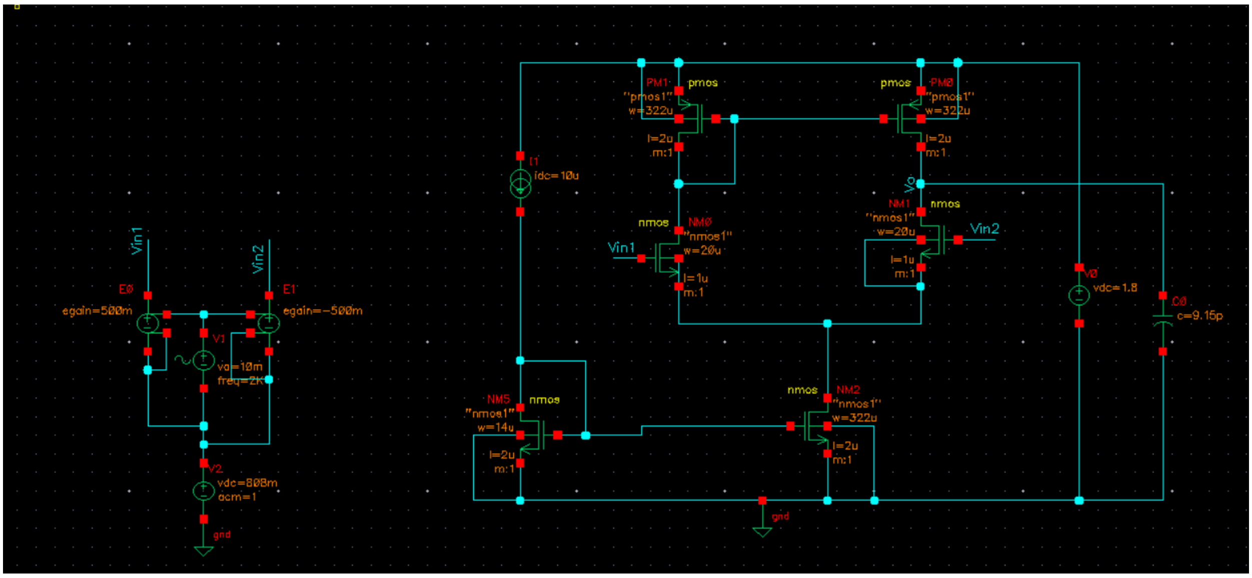

Figure 21: Ckt diagram for frequency relationship of Avcm

$$Avcm = -\frac{1}{1 + 2g_{m1}R_{ss}}\frac{g_{m1}}{g_{m3}} \tag{15}$$

$$|Avcm| = \frac{1}{1 + 2 * 1.09m * 7k}\frac{1.09m}{1.33m} = 0.0504 \tag{16}$$

$$|Avcm, cm|dB = 20log(0.0504) = -25dB \tag{17}$$

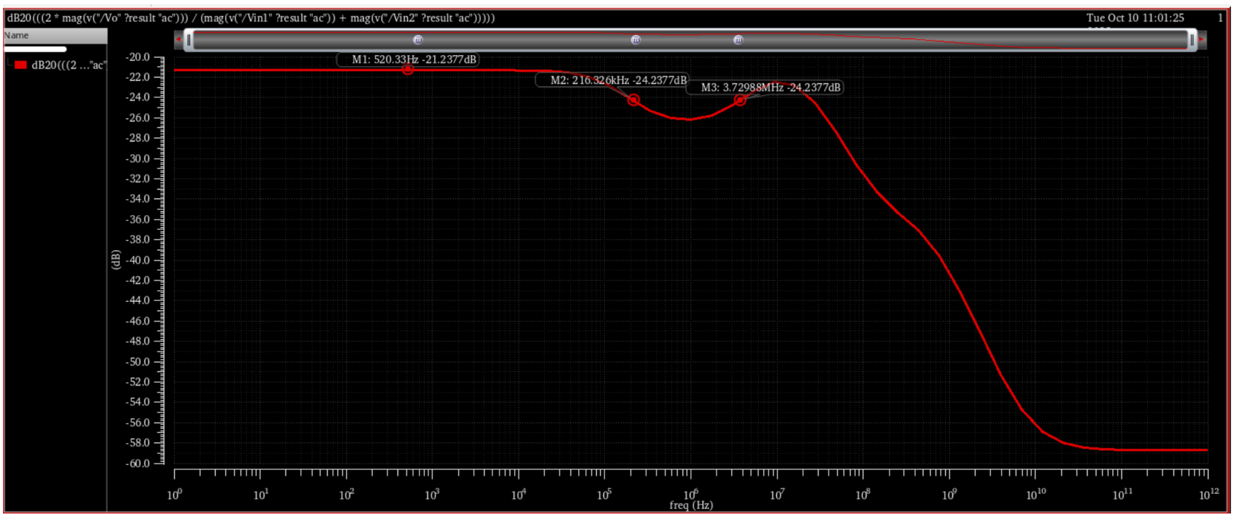

Figure 22: Avcm plot wrt frequency

2.3 What is the step input voltage at which this amplifier connected as a unity gain voltage buffer starts to slew?

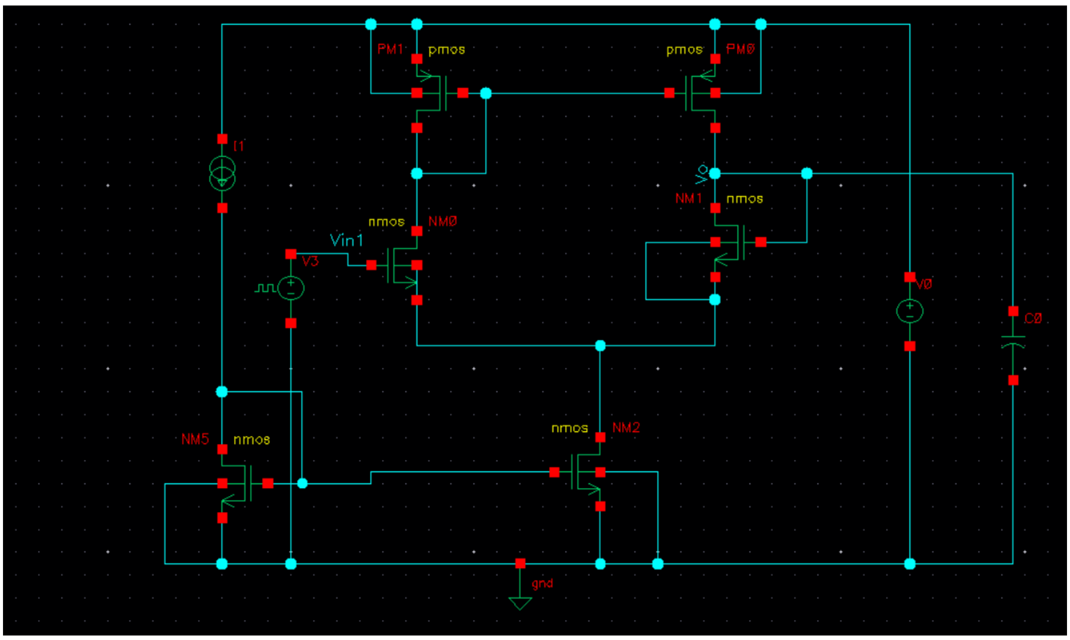

Figure 23: Ckt for slew rate

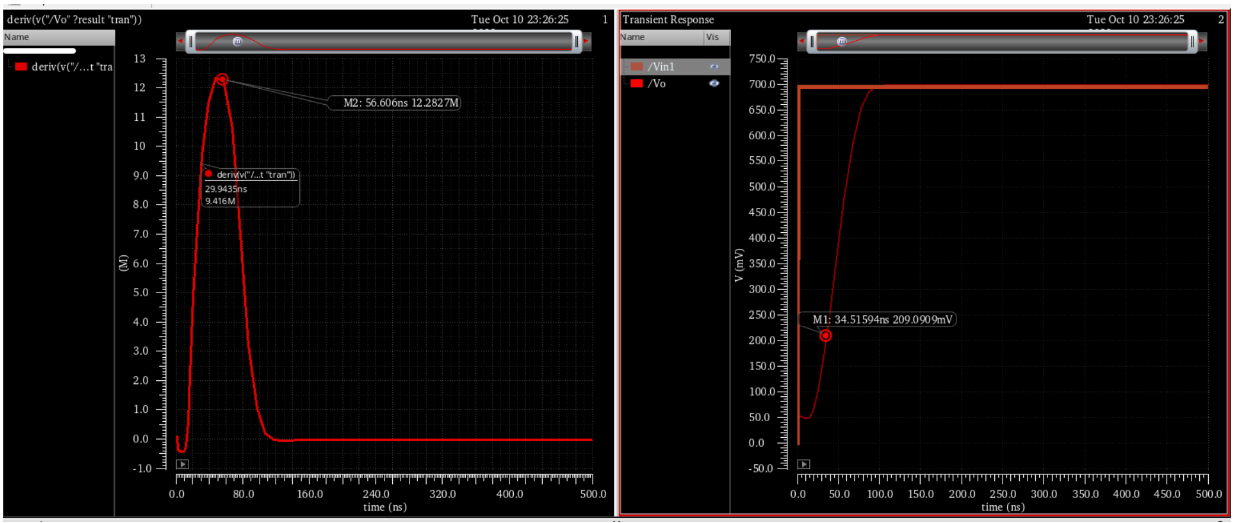

Figure 24: Plot observed

Calculations Slew rate

$$Vo = Vmax(exp(\frac{-t}{\tau}) - 1) \tag{18}$$

$$\frac{dVo}{dt} = \frac{Vomax}{\tau} \tag{19}$$

For slewing

$$\frac{Io}{Cl} < \frac{Vomax}{\tau} \tag{20}$$

$$\tau = Cl/gm \tag{21}$$

or

$$Io/Cl < Vomax * gm/Cl \tag{22}$$

or

$$Vomax > \frac{Vo}{gm} \tag{23}$$

$$\text{Io} = \text{Tail current Source} = 230\ \mu\text{A gm2} = 1.10\ \text{mS}$$

$$\mathcal{T} = \frac{C_L}{g_{m2}} \tag{24}$$

$$\mathcal{T} = \frac{9.15pF}{1.10m} = 8.318nSec \tag{25}$$

$$\frac{I_o}{C_L} < \frac{V_{omax}}{C_L} * g_{m2} \tag{26}$$

$$V_{omax} > \frac{I_o}{g_{m2}} \tag{27}$$

$$V_{omax} > \frac{230\mu A}{1.10m} \tag{28}$$

$$V_{omax} > 209.0909mV \tag{29}$$

2.4 Calculate the output pole, mirror pole and mirror zero. Compare the calculated and simulated values using pz analysis.

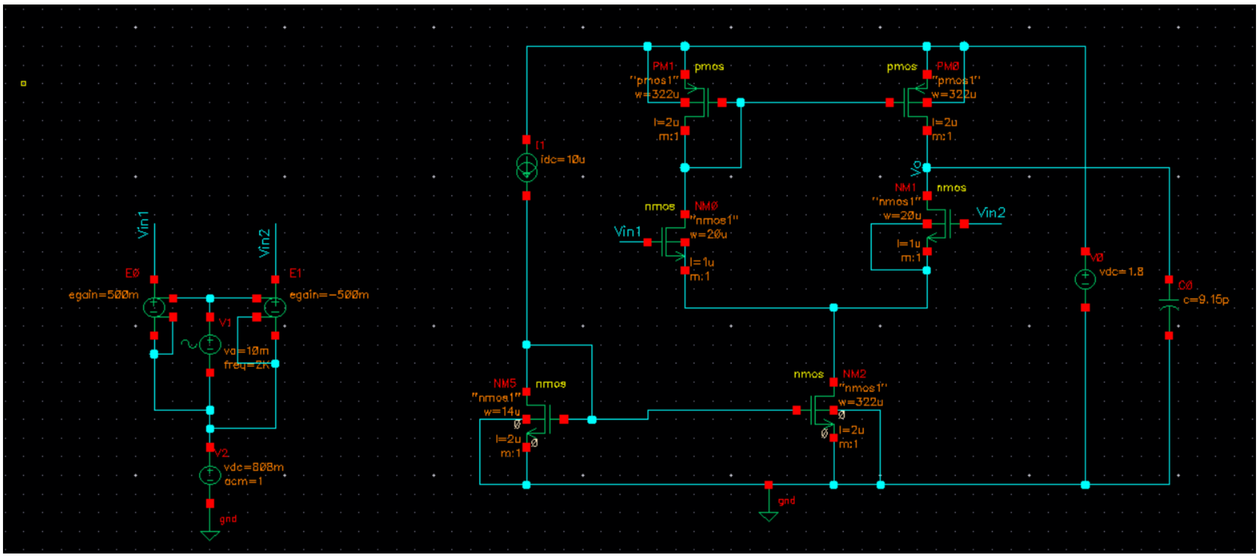

Figure 25: Ckt for pz analysis

	Real	Imaginary	Qfactor
1	-1.34338e+05	0.00000e+00	5.00000e-01
2	-2.38288e+07	0.00000e+00	5.00000e-01

Zeros (Hz)
at V(Vo,net011)/V1

	Real	Imaginary	Qfactor
1	-2.32302e+07	0.00000e+00	5.00000e-01
2	2.31908e+10	0.00000e+00	-5.00000e-01

Constant factor = 7.96969e-04

Figure 26: Pole Zero outputs