Design of an operational amplifier

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Outline

- Introduction
- Motivation
- Literature
- Folded Cascode Operational Amplifier
- Biasing of the Circuit
- Loopgain and Phase Margin
- CMRR and PSRR
- Current supplied and Offset
- Conclusion
- Future Works

Introduction

- Operational amplifiers are one of the most basic blocks in IC design
- The main aim of the amplifiers is to have high gain and stability
- The basic circuit that gives gain is the common source amplifier
- Common source amplifier cannot provide very high gain

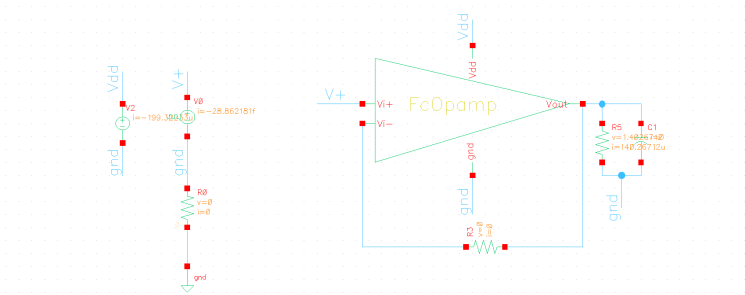

Figure: Operational amplifier

Specification Matrix

Parameters	**Specifications**	**Simulation**	**Comments**
Loop Gain	80dB,	74dB	For 6σ
Phase Margin	65^o	66^o	For 6σ
ICMR	0.8V	0.5V	
Load Resistance	10kΩ		
Load Capacitance	10pF		
CMRR	80dB	71dB(min)	Very high deviation
PSRR	-60dB	-27dB	6σ
Slew Rate	$1V/\mu s$		
Temperature	-$40^oC - 150^oC$		
Offset	±4mV	±14mV	
Supply	3.3V - 5V		
OCMR(Max)	3.3V@150=2.58V @27=2.47V@-40 =2.40V	5V@150=4.2V @27=4.114V@-40=4.054V	Non inverting amplifier

Motivation

OTA

- OTA can provide us with very high gain
- OTA gain is because of the very high output impedance
- Applying a resistor at the output will reduce its gain drastically
- Buffer is required with the OTA for loading resistors

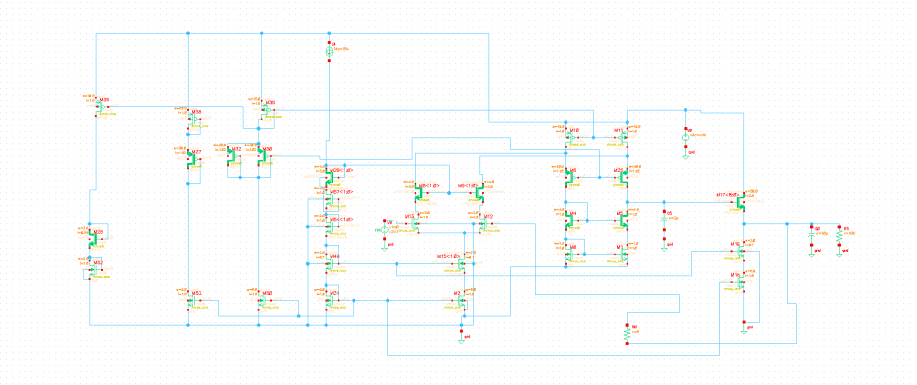

Figure: Folded cascode Opamp

Literature Review

- Most basic gain block is the Common source
- Gain is not very large
- Gain is then increased by increasing the resistance at the output
- Telescopic cascode structure provides us with very high gain but swing is limited in unity feedback

Folded Cascode Operational Amplifier

- Folded cascode provides a high gain
- Swing is also very good in unity feedback configuration
- Differential Gain of Folded cascode

$$A_v = \frac{(g_m r_o)^2}{2} \tag{1}$$

- Common mode gain

$$A = \frac{1}{1 + 2(g_m r_o)^2} \tag{2}$$

- All these gains are calculated assuming same g_m and r_o for all devices

Continued...

- CMRR: Ability to reject the Common mode Variations

$$CMRR = \frac{Av}{A} \tag{3}$$

- PSRR: Ability to reject the Supply variations

$$PSRR = \frac{\Delta Vdd}{R_{buffer} + Ro} \tag{4}$$

- Slew Rate: How fast is the response. For folded cascode OTA,
  - Case 1: $I_1 > \frac{I_o}{2}$

$$SR = \frac{I_o}{C_l} \tag{5}$$

  - Case 2 : $I_1 < \frac{I_o}{2}$

$$SR = \frac{2I_1}{C_l} \tag{6}$$

Continued...

- ICMR: Common mode DC voltages for input

$$V_{gs_{in}} + 2\Delta V < ICMR < V_{g_{ipcas}} - Vthcas - \Delta V + V_{th_{in}} \tag{7}$$

- Output Common Mode Range: DC values taken by the output

$$2\Delta V < OCMR < V_{g\,M17} - V_t - \Delta V \tag{8}$$

$$V_{t\,Mo/M1} + 2\Delta V < V_{g17} < V_{b_{M_6}} + |V_{t\,M_6}| \tag{9}$$

- Slew Rate: How fast is the response. For folded cascode OTA,
  - Case 1: $I_1 > \frac{I_o}{2}$

$$SR = \frac{I_o}{C_l} \tag{10}$$

  - Case 2 : $I_1 < \frac{I_o}{2}$

$$SR = \frac{2I_1}{C_l} \tag{11}$$

Why is the circuit different from traditional circuit?

- Supply voltage varies from 3.3V to 5V
- Current source implementation requires good matching
- For good matching ana device is used
- Ana device can hold a potential difference of 1.5V across V_{ds}
- Pmos5 and nmos5 devices are used for taking the high voltages
- Cascode structures are used as they protect from variations
- Cascode current sources are used as they are nearest to the ideal ones

Effects of temperature variations

- Temperature is varied from -40^oC to 150^oC
- As temperature reduces the threshold voltage starts increasing, reducing the V_{gs} margin set
- Threshold voltage of the Mosfet:

$$V_{th} = \frac{\sqrt{2qN_a\phi_t\epsilon_s}}{C_{ox}} + \phi_t \tag{12}$$

- $$\phi_t = 2V_t ln(\frac{N_a}{n_i}) \tag{13}$$

- $$-ln(n_i) = -lnkT^{\frac{3}{2}} + \frac{E_g}{2kT} \tag{14}$$

- Hence ϕ_t is increased hence increasing the threshold voltage
- As the temperature increases, the V_{th} reduces hence increasing $V_{d_{sat}}$ at higher temperatures

Effects of temperature variations on trans conductance

- Trans conductance of the mosfet is given by $\frac{\partial I_d}{\partial V_{gs}}$
- As the current is already decided by the slew rate, the trans conductance is given by

$$g_m = \frac{2I_d}{V_{gs} - V_{th}} \tag{15}$$

- The same concepts as above can be used to explain this phenomenon as well
- Trans conductance is inversely proportional to the $V_{gs} - V_{th}$
- As the temperature is reduced, $V_{gs} - V_{th}$ reduces implying increased g_m
- For temperature increase $V_{gs} - V_{th}$ increases hence reducing the g_m

Circuit Diagram

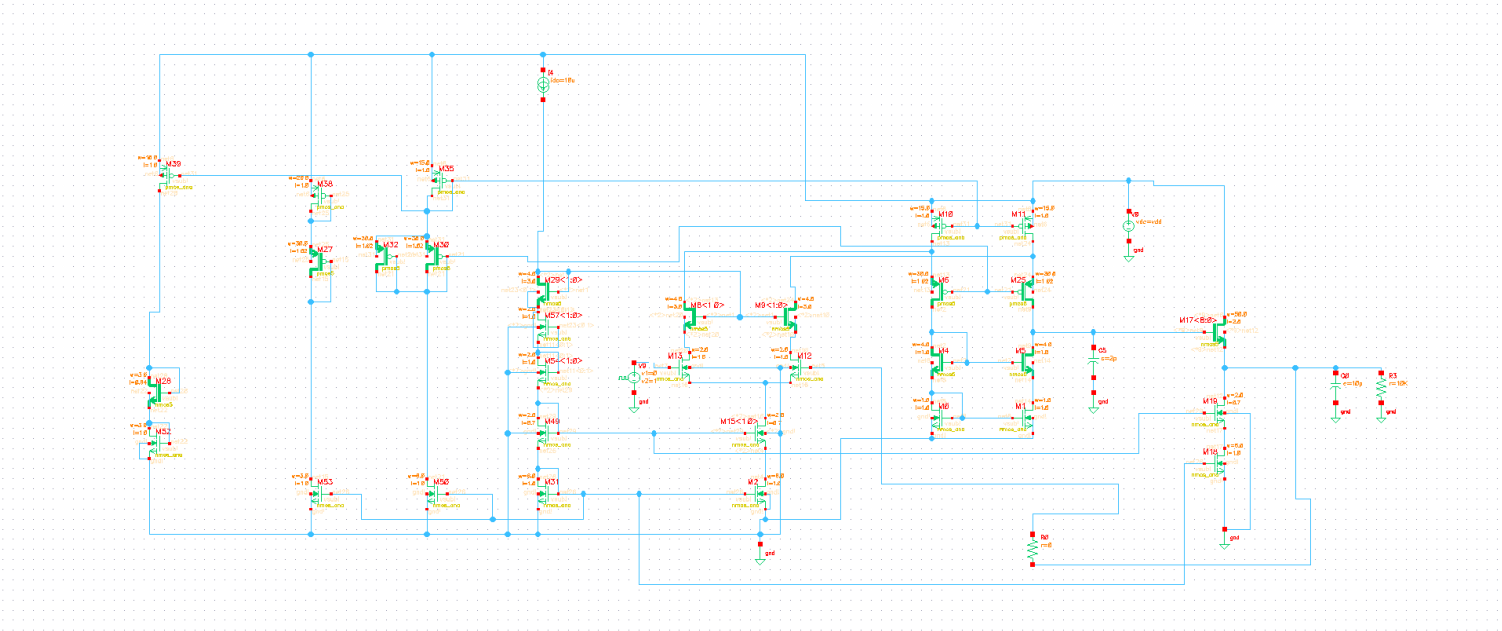

Figure: Operational amplifier

Biasing of the circuit

vds_margin1_new

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	678m	86.92m	454.8m	678.1m	941.3m	50m	inf
27	5.5	1	1.043	86.68m	821m	1.043	1.305	50m	inf
27	5.5	0.9	1.134	86.64m	912.2m	1.134	1.396	50m	inf
27	3.3	1.4	676.8m	86.92m	453.9m	676.9m	940.1m	50m	inf
27	3.3	1	1.042	86.67m	820.1m	1.042	1.304	50m	inf
27	3.3	0.9	1.133	86.63m	911.2m	1.133	1.395	50m	inf
27	2.97	1.4	676.6m	86.91m	453.7m	676.7m	939.8m	50m	inf
27	2.97	1	1.042	86.66m	819.9m	1.042	1.304	50m	inf
27	2.97	0.9	1.133	86.62m	911.1m	1.133	1.395	50m	inf
27	5	1.4	677.7m	86.93m	454.6m	677.8m	941m	50m	inf
27	5	1	1.043	86.68m	820.8m	1.043	1.305	50m	inf
27	5	0.9	1.134	86.64m	912m	1.134	1.396	50m	inf
150	5.5	1.4	465.3m	88.91m	245.6m	465.4m	735m	50m	inf
150	5.5	1	828.4m	88.69m	609.7m	828.4m	1.097	50m	inf
150	5.5	0.9	918.8m	88.64m	700.4m	918.9m	1.188	50m	inf
150	3.3	1.4	464.1m	88.91m	244.7m	464.2m	733.8m	50m	inf
150	3.3	1	827.2m	88.69m	608.9m	827.3m	1.096	50m	inf
150	3.3	0.9	917.6m	88.65m	699.6m	917.7m	1.186	50m	inf
150	2.97	1.4	463.9m	88.9m	244.5m	464m	733.6m	50m	inf
150	2.97	1	827m	88.68m	608.7m	827.1m	1.096	50m	inf
150	2.97	0.9	917.5m	88.64m	699.4m	917.5m	1.186	50m	inf
150	5	1.4	465m	88.92m	245.4m	465.1m	734.7m	50m	inf
150	5	1	828.1m	88.7m	609.5m	828.1m	1.097	50m	inf
150	5	0.9	918.5m	88.65m	700.2m	918.5m	1.187	50m	inf
-40	5.5	1.4	797.2m	86.14m	570.9m	797.3m	1.058	50m	inf
-40	5.5	1	1.163	85.89m	938.3m	1.163	1.423	50m	inf
-40	5.5	0.9	1.255	85.86m	1.03	1.255	1.514	50m	inf
-40	3.3	1.4	796m	86.13m	570m	796.1m	1.057	50m	inf
-40	3.3	1	1.162	85.87m	937.3m	1.162	1.422	50m	inf
-40	3.3	0.9	1.253	85.85m	1.029	1.253	1.513	50m	inf
-40	2.97	1.4	795.8m	86.12m	569.8m	795.9m	1.056	50m	inf
-40	2.97	1	1.162	85.86m	937.1m	1.162	1.422	50m	inf
-40	2.97	0.9	1.253	85.83m	1.029	1.253	1.513	50m	inf
-40	5	1.4	796.9m	86.14m	570.8m	797m	1.058	50m	inf
-40	5	1	1.163	85.89m	938.1m	1.163	1.423	50m	inf
-40	5	0.9	1.254	85.86m	1.029	1.254	1.514	50m	inf

Figure: Vds margin of M13

vds_margin2

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	678m	87.36m	461.2m	678.1m	943.4m	50m	inf
27	5.5	1	1.043	87.11m	827.4m	1.043	1.308	50m	inf
27	5.5	0.9	1.134	87.07m	918.5m	1.134	1.398	50m	inf
27	3.3	1.4	676.8m	87.3m	459.4m	677m	942.3m	50m	inf
27	3.3	1	1.042	87.05m	825.5m	1.042	1.307	50m	inf
27	3.3	0.9	1.133	87.01m	916.7m	1.133	1.397	50m	inf
27	2.97	1.4	676.6m	87.28m	459.2m	676.8m	942.1m	50m	inf
27	2.97	1	1.042	87.03m	825.3m	1.042	1.306	50m	inf
27	2.97	0.9	1.133	87m	916.5m	1.133	1.397	50m	inf
27	5	1.4	677.7m	87.34m	460.6m	677.8m	943.2m	50m	inf
27	5	1	1.043	87.09m	826.8m	1.043	1.307	50m	inf
27	5	0.9	1.134	87.05m	917.9m	1.134	1.398	50m	inf
150	5.5	1.4	465.4m	89.33m	252.8m	465.5m	736.1m	50m	inf
150	5.5	1	828.4m	89.1m	616.8m	828.5m	1.098	50m	inf
150	5.5	0.9	918.8m	89.06m	707.5m	918.9m	1.189	50m	inf
150	3.3	1.4	464.2m	89.26m	250.7m	464.3m	735.1m	50m	inf
150	3.3	1	827.2m	89.04m	614.7m	827.3m	1.097	50m	inf
150	3.3	0.9	917.7m	89m	705.4m	917.7m	1.188	50m	inf
150	2.97	1.4	464.1m	89.25m	250.5m	464.1m	734.8m	50m	inf
150	2.97	1	827.1m	89.03m	614.5m	827.1m	1.097	50m	inf
150	2.97	0.9	917.5m	88.99m	705.2m	917.6m	1.187	50m	inf
150	5	1.4	465.1m	89.31m	252m	465.1m	735.8m	50m	inf
150	5	1	828.1m	89.08m	616.1m	828.2m	1.098	50m	inf
150	5	0.9	918.5m	89.04m	706.7m	918.6m	1.188	50m	inf
-40	5.5	1.4	797.2m	86.6m	577.1m	797.3m	1.061	50m	inf
-40	5.5	1	1.163	86.34m	944.4m	1.164	1.426	50m	inf
-40	5.5	0.9	1.254	86.31m	1.036	1.255	1.517	50m	inf
-40	3.3	1.4	796m	86.54m	575.4m	796.2m	1.06	50m	inf
-40	3.3	1	1.162	86.28m	942.6m	1.162	1.425	50m	inf
-40	3.3	0.9	1.253	86.25m	1.034	1.253	1.516	50m	inf
-40	2.97	1.4	795.8m	86.52m	575.2m	796m	1.06	50m	inf
-40	2.97	1	1.162	86.26m	942.4m	1.162	1.425	50m	inf
-40	2.97	0.9	1.253	86.23m	1.034	1.253	1.516	50m	inf
-40	5	1.4	796.9m	86.58m	576.6m	797.1m	1.061	50m	inf
-40	5	1	1.163	86.31m	943.8m	1.163	1.426	50m	inf
-40	5	0.9	1.254	86.28m	1.035	1.254	1.517	50m	inf

Figure: Vds margin of M12

Biasing of the circuit

vds_margin7

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	269.9m	12.89m	235.2m	269.9m	306.4m	50m	inf
27	5.5	1	269.9m	12.89m	235.2m	269.9m	306.4m	50m	inf
27	5.5	0.9	269.9m	12.88m	235.2m	269.9m	306.4m	50m	inf
27	3.3	1.4	271.6m	12.83m	237.2m	271.6m	307.3m	50m	inf
27	3.3	1	271.5m	12.83m	237.2m	271.5m	307.3m	50m	inf
27	3.3	0.9	271.5m	12.82m	237.1m	271.5m	307.3m	50m	inf
27	2.97	1.4	271.1m	12.82m	236.7m	271m	306.8m	50m	inf
27	2.97	1	271m	12.82m	236.7m	271m	306.7m	50m	inf
27	2.97	0.9	271m	12.82m	236.6m	271m	306.7m	50m	inf
27	5	1.4	271.3m	12.87m	236.7m	271.3m	307.6m	50m	inf
27	5	1	271.3m	12.87m	236.7m	271.3m	307.6m	50m	inf
27	5	0.9	271.2m	12.87m	236.7m	271.2m	307.5m	50m	inf
150	5.5	1.4	171m	12.98m	136.6m	171m	207.1m	50m	inf
150	5.5	1	171m	12.98m	136.5m	171m	207.1m	50m	inf
150	5.5	0.9	171m	12.98m	136.5m	171m	207m	50m	inf
150	3.3	1.4	175.5m	12.89m	141.4m	175.5m	210.6m	50m	inf
150	3.3	1	175.4m	12.89m	141.3m	175.4m	210.5m	50m	inf
150	3.3	0.9	175.4m	12.89m	141.3m	175.4m	210.5m	50m	inf
150	2.97	1.4	175m	12.88m	140.9m	174.9m	210m	50m	inf
150	2.97	1	174.9m	12.88m	140.8m	174.9m	209.9m	50m	inf
150	2.97	0.9	174.9m	12.88m	140.8m	174.9m	209.9m	50m	inf
150	5	1.4	173.6m	12.96m	139.2m	173.6m	209.4m	50m	inf
150	5	1	173.5m	12.96m	139.1m	173.5m	209.3m	50m	inf
150	5	0.9	173.5m	12.96m	139.1m	173.5m	209.3m	50m	inf
-40	5.5	1.4	325.1m	12.83m	290.4m	325.1m	361.9m	50m	inf
-40	5.5	1	325.1m	12.83m	290.4m	325.1m	361.9m	50m	inf
-40	5.5	0.9	325m	12.82m	290.4m	325m	361.8m	50m	inf
-40	3.3	1.4	325.7m	12.79m	291.3m	325.7m	361.8m	50m	inf
-40	3.3	1	325.7m	12.79m	291.2m	325.6m	361.8m	50m	inf
-40	3.3	0.9	325.6m	12.78m	291.2m	325.6m	361.7m	50m	inf
-40	2.97	1.4	325.2m	12.78m	290.8m	325.2m	361.3m	50m	inf
-40	2.97	1	325.2m	12.78m	290.8m	325.1m	361.3m	50m	inf
-40	2.97	0.9	325.1m	12.78m	290.8m	325.1m	361.2m	50m	inf
-40	5	1.4	326m	12.82m	291.4m	326m	362.6m	50m	inf
-40	5	1	325.9m	12.82m	291.4m	325.9m	362.6m	50m	inf
-40	5	0.9	325.9m	12.81m	291.4m	325.9m	362.5m	50m	inf

Figure: Vds margin of M10

vds_margin8

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	268.6m	13.2m	233.2m	268.6m	305.7m	50m	inf
27	5.5	1	269.3m	13.2m	233.8m	269.3m	306.4m	50m	inf
27	5.5	0.9	269.4m	13.2m	234m	269.4m	306.5m	50m	inf
27	3.3	1.4	268.8m	13.13m	233.7m	268.8m	305.3m	50m	inf
27	3.3	1	270.3m	13.14m	235.1m	270.3m	306.7m	50m	inf
27	3.3	0.9	270.6m	13.14m	235.4m	270.6m	307m	50m	inf
27	2.97	1.4	267.5m	13.11m	232.4m	267.5m	303.9m	50m	inf
27	2.97	1	269.5m	13.14m	234.3m	269.5m	305.9m	50m	inf
27	2.97	0.9	269.8m	13.14m	234.7m	269.8m	306.2m	50m	inf
27	5	1.4	269.9m	13.19m	234.6m	269.9m	306.8m	50m	inf
27	5	1	270.6m	13.19m	235.3m	270.6m	307.5m	50m	inf
27	5	0.9	270.8m	13.19m	235.4m	270.8m	307.6m	50m	inf
150	5.5	1.4	169.4m	13.29m	134m	169.4m	206m	50m	inf
150	5.5	1	170.2m	13.29m	134.8m	170.2m	206.8m	50m	inf
150	5.5	0.9	170.4m	13.29m	135m	170.4m	207m	50m	inf
150	3.3	1.4	172.3m	13.19m	137.2m	172.3m	208m	50m	inf
150	3.3	1	174m	13.2m	138.9m	174m	209.7m	50m	inf
150	3.3	0.9	174.3m	13.2m	139.3m	174.3m	210m	50m	inf
150	2.97	1.4	171m	13.17m	136m	171m	206.7m	50m	inf
150	2.97	1	173.1m	13.19m	138.1m	173.1m	208.8m	50m	inf
150	2.97	0.9	173.6m	13.19m	138.5m	173.6m	209.2m	50m	inf
150	5	1.4	171.9m	13.27m	136.6m	171.9m	208.2m	50m	inf
150	5	1	172.7m	13.27m	137.4m	172.7m	209m	50m	inf
150	5	0.9	172.9m	13.27m	137.6m	172.9m	209.2m	50m	inf
-40	5.5	1.4	324m	13.14m	288.8m	324m	361.4m	50m	inf
-40	5.5	1	324.5m	13.14m	289.3m	324.5m	362m	50m	inf
-40	5.5	0.9	324.6m	13.14m	289.4m	324.7m	362m	50m	inf
-40	3.3	1.4	323.2m	13.09m	288.2m	323.2m	360.1m	50m	inf
-40	3.3	1	324.5m	13.1m	289.5m	324.5m	361.4m	50m	inf
-40	3.3	0.9	324.8m	13.1m	289.8m	324.8m	361.6m	50m	inf
-40	2.97	1.4	321.8m	13.06m	286.8m	321.8m	358.7m	50m	inf
-40	2.97	1	323.8m	13.09m	288.7m	323.8m	360.6m	50m	inf
-40	2.97	0.9	324.1m	13.09m	289.1m	324.1m	360.9m	50m	inf
-40	5	1.4	324.8m	13.13m	289.6m	324.8m	362.1m	50m	inf
-40	5	1	325.4m	13.13m	290.2m	325.4m	362.6m	50m	inf
-40	5	0.9	325.5m	13.13m	290.3m	325.5m	362.7m	50m	inf

Figure: Vds margin of M11

Biasing of the circuit

vds_margin6

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	243.3m	18.2m	196.9m	243.3m	300.6m	50m	inf
27	5.5	1	242.9m	18.19m	196.6m	242.9m	300.3m	50m	inf
27	5.5	0.9	242.8m	18.19m	196.5m	242.8m	300.2m	50m	inf
27	3.3	1.4	237.2m	18.17m	191.1m	237.3m	294.5m	50m	inf
27	3.3	1	236.9m	18.17m	190.8m	236.9m	294.2m	50m	inf
27	3.3	0.9	236.8m	18.17m	190.7m	236.9m	294.2m	50m	inf
27	2.97	1.4	236.9m	18.17m	190.8m	237m	294.2m	50m	inf
27	2.97	1	236.6m	18.17m	190.5m	236.6m	293.9m	50m	inf
27	2.97	0.9	236.5m	18.17m	190.4m	236.6m	293.9m	50m	inf
27	5	1.4	240.7m	18.19m	194.4m	240.7m	298m	50m	inf
27	5	1	240.4m	18.18m	194.1m	240.4m	297.7m	50m	inf
27	5	0.9	240.3m	18.18m	194m	240.3m	297.6m	50m	inf
150	5.5	1.4	162.4m	17.65m	116.8m	162.4m	217.7m	50m	inf
150	5.5	1	162m	17.65m	116.4m	162m	217.4m	50m	inf
150	5.5	0.9	161.9m	17.64m	116.3m	161.9m	217.2m	50m	inf
150	3.3	1.4	154.5m	17.61m	109.2m	154.5m	209.8m	50m	inf
150	3.3	1	154.2m	17.61m	108.9m	154.2m	209.4m	50m	inf
150	3.3	0.9	154.1m	17.61m	108.8m	154.1m	209.3m	50m	inf
150	2.97	1.4	154.2m	17.61m	108.9m	154.2m	209.4m	50m	inf
150	2.97	1	153.8m	17.61m	108.5m	153.8m	209.1m	50m	inf
150	2.97	0.9	153.7m	17.61m	108.4m	153.8m	209m	50m	inf
150	5	1.4	159.1m	17.63m	113.6m	159.1m	214.4m	50m	inf
150	5	1	158.7m	17.63m	113.2m	158.8m	214.1m	50m	inf
150	5	0.9	158.6m	17.63m	113.1m	158.6m	214m	50m	inf
-40	5.5	1.4	287.6m	18.81m	240.5m	287.6m	346.8m	50m	inf
-40	5.5	1	287.3m	18.81m	240.2m	287.3m	346.5m	50m	inf
-40	5.5	0.9	287.2m	18.81m	240.1m	287.2m	346.4m	50m	inf
-40	3.3	1.4	282.6m	18.8m	235.7m	282.6m	341.7m	50m	inf
-40	3.3	1	282.3m	18.8m	235.4m	282.3m	341.4m	50m	inf
-40	3.3	0.9	282.2m	18.8m	235.3m	282.2m	341.4m	50m	inf
-40	2.97	1.4	282.3m	18.8m	235.4m	282.4m	341.4m	50m	inf
-40	2.97	1	282m	18.79m	235.1m	282m	341.1m	50m	inf
-40	2.97	0.9	281.9m	18.8m	235m	282m	341.1m	50m	inf
-40	5	1.4	285.4m	18.8m	238.4m	285.4m	344.6m	50m	inf
-40	5	1	285.1m	18.8m	238m	285.1m	344.3m	50m	inf
-40	5	0.9	285m	18.81m	238m	285.1m	344.2m	50m	inf

Figure: Vds margin of M1

vds_margin5

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	242.5m	16.39m	200.2m	242.5m	291.3m	50m	inf
27	5.5	1	242.5m	16.39m	200.2m	242.5m	291.3m	50m	inf
27	5.5	0.9	242.5m	16.4m	200.2m	242.5m	291.4m	50m	inf
27	3.3	1.4	236.5m	16.35m	194.3m	236.5m	285.2m	50m	inf
27	3.3	1	236.5m	16.35m	194.3m	236.5m	285.2m	50m	inf
27	3.3	0.9	236.5m	16.36m	194.3m	236.5m	285.2m	50m	inf
27	2.97	1.4	236.2m	16.35m	194m	236.2m	284.9m	50m	inf
27	2.97	1	236.2m	16.35m	194m	236.2m	284.9m	50m	inf
27	2.97	0.9	236.2m	16.35m	194m	236.2m	284.9m	50m	inf
27	5	1.4	239.9m	16.38m	197.6m	239.9m	288.7m	50m	inf
27	5	1	239.9m	16.38m	197.6m	239.9m	288.7m	50m	inf
27	5	0.9	239.9m	16.38m	197.6m	240m	288.7m	50m	inf
150	5.5	1.4	161.5m	16.45m	119.3m	161.5m	210.5m	50m	inf
150	5.5	1	161.5m	16.45m	119.3m	161.5m	210.5m	50m	inf
150	5.5	0.9	161.5m	16.45m	119.3m	161.5m	210.6m	50m	inf
150	3.3	1.4	153.6m	16.39m	111.6m	153.6m	202.5m	50m	inf
150	3.3	1	153.6m	16.39m	111.6m	153.6m	202.5m	50m	inf
150	3.3	0.9	153.6m	16.4m	111.6m	153.6m	202.6m	50m	inf
150	2.97	1.4	153.2m	16.39m	111.3m	153.3m	202.2m	50m	inf
150	2.97	1	153.3m	16.39m	111.3m	153.3m	202.2m	50m	inf
150	2.97	0.9	153.3m	16.39m	111.3m	153.3m	202.2m	50m	inf
150	5	1.4	158.2m	16.42m	116.1m	158.2m	207.2m	50m	inf
150	5	1	158.2m	16.42m	116.1m	158.2m	207.2m	50m	inf
150	5	0.9	158.2m	16.43m	116.1m	158.2m	207.2m	50m	inf
-40	5.5	1.4	286.9m	16.37m	244.4m	286.9m	335.6m	50m	inf
-40	5.5	1	286.9m	16.37m	244.4m	286.9m	335.6m	50m	inf
-40	5.5	0.9	286.9m	16.38m	244.4m	286.9m	335.6m	50m	inf
-40	3.3	1.4	281.9m	16.34m	239.5m	281.9m	330.5m	50m	inf
-40	3.3	1	281.9m	16.34m	239.5m	281.9m	330.5m	50m	inf
-40	3.3	0.9	281.9m	16.35m	239.5m	281.9m	330.5m	50m	inf
-40	2.97	1.4	281.6m	16.34m	239.2m	281.6m	330.2m	50m	inf
-40	2.97	1	281.6m	16.34m	239.2m	281.6m	330.2m	50m	inf
-40	2.97	0.9	281.6m	16.35m	239.2m	281.6m	330.3m	50m	inf
-40	5	1.4	284.7m	16.36m	242.2m	284.7m	333.4m	50m	inf
-40	5	1	284.7m	16.36m	242.2m	284.7m	333.4m	50m	inf
-40	5	0.9	284.7m	16.37m	242.2m	284.7m	333.4m	50m	inf

Figure: Vds margin of M0

Biasing of the circuit

vds_margin18

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	37.75	42.94m	37.63	37.75	37.89	50m	inf
27	5.5	1	41.25	42.52m	41.14	41.25	41.38	50m	inf
27	5.5	0.9	42.12	42.43m	42.01	42.12	42.26	50m	inf
27	3.3	1.4	17.96	39m	17.85	17.96	18.08	50m	inf
27	3.3	1	21.46	38.58m	21.36	21.46	21.58	50m	inf
27	3.3	0.9	22.33	38.49m	22.23	22.33	22.45	50m	inf
27	2.97	1.4	14.99	38.82m	14.89	14.99	15.11	50m	inf
27	2.97	1	18.49	38.4m	18.39	18.49	18.61	50m	inf
27	2.97	0.9	19.36	38.31m	19.26	19.36	19.48	50m	inf
27	5	1.4	33.25	41.19m	33.14	33.25	33.38	50m	inf
27	5	1	36.75	40.77m	36.64	36.75	36.88	50m	inf
27	5	0.9	37.63	40.68m	37.52	37.63	37.75	50m	inf
150	5.5	1.4	38.06	44.27m	37.94	38.06	38.2	50m	inf
150	5.5	1	41.53	43.53m	41.41	41.53	41.67	50m	inf
150	5.5	0.9	42.39	43.37m	42.27	42.39	42.53	50m	inf
150	3.3	1.4	18.27	39.84m	18.16	18.27	18.4	50m	inf
150	3.3	1	21.74	39.11m	21.63	21.74	21.86	50m	inf
150	3.3	0.9	22.6	38.94m	22.5	22.6	22.73	50m	inf
150	2.97	1.4	15.3	39.66m	15.19	15.3	15.43	50m	inf
150	2.97	1	18.77	38.94m	18.66	18.77	18.89	50m	inf
150	2.97	0.9	19.63	38.77m	19.53	19.63	19.76	50m	inf
150	5	1.4	33.56	42.34m	33.45	33.56	33.7	50m	inf
150	5	1	37.03	41.61m	36.92	37.03	37.16	50m	inf
150	5	0.9	37.89	41.44m	37.78	37.89	38.03	50m	inf
-40	5.5	1.4	37.59	42.33m	37.47	37.59	37.72	50m	inf
-40	5.5	1	41.1	42.06m	40.99	41.1	41.24	50m	inf
-40	5.5	0.9	41.98	42.01m	41.87	41.98	42.11	50m	inf
-40	3.3	1.4	17.79	38.66m	17.69	17.79	17.92	50m	inf
-40	3.3	1	21.31	38.38m	21.21	21.31	21.43	50m	inf
-40	3.3	0.9	22.19	38.32m	22.09	22.19	22.31	50m	inf
-40	2.97	1.4	14.82	38.48m	14.72	14.82	14.95	50m	inf
-40	2.97	1	18.34	38.19m	18.24	18.34	18.46	50m	inf
-40	2.97	0.9	19.22	38.14m	19.12	19.22	19.34	50m	inf
-40	5	1.4	33.09	40.69m	32.98	33.09	33.22	50m	inf
-40	5	1	36.61	40.41m	36.5	36.61	36.73	50m	inf
-40	5	0.9	37.48	40.36m	37.38	37.48	37.61	50m	inf

Figure: Vds margin of M17<0:8>

vds_margin4

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	260.7m	14.16m	220.5m	260.7m	300.3m	50m	inf
27	5.5	1	256.8m	13.77m	217.4m	256.8m	294.2m	50m	inf
27	5.5	0.9	252.6m	11.26m	216m	253.8m	276.3m	50m	inf
27	3.3	1.4	260.7m	14.16m	220.5m	260.7m	300.3m	50m	inf
27	3.3	1	256.8m	13.77m	217.4m	256.8m	294.2m	50m	inf
27	3.3	0.9	252.6m	11.26m	216m	253.8m	276.2m	50m	inf
27	2.97	1.4	260.7m	14.16m	220.5m	260.7m	300.3m	50m	inf
27	2.97	1	256.8m	13.77m	217.4m	256.8m	294.2m	50m	inf
27	2.97	0.9	252.6m	11.26m	216m	253.8m	276.2m	50m	inf
27	5	1.4	260.7m	14.16m	220.5m	260.7m	300.3m	50m	inf
27	5	1	256.8m	13.77m	217.4m	256.8m	294.2m	50m	inf
27	5	0.9	252.6m	11.26m	216m	253.8m	276.3m	50m	inf
150	5.5	1.4	186.5m	14.14m	146.8m	186.5m	225.9m	50m	inf
150	5.5	1	182.5m	13.87m	143.6m	182.6m	220.6m	50m	inf
150	5.5	0.9	180m	12.68m	142.3m	180.5m	208.7m	50m	inf
150	3.3	1.4	186.5m	14.14m	146.8m	186.5m	225.9m	50m	inf
150	3.3	1	182.5m	13.87m	143.6m	182.6m	220.6m	50m	inf
150	3.3	0.9	180m	12.68m	142.3m	180.5m	208.8m	50m	inf
150	2.97	1.4	186.5m	14.14m	146.8m	186.5m	225.9m	50m	inf
150	2.97	1	182.5m	13.87m	143.6m	182.6m	220.6m	50m	inf
150	2.97	0.9	180m	12.68m	142.3m	180.5m	208.8m	50m	inf
150	5	1.4	186.5m	14.14m	146.8m	186.5m	225.9m	50m	inf
150	5	1	182.5m	13.87m	143.6m	182.6m	220.6m	50m	inf
150	5	0.9	180m	12.68m	142.3m	180.5m	208.8m	50m	inf
-40	5.5	1.4	302.5m	14.21m	261.7m	302.5m	342.2m	50m	inf
-40	5.5	1	298.7m	13.71m	258.9m	298.8m	335.3m	50m	inf
-40	5.5	0.9	292.5m	9.657m	257.4m	294.4m	311.1m	50m	inf
-40	3.3	1.4	302.5m	14.21m	261.7m	302.5m	342.2m	50m	inf
-40	3.3	1	298.7m	13.71m	258.9m	298.8m	335.3m	50m	inf
-40	3.3	0.9	292.5m	9.656m	257.4m	294.4m	311m	50m	inf
-40	2.97	1.4	302.5m	14.21m	261.7m	302.5m	342.2m	50m	inf
-40	2.97	1	298.7m	13.71m	258.9m	298.8m	335.3m	50m	inf
-40	2.97	0.9	292.5m	9.656m	257.4m	294.4m	311m	50m	inf
-40	5	1.4	302.5m	14.21m	261.7m	302.5m	342.2m	50m	inf
-40	5	1	298.7m	13.71m	258.9m	298.8m	335.3m	50m	inf
-40	5	0.9	292.5m	9.657m	257.4m	294.4m	311.1m	50m	inf

Figure: Vds margin of M2

Biasing of the circuit

vds_margin1_new

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	678m	86.92m	454.8m	678.1m	941.3m	50m	inf
27	5.5	1	1.043	86.68m	821m	1.043	1.305	50m	inf
27	5.5	0.9	1.134	86.64m	912.2m	1.134	1.396	50m	inf
27	3.3	1.4	676.8m	86.92m	453.9m	676.9m	940.1m	50m	inf
27	3.3	1	1.042	86.67m	820.1m	1.042	1.304	50m	inf
27	3.3	0.9	1.133	86.63m	911.2m	1.133	1.395	50m	inf
27	2.97	1.4	676.6m	86.91m	453.7m	676.7m	939.8m	50m	inf
27	2.97	1	1.042	86.66m	819.9m	1.042	1.304	50m	inf
27	2.97	0.9	1.133	86.62m	911.1m	1.133	1.395	50m	inf
27	5	1.4	677.7m	86.93m	454.6m	677.8m	941m	50m	inf
27	5	1	1.043	86.68m	820.8m	1.043	1.305	50m	inf
27	5	0.9	1.134	86.64m	912m	1.134	1.396	50m	inf
150	5.5	1.4	465.3m	88.91m	245.6m	465.4m	735m	50m	inf
150	5.5	1	828.4m	88.69m	609.7m	828.4m	1.097	50m	inf
150	5.5	0.9	918.8m	88.64m	700.4m	918.9m	1.188	50m	inf
150	3.3	1.4	464.1m	88.91m	244.7m	464.2m	733.8m	50m	inf
150	3.3	1	827.2m	88.69m	608.9m	827.3m	1.096	50m	inf
150	3.3	0.9	917.6m	88.65m	699.6m	917.7m	1.186	50m	inf
150	2.97	1.4	463.9m	88.9m	244.5m	464m	733.6m	50m	inf
150	2.97	1	827m	88.68m	608.7m	827.1m	1.096	50m	inf
150	2.97	0.9	917.5m	88.64m	699.4m	917.5m	1.186	50m	inf
150	5	1.4	465m	88.92m	245.4m	465.1m	734.7m	50m	inf
150	5	1	828.1m	88.7m	609.5m	828.1m	1.097	50m	inf
150	5	0.9	918.5m	88.65m	700.2m	918.5m	1.187	50m	inf
-40	5.5	1.4	797.2m	86.14m	570.9m	797.3m	1.058	50m	inf
-40	5.5	1	1.163	85.89m	938.3m	1.163	1.423	50m	inf
-40	5.5	0.9	1.255	85.86m	1.03	1.255	1.514	50m	inf
-40	3.3	1.4	796m	86.13m	570m	796.1m	1.057	50m	inf
-40	3.3	1	1.162	85.87m	937.3m	1.162	1.422	50m	inf
-40	3.3	0.9	1.253	85.85m	1.029	1.253	1.513	50m	inf
-40	2.97	1.4	795.8m	86.12m	569.8m	795.9m	1.056	50m	inf
-40	2.97	1	1.162	85.86m	937.1m	1.162	1.422	50m	inf
-40	2.97	0.9	1.253	85.83m	1.029	1.253	1.513	50m	inf
-40	5	1.4	796.9m	86.14m	570.8m	797m	1.058	50m	inf
-40	5	1	1.163	85.89m	938.1m	1.163	1.423	50m	inf
-40	5	0.9	1.254	85.86m	1.029	1.254	1.514	50m	inf

Figure: Vds margin of M13

vds_margin2

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	678m	87.36m	461.2m	678.1m	943.4m	50m	inf
27	5.5	1	1.043	87.11m	827.4m	1.043	1.308	50m	inf
27	5.5	0.9	1.134	87.07m	918.5m	1.134	1.398	50m	inf
27	3.3	1.4	676.8m	87.3m	459.4m	677m	942.3m	50m	inf
27	3.3	1	1.042	87.05m	825.5m	1.042	1.307	50m	inf
27	3.3	0.9	1.133	87.01m	916.7m	1.133	1.397	50m	inf
27	2.97	1.4	676.6m	87.28m	459.2m	676.8m	942.1m	50m	inf
27	2.97	1	1.042	87.03m	825.3m	1.042	1.306	50m	inf
27	2.97	0.9	1.133	87m	916.5m	1.133	1.397	50m	inf
27	5	1.4	677.7m	87.34m	460.6m	677.8m	943.2m	50m	inf
27	5	1	1.043	87.09m	826.8m	1.043	1.307	50m	inf
27	5	0.9	1.134	87.05m	917.9m	1.134	1.398	50m	inf
150	5.5	1.4	465.4m	89.33m	252.8m	465.5m	736.1m	50m	inf
150	5.5	1	828.4m	89.1m	616.8m	828.5m	1.098	50m	inf
150	5.5	0.9	918.8m	89.06m	707.5m	918.9m	1.189	50m	inf
150	3.3	1.4	464.2m	89.26m	250.7m	464.3m	735.1m	50m	inf
150	3.3	1	827.2m	89.04m	614.7m	827.3m	1.097	50m	inf
150	3.3	0.9	917.7m	89m	705.4m	917.7m	1.188	50m	inf
150	2.97	1.4	464.1m	89.25m	250.5m	464.1m	734.8m	50m	inf
150	2.97	1	827.1m	89.03m	614.5m	827.1m	1.097	50m	inf
150	2.97	0.9	917.5m	88.99m	705.2m	917.6m	1.187	50m	inf
150	5	1.4	465.1m	89.31m	252m	465.1m	735.8m	50m	inf
150	5	1	828.1m	89.08m	616.1m	828.2m	1.098	50m	inf
150	5	0.9	918.5m	89.04m	706.7m	918.6m	1.188	50m	inf
-40	5.5	1.4	797.2m	86.6m	577.1m	797.3m	1.061	50m	inf
-40	5.5	1	1.163	86.34m	944.4m	1.164	1.426	50m	inf
-40	5.5	0.9	1.254	86.31m	1.036	1.255	1.517	50m	inf
-40	3.3	1.4	796m	86.54m	575.4m	796.2m	1.06	50m	inf
-40	3.3	1	1.162	86.28m	942.6m	1.162	1.425	50m	inf
-40	3.3	0.9	1.253	86.25m	1.034	1.253	1.516	50m	inf
-40	2.97	1.4	795.8m	86.52m	575.2m	796m	1.06	50m	inf
-40	2.97	1	1.162	86.26m	942.4m	1.162	1.425	50m	inf
-40	2.97	0.9	1.253	86.23m	1.034	1.253	1.516	50m	inf
-40	5	1.4	796.9m	86.58m	576.6m	797.1m	1.061	50m	inf
-40	5	1	1.163	86.31m	943.8m	1.163	1.426	50m	inf
-40	5	0.9	1.254	86.28m	1.035	1.254	1.517	50m	inf

Figure: Vds margin of M12

Biasing of the circuit

vds_margin7

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	269.9m	12.89m	235.2m	269.9m	306.4m	50m	inf
27	5.5	1	269.9m	12.89m	235.2m	269.9m	306.4m	50m	inf
27	5.5	0.9	269.9m	12.88m	235.2m	269.9m	306.4m	50m	inf
27	3.3	1.4	271.6m	12.83m	237.2m	271.6m	307.3m	50m	inf
27	3.3	1	271.5m	12.83m	237.2m	271.5m	307.3m	50m	inf
27	3.3	0.9	271.5m	12.82m	237.1m	271.5m	307.3m	50m	inf
27	2.97	1.4	271.1m	12.82m	236.7m	271m	306.8m	50m	inf
27	2.97	1	271m	12.82m	236.7m	271m	306.7m	50m	inf
27	2.97	0.9	271m	12.82m	236.6m	271m	306.7m	50m	inf
27	5	1.4	271.3m	12.87m	236.7m	271.3m	307.6m	50m	inf
27	5	1	271.3m	12.87m	236.7m	271.3m	307.6m	50m	inf
27	5	0.9	271.2m	12.87m	236.7m	271.2m	307.5m	50m	inf
150	5.5	1.4	171m	12.98m	136.6m	171m	207.1m	50m	inf
150	5.5	1	171m	12.98m	136.5m	171m	207.1m	50m	inf
150	5.5	0.9	171m	12.98m	136.5m	171m	207m	50m	inf
150	3.3	1.4	175.5m	12.89m	141.4m	175.5m	210.6m	50m	inf
150	3.3	1	175.4m	12.89m	141.3m	175.4m	210.5m	50m	inf
150	3.3	0.9	175.4m	12.89m	141.3m	175.4m	210.5m	50m	inf
150	2.97	1.4	175m	12.88m	140.9m	174.9m	210m	50m	inf
150	2.97	1	174.9m	12.88m	140.8m	174.9m	209.9m	50m	inf
150	2.97	0.9	174.9m	12.88m	140.8m	174.9m	209.9m	50m	inf
150	5	1.4	173.6m	12.96m	139.2m	173.6m	209.4m	50m	inf
150	5	1	173.5m	12.96m	139.1m	173.5m	209.3m	50m	inf
150	5	0.9	173.5m	12.96m	139.1m	173.5m	209.3m	50m	inf
-40	5.5	1.4	325.1m	12.83m	290.4m	325.1m	361.9m	50m	inf
-40	5.5	1	325.1m	12.83m	290.4m	325.1m	361.9m	50m	inf
-40	5.5	0.9	325m	12.82m	290.4m	325m	361.8m	50m	inf
-40	3.3	1.4	325.7m	12.79m	291.3m	325.7m	361.8m	50m	inf
-40	3.3	1	325.7m	12.79m	291.2m	325.6m	361.8m	50m	inf
-40	3.3	0.9	325.6m	12.78m	291.2m	325.6m	361.7m	50m	inf
-40	2.97	1.4	325.2m	12.78m	290.8m	325.2m	361.3m	50m	inf
-40	2.97	1	325.2m	12.78m	290.8m	325.1m	361.3m	50m	inf
-40	2.97	0.9	325.1m	12.78m	290.8m	325.1m	361.2m	50m	inf
-40	5	1.4	326m	12.82m	291.4m	326m	362.6m	50m	inf
-40	5	1	325.9m	12.82m	291.4m	325.9m	362.6m	50m	inf
-40	5	0.9	325.9m	12.81m	291.4m	325.9m	362.5m	50m	inf

Figure: Vds margin of M10

vds_margin8

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	268.6m	13.2m	233.2m	268.6m	305.7m	50m	inf
27	5.5	1	269.3m	13.2m	233.8m	269.3m	306.4m	50m	inf
27	5.5	0.9	269.4m	13.2m	234m	269.4m	306.5m	50m	inf
27	3.3	1.4	268.8m	13.13m	233.7m	268.8m	305.3m	50m	inf
27	3.3	1	270.3m	13.14m	235.1m	270.3m	306.7m	50m	inf
27	3.3	0.9	270.6m	13.14m	235.4m	270.6m	307m	50m	inf
27	2.97	1.4	267.5m	13.11m	232.4m	267.5m	303.9m	50m	inf
27	2.97	1	269.5m	13.14m	234.3m	269.5m	305.9m	50m	inf
27	2.97	0.9	269.8m	13.14m	234.7m	269.8m	306.2m	50m	inf
27	5	1.4	269.9m	13.19m	234.6m	269.9m	306.8m	50m	inf
27	5	1	270.6m	13.19m	235.3m	270.6m	307.5m	50m	inf
27	5	0.9	270.8m	13.19m	235.4m	270.8m	307.6m	50m	inf
150	5.5	1.4	169.4m	13.29m	134m	169.4m	206m	50m	inf
150	5.5	1	170.2m	13.29m	134.8m	170.2m	206.8m	50m	inf
150	5.5	0.9	170.4m	13.29m	135m	170.4m	207m	50m	inf
150	3.3	1.4	172.3m	13.19m	137.2m	172.3m	208m	50m	inf
150	3.3	1	174m	13.2m	138.9m	174m	209.7m	50m	inf
150	3.3	0.9	174.3m	13.2m	139.3m	174.3m	210m	50m	inf
150	2.97	1.4	171m	13.17m	136m	171m	206.7m	50m	inf
150	2.97	1	173.1m	13.19m	138.1m	173.1m	208.8m	50m	inf
150	2.97	0.9	173.6m	13.19m	138.5m	173.6m	209.2m	50m	inf
150	5	1.4	171.9m	13.27m	136.6m	171.9m	208.2m	50m	inf
150	5	1	172.7m	13.27m	137.4m	172.7m	209m	50m	inf
150	5	0.9	172.9m	13.27m	137.6m	172.9m	209.2m	50m	inf
-40	5.5	1.4	324m	13.14m	288.8m	324m	361.4m	50m	inf
-40	5.5	1	324.5m	13.14m	289.3m	324.5m	362m	50m	inf
-40	5.5	0.9	324.6m	13.14m	289.4m	324.7m	362m	50m	inf
-40	3.3	1.4	323.2m	13.09m	288.2m	323.2m	360.1m	50m	inf
-40	3.3	1	324.5m	13.1m	289.5m	324.5m	361.4m	50m	inf
-40	3.3	0.9	324.8m	13.1m	289.8m	324.8m	361.6m	50m	inf
-40	2.97	1.4	321.8m	13.06m	286.8m	321.8m	358.7m	50m	inf
-40	2.97	1	323.8m	13.09m	288.7m	323.8m	360.6m	50m	inf
-40	2.97	0.9	324.1m	13.09m	289.1m	324.1m	360.9m	50m	inf
-40	5	1.4	324.8m	13.13m	289.6m	324.8m	362.1m	50m	inf
-40	5	1	325.4m	13.13m	290.2m	325.4m	362.6m	50m	inf
-40	5	0.9	325.5m	13.13m	290.3m	325.5m	362.7m	50m	inf

Figure: Vds margin of M11

Biasing of the circuit

vds_margin6

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	243.3m	18.2m	196.9m	243.3m	300.6m	50m	inf
27	5.5	1	242.9m	18.19m	196.6m	242.9m	300.3m	50m	inf
27	5.5	0.9	242.8m	18.19m	196.5m	242.8m	300.2m	50m	inf
27	3.3	1.4	237.2m	18.17m	191.1m	237.3m	294.5m	50m	inf
27	3.3	1	236.9m	18.17m	190.8m	236.9m	294.2m	50m	inf
27	3.3	0.9	236.8m	18.17m	190.7m	236.9m	294.2m	50m	inf
27	2.97	1.4	236.9m	18.17m	190.8m	237m	294.2m	50m	inf
27	2.97	1	236.6m	18.17m	190.5m	236.6m	293.9m	50m	inf
27	2.97	0.9	236.5m	18.17m	190.4m	236.6m	293.9m	50m	inf
27	5	1.4	240.7m	18.19m	194.4m	240.7m	298m	50m	inf
27	5	1	240.4m	18.18m	194.1m	240.4m	297.7m	50m	inf
27	5	0.9	240.3m	18.18m	194m	240.3m	297.6m	50m	inf
150	5.5	1.4	162.4m	17.65m	116.8m	162.4m	217.7m	50m	inf
150	5.5	1	162m	17.65m	116.4m	162m	217.4m	50m	inf
150	5.5	0.9	161.9m	17.64m	116.3m	161.9m	217.2m	50m	inf
150	3.3	1.4	154.5m	17.61m	109.2m	154.5m	209.8m	50m	inf
150	3.3	1	154.2m	17.61m	108.9m	154.2m	209.4m	50m	inf
150	3.3	0.9	154.1m	17.61m	108.8m	154.1m	209.3m	50m	inf
150	2.97	1.4	154.2m	17.61m	108.9m	154.2m	209.4m	50m	inf
150	2.97	1	153.8m	17.61m	108.5m	153.8m	209.1m	50m	inf
150	2.97	0.9	153.7m	17.61m	108.4m	153.8m	209m	50m	inf
150	5	1.4	159.1m	17.63m	113.6m	159.1m	214.4m	50m	inf
150	5	1	158.7m	17.63m	113.2m	158.8m	214.1m	50m	inf
150	5	0.9	158.6m	17.63m	113.1m	158.6m	214m	50m	inf
-40	5.5	1.4	287.6m	18.81m	240.5m	287.6m	346.8m	50m	inf
-40	5.5	1	287.3m	18.81m	240.2m	287.3m	346.5m	50m	inf
-40	5.5	0.9	287.2m	18.81m	240.1m	287.2m	346.4m	50m	inf
-40	3.3	1.4	282.6m	18.8m	235.7m	282.6m	341.7m	50m	inf
-40	3.3	1	282.3m	18.8m	235.4m	282.3m	341.4m	50m	inf
-40	3.3	0.9	282.2m	18.8m	235.3m	282.2m	341.4m	50m	inf
-40	2.97	1.4	282.3m	18.8m	235.4m	282.4m	341.4m	50m	inf
-40	2.97	1	282m	18.79m	235.1m	282m	341.1m	50m	inf
-40	2.97	0.9	281.9m	18.8m	235m	282m	341.1m	50m	inf
-40	5	1.4	285.4m	18.8m	238.4m	285.4m	344.6m	50m	inf
-40	5	1	285.1m	18.8m	238m	285.1m	344.3m	50m	inf
-40	5	0.9	285m	18.81m	238m	285.1m	344.2m	50m	inf

Figure: Vds margin of M1

vds_margin5

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	242.5m	16.39m	200.2m	242.5m	291.3m	50m	inf
27	5.5	1	242.5m	16.39m	200.2m	242.5m	291.3m	50m	inf
27	5.5	0.9	242.5m	16.4m	200.2m	242.5m	291.4m	50m	inf
27	3.3	1.4	236.5m	16.35m	194.3m	236.5m	285.2m	50m	inf
27	3.3	1	236.5m	16.35m	194.3m	236.5m	285.2m	50m	inf
27	3.3	0.9	236.5m	16.36m	194.3m	236.5m	285.2m	50m	inf
27	2.97	1.4	236.2m	16.35m	194m	236.2m	284.9m	50m	inf
27	2.97	1	236.2m	16.35m	194m	236.2m	284.9m	50m	inf
27	2.97	0.9	236.2m	16.35m	194m	236.2m	284.9m	50m	inf
27	5	1.4	239.9m	16.38m	197.6m	239.9m	288.7m	50m	inf
27	5	1	239.9m	16.38m	197.6m	239.9m	288.7m	50m	inf
27	5	0.9	239.9m	16.38m	197.6m	240m	288.7m	50m	inf
150	5.5	1.4	161.5m	16.45m	119.3m	161.5m	210.5m	50m	inf
150	5.5	1	161.5m	16.45m	119.3m	161.5m	210.5m	50m	inf
150	5.5	0.9	161.5m	16.45m	119.3m	161.5m	210.6m	50m	inf
150	3.3	1.4	153.6m	16.39m	111.6m	153.6m	202.5m	50m	inf
150	3.3	1	153.6m	16.39m	111.6m	153.6m	202.5m	50m	inf
150	3.3	0.9	153.6m	16.4m	111.6m	153.6m	202.6m	50m	inf
150	2.97	1.4	153.2m	16.39m	111.3m	153.3m	202.2m	50m	inf
150	2.97	1	153.3m	16.39m	111.3m	153.3m	202.2m	50m	inf
150	2.97	0.9	153.3m	16.39m	111.3m	153.3m	202.2m	50m	inf
150	5	1.4	158.2m	16.42m	116.1m	158.2m	207.2m	50m	inf
150	5	1	158.2m	16.42m	116.1m	158.2m	207.2m	50m	inf
150	5	0.9	158.2m	16.43m	116.1m	158.2m	207.2m	50m	inf
-40	5.5	1.4	286.9m	16.37m	244.4m	286.9m	335.6m	50m	inf
-40	5.5	1	286.9m	16.37m	244.4m	286.9m	335.6m	50m	inf
-40	5.5	0.9	286.9m	16.38m	244.4m	286.9m	335.6m	50m	inf
-40	3.3	1.4	281.9m	16.34m	239.5m	281.9m	330.5m	50m	inf
-40	3.3	1	281.9m	16.34m	239.5m	281.9m	330.5m	50m	inf
-40	3.3	0.9	281.9m	16.35m	239.5m	281.9m	330.5m	50m	inf
-40	2.97	1.4	281.6m	16.34m	239.2m	281.6m	330.2m	50m	inf
-40	2.97	1	281.6m	16.34m	239.2m	281.6m	330.2m	50m	inf
-40	2.97	0.9	281.6m	16.35m	239.2m	281.6m	330.3m	50m	inf
-40	5	1.4	284.7m	16.36m	242.2m	284.7m	333.4m	50m	inf
-40	5	1	284.7m	16.36m	242.2m	284.7m	333.4m	50m	inf
-40	5	0.9	284.7m	16.37m	242.2m	284.7m	333.4m	50m	inf

Figure: Vds margin of M0

Biasing of the circuit

vgs_margin2

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	95.99m	3.837m	84.42m	95.96m	107.8m	50m	inf
27	5.5	1	95.75m	3.891m	84.11m	95.72m	107.7m	50m	inf
27	5.5	0.9	95.81m	3.899m	84.1m	95.79m	107.8m	50m	inf
27	3.3	1.4	96m	3.707m	85.48m	95.96m	107.3m	50m	inf
27	3.3	1	95.76m	3.765m	85.17m	95.73m	107.1m	50m	inf
27	3.3	0.9	95.81m	3.772m	85.16m	95.79m	107.3m	50m	inf
27	2.97	1.4	96m	3.701m	85.53m	95.96m	107.3m	50m	inf
27	2.97	1	95.76m	3.759m	85.22m	95.73m	107.1m	50m	inf
27	2.97	0.9	95.81m	3.767m	85.21m	95.79m	107.2m	50m	inf
27	5	1.4	96m	3.778m	84.88m	95.96m	107.6m	50m	inf
27	5	1	95.75m	3.834m	84.57m	95.73m	107.4m	50m	inf
27	5	0.9	95.81m	3.841m	84.56m	95.79m	107.6m	50m	inf
150	5.5	1.4	130.3m	4.461m	117.3m	130.2m	144.2m	50m	inf
150	5.5	1	130.3m	4.558m	117.4m	130.3m	144.2m	50m	inf
150	5.5	0.9	130.5m	4.576m	117.5m	130.5m	144.5m	50m	inf
150	3.3	1.4	130.3m	4.334m	118.4m	130.2m	143.6m	50m	inf
150	3.3	1	130.3m	4.437m	118.1m	130.3m	143.6m	50m	inf
150	3.3	0.9	130.5m	4.456m	118.2m	130.5m	143.8m	50m	inf
150	2.97	1.4	130.3m	4.33m	118.5m	130.2m	143.5m	50m	inf
150	2.97	1	130.3m	4.433m	118.1m	130.3m	143.6m	50m	inf
150	2.97	0.9	130.5m	4.451m	118.1m	130.5m	143.8m	50m	inf
150	5	1.4	130.3m	4.404m	117.8m	130.2m	143.9m	50m	inf
150	5	1	130.3m	4.504m	117.9m	130.3m	144m	50m	inf
150	5	0.9	130.5m	4.522m	118m	130.5m	144.2m	50m	inf
-40	5.5	1.4	78.63m	3.498m	67.9m	78.61m	89.2m	50m	inf
-40	5.5	1	78.1m	3.532m	67.26m	78.09m	88.78m	50m	inf
-40	5.5	0.9	78.05m	3.534m	67.11m	78.05m	88.8m	50m	inf
-40	3.3	1.4	78.64m	3.365m	68.92m	78.61m	88.71m	50m	inf
-40	3.3	1	78.11m	3.402m	68.28m	78.09m	88.3m	50m	inf
-40	3.3	0.9	78.06m	3.404m	68.13m	78.05m	88.31m	50m	inf
-40	2.97	1.4	78.64m	3.359m	68.97m	78.61m	88.69m	50m	inf
-40	2.97	1	78.11m	3.396m	68.33m	78.09m	88.28m	50m	inf
-40	2.97	0.9	78.06m	3.397m	68.18m	78.05m	88.29m	50m	inf
-40	5	1.4	78.64m	3.437m	68.35m	78.61m	88.98m	50m	inf
-40	5	1	78.11m	3.473m	67.71m	78.09m	88.57m	50m	inf
-40	5	0.9	78.05m	3.475m	67.56m	78.05m	88.58m	50m	inf

Figure: Vgs margin of M12

vgs_margin1

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	96m	3.999m	83.05m	95.98m	108.4m	50m	inf
27	5.5	1	95.74m	4.061m	82.52m	95.73m	108.2m	50m	inf
27	5.5	0.9	95.8m	4.07m	82.54m	95.8m	108.3m	50m	inf
27	3.3	1.4	96.01m	3.851m	83.26m	95.98m	107.5m	50m	inf
27	3.3	1	95.75m	3.915m	82.72m	95.74m	107.3m	50m	inf
27	3.3	0.9	95.81m	3.924m	82.74m	95.8m	107.4m	50m	inf
27	2.97	1.4	96.01m	3.844m	83.27m	95.99m	107.4m	50m	inf
27	2.97	1	95.75m	3.908m	82.73m	95.74m	107.3m	50m	inf
27	2.97	0.9	95.81m	3.917m	82.75m	95.8m	107.4m	50m	inf
27	5	1.4	96m	3.932m	83.14m	95.98m	108m	50m	inf
27	5	1	95.75m	3.995m	82.61m	95.73m	107.8m	50m	inf
27	5	0.9	95.8m	4.004m	82.63m	95.8m	107.9m	50m	inf
150	5.5	1.4	130.3m	4.65m	115.3m	130.3m	143.9m	50m	inf
150	5.5	1	130.3m	4.755m	114.8m	130.3m	143.8m	50m	inf
150	5.5	0.9	130.5m	4.774m	114.8m	130.5m	144m	50m	inf
150	3.3	1.4	130.3m	4.496m	115.6m	130.3m	142.9m	50m	inf
150	3.3	1	130.3m	4.604m	115m	130.3m	142.8m	50m	inf
150	3.3	0.9	130.5m	4.624m	115.1m	130.5m	143m	50m	inf
150	2.97	1.4	130.3m	4.491m	115.6m	130.3m	142.8m	50m	inf
150	2.97	1	130.4m	4.599m	115m	130.3m	142.8m	50m	inf
150	2.97	0.9	130.5m	4.618m	115.1m	130.5m	143m	50m	inf
150	5	1.4	130.3m	4.582m	115.4m	130.3m	143.5m	50m	inf
150	5	1	130.3m	4.688m	114.9m	130.3m	143.4m	50m	inf
150	5	0.9	130.5m	4.708m	115m	130.5m	143.6m	50m	inf
-40	5.5	1.4	78.63m	3.642m	66.98m	78.62m	90.24m	50m	inf
-40	5.5	1	78.09m	3.683m	66.27m	78.09m	89.86m	50m	inf
-40	5.5	0.9	78.04m	3.686m	66.21m	78.05m	89.88m	50m	inf
-40	3.3	1.4	78.64m	3.496m	67.15m	78.63m	89.44m	50m	inf
-40	3.3	1	78.1m	3.538m	66.45m	78.1m	89.05m	50m	inf
-40	3.3	0.9	78.05m	3.541m	66.39m	78.05m	89.07m	50m	inf
-40	2.97	1.4	78.64m	3.489m	67.16m	78.63m	89.4m	50m	inf
-40	2.97	1	78.1m	3.531m	66.46m	78.1m	89m	50m	inf
-40	2.97	0.9	78.05m	3.534m	66.39m	78.05m	89.03m	50m	inf
-40	5	1.4	78.63m	3.576m	67.05m	78.62m	89.88m	50m	inf
-40	5	1	78.1m	3.617m	66.35m	78.09m	89.5m	50m	inf
-40	5	0.9	78.04m	3.621m	66.29m	78.05m	89.52m	50m	inf

Figure: Vgs margin of M13

Biasing of the circuit

vgs_margin4

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	5.5	1	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	5.5	0.9	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	3.3	1.4	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	3.3	1	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	3.3	0.9	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	2.97	1.4	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	2.97	1	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	2.97	0.9	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	5	1.4	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	5	1	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
27	5	0.9	73.87m	2.995m	63.8m	73.84m	81.51m	50m	inf
150	5.5	1.4	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	5.5	1	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	5.5	0.9	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	3.3	1.4	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	3.3	1	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	3.3	0.9	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	2.97	1.4	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	2.97	1	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	2.97	0.9	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	5	1.4	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	5	1	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
150	5	0.9	104.6m	3.64m	92.73m	104.5m	113.4m	50m	inf
-40	5.5	1.4	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	5.5	1	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	5.5	0.9	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	3.3	1.4	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	3.3	1	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	3.3	0.9	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	2.97	1.4	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	2.97	1	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	2.97	0.9	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	5	1.4	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	5	1	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf
-40	5	0.9	58.64m	2.65m	49.58m	58.62m	65.59m	50m	inf

Figure: Vgs margin of M2

vgs_margin18

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	11.83	471m	10.45	11.83	13.02	50m	inf
27	5.5	1	11.62	470.5m	10.25	11.62	12.81	50m	inf
27	5.5	0.9	11.56	470.3m	10.19	11.56	12.75	50m	inf
27	3.3	1.4	11.84	470.9m	10.46	11.84	13.03	50m	inf
27	3.3	1	11.64	470.4m	10.26	11.64	12.83	50m	inf
27	3.3	0.9	11.58	470.3m	10.2	11.58	12.77	50m	inf
27	2.97	1.4	11.84	470.9m	10.46	11.84	13.03	50m	inf
27	2.97	1	11.64	470.4m	10.26	11.64	12.83	50m	inf
27	2.97	0.9	11.58	470.3m	10.2	11.58	12.77	50m	inf
27	5	1.4	11.83	471m	10.45	11.83	13.02	50m	inf
27	5	1	11.63	470.5m	10.25	11.63	12.82	50m	inf
27	5	0.9	11.57	470.3m	10.19	11.57	12.76	50m	inf
150	5.5	1.4	9.377	472.1m	7.999	9.377	10.57	50m	inf
150	5.5	1	9.12	471.4m	7.744	9.12	10.31	50m	inf
150	5.5	0.9	9.046	471.2m	7.67	9.045	10.24	50m	inf
150	3.3	1.4	9.39	472m	8.012	9.39	10.59	50m	inf
150	3.3	1	9.136	471.4m	7.759	9.136	10.33	50m	inf
150	3.3	0.9	9.062	471.2m	7.686	9.062	10.26	50m	inf
150	2.97	1.4	9.391	472m	8.013	9.391	10.59	50m	inf
150	2.97	1	9.137	471.4m	7.761	9.137	10.33	50m	inf
150	2.97	0.9	9.063	471.2m	7.687	9.063	10.26	50m	inf
150	5	1.4	9.381	472.1m	8.003	9.381	10.58	50m	inf
150	5	1	9.126	471.4m	7.749	9.126	10.32	50m	inf
150	5	0.9	9.051	471.2m	7.675	9.051	10.25	50m	inf
-40	5.5	1.4	13.22	470.4m	11.84	13.22	14.41	50m	inf
-40	5.5	1	13.05	470m	11.67	13.05	14.23	50m	inf
-40	5.5	0.9	13	469.9m	11.62	13	14.18	50m	inf
-40	3.3	1.4	13.23	470.4m	11.86	13.23	14.42	50m	inf
-40	3.3	1	13.06	470m	11.69	13.06	14.25	50m	inf
-40	3.3	0.9	13.01	469.8m	11.64	13.01	14.2	50m	inf
-40	2.97	1.4	13.23	470.4m	11.86	13.23	14.42	50m	inf
-40	2.97	1	13.06	470m	11.69	13.06	14.25	50m	inf
-40	2.97	0.9	13.01	469.8m	11.64	13.01	14.2	50m	inf
-40	5	1.4	13.22	470.4m	11.85	13.22	14.41	50m	inf
-40	5	1	13.05	470m	11.68	13.05	14.24	50m	inf
-40	5	0.9	13	469.9m	11.63	13	14.19	50m	inf

Figure: Vgs margin of M17<0:8>

Biasing of the circuit

vgs_margin5

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	214.2m	6.653m	195.2m	214.1m	228.7m	50m	inf
27	5.5	1	214.2m	6.652m	195.3m	214.2m	228.8m	50m	inf
27	5.5	0.9	214.3m	6.656m	195.3m	214.2m	228.8m	50m	inf
27	3.3	1.4	179.8m	6.596m	162.6m	179.8m	194.9m	50m	inf
27	3.3	1	179.9m	6.595m	162.7m	179.8m	195m	50m	inf
27	3.3	0.9	179.9m	6.598m	162.7m	179.9m	195m	50m	inf
27	2.97	1.4	178.2m	6.611m	160.9m	178.2m	193.4m	50m	inf
27	2.97	1	178.2m	6.609m	160.9m	178.2m	193.4m	50m	inf
27	2.97	0.9	178.3m	6.613m	161m	178.3m	193.4m	50m	inf
27	5	1.4	199.2m	6.559m	181m	199.1m	213.6m	50m	inf
27	5	1	199.2m	6.558m	181m	199.2m	213.6m	50m	inf
27	5	0.9	199.3m	6.562m	181.1m	199.2m	213.6m	50m	inf
150	5.5	1.4	290.4m	7.522m	268.8m	290.3m	307.2m	50m	inf
150	5.5	1	290.5m	7.521m	268.8m	290.4m	307.2m	50m	inf
150	5.5	0.9	290.5m	7.524m	268.8m	290.4m	307.2m	50m	inf
150	3.3	1.4	239.5m	7.296m	220m	239.4m	256.2m	50m	inf
150	3.3	1	239.6m	7.294m	220m	239.5m	256.2m	50m	inf
150	3.3	0.9	239.6m	7.297m	220.1m	239.5m	256.2m	50m	inf
150	2.97	1.4	237.4m	7.314m	217.8m	237.4m	254.2m	50m	inf
150	2.97	1	237.5m	7.313m	217.9m	237.4m	254.2m	50m	inf
150	2.97	0.9	237.5m	7.316m	217.9m	237.5m	254.2m	50m	inf
150	5	1.4	268.7m	7.329m	248.2m	268.6m	284.7m	50m	inf
150	5	1	268.8m	7.327m	248.3m	268.7m	284.8m	50m	inf
150	5	0.9	268.8m	7.33m	248.3m	268.7m	284.8m	50m	inf
-40	5.5	1.4	173.5m	6.268m	155.9m	173.5m	187m	50m	inf
-40	5.5	1	173.6m	6.267m	156m	173.5m	187.1m	50m	inf
-40	5.5	0.9	173.6m	6.271m	156m	173.5m	187.1m	50m	inf
-40	3.3	1.4	147m	6.264m	130.6m	147m	161.2m	50m	inf
-40	3.3	1	147.1m	6.263m	130.7m	147m	161.3m	50m	inf
-40	3.3	0.9	147.1m	6.265m	130.7m	147.1m	161.3m	50m	inf
-40	2.97	1.4	145.6m	6.276m	129.2m	145.6m	159.9m	50m	inf
-40	2.97	1	145.7m	6.275m	129.2m	145.7m	159.9m	50m	inf
-40	2.97	0.9	145.7m	6.278m	129.2m	145.7m	159.9m	50m	inf
-40	5	1.4	161.8m	6.211m	144.8m	161.8m	175.5m	50m	inf
-40	5	1	161.9m	6.211m	144.9m	161.8m	175.5m	50m	inf
-40	5	0.9	161.9m	6.214m	144.9m	161.9m	175.5m	50m	inf

Figure: Vgs margin of M0

vgs_margin6

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	214.2m	6.29m	196m	214.1m	230.2m	50m	inf
27	5.5	1	214.2m	6.29m	196m	214.2m	230.3m	50m	inf
27	5.5	0.9	214.3m	6.294m	196m	214.2m	230.4m	50m	inf
27	3.3	1.4	179.8m	6.194m	161.6m	179.8m	194.3m	50m	inf
27	3.3	1	179.9m	6.193m	161.7m	179.8m	194.4m	50m	inf
27	3.3	0.9	179.9m	6.197m	161.7m	179.9m	194.4m	50m	inf
27	2.97	1.4	178.2m	6.21m	159.9m	178.2m	192.8m	50m	inf
27	2.97	1	178.2m	6.209m	160m	178.2m	192.8m	50m	inf
27	2.97	0.9	178.3m	6.213m	160m	178.3m	192.8m	50m	inf
27	5	1.4	199.2m	6.179m	181.1m	199.1m	214.4m	50m	inf
27	5	1	199.2m	6.178m	181.2m	199.2m	214.5m	50m	inf
27	5	0.9	199.3m	6.182m	181.2m	199.2m	214.6m	50m	inf
150	5.5	1.4	290.4m	7.214m	269.4m	290.3m	308.8m	50m	inf
150	5.5	1	290.5m	7.213m	269.4m	290.4m	308.9m	50m	inf
150	5.5	0.9	290.5m	7.216m	269.5m	290.4m	309m	50m	inf
150	3.3	1.4	239.5m	6.935m	218.8m	239.4m	255.6m	50m	inf
150	3.3	1	239.6m	6.934m	218.9m	239.5m	255.6m	50m	inf
150	3.3	0.9	239.6m	6.937m	218.9m	239.5m	255.7m	50m	inf
150	2.97	1.4	237.4m	6.955m	216.7m	237.4m	253.6m	50m	inf
150	2.97	1	237.5m	6.953m	216.8m	237.4m	253.6m	50m	inf
150	2.97	0.9	237.5m	6.957m	216.8m	237.5m	253.7m	50m	inf
150	5	1.4	268.7m	7m	248m	268.6m	286m	50m	inf
150	5	1	268.8m	6.999m	248.1m	268.7m	286.1m	50m	inf
150	5	0.9	268.8m	7.002m	248.1m	268.7m	286.2m	50m	inf
-40	5.5	1.4	173.5m	5.873m	156.8m	173.5m	188.5m	50m	inf
-40	5.5	1	173.6m	5.873m	156.9m	173.5m	188.5m	50m	inf
-40	5.5	0.9	173.6m	5.877m	156.9m	173.5m	188.7m	50m	inf
-40	3.3	1.4	147m	5.837m	130.2m	147m	160.6m	50m	inf
-40	3.3	1	147.1m	5.836m	130.3m	147m	160.6m	50m	inf
-40	3.3	0.9	147.1m	5.84m	130.3m	147.1m	160.8m	50m	inf
-40	2.97	1.4	145.6m	5.851m	128.8m	145.6m	159.3m	50m	inf
-40	2.97	1	145.7m	5.85m	128.8m	145.7m	159.3m	50m	inf
-40	2.97	0.9	145.7m	5.853m	128.8m	145.7m	159.4m	50m	inf
-40	5	1.4	161.8m	5.802m	145.2m	161.8m	176.2m	50m	inf
-40	5	1	161.9m	5.801m	145.3m	161.8m	176.2m	50m	inf
-40	5	0.9	161.9m	5.806m	145.3m	161.9m	176.4m	50m	inf

Figure: Vgs margin of M1

Biasing of the circuit

vgs_margin7

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	86.29m	3.309m	76.87m	86.29m	95.34m	50m	inf
27	5.5	1	86.29m	3.309m	76.87m	86.29m	95.34m	50m	inf
27	5.5	0.9	86.29m	3.309m	76.87m	86.29m	95.34m	50m	inf
27	3.3	1.4	72.59m	3.294m	62.63m	72.6m	81.42m	50m	inf
27	3.3	1	72.59m	3.294m	62.63m	72.6m	81.42m	50m	inf
27	3.3	0.9	72.59m	3.294m	62.63m	72.6m	81.42m	50m	inf
27	2.97	1.4	71.96m	3.296m	61.98m	71.96m	80.83m	50m	inf
27	2.97	1	71.96m	3.296m	61.98m	71.96m	80.83m	50m	inf
27	2.97	0.9	71.96m	3.296m	61.98m	71.96m	80.83m	50m	inf
27	5	1.4	80.23m	3.279m	70.67m	80.23m	89.12m	50m	inf
27	5	1	80.23m	3.279m	70.67m	80.23m	89.12m	50m	inf
27	5	0.9	80.23m	3.279m	70.67m	80.23m	89.12m	50m	inf
150	5.5	1.4	103.9m	3.509m	94.19m	103.9m	113.7m	50m	inf
150	5.5	1	103.9m	3.509m	94.19m	103.9m	113.7m	50m	inf
150	5.5	0.9	103.9m	3.509m	94.19m	103.9m	113.7m	50m	inf
150	3.3	1.4	85.34m	3.49m	74.83m	85.34m	94.88m	50m	inf
150	3.3	1	85.34m	3.49m	74.83m	85.34m	94.88m	50m	inf
150	3.3	0.9	85.34m	3.49m	74.83m	85.34m	94.88m	50m	inf
150	2.97	1.4	84.61m	3.495m	74.06m	84.61m	94.19m	50m	inf
150	2.97	1	84.61m	3.495m	74.06m	84.61m	94.19m	50m	inf
150	2.97	0.9	84.61m	3.495m	74.06m	84.61m	94.19m	50m	inf
150	5	1.4	95.89m	3.469m	85.96m	95.88m	105.5m	50m	inf
150	5	1	95.89m	3.469m	85.96m	95.88m	105.5m	50m	inf
150	5	0.9	95.89m	3.469m	85.96m	95.88m	105.5m	50m	inf
-40	5.5	1.4	76.62m	3.18m	67.57m	76.62m	85.2m	50m	inf
-40	5.5	1	76.62m	3.18m	67.57m	76.62m	85.2m	50m	inf
-40	5.5	0.9	76.62m	3.18m	67.57m	76.62m	85.2m	50m	inf
-40	3.3	1.4	65.57m	3.166m	56.1m	65.58m	73.97m	50m	inf
-40	3.3	1	65.57m	3.166m	56.1m	65.58m	73.97m	50m	inf
-40	3.3	0.9	65.57m	3.166m	56.1m	65.58m	73.97m	50m	inf
-40	2.97	1.4	65.01m	3.167m	55.53m	65.02m	73.44m	50m	inf
-40	2.97	1	65.01m	3.167m	55.53m	65.02m	73.44m	50m	inf
-40	2.97	0.9	65.01m	3.167m	55.53m	65.02m	73.44m	50m	inf
-40	5	1.4	71.69m	3.155m	62.53m	71.69m	80.13m	50m	inf
-40	5	1	71.69m	3.155m	62.53m	71.69m	80.13m	50m	inf
-40	5	0.9	71.69m	3.155m	62.53m	71.69m	80.13m	50m	inf

Figure: Vgs margin of M10

vgs_margin8

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	86.29m	3.225m	78.25m	86.29m	95.11m	50m	inf
27	5.5	1	86.29m	3.225m	78.25m	86.29m	95.11m	50m	inf
27	5.5	0.9	86.29m	3.225m	78.25m	86.29m	95.11m	50m	inf
27	3.3	1.4	72.59m	3.208m	64.01m	72.6m	81.19m	50m	inf
27	3.3	1	72.59m	3.208m	64.01m	72.6m	81.19m	50m	inf
27	3.3	0.9	72.59m	3.208m	64.01m	72.6m	81.19m	50m	inf
27	2.97	1.4	71.96m	3.21m	63.36m	71.96m	80.6m	50m	inf
27	2.97	1	71.96m	3.21m	63.36m	71.96m	80.6m	50m	inf
27	2.97	0.9	71.96m	3.21m	63.36m	71.96m	80.6m	50m	inf
27	5	1.4	80.23m	3.194m	72.05m	80.23m	88.89m	50m	inf
27	5	1	80.23m	3.194m	72.05m	80.23m	88.89m	50m	inf
27	5	0.9	80.23m	3.194m	72.05m	80.23m	88.89m	50m	inf
150	5.5	1.4	103.9m	3.428m	95.53m	103.9m	113.5m	50m	inf
150	5.5	1	103.9m	3.428m	95.53m	103.9m	113.5m	50m	inf
150	5.5	0.9	103.9m	3.428m	95.53m	103.9m	113.5m	50m	inf
150	3.3	1.4	85.34m	3.407m	76.17m	85.34m	94.74m	50m	inf
150	3.3	1	85.34m	3.407m	76.17m	85.34m	94.74m	50m	inf
150	3.3	0.9	85.34m	3.407m	76.17m	85.34m	94.74m	50m	inf
150	2.97	1.4	84.61m	3.413m	75.4m	84.61m	94.03m	50m	inf
150	2.97	1	84.61m	3.413m	75.4m	84.61m	94.03m	50m	inf
150	2.97	0.9	84.61m	3.413m	75.4m	84.61m	94.03m	50m	inf
150	5	1.4	95.89m	3.387m	87.3m	95.88m	105.3m	50m	inf
150	5	1	95.89m	3.387m	87.3m	95.88m	105.3m	50m	inf
150	5	0.9	95.89m	3.387m	87.3m	95.88m	105.3m	50m	inf
-40	5.5	1.4	76.62m	3.098m	68.96m	76.62m	84.96m	50m	inf
-40	5.5	1	76.62m	3.098m	68.96m	76.62m	84.96m	50m	inf
-40	5.5	0.9	76.62m	3.098m	68.96m	76.62m	84.96m	50m	inf
-40	3.3	1.4	65.57m	3.082m	57.49m	65.58m	73.73m	50m	inf
-40	3.3	1	65.57m	3.082m	57.49m	65.58m	73.73m	50m	inf
-40	3.3	0.9	65.57m	3.082m	57.49m	65.58m	73.73m	50m	inf
-40	2.97	1.4	65.01m	3.084m	56.92m	65.02m	73.21m	50m	inf
-40	2.97	1	65.01m	3.084m	56.92m	65.02m	73.21m	50m	inf
-40	2.97	0.9	65.01m	3.084m	56.92m	65.02m	73.21m	50m	inf
-40	5	1.4	71.69m	3.073m	63.92m	71.69m	79.9m	50m	inf
-40	5	1	71.69m	3.073m	63.92m	71.69m	79.9m	50m	inf
-40	5	0.9	71.69m	3.073m	63.92m	71.69m	79.9m	50m	inf

Figure: Vgs margin of M11

Gain of the circuit

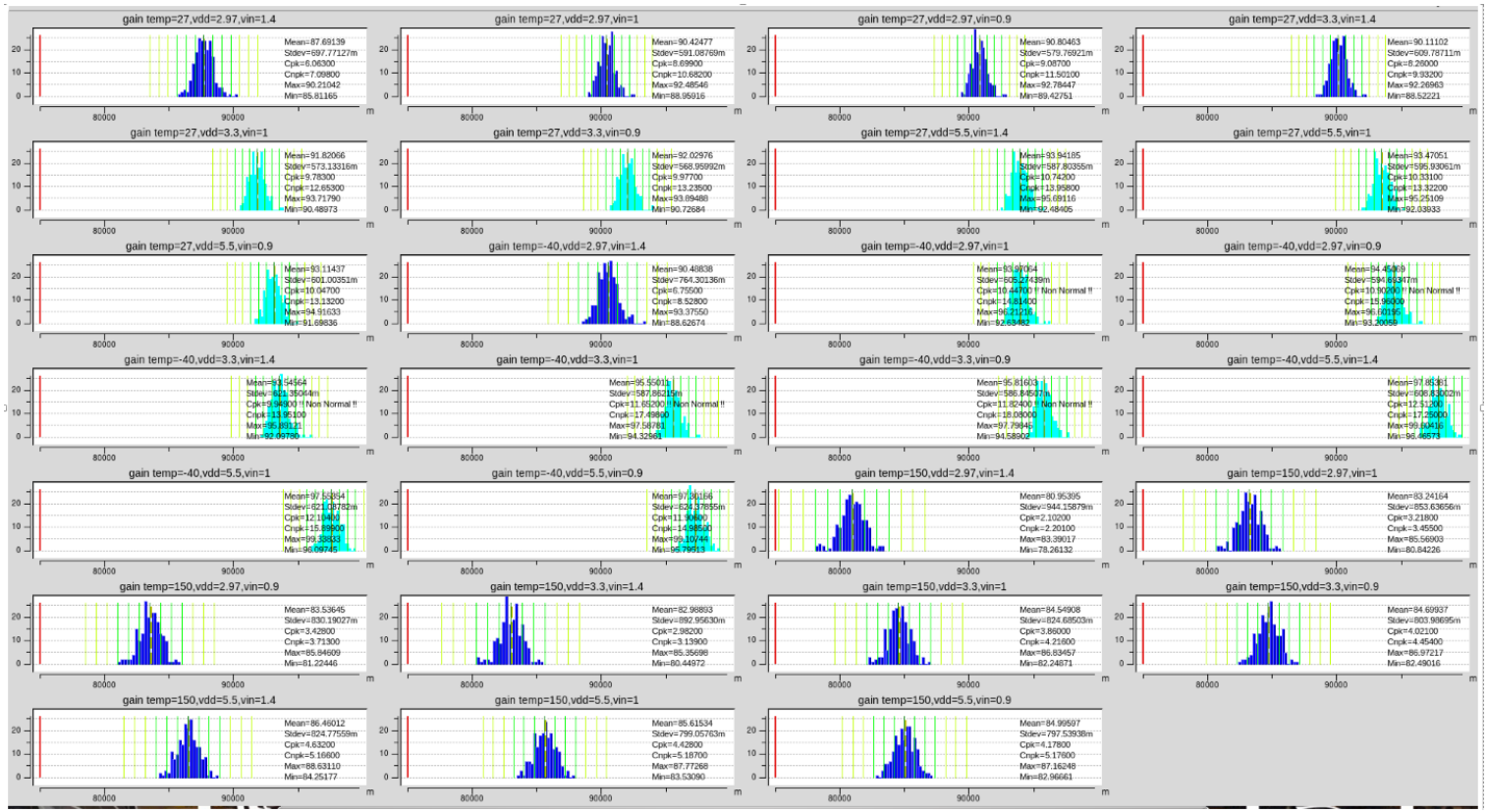

Figure: Loop gain at different conditions

Phase Margin

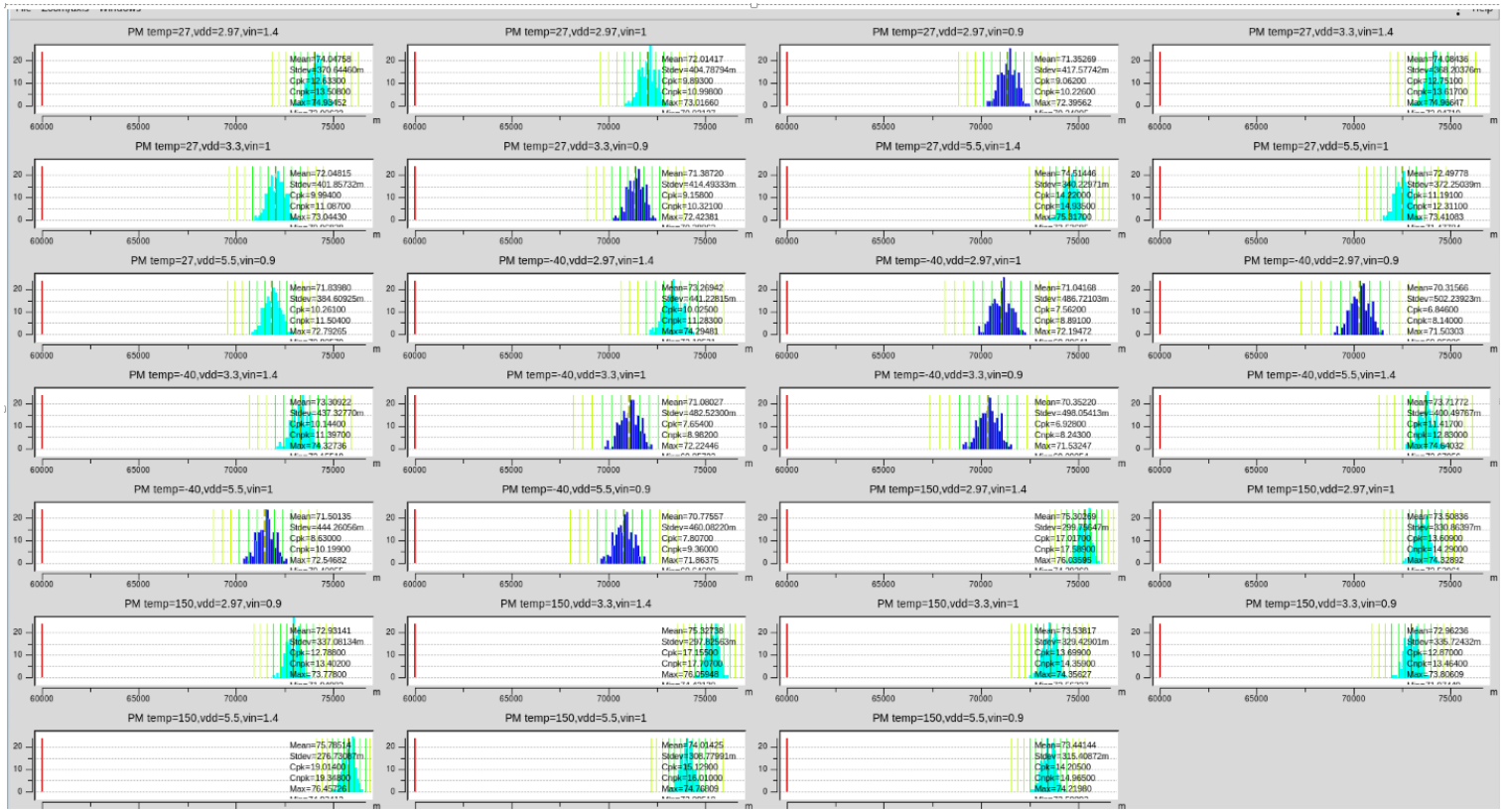

Figure: Phase Margin at different conditions

Test bench for CMRR and PSRR

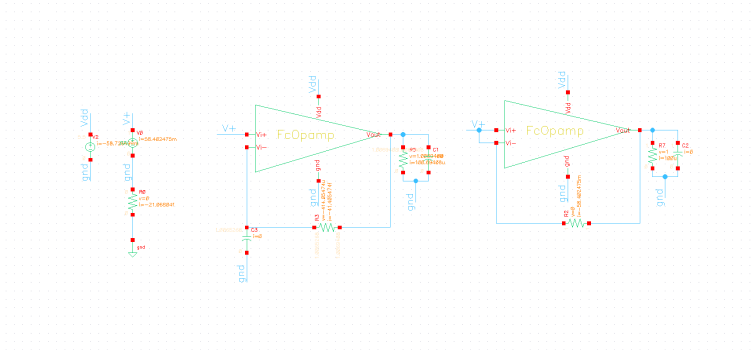

Figure: Testbench for CMRR

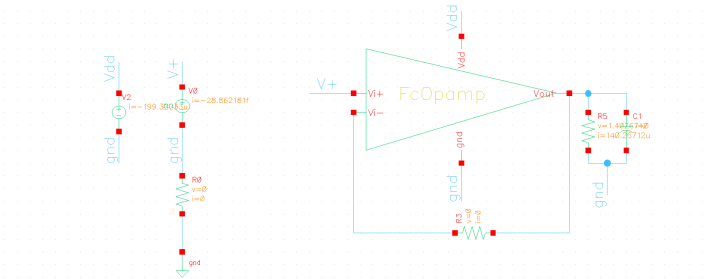

Figure: Testbench for PSRR

CM gain and CMRR

CMgain

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
150	5.5	1.4	65.11	14.2	12.49	56.59	121.3	50	inf
150	5.5	1	63.94	12.15	8.289	57.1	93.45	50	inf
150	5.5	0.9	59.44	12.24	5.387	55.64	95.58	50	inf
150	3.3	1.4	65.77	12.97	34.9	54.7	110.1	50	inf
150	3.3	1	64.11	10.46	30.38	55.57	94.69	50	inf
150	3.3	0.9	59.67	10.95	24.64	54.52	97.78	50	inf
150	2.97	1.4	65.79	12.92	35.91	55.36	108.3	50	inf
150	2.97	1	64.15	10.44	31.59	56.2	95.36	50	inf
150	2.97	0.9	59.69	10.89	25.97	55	98.42	50	inf
27	5.5	1.4	68.64	13.03	17.91	49.9	103.3	50	inf
27	5.5	1	58.18	11.38	601m	50.97	93.63	50	inf
27	5.5	0.9	54.36	11.73	7.107	50.35	112.9	50	inf
27	3.3	1.4	68.82	12.51	35.04	49.04	103.1	50	inf
27	3.3	1	58.19	10.5	25.36	50.22	96.21	50	inf
27	3.3	0.9	53.95	11.01	18.76	49.6	96.61	50	inf
27	2.97	1.4	68.82	12.48	36.33	49.76	103.5	50	inf
27	2.97	1	58.2	10.48	27.01	50.94	97.56	50	inf
27	2.97	0.9	53.94	10.95	20.37	50.17	95.83	50	inf
-40	5.5	1.4	65.26	11.64	21.3	47.01	99.98	50	inf
-40	5.5	1	57.03	10.89	19.99	48.21	92.06	50	inf
-40	5.5	0.9	52.26	11.63	17.83	47.59	100.8	50	inf
-40	3.3	1.4	65.11	11.6	33.49	46.68	100	50	inf
-40	3.3	1	56.79	10.86	25.15	47.95	90.42	50	inf
-40	3.3	0.9	51.5	11.23	16.09	47.16	86.23	50	inf
-40	2.97	1.4	65.12	11.59	34.6	47.48	100.8	50	inf
-40	2.97	1	56.8	10.83	26.55	48.74	91.04	50	inf
-40	2.97	0.9	51.49	11.17	17.64	47.76	85.85	50	inf

Figure: CM gain at different conditions(absolute)

CMRR

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
150	5.5	1.4	151.9	16.23	88.51	143.1	201.4	80	inf
150	5.5	1	148	13.65	91.87	142.8	187.8	80	inf
150	5.5	0.9	142.9	13.48	86.37	140.7	193.8	80	inf
150	3.3	1.4	148.4	15.12	85.9	137.8	181.6	80	inf
150	3.3	1	146.9	12.81	100.8	140.2	193.4	80	inf
150	3.3	0.9	142.3	12.1	94.5	139.3	175	80	inf
150	2.97	1.4	146.6	14.69	84.59	136.4	179.2	80	inf
150	2.97	1	145.7	12.45	100.5	139.5	191.8	80	inf
150	2.97	0.9	141.2	11.75	94.33	138.6	173.2	80	inf
27	5.5	1.4	160.9	15.39	96.92	143.9	196.5	80	inf
27	5.5	1	151	15.1	82.91	144.5	196.8	80	inf
27	5.5	0.9	146.2	14.98	71.56	143.5	201.6	80	inf
27	3.3	1.4	157.8	12.23	127.3	139.2	189.4	80	inf
27	3.3	1	150	12.26	106.6	142.1	193	80	inf
27	3.3	0.9	145.4	12	101.8	141.7	192	80	inf
27	2.97	1.4	155.4	12.13	124.4	137.5	186.4	80	inf
27	2.97	1	148.7	12.11	113.2	141.4	191.1	80	inf
27	2.97	0.9	144.2	11.84	109.4	141	189.9	80	inf
-40	5.5	1.4	162.2	15.42	85.79	144.9	205.3	80	inf
-40	5.5	1	154.1	14.29	85.08	145.8	202.3	80	inf
-40	5.5	0.9	148.6	14.5	84.29	144.9	210.1	80	inf
-40	3.3	1.4	158.5	13	119.8	140.3	191.8	80	inf
-40	3.3	1	152.5	13.16	105.8	143.5	215.9	80	inf
-40	3.3	0.9	146.9	12.89	95.96	143	193.9	80	inf
-40	2.97	1.4	155.5	12.89	121.4	138	190.2	80	inf
-40	2.97	1	151.1	12.91	113.3	142.7	215.1	80	inf
-40	2.97	0.9	145.6	12.43	108.4	142.2	191.8	80	inf

Figure: CMRR at different conditions

Minimum CMRR = 71.56dB at 27^o, 5.5V

PSRR of the circuit

psrr

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
150	5.5	1.4	-69.65	9.513	-103.4	-98.92	-53.04	-inf	inf
150	5.5	1	-69.72	9.591	-101	-105.2	-53.12	-inf	inf
150	5.5	0.9	-69.76	9.711	-104	-110.5	-53.13	-inf	inf
150	3.3	1.4	-86.84	9.36	-121.9	-93.65	-71.76	-inf	inf
150	3.3	1	-87.67	10.09	-129.6	-101.7	-71.37	-inf	inf
150	3.3	0.9	-87.65	9.885	-128.2	-104.4	-71.3	-inf	inf
150	2.97	1.4	-86.2	8.611	-119.9	-89.68	-71.71	-inf	inf
150	2.97	1	-87.73	9.908	-128.4	-98.41	-71.83	-inf	inf
150	2.97	0.9	-88.05	10.56	-138.2	-101.2	-71.73	-inf	inf
150	4	1.4	-81.95	10.03	-119.7	-101.1	-65.45	-inf	inf
150	4	1	-82.18	10.76	-141.6	-108.1	-65.39	-inf	inf
150	4	0.9	-82.09	10.36	-129	-110.3	-65.38	-inf	inf
27	5.5	1.4	-70.58	10.36	-126.9	-109.2	-53.8	-inf	inf
27	5.5	1	-70.54	10.07	-118.7	-114.7	-53.82	-inf	inf
27	5.5	0.9	-70.52	9.986	-114.9	-118.7	-53.81	-inf	inf
27	3.3	1.4	-87.54	9.899	-126.9	-100.4	-71.35	-inf	inf
27	3.3	1	-87.4	9.053	-114.1	-108.9	-71.18	-inf	inf
27	3.3	0.9	-87.45	9.177	-117.1	-111.6	-71.14	-inf	inf
27	2.97	1.4	-86.65	9.198	-117	-95.59	-71.1	-inf	inf
27	2.97	1	-87.09	9.814	-142.6	-105	-70.8	-inf	inf
27	2.97	0.9	-86.93	9.048	-114.4	-107.9	-70.74	-inf	inf
27	4	1.4	-83.15	9.366	-114.2	-108.5	-66.7	-inf	inf
27	4	1	-83.68	11.32	-145.4	-115.8	-66.67	-inf	inf
27	4	0.9	-83.96	12.63	-152	-118.1	-66.66	-inf	inf
-40	5.5	1.4	-70.79	9.423	-105.8	-114.6	-54.19	-inf	inf
-40	5.5	1	-70.77	9.377	-104.6	-120	-54.19	-inf	inf
-40	5.5	0.9	-70.76	9.363	-104.3	-123.4	-54.18	-inf	inf
-40	3.3	1.4	-87.53	9.898	-129.5	-103.2	-71.17	-inf	inf
-40	3.3	1	-87.41	9.274	-123.5	-112.1	-71.03	-inf	inf
-40	3.3	0.9	-87.59	10.16	-153.7	-114.9	-71	-inf	inf
-40	2.97	1.4	-86.62	9.932	-127.4	-97.25	-70.57	-inf	inf
-40	2.97	1	-86.74	9.928	-150.6	-107.7	-70.32	-inf	inf
-40	2.97	0.9	-86.62	9.243	-119.9	-110.7	-70.28	-inf	inf
-40	4	1.4	-83.94	9.555	-126	-112.1	-67.39	-inf	inf
-40	4	1	-84.1	10.2	-134	-119.6	-67.35	-inf	inf
-40	4	0.9	-84.14	10.45	-148	-122	-67.34	-inf	inf

Figure: PSRR at different conditions

Max PSRR =-53.04dB Psrr is low at high voltages

Current supplied and the offset

current_supply

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
150	5.5	1.4	200.1u	1.078u	197.4u	200.1u	202.5u	-inf	inf
150	5.5	1	160.1u	1.077u	157.4u	160.1u	162.5u	-inf	inf
150	5.5	0.9	150.1u	1.077u	147.4u	150.1u	152.5u	-inf	inf
150	3.3	1.4	192.9u	929n	190.6u	192.9u	195.1u	-inf	inf
150	3.3	1	152.9u	927.9n	150.6u	152.9u	155u	-inf	inf
150	3.3	0.9	142.9u	927.7n	140.6u	142.9u	145u	-inf	inf
150	2.97	1.4	192.6u	922.9n	190.3u	192.6u	194.8u	-inf	inf
150	2.97	1	152.6u	921.8n	150.3u	152.6u	154.8u	-inf	inf
150	2.97	0.9	142.6u	921.7n	140.3u	142.6u	144.8u	-inf	inf
150	4	1.4	193.7u	944.1n	191.3u	193.7u	195.9u	-inf	inf
150	4	1	153.7u	943n	151.3u	153.7u	155.9u	-inf	inf
150	4	0.9	143.7u	942.8n	141.3u	143.7u	145.9u	-inf	inf
27	5.5	1.4	199u	1.296u	195.6u	199u	202.1u	-inf	inf
27	5.5	1	159u	1.296u	155.6u	159u	162.1u	-inf	inf
27	5.5	0.9	149u	1.296u	145.6u	149u	152.1u	-inf	inf
27	3.3	1.4	192.7u	1.142u	189.6u	192.6u	195.4u	-inf	inf
27	3.3	1	152.7u	1.141u	149.6u	152.6u	155.4u	-inf	inf
27	3.3	0.9	142.7u	1.141u	139.6u	142.6u	145.4u	-inf	inf
27	2.97	1.4	192.4u	1.134u	189.3u	192.4u	195u	-inf	inf
27	2.97	1	152.4u	1.133u	149.3u	152.4u	155u	-inf	inf
27	2.97	0.9	142.4u	1.133u	139.3u	142.4u	145u	-inf	inf
27	4	1.4	193.4u	1.158u	190.3u	193.4u	196.1u	-inf	inf
27	4	1	153.4u	1.158u	150.3u	153.4u	156.1u	-inf	inf
27	4	0.9	143.4u	1.157u	140.3u	143.4u	146.1u	-inf	inf
-40	5.5	1.4	198.4u	1.52u	194.2u	198.4u	202.3u	-inf	inf
-40	5.5	1	158.4u	1.52u	154.2u	158.4u	162.3u	-inf	inf
-40	5.5	0.9	148.4u	1.52u	144.2u	148.4u	152.3u	-inf	inf
-40	3.3	1.4	192.5u	1.352u	188.7u	192.5u	195.7u	-inf	inf
-40	3.3	1	152.5u	1.351u	148.7u	152.5u	155.7u	-inf	inf
-40	3.3	0.9	142.5u	1.351u	138.7u	142.5u	145.7u	-inf	inf
-40	2.97	1.4	192.2u	1.343u	188.5u	192.2u	195.4u	-inf	inf
-40	2.97	1	152.2u	1.342u	148.5u	152.2u	155.4u	-inf	inf
-40	2.97	0.9	142.2u	1.342u	138.5u	142.2u	145.4u	-inf	inf
-40	4	1.4	193.2u	1.37u	189.4u	193.2u	196.4u	-inf	inf
-40	4	1	153.2u	1.37u	149.4u	153.2u	156.4u	-inf	inf
-40	4	0.9	143.2u	1.37u	139.4u	143.2u	146.4u	-inf	inf

Figure: Current supplied at different conditions

offset

temp	vdd	vin	mean	stdev	min	typ	max	ll	ul
27	5.5	1.4	3.645u	4.88m	-12.88m	16.91u	13.68m	-inf	4m
27	5.5	1	-4.348u	4.867m	-12.86m	8.784u	13.63m	-inf	4m
27	5.5	0.9	-6.444u	4.866m	-12.86m	6.643u	13.62m	-inf	4m
27	3.3	1.4	8.623u	4.425m	-11.27m	22u	12.49m	-inf	4m
27	3.3	1	-2.451u	4.411m	-11.25m	10.85u	12.44m	-inf	4m
27	3.3	0.9	-4.933u	4.41m	-11.25m	8.345u	12.43m	-inf	4m
27	2.97	1.4	12.87u	4.404m	-11.18m	26.15u	12.44m	-inf	4m
27	2.97	1	-905n	4.39m	-11.17m	12.34u	12.38m	-inf	4m
27	2.97	0.9	-3.801u	4.389m	-11.17m	9.419u	12.38m	-inf	4m
27	5	1.4	2.765u	4.678m	-12.18m	16.04u	13.15m	-inf	4m
27	5	1	-4.809u	4.664m	-12.16m	8.347u	13.1m	-inf	4m
27	5	0.9	-6.722u	4.663m	-12.16m	6.396u	13.1m	-inf	4m
150	5.5	1.4	29.6u	5.022m	-13.18m	40.15u	14.02m	-inf	4m
150	5.5	1	10.1u	4.999m	-13.14m	20.62u	13.93m	-inf	4m
150	5.5	0.9	4.722u	4.997m	-13.14m	15.26u	13.92m	-inf	4m
150	3.3	1.4	40.3u	4.498m	-11.36m	50.59u	12.65m	-inf	4m
150	3.3	1	14.63u	4.477m	-11.33m	25.04u	12.56m	-inf	4m
150	3.3	0.9	8.785u	4.475m	-11.33m	19.23u	12.55m	-inf	4m
150	2.97	1.4	49.14u	4.478m	-11.27m	59.22u	12.6m	-inf	4m
150	2.97	1	18.01u	4.457m	-11.25m	28.32u	12.51m	-inf	4m
150	2.97	0.9	11.27u	4.455m	-11.25m	21.63u	12.5m	-inf	4m
150	5	1.4	26.67u	4.794m	-12.41m	37.16u	13.42m	-inf	4m
150	5	1	8.731u	4.772m	-12.37m	19.19u	13.34m	-inf	4m
150	5	0.9	4.092u	4.77m	-12.37m	14.56u	13.33m	-inf	4m
-40	5.5	1.4	-4.542u	4.808m	-12.72m	10.75u	13.52m	-inf	4m
-40	5.5	1	-9.57u	4.799m	-12.71m	5.617u	13.48m	-inf	4m
-40	5.5	0.9	-10.83u	4.8m	-12.72m	4.289u	13.48m	-inf	4m
-40	3.3	1.4	-1.184u	4.388m	-11.23m	14.39u	12.42m	-inf	4m
-40	3.3	1	-8.484u	4.377m	-11.22m	7.038u	12.39m	-inf	4m
-40	3.3	0.9	-10.06u	4.378m	-11.23m	5.412u	12.38m	-inf	4m
-40	2.97	1.4	2.114u	4.366m	-11.14m	17.61u	12.37m	-inf	4m
-40	2.97	1	-7.376u	4.356m	-11.14m	8.097u	12.33m	-inf	4m
-40	2.97	0.9	-9.259u	4.356m	-11.15m	6.17u	12.33m	-inf	4m
-40	5	1.4	-5.07u	4.619m	-12.07m	10.3u	13.03m	-inf	4m
-40	5	1	-9.894u	4.61m	-12.06m	5.384u	13m	-inf	4m
-40	5	0.9	-11.07u	4.61m	-12.07m	4.148u	12.99m	-inf	4m

Figure: Offset at different conditions

Maximum power dissipated =1.113mW at 150^o C,5.5V

Conclusion

- The loopgain and phase margin of the circuit are 74dB and 66° for 6σ
- The circuit operates properly in the given temperature range
- Offset is $\pm$ 12mV
- Maximum power dissipated is 1.113mW at 150° C,5.5V
- The ICMR comes around to be 0.5V
- OCMR+ is at 150,3.3V is 2.58V, at 150, 5V is 4.2V, at 27, 3.3V 2.47V,at 27, 5V 4.114V at -40, 3.3V 2.40V,at -40, 5V 4.054V for non inverting amplifier

Future works

- The standard deviation for CMRR, PSRR, and for some devices for biasing needs to be reduced for 6σ
- Offset of $\pm$14V needs to be further reduced to $\pm$4V
- ICMR is low for the design
- Work is to be done on Current sinking ability of the opamp

Thank You