EE537 Circuit Simulation Lab
Experiment 8

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AIM: Design of an inverting amplifier using a two stage OTA.

1 Design of an inverting amplifier using a two stage OTA

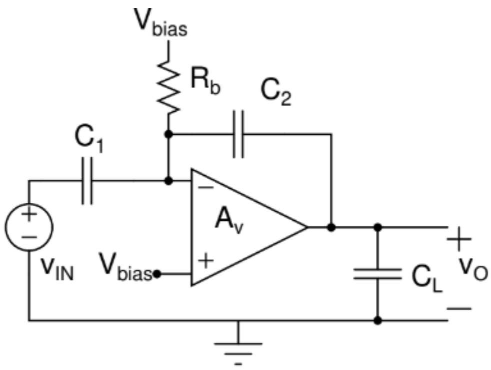

Figure 1: Inverting amplifier with capacitive voltage feedback

Spec.	Value
Midband gain	20 dB
Bandwidth	> 1 MHz
Input capacitance	1 pF
Load capacitance	10 pF
Slew rate	$\geq 10\ V/\mu s$
Gain error	0.1 %
Phase margin	$\geq 65\ °$
Operating temperature range	0 °C to 70 °C

Figure 2: Given Specifications

1.1 Implement the 2 stage using a miller compensated 2 stage OTA. Show the calculations used for all the specifications and detailed design procedure.

1.2 Mathematical analysis

1.2.1 Finding poles without miller compensation

The Circuit is as above but without the C_c. Considering the pole between stage 1 and 2 as P_1. The pole is given by

$$P_1 = \frac{-1}{(ro_{nm0}||ro_{pm3})C_{o1}} \tag{1}$$

Here C_{o1} is the internal parasitic capacitances between stage 1 and 2. P_2 is the pole considered for stage 2 i.e. the point from where the output is taken.

$$P_2 = \frac{-1}{C_l(r_{onm3}||r_{opm1})} \tag{2}$$

Here the capacitance taken is the output capacitance only. The minus sign represents the Left half Poles.

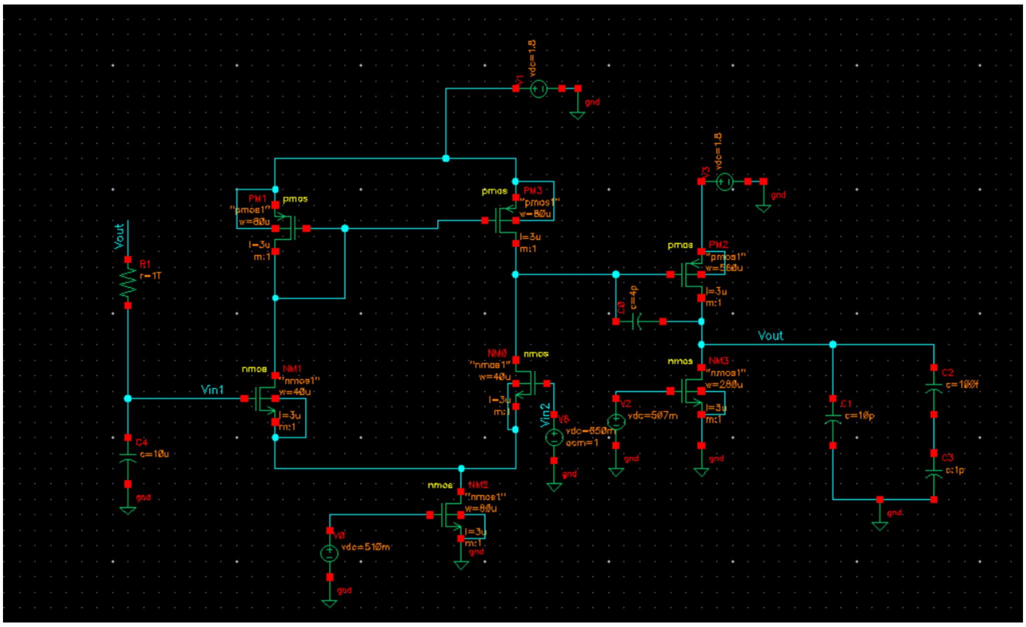

Figure 3: Ckt for calculations of Open loop gain and phase margin

1.2.2 Finding zero without miller Capacitor

The zero considered here is between the pmos PM1 and PM3. The impedance seen from the gate of PM1 is

$$\text{impedance} = \tfrac{1}{g_{pm1}} \; || \; r_{opm1}$$

$$Z = \frac{1}{(\frac{1}{g_{pm1}}||r_{0pm1})Cp} \tag{3}$$

The C_p here is the internal capacitance seen from the gate of pm1.

1.2.3 Transfer Function

The transfer function of the uncompensated OTA is given by:

$$L(s) = \frac{-A_o(1 - \frac{s}{Z})}{(1 + \frac{s}{P_1})(1 + \frac{s}{P_2})} \tag{4}$$

where A_o is the Dc gain of the circuit.

1.2.4 Finding Poles for Compensated OTA

In compensated opamp a capacitor is used to slow the response of the system and make it appear like a 1st order system with the gain of the higher order system and the stability of the 1st order system. Here the P_1 and P_2 are on the same positions as for the case of uncompensated opamp.

$$w_{P1} = \frac{1}{g_{pm2}C_c(r_{nmo}||r_{pm3})(r_{pm2}||r_{nm3})} \tag{5}$$

The above calculation is done using the Miller theorem because of which gain of the pm2 is used.

$$w_{P2} = \frac{gm_{Pm2}}{C_c + C_l} \tag{6}$$

which is equal to

$$\tfrac{gm_{pm2}}{C_l}$$

1.2.5 Finding Zeroes of the compensated Opamp

$$Z = \frac{gm_{pm2}}{C_c} \tag{7}$$

All other zeroes are neglected as they appear to be at very high frequencies and because of which there effect is minute on the response.

1.2.6 Loop Gain of compensated opamp

$$L(s) = \frac{A_o C_2}{(1 + \frac{s}{w_{P1}})(1 + \frac{s}{w_{P2}})(C_1 + C_2)} \tag{8}$$

A_o is the dc gain

1.2.7 Finding relations between different parameters

$$\text{Slew rate} = 10\text{V}/\mu \text{ s}$$

$$SR = \frac{IdthroughNM2}{C_c} = \frac{I(NM3)}{C_c + C_l + \frac{C_1 C_2}{C_1 + C_2}} \tag{9}$$

as

$$\frac{C_1 C_2}{C_1 + C_2} <<< C_c + C_l$$

we can write

$$SR = \frac{I(NM3)}{C_c + C_l} \tag{10}$$

Phase margin of the circuit is given by

$$PM = 180 - tan^{-1}(\frac{w_u}{w_{p1}}) - tan^{-1}(\frac{w_u}{w_{p2}}) - tan^{-1}(\frac{w_u}{w_z}) \tag{11}$$

Because we need the zero far away from the wu that's why the last term goes to zero. w_{p1} is very small as compared to the w_u.

$$65 = 180 - 90 - tan^{-1}(\frac{w_u}{w_{p2}}) \tag{12}$$

which gives

$$\frac{w_u}{w_{P2}} = tan25 \tag{13}$$

or $w_{P2} = 2.14 w_u$

$$w_z = 10 w_u \tag{14}$$

1.2.8 Finding Unity gain bandwidth frequency

As Af = 1 is the limiting value so we can write, where f is the feedback factor,

$$\frac{AoC_2}{(1 + \frac{s}{P_1})(C_1 + C_2)} = 1 \tag{15}$$

as jw is greater than 1 we can write

$$\frac{A_o P_1 C_2}{(C_1 + C_2) jw} = 1 \tag{16}$$

or

$$w = P_1(LoopGain) \tag{17}$$

or

$$w = \frac{g_{nm1}(rnm0||rpm3) g_{PM2}(r_{nm3}||r_{pm2}) C_2}{g_{pm2} C_c (r_{nm3}||r_{pm2})(rnm0||rpm3)(C_1 + C_2)} \tag{18}$$

$$w_u = \frac{g_{nm1} C_2}{C_c(C_1 + C_2)} \tag{19}$$

Putting the values in the above equation relating wz and wu we get

$$\frac{g_{pm2}}{C_c} = \frac{10 g_{nm1} C_2}{C_c(C_1 + C_2)} \tag{20}$$

or we get

$$g_{pm2} = g_{nm1} \tag{21}$$

Using the other equation

$$w_{P2} = 4w_u \tag{22}$$

we get

$$C_c = 0.4C_l \tag{23}$$

the feedback factor is

$$\frac{C_2}{C_1 + C_2} = 0.1 \tag{24}$$

Now using the slew rate equations (9) and (10)

$$I_{nm2} = 10^7(4)(10^{-12}) = 40\mu A \tag{25}$$

The equation 10 gives us

$$I_{NM3} = 10^7(10p + 4p) = 140\mu A \tag{26}$$

Now we have the currents so we can easily find the values of the aspect ratios For the current source below the differential amplifier we can say

$$40\mu = \frac{300\mu W(V_{GS} - V_T)^2}{2L} \tag{27}$$

Considering the overdrive voltage to be 0.1V. We get,

$$W/L = 80/3 \tag{28}$$

by intuition we can say that the nmos transistors of the differential amplifier is 40/3 Similarly we can argue that the pmos transistors present in the differential pair will have the W/L to be 80/3 because of the difference in the mobility values. Similarly we can solve for the W/L values of the Current source in the Second stage of the OTA.

$$140\mu = \frac{300\mu W(0.01)}{2L} \tag{29}$$

and we get the value to be equal to 280/3. Similar arguements as above are valid for the PMOS transistor of the 2nd satge of the OTA. Hence the W/L of Pmos is 560/3.

2 Show all the plots required to verify the achieved specifications.

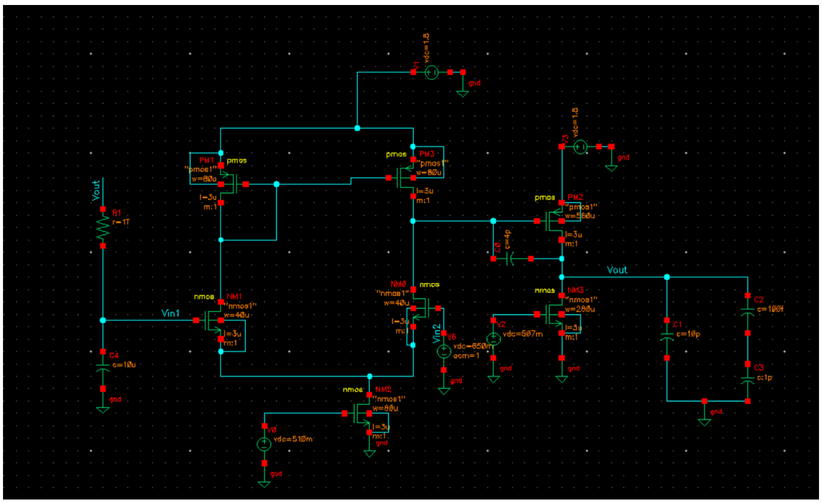

Figure 4: Ckt for calculations of Open loop gain and phase margin

The gain of the OTA observed is around 77.97dB and the phase margin is $180^o - 106.612^o = 73.388^o$

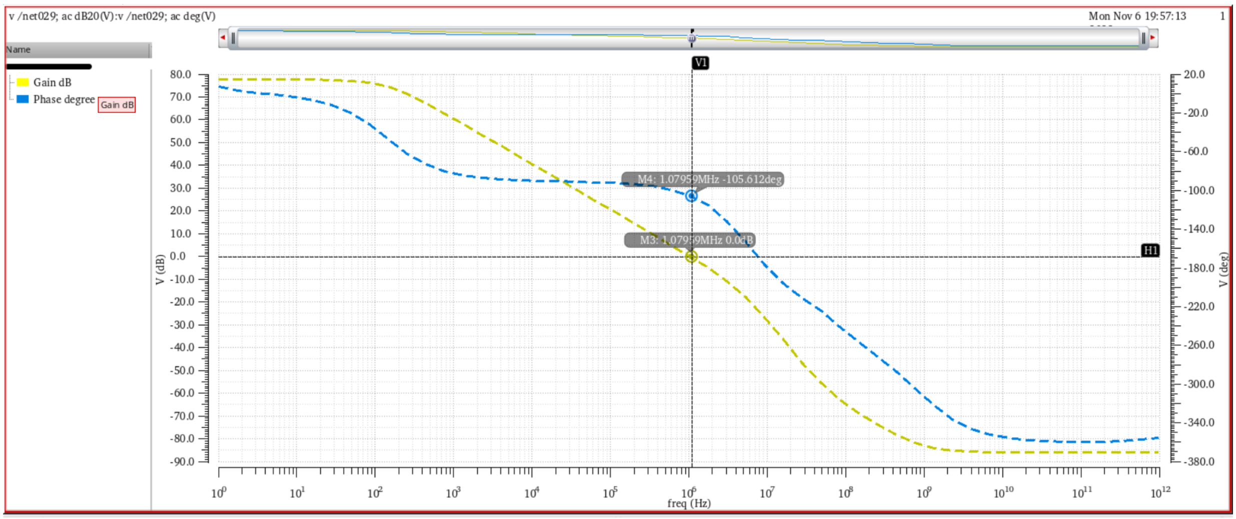

Figure 5: Plot of gain and phase margin

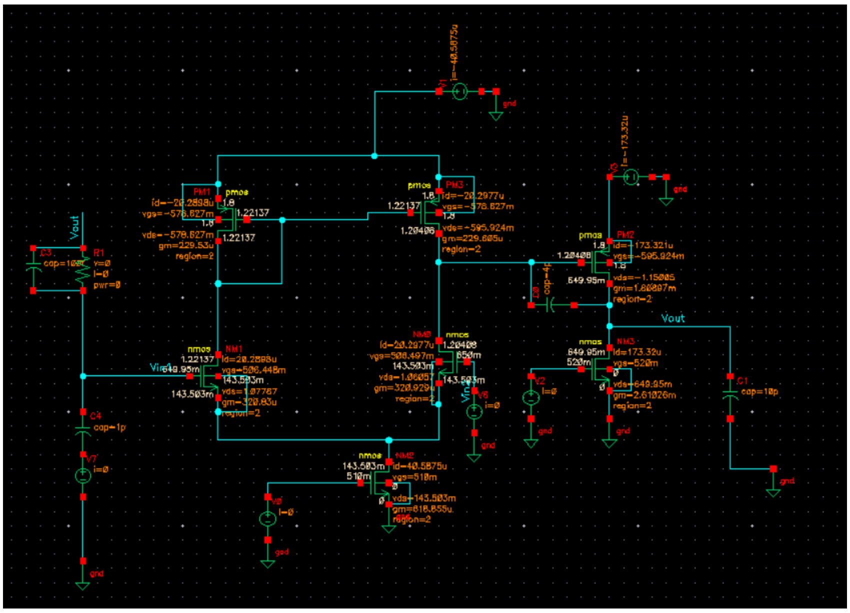

Figure 6: Extended Ckt diagram of Inverting amplifier

The closed gain of the inverting amplifier is 19.9987dB and the bandwidth is 1.01361MHz -1.6453Hz > 1MHz

$$Gainerror = \frac{A}{1+Af} - \frac{1}{f} \tag{30}$$

$$\frac{\delta A}{A} = \frac{-1}{Af(1+Af)} \approx 0.01266 percent \tag{31}$$

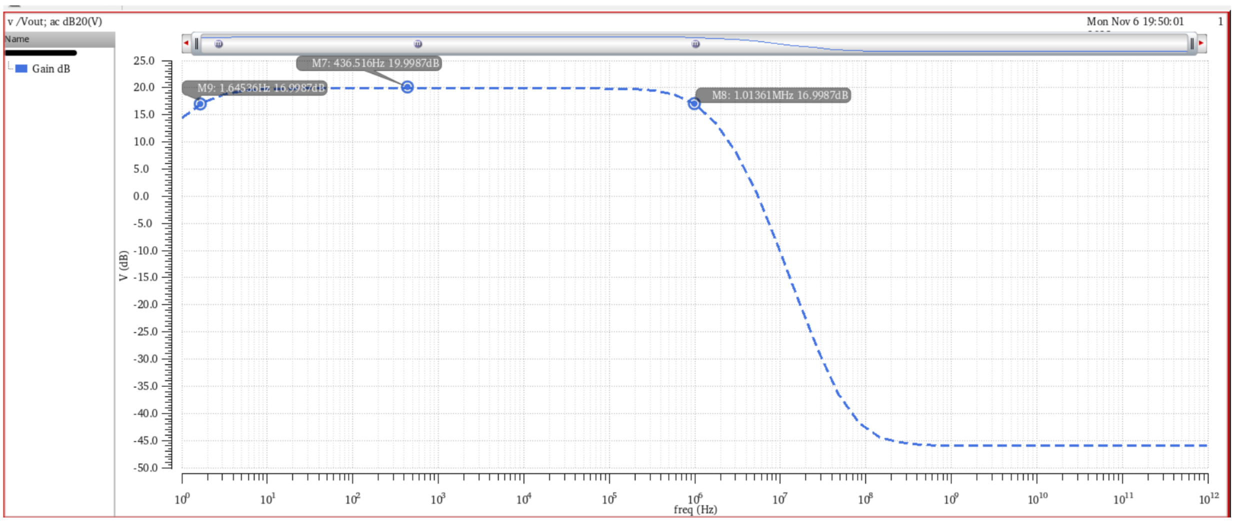

Figure 7: Gain, bandwidth plot