CS373 LM9: Introduction to Sequential VHDL   
A True Divide-By-Three 50% Duty Cycle Clock

Name(s) Brycen Martin, Ben Greenwood

|  |  |  |
| --- | --- | --- |
| **CATEGORY** | **POINTS** |  |
| DivideBy3FSM | 47 | 50 |
| TOTAL | 47 | 50 |

## Learning Goals for This Study Guide

* Gain an understand of how to create VHDL from a hardware diagram.
* Understand how to simulate and implement a true divide by 3 circuit
* Learn how to implement sequential circuits in VHDL
* Challenge critical thinking skills by implementing a new project.

## Instructions for This Project

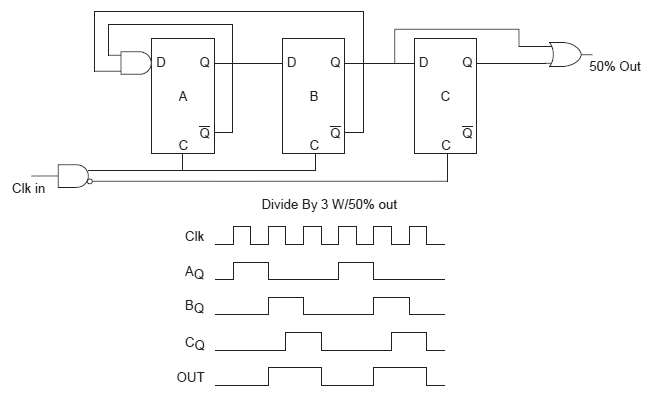
* You may work by yourself or with another person. You must **both** submit the code to whitgit along with your changes to this document. You must each answer the questions in this document by yourself, but you may consult each other on your answers.
* Answer the questions on the last page of this document and submit this document (with your answers in it) to Blackboard.
* Follow the instructions given in class to install Vivado on your machine (or use the machines in the lab – if you use lab machines which already have Vivado installed, you will need to install the board files for the BASYS 3)
* Create the majority project using the TCL/Bash scripts provided in class. You will need to configure the TCL script so that it builds your majority project.

## Divide by 3 Project

Now it’s time to put your newly learned skills to use. For this project you will design and implement the VHDL for a 50% duty cycle divide by three circuit.

## DivideByThree Project Specifications

* Pull the LM9\_Sequential\_VHDL starter project folder that contains this document from whitgit using vscode and git.
* **Complete the VHDL code in the DivideBy3FSM\_50.vhd file.**
* Run the provided testbench simulation to verify that it works correctly.
* Program the BASYS 3 Board and verify LED(1) and LED(0) are lighting up appropriately.



**reset**

## Divide by Three Circuit Design

**y**

**RESET**

**RESET**

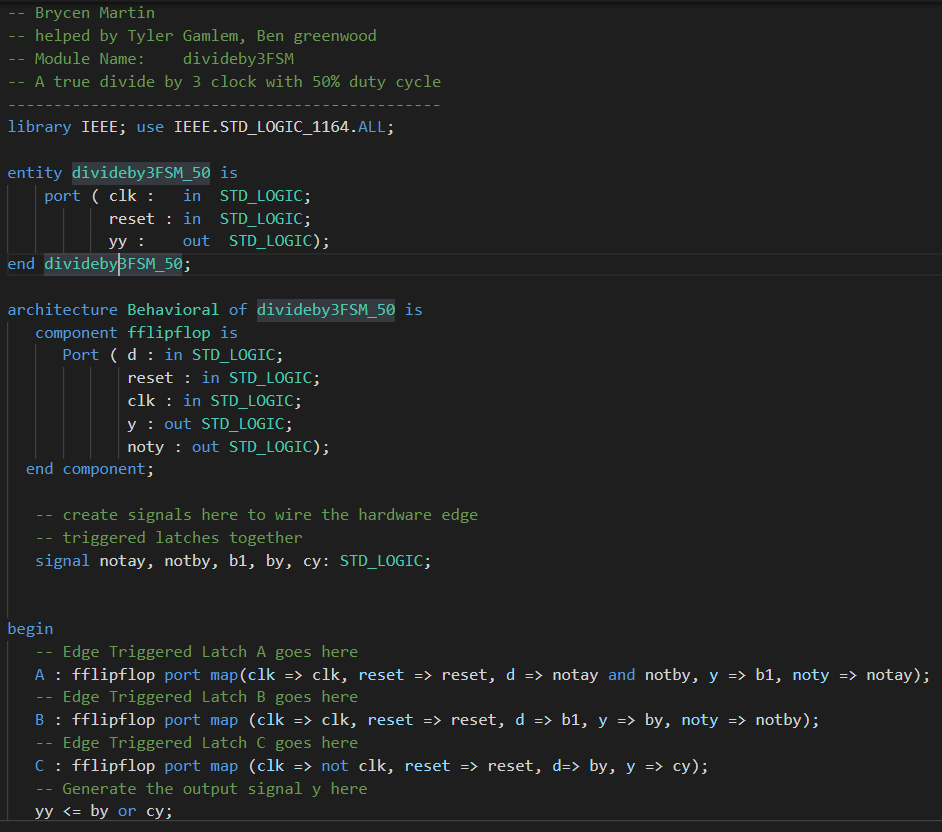
**RESET**

**VHDL Design**

Implement the circuit as shown in this diagram.

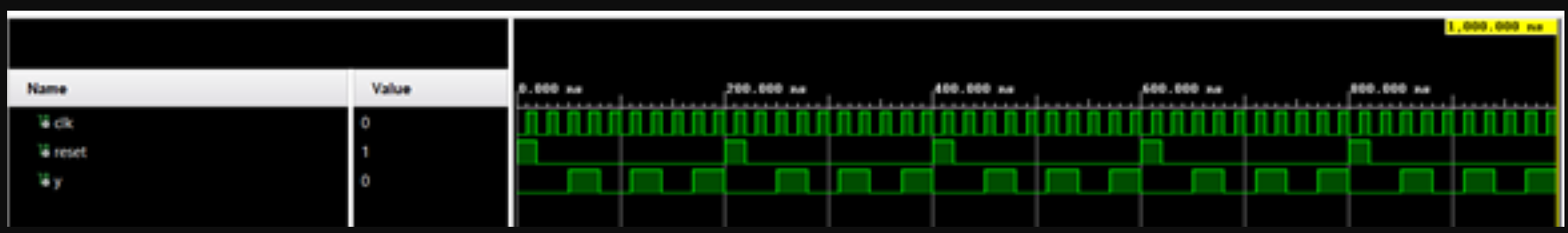
## Complete the Following:

1. Copy and paste the VHDL for your divide by 3 circuit here:

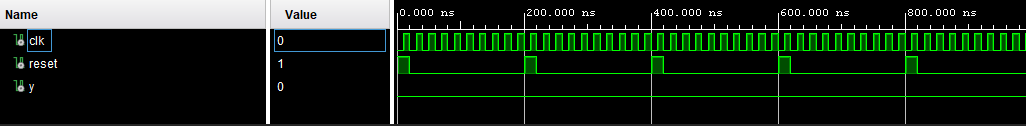


1. Paste a screen shot of your divide by 3 simulation working here:

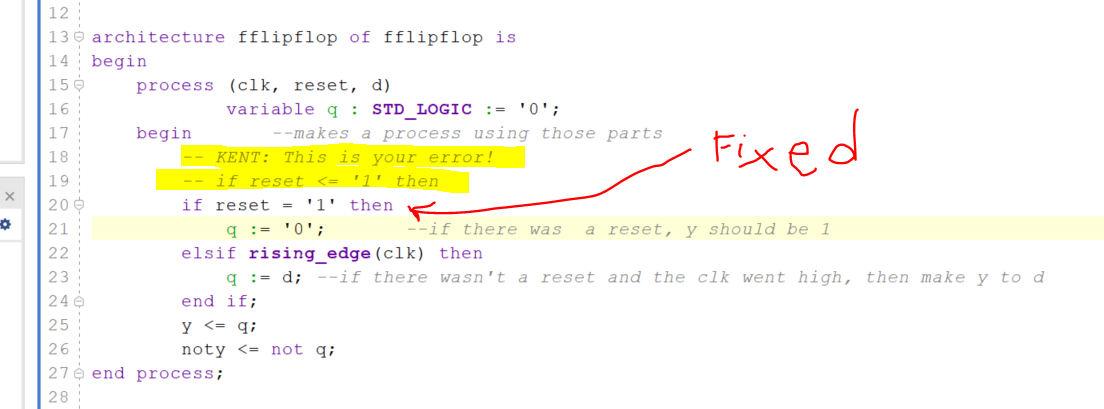
How it should look:



How mine looks:



Your error was in fflipflop you were checking for reset less than or equal to 1 !!!!!!



1. How could you modify this circuit to become a divide by 6?

Divide the source clock from divide by three to make it into a divide by 6 as the clock should have 3 high and 3 low cycles we know will happen due to it being divided by an even number

1. Explain how the main clk signal is generated that feeds this circuit. Hint: Look in the top level module file. How is the clk that connects to this circuit generated? Explain how it works here:

The clock is a 26 bit register that increments by one for each 100MHZ cycle and every 25 100MHZ cycle the clock goes high and adds 1 to the binary value of q going from ‘000’ -> ‘001’ -> ‘010 ->….