Enhanced Pulse Shape Discrimination (PSD) System For Nuclear Physics Applications

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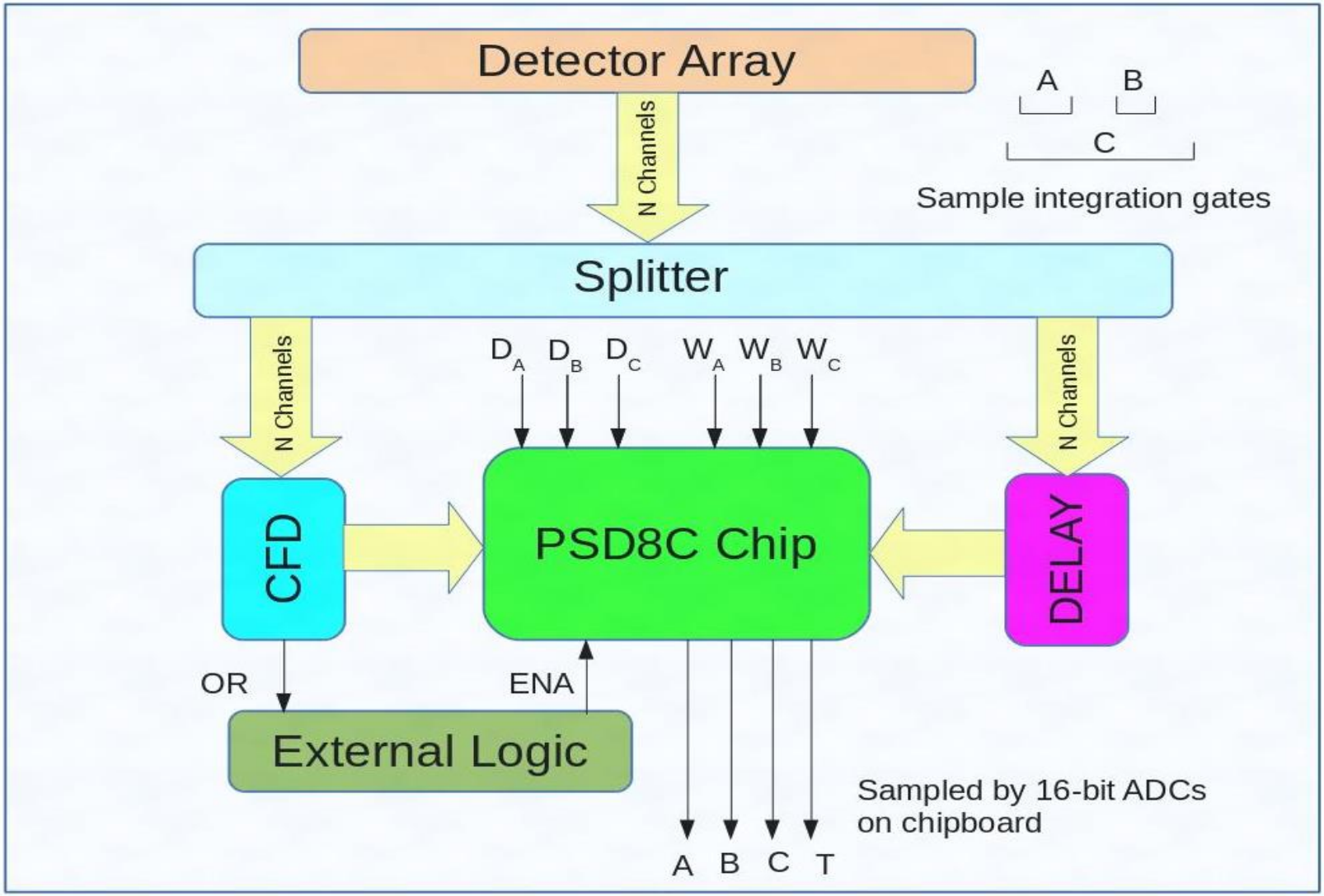
Presentation Outline

- PSD Chip and System Overview
- PSD3 Shortcomings
- PSD4 (Enter our 4th Generation IC!!!!)
- **Scheduled for fabrication … Dec. 4, 2017**
- Summary

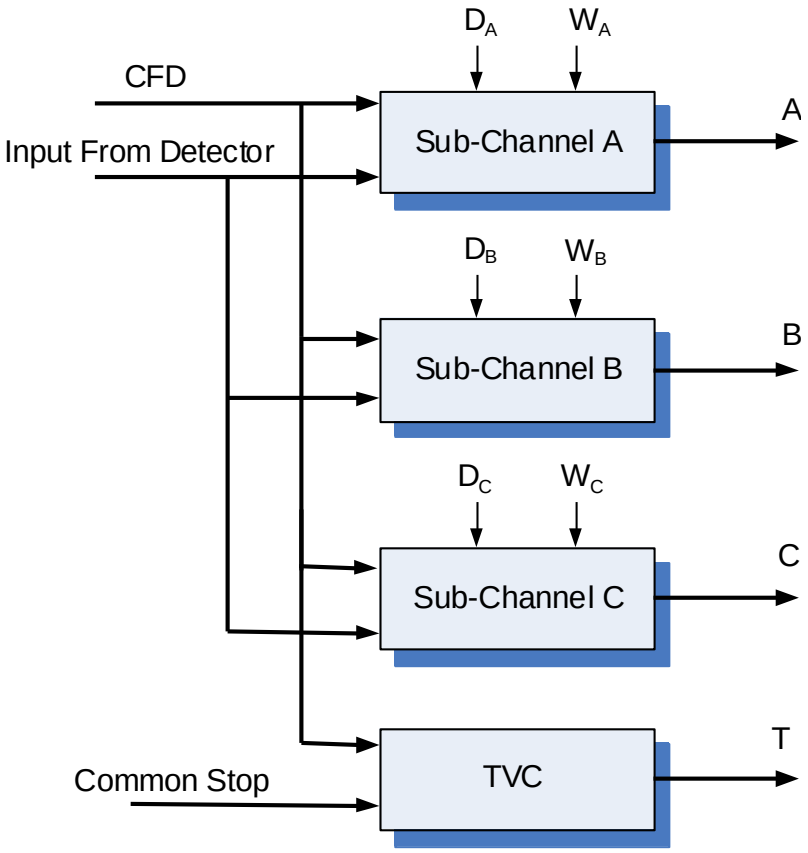
Our PSD Chip

- PSD3 (3rd Generation IC) is our current mass integrator chip (8 channels) capable of yielding particle identification from scintillators with pulse-shape discrimination.
- Nine years ago we fielded an ASIC (PSD1 i.e. 1st Generation), which when used in conjunction with external discrimination, can be used to generate the integrals from three user selected regions of the light pulse from a scintillator .
- Our chip greatly simplifies the task of creating a large array of scintillators that contain particle identification information in the pulse shape.

PSD System

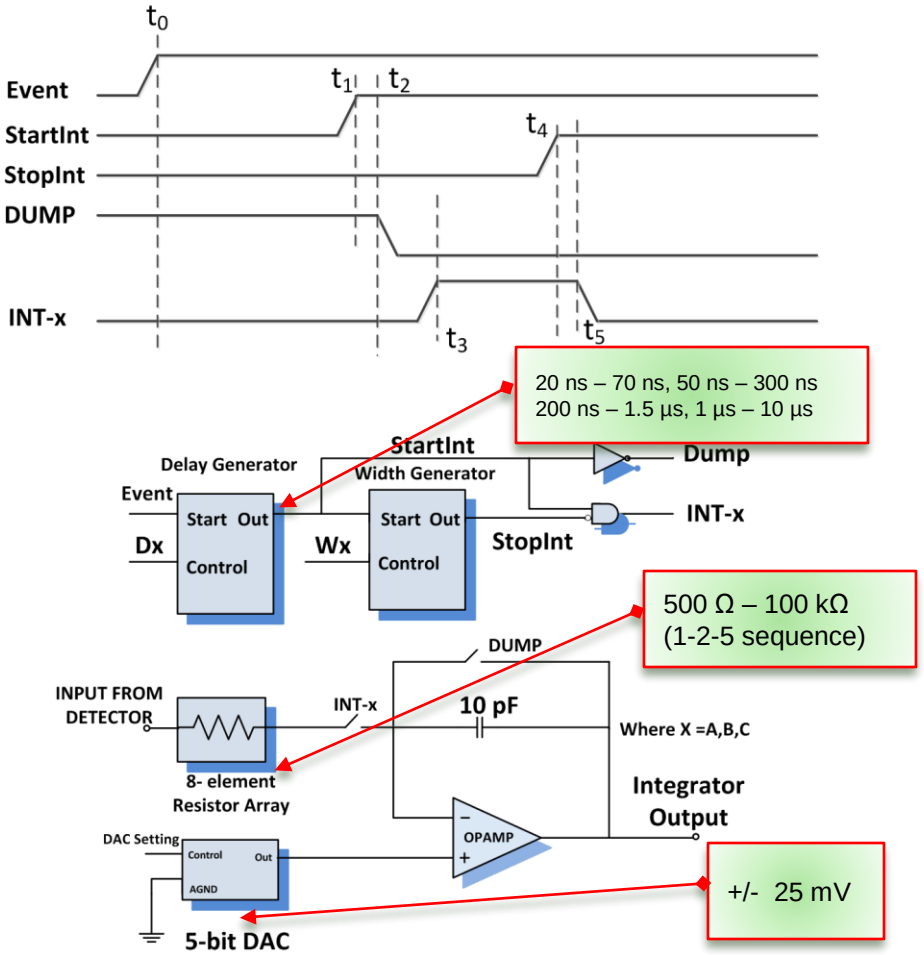

Detector Array
N Channels
A
B
C
Sample integration gates
Splitter
N Channels
D_A D_B D_C W_A W_B W_C
N Channels
CFD
PSD8C Chip
DELAY
OR
ENA
External Logic
A B C T
Sampled by 16-bit ADCs
on chipboard

PSD Chip Overview



PSD3 TVC ranges (500 ns, 2 µs)
PSD4 TVC ranges (250 ns, 2 µs).

PSD8C Channel



PSD8C Sub-Channel

PSD3 Works Well … But ! (Part I)

- PSD3 operates from a single 5 Volt supply. The use of 5 Volts helps ensure a large dynamic range but the FPGA which directly interfaces to the IC operates at 3.3 Volts, cluttering the chip-board with a large number of level translators.

- Analog signals (A, B, and C integrator outputs) from PSD3 come off chip differentially and are digitized by off-chip ADCs. Since the IC supports both negative and positive polarity inputs, it is necessary for the off-chip ADC to “swap” the differential input lines when processing negative polarity inputs. The only 16-bit ADC currently available to do this “swap” is the Linear Technology’s LTC1865.

PSD3 Works Well … But ! (Part II)

- The on-board time-to-voltage converters (TVCs) suffer from a logic bug (which has a work around, thankfully!)

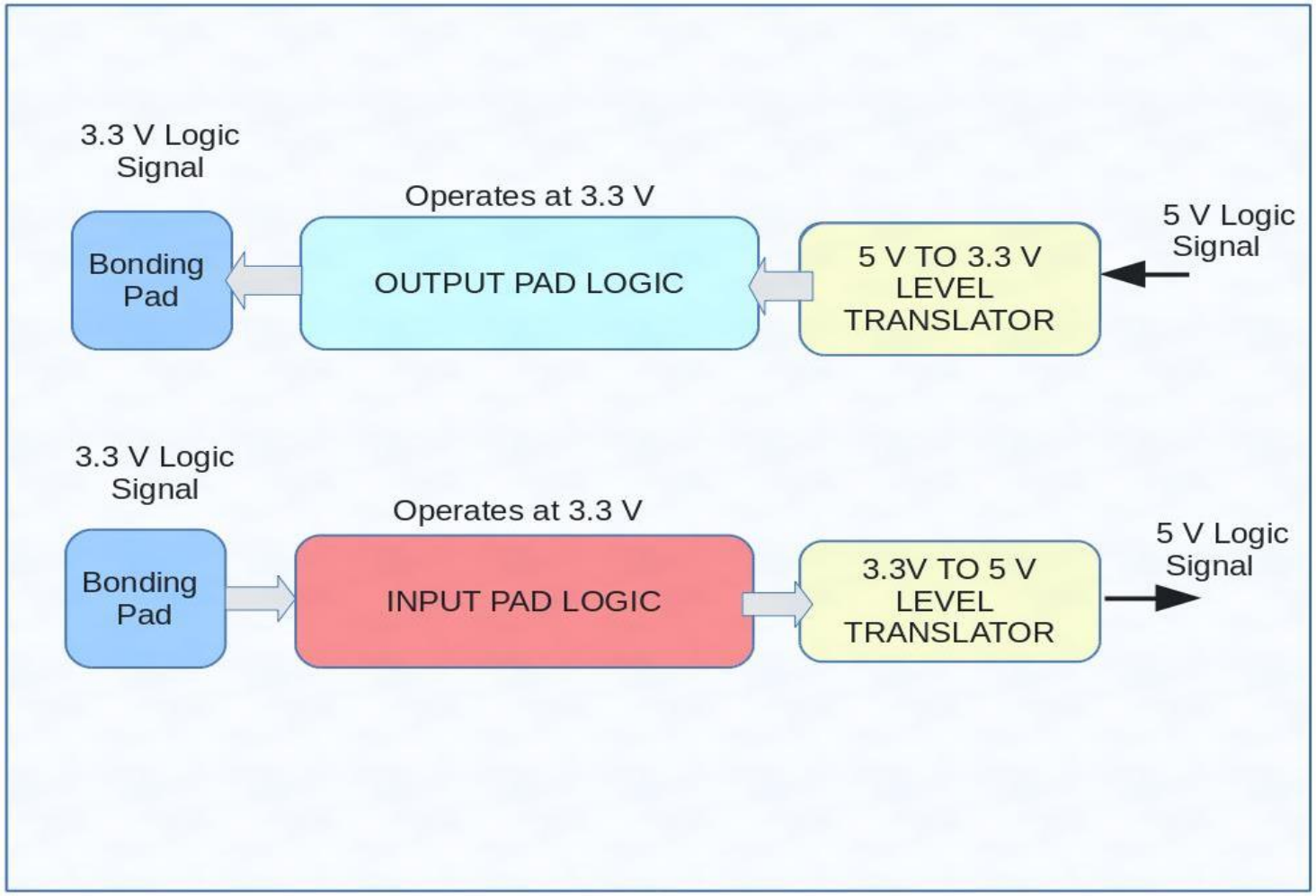
- While the TVC timing resolution is acceptable for most applications, some potential applications would benefit from improved resolution.

Enter PSD4 (our 4th Generation IC)!!!

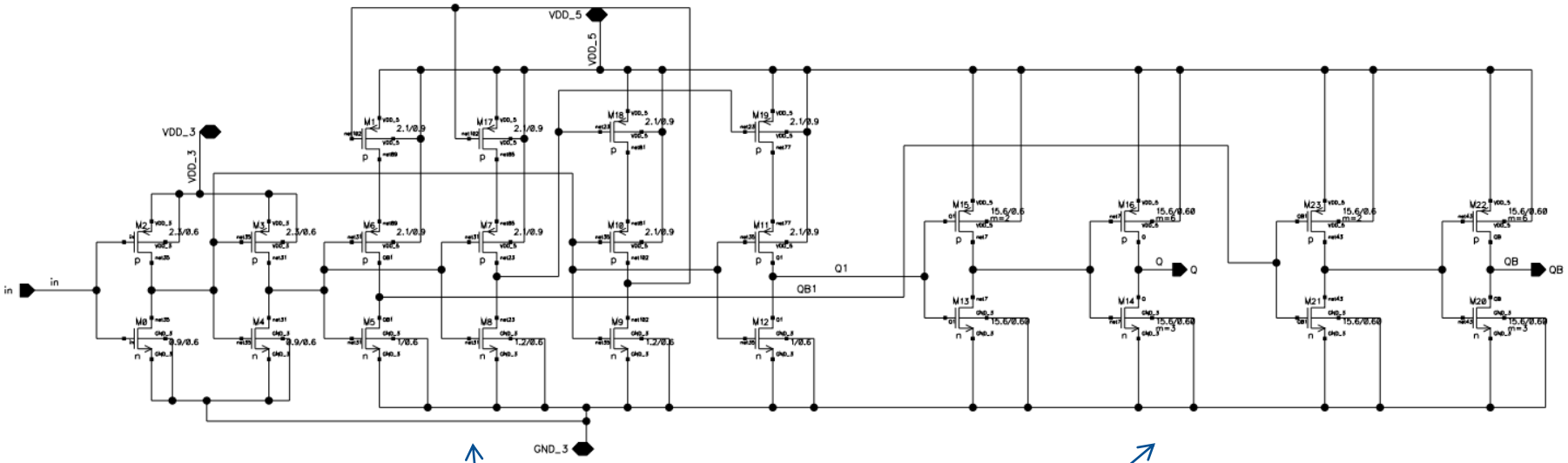
- Let's walk through the enhancements one-by-one!!!

- We'll look at schematic-level changes, modified layout, and simulation results.

Addition of Level Translators



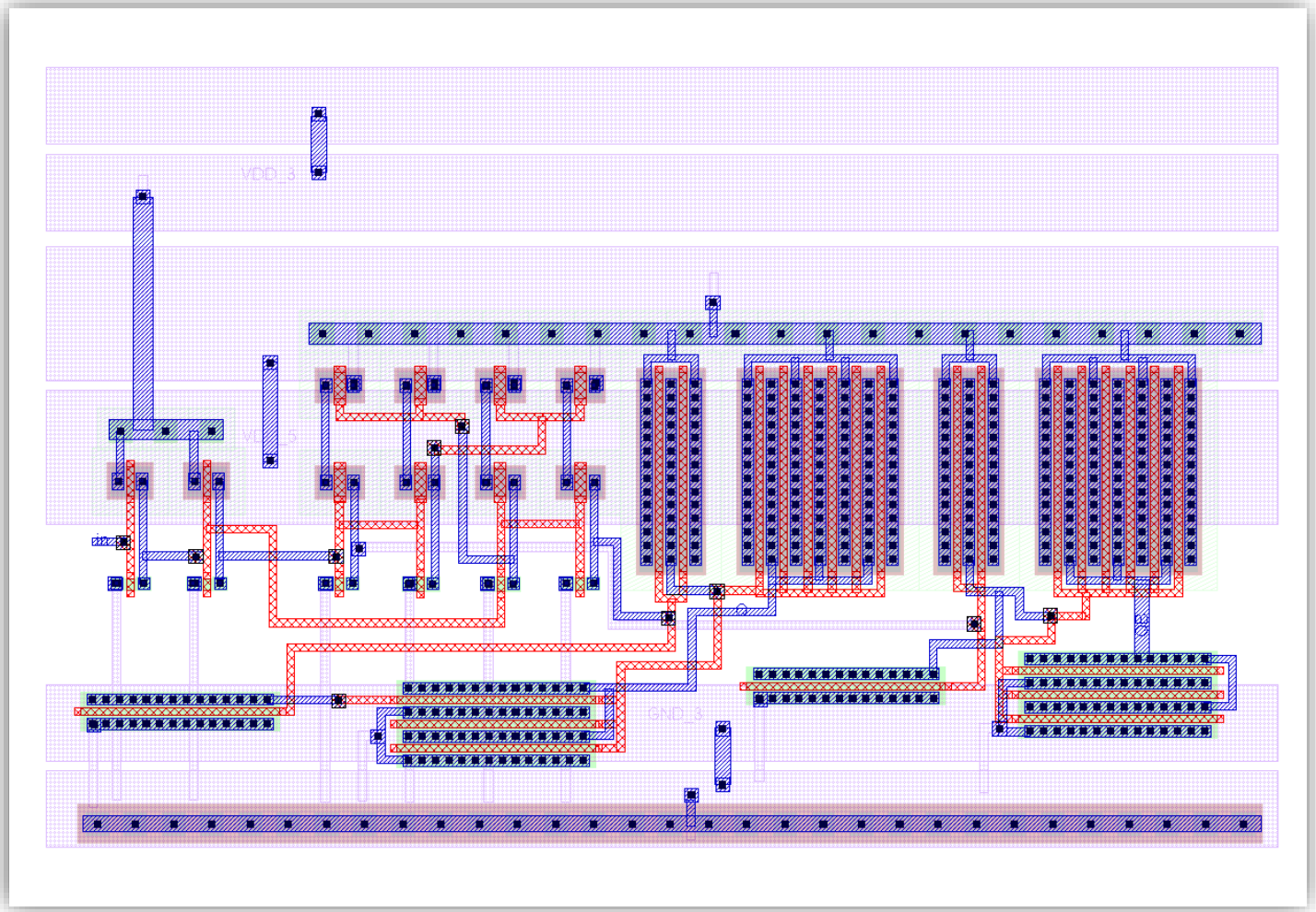
Level Translator Schematic



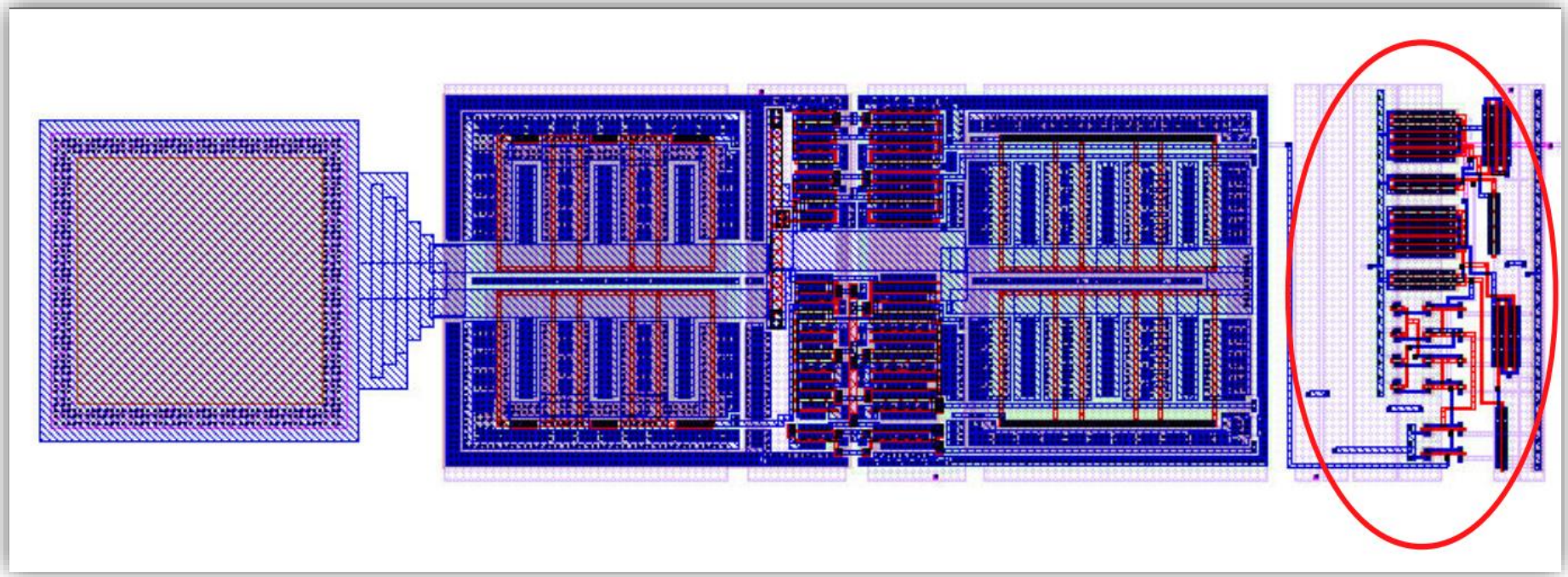
Level shifters.

Buffers similar to those in original pad.

Level Translator Layout

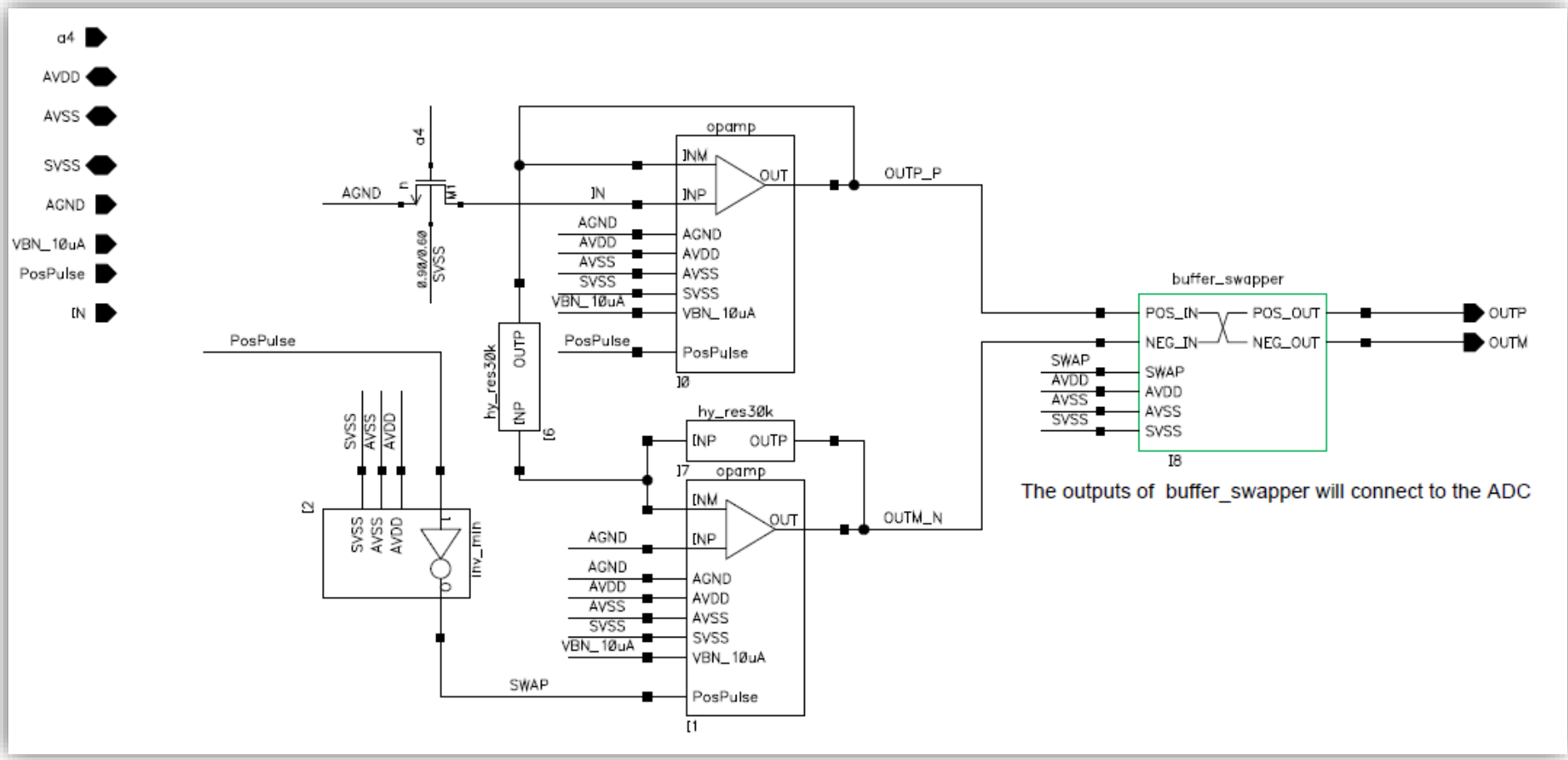


Digital I/O Pad With Level Translation!

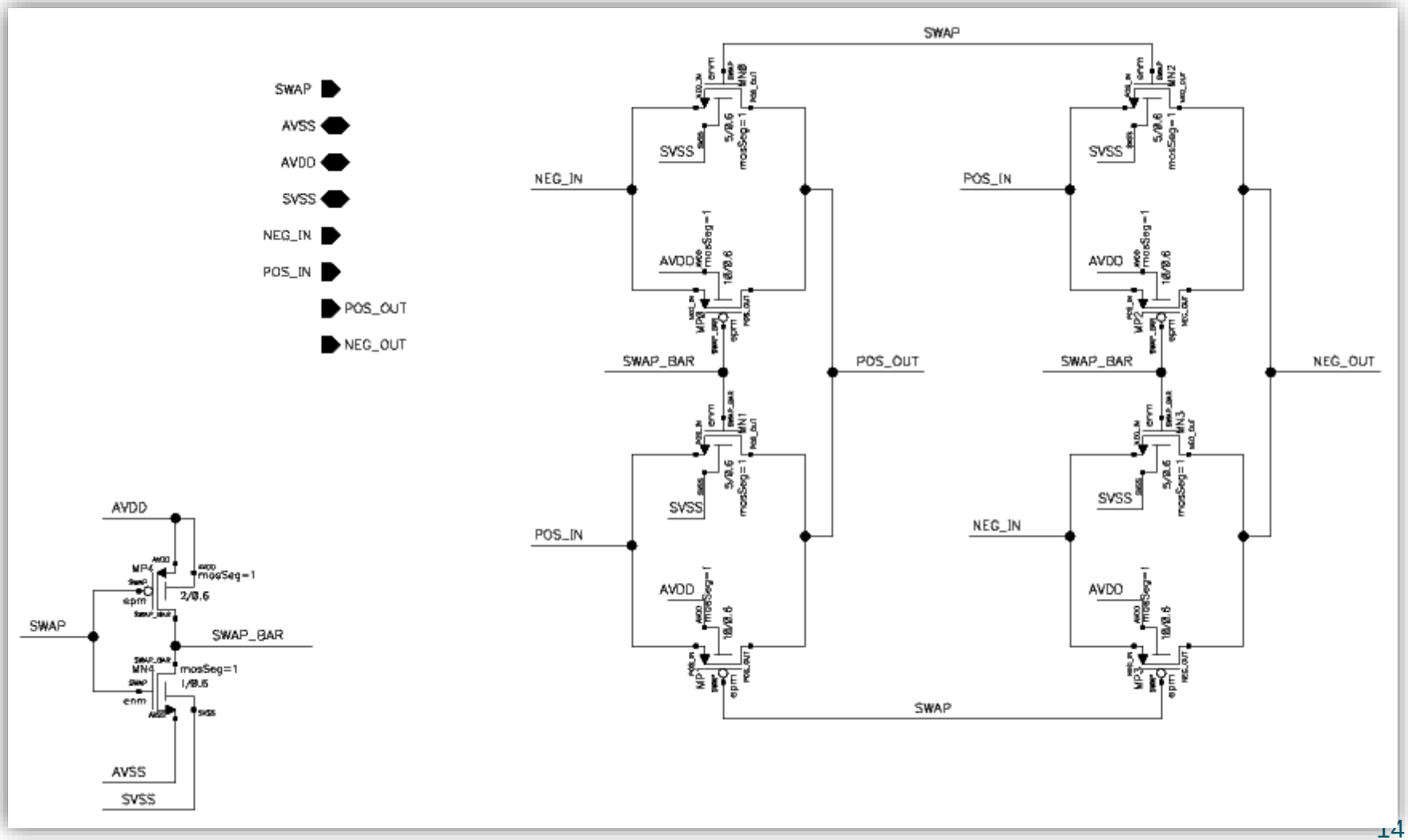


Internal pull-down resistors (10 KΩ) were also added to the bi-directional pins used by the chip ID bus.

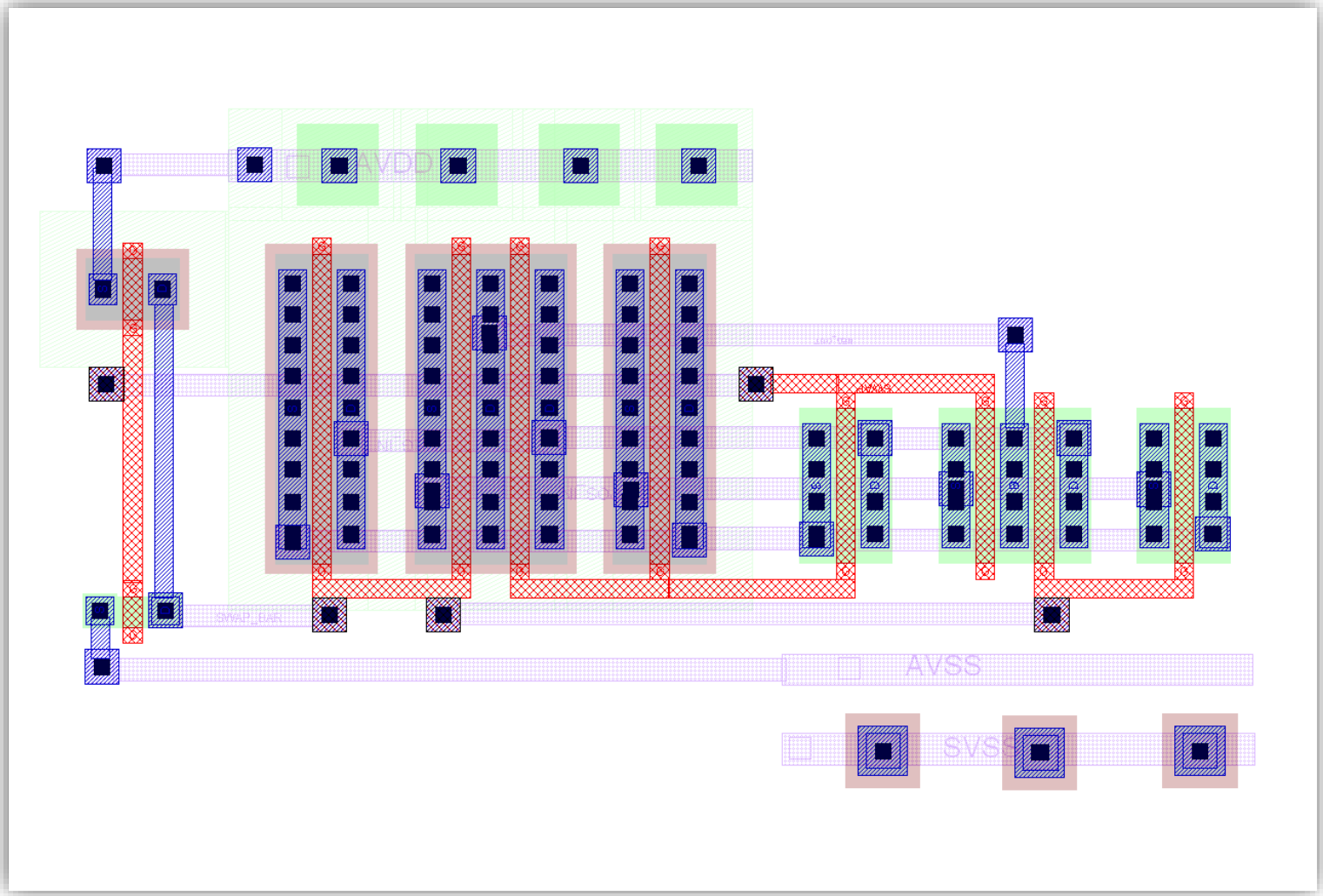
"Swapper" Function Added to PSD4



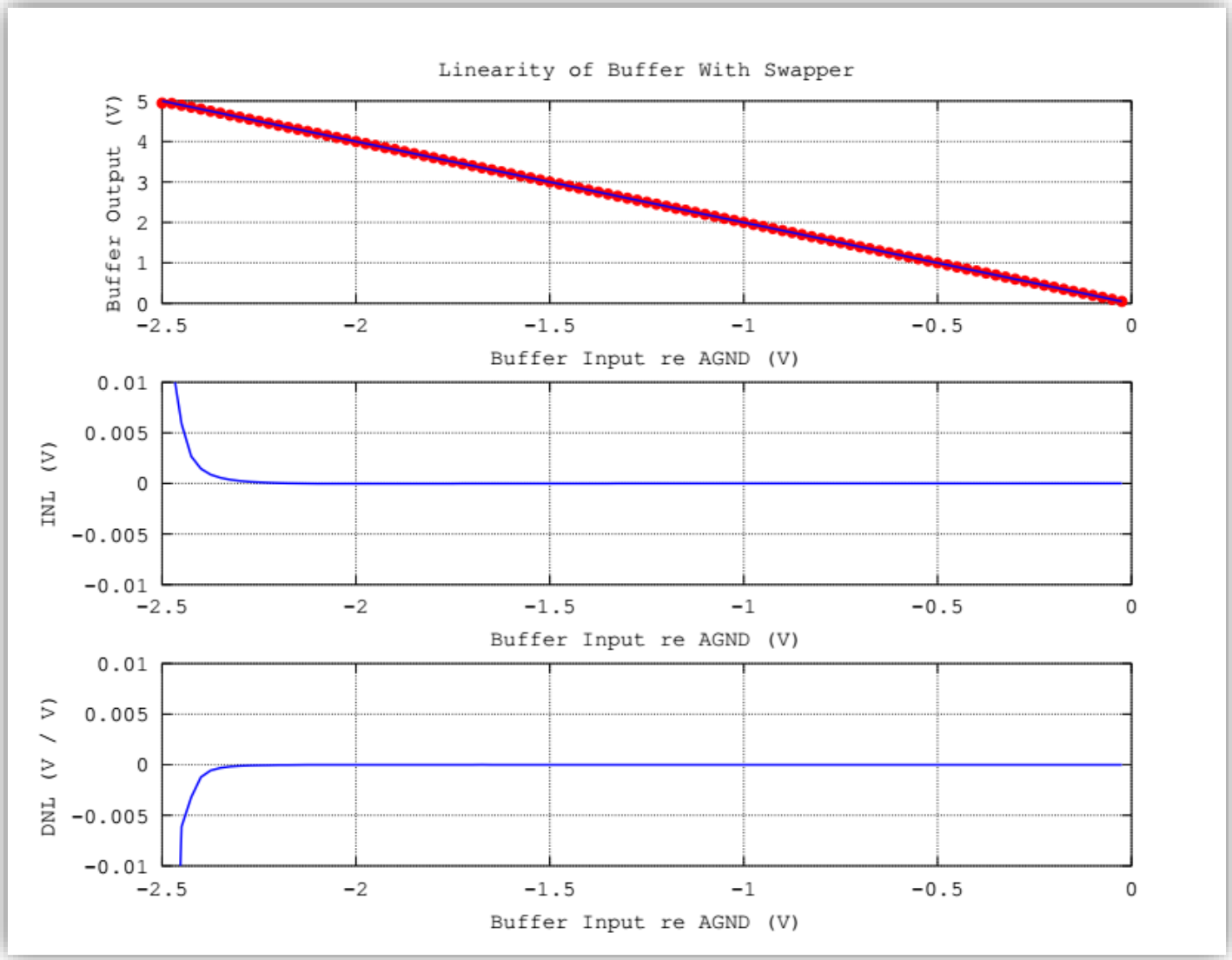
"Swapping" Outputs is Easy!



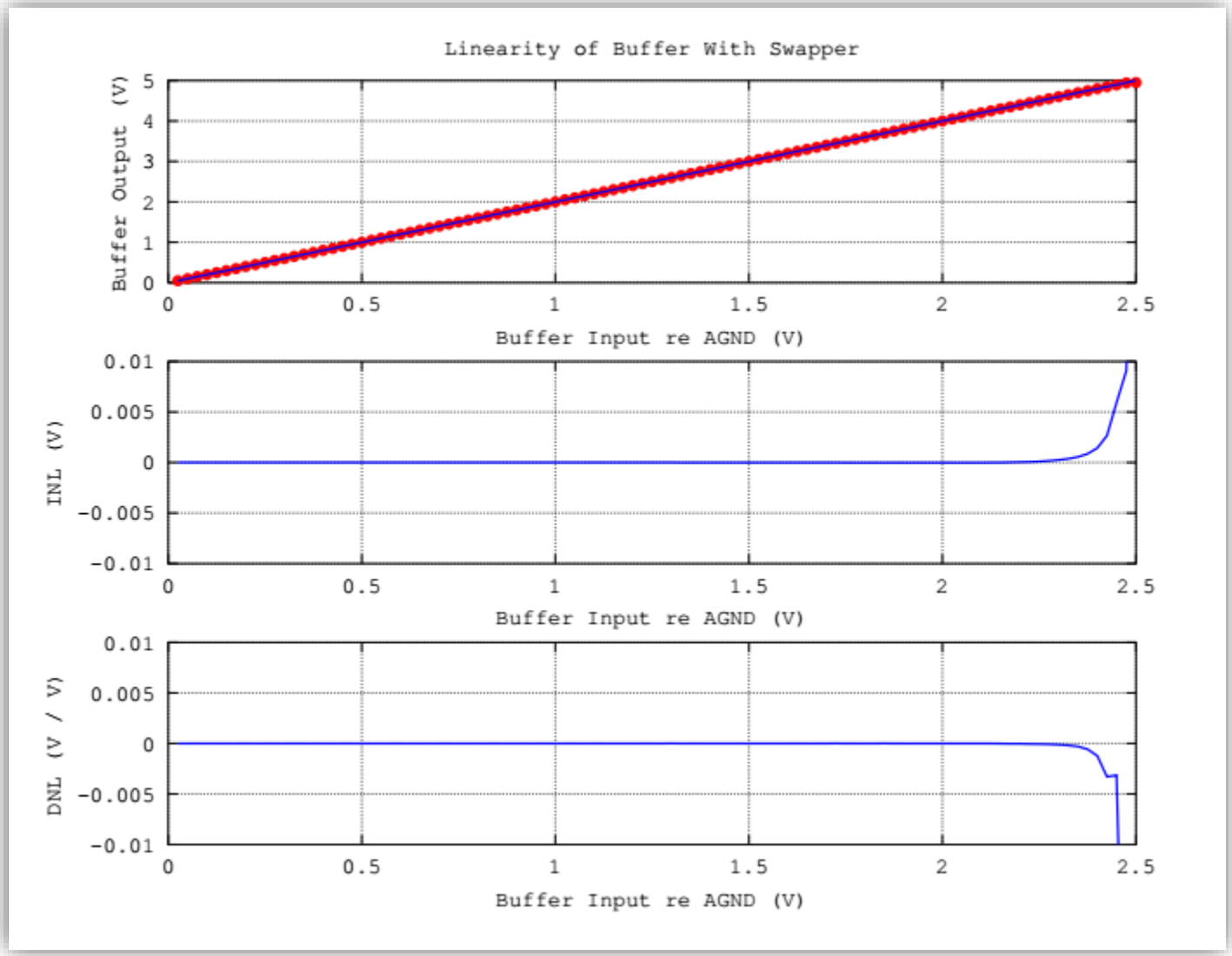
"Swapper" Layout



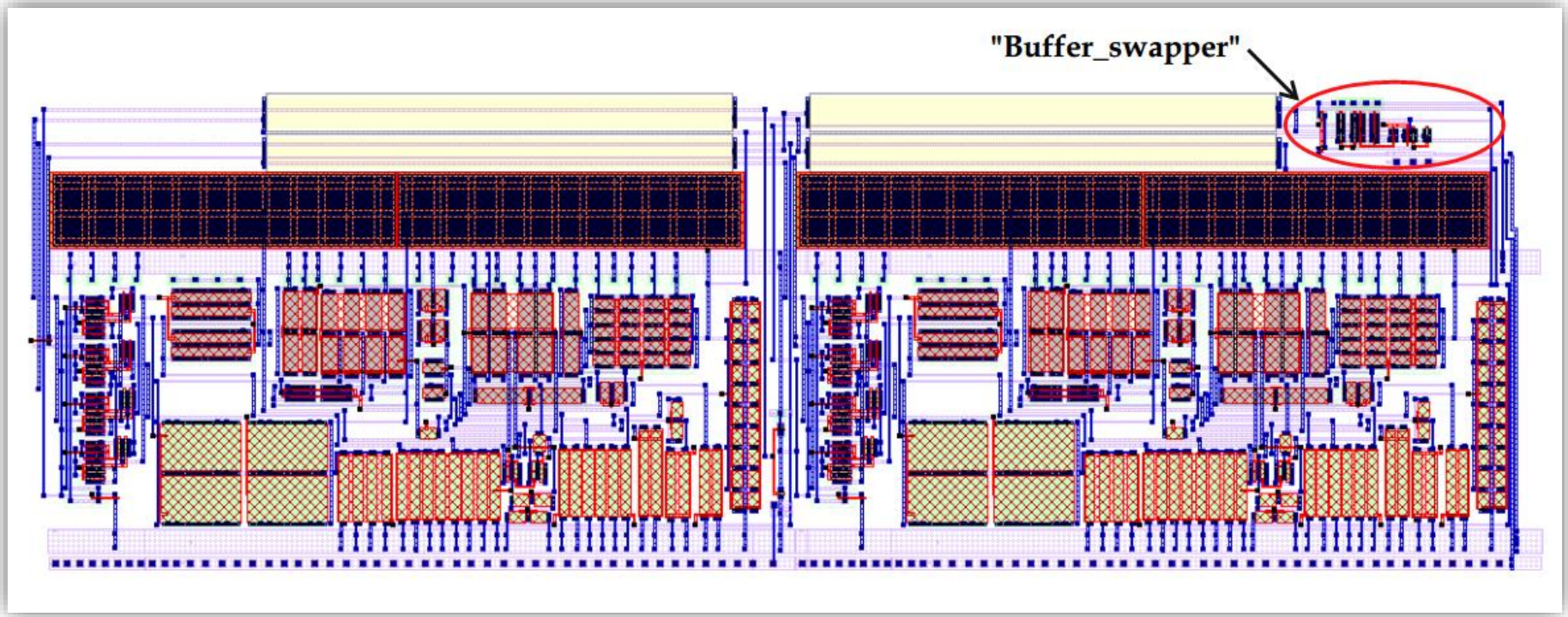
Linearity of Buffer with "Swapper"



Linearity of Buffer with "No Swapper"

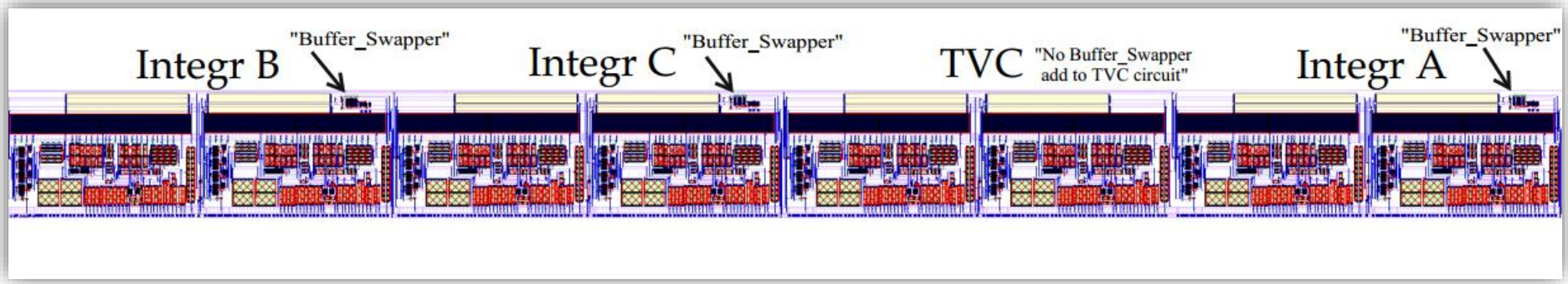


There was just a enough room … Whew!!!!



Changes to the Off-Chip Driver Block

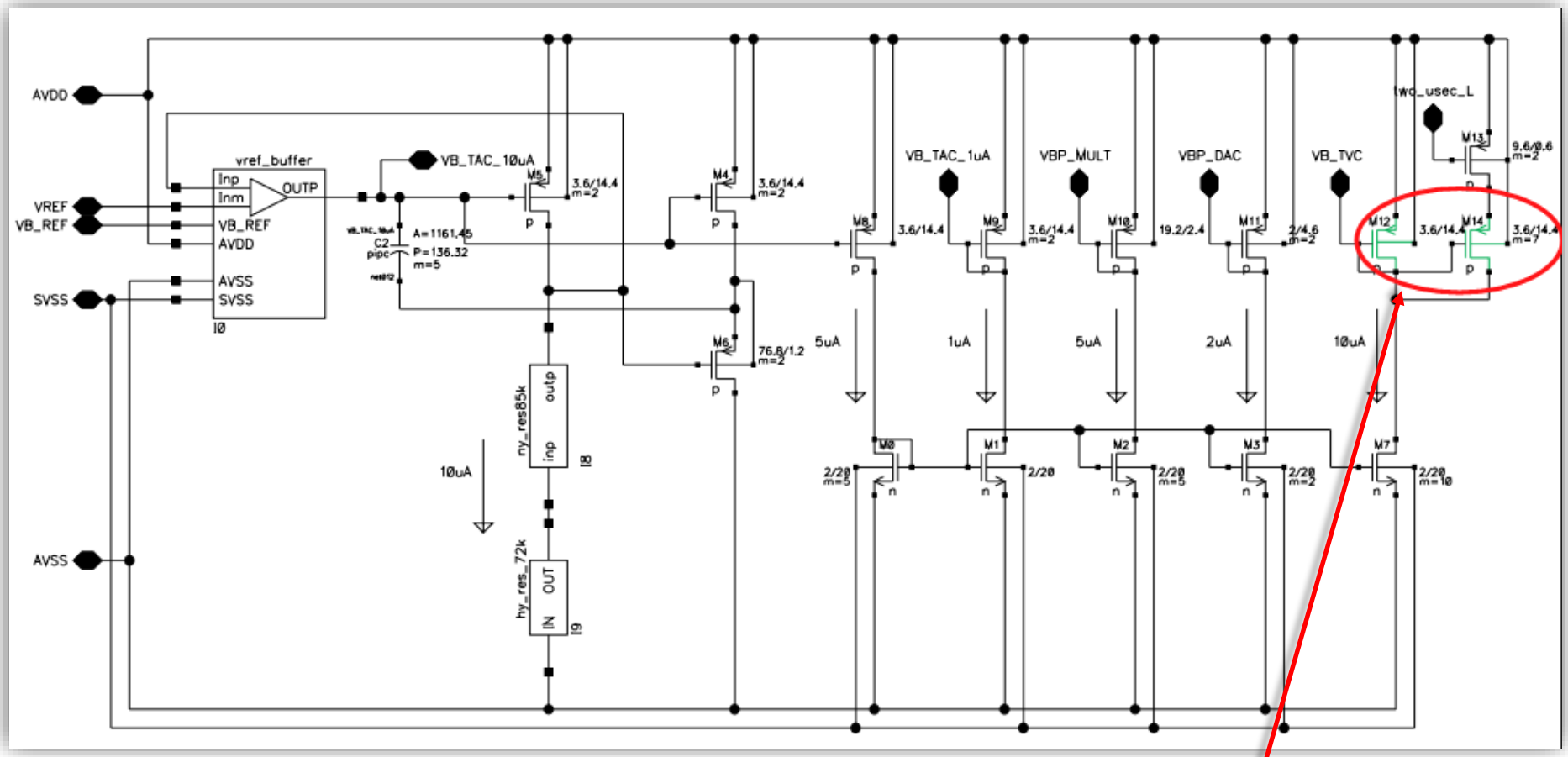
The “Swapper” circuit was only added to the integrator A, B, and C output buffers. The TVC output is always of one polarity!



Change 500 ns TVC range to 250 ns

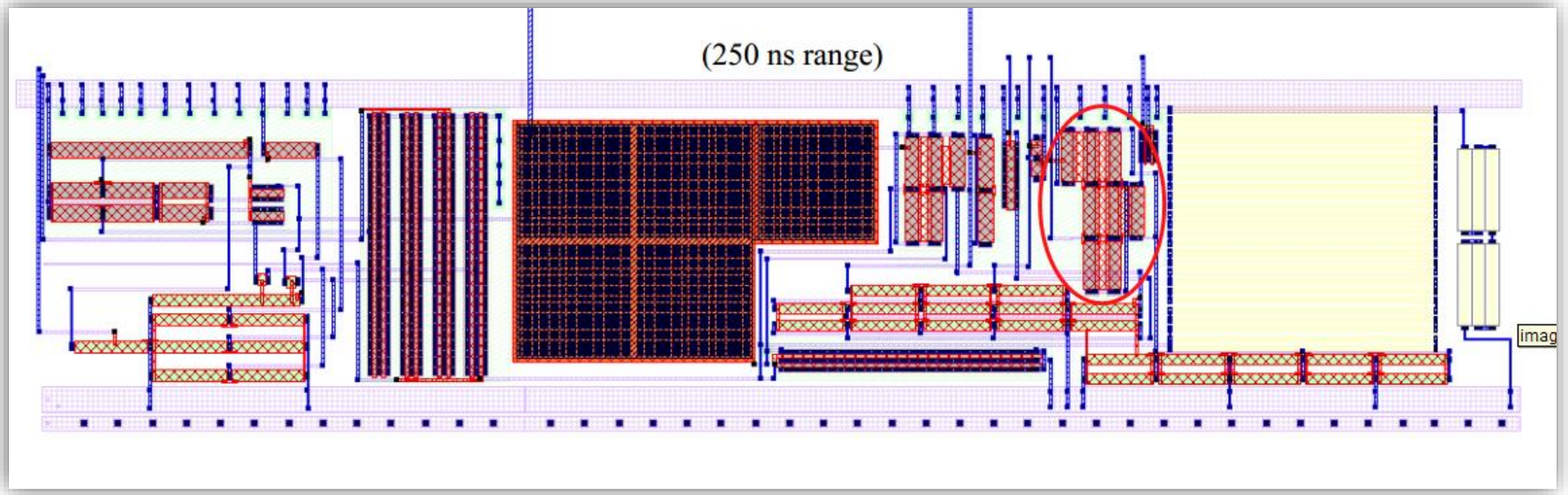
- This change will improve the timing resolution but range is so short that it is would be almost unusable unless we delay the start of the TVC.
- We decided for PSD4, rather than start the TVC on the **rising** edge of the CFD pulse, we would start the TVC on the **falling** edge of its CFD input. Width of CFD pulse implements the delay that we need! This implies that **both** edges of the CFD pulse must possess very low jitter. Integrator delays are still relative to the rising edge of the CFD pulse, just as in PSD3.
- A *common stop* signal stops the TVCs in all channels.

Double Currrent for 250ns Mode



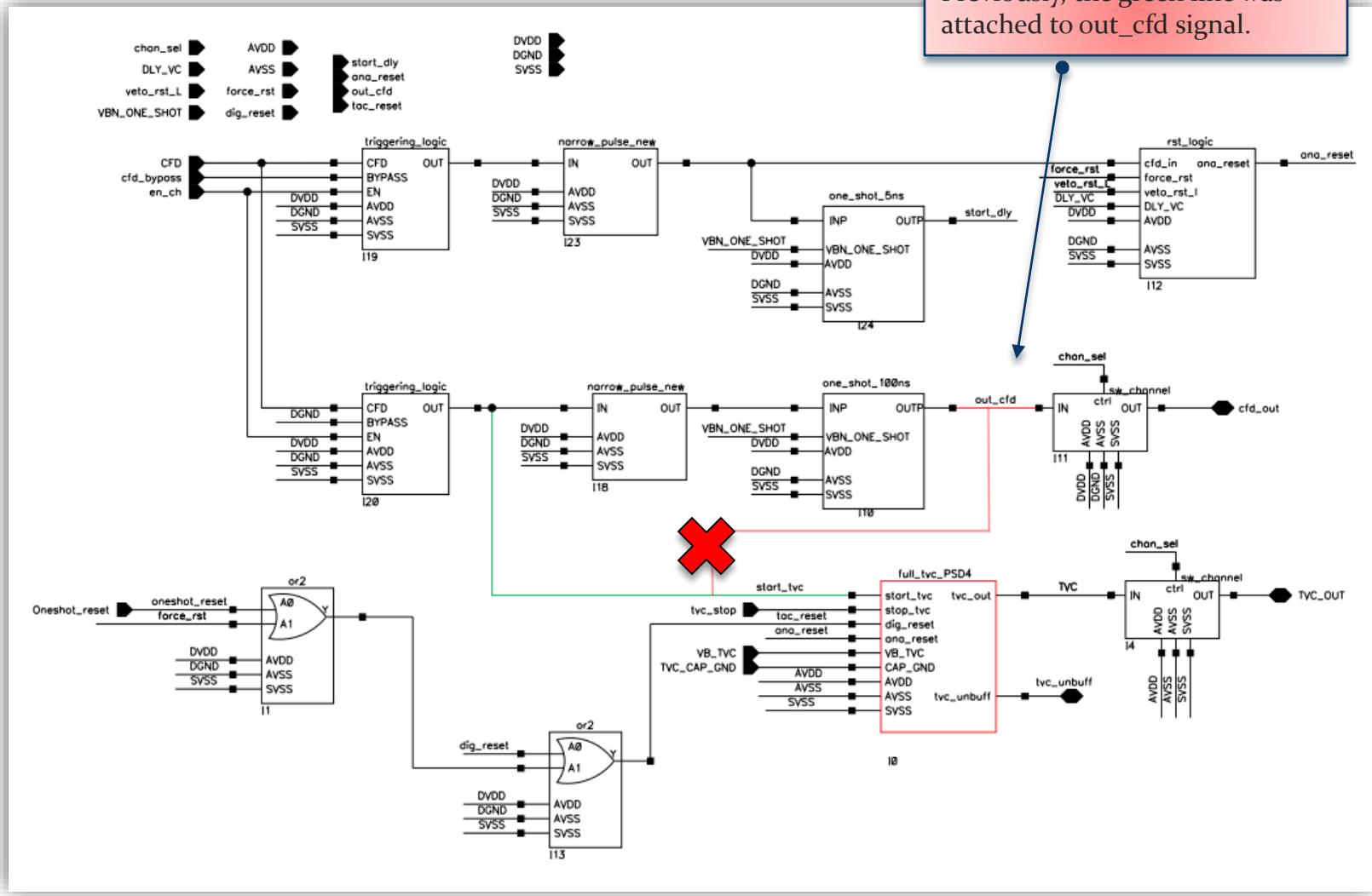
We Changed the size of M12 (m=2) and M14 (m=6) to M12 (m=1) and M14 (m=7)

Small Layout Change in Constant Current Source Cell

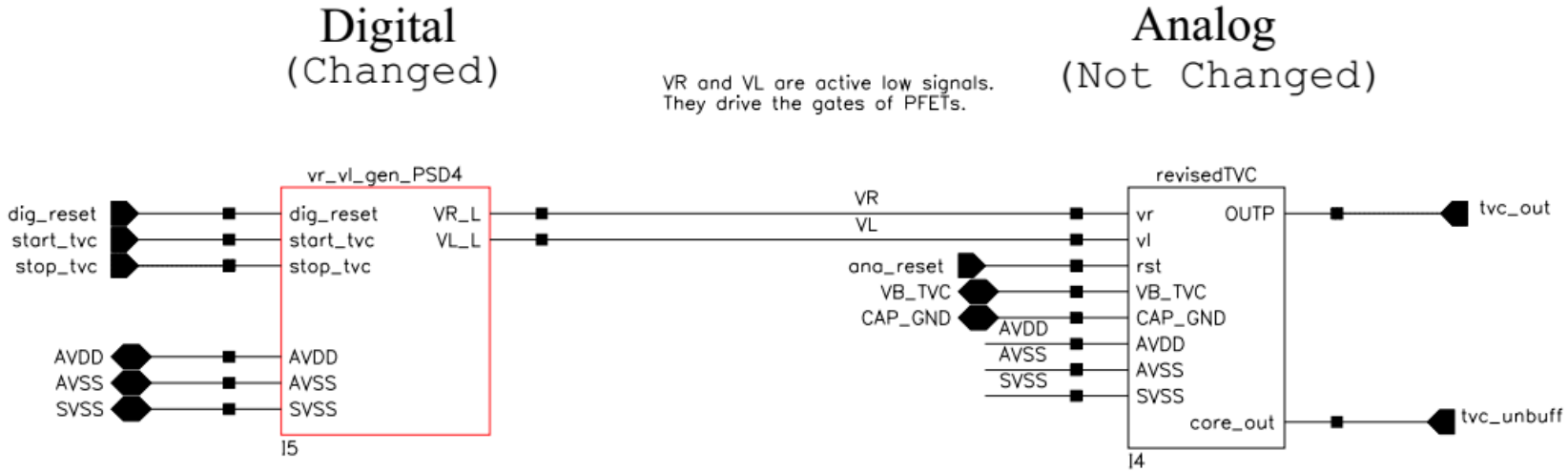


TVC Needs to See Original CFD Signal

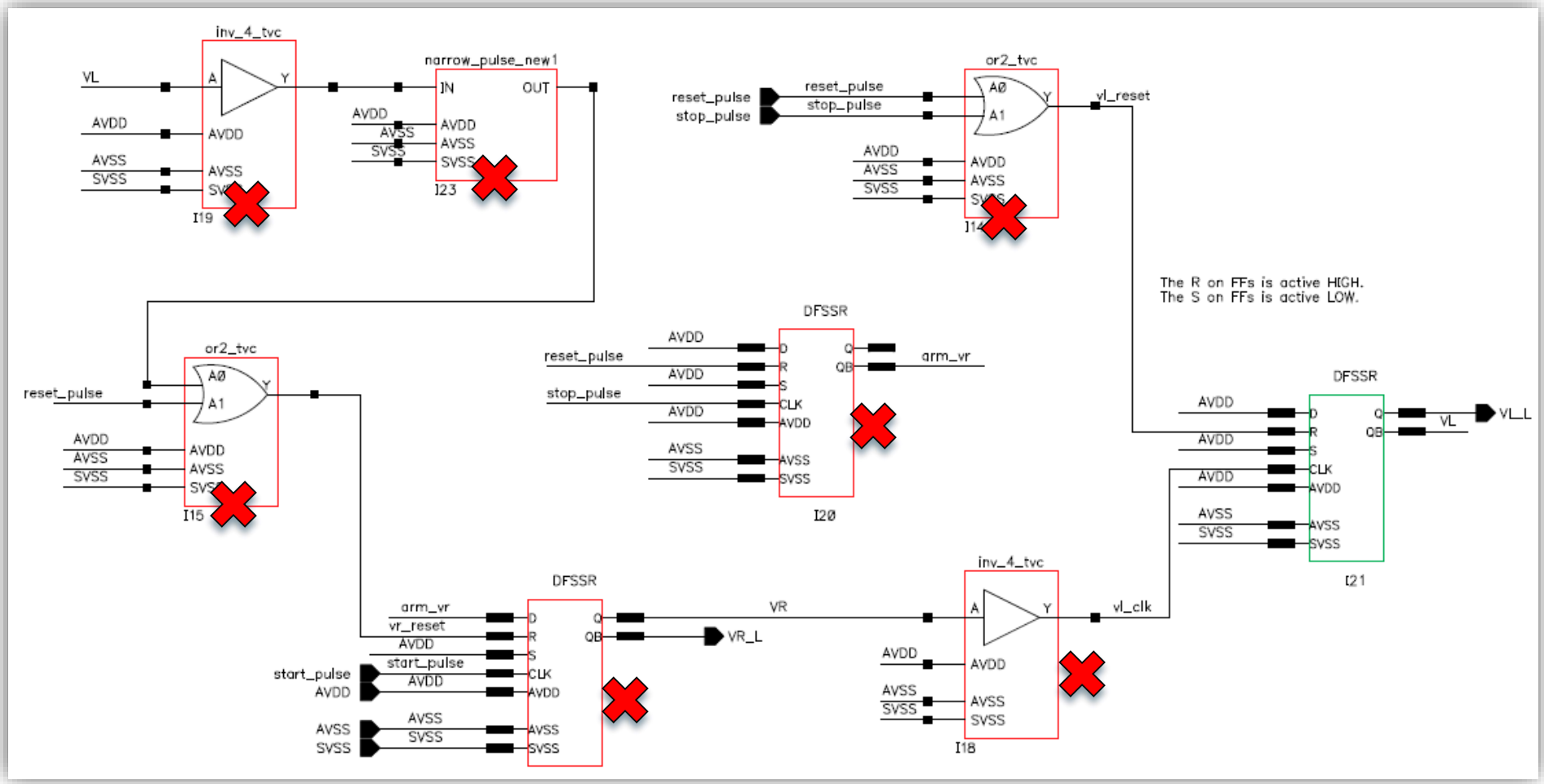
Previously, the green line was attached to out_cfd signal.



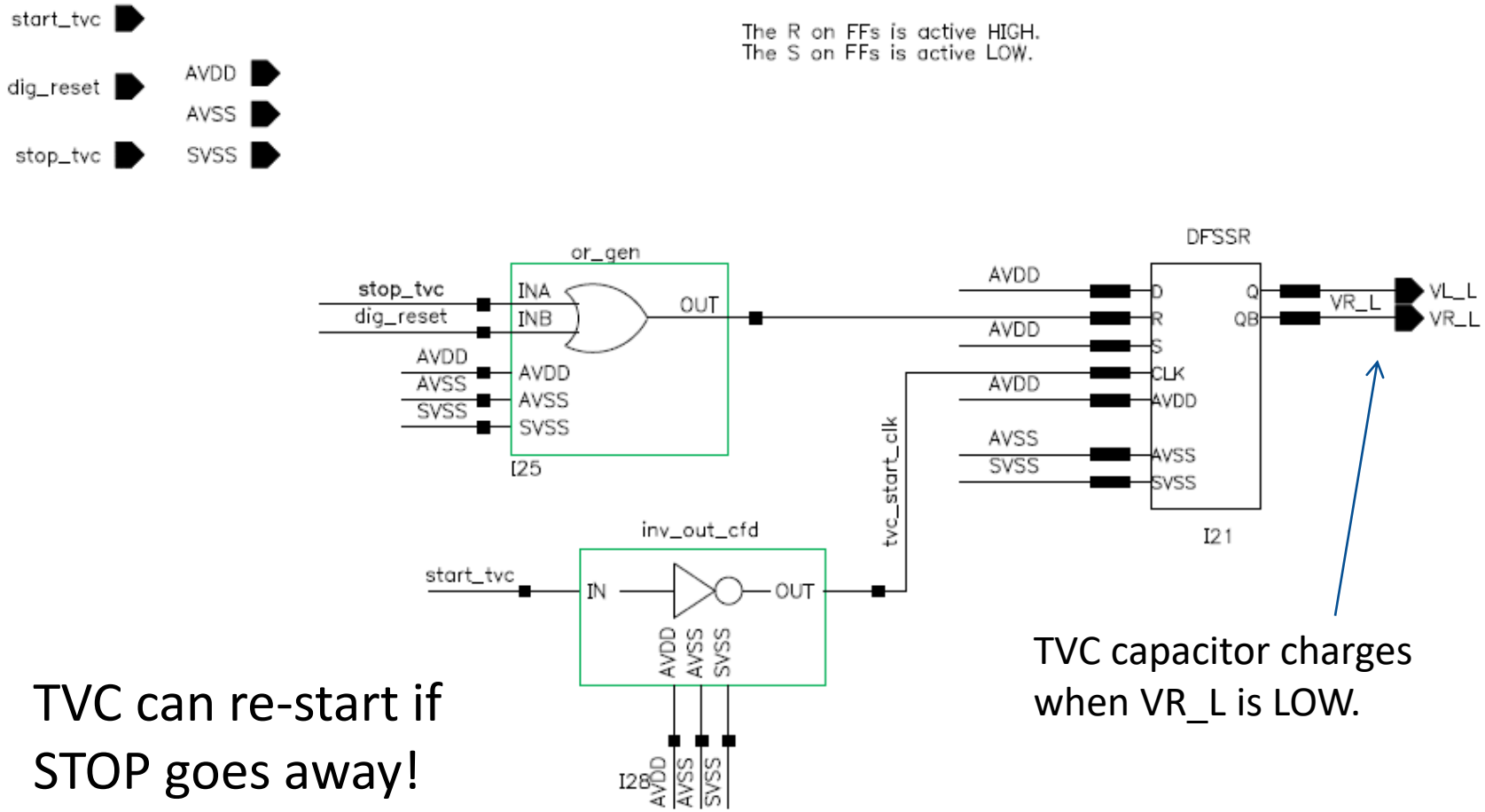
TVC Circuit Modifications



Digital Control Simplified



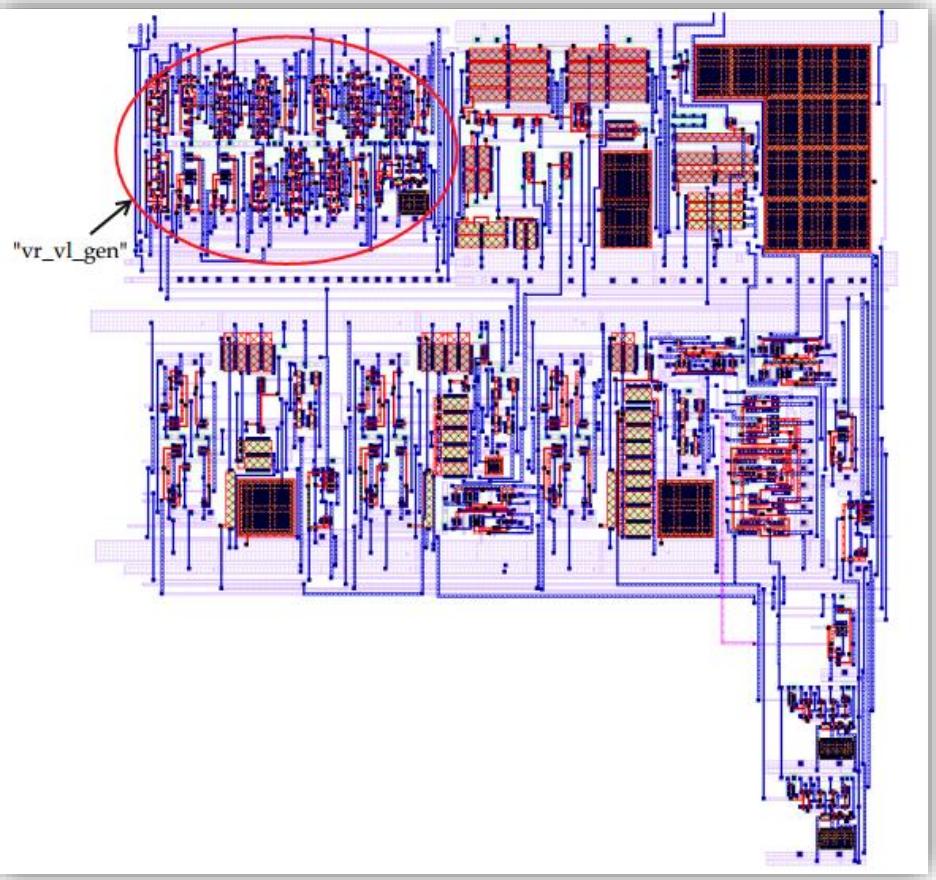
Starting and Stopping TVC

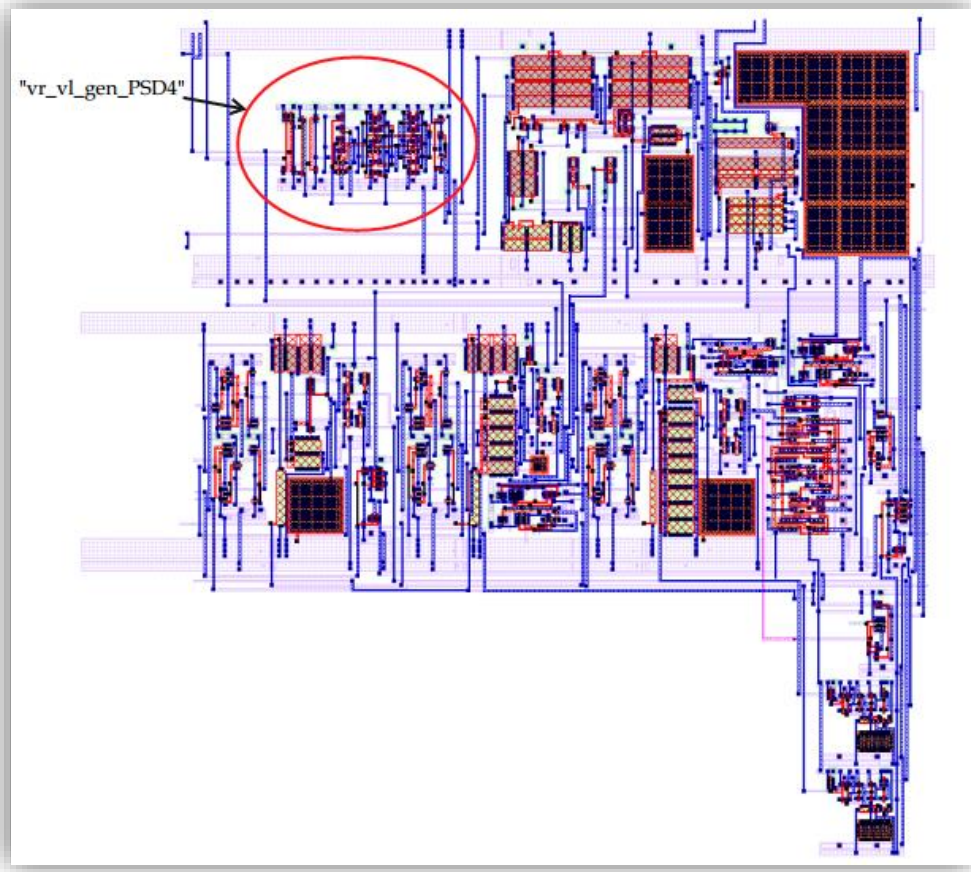


TVC can re-start if STOP goes away!

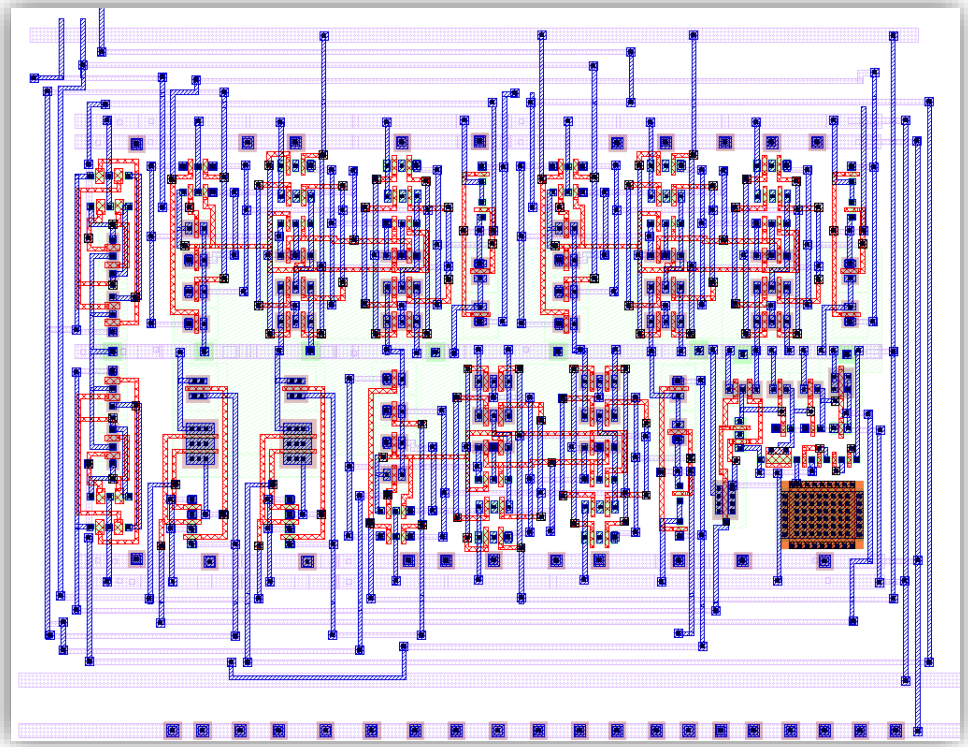
TVC capacitor charges when VR_L is LOW.

TVC Layout (before and after!)

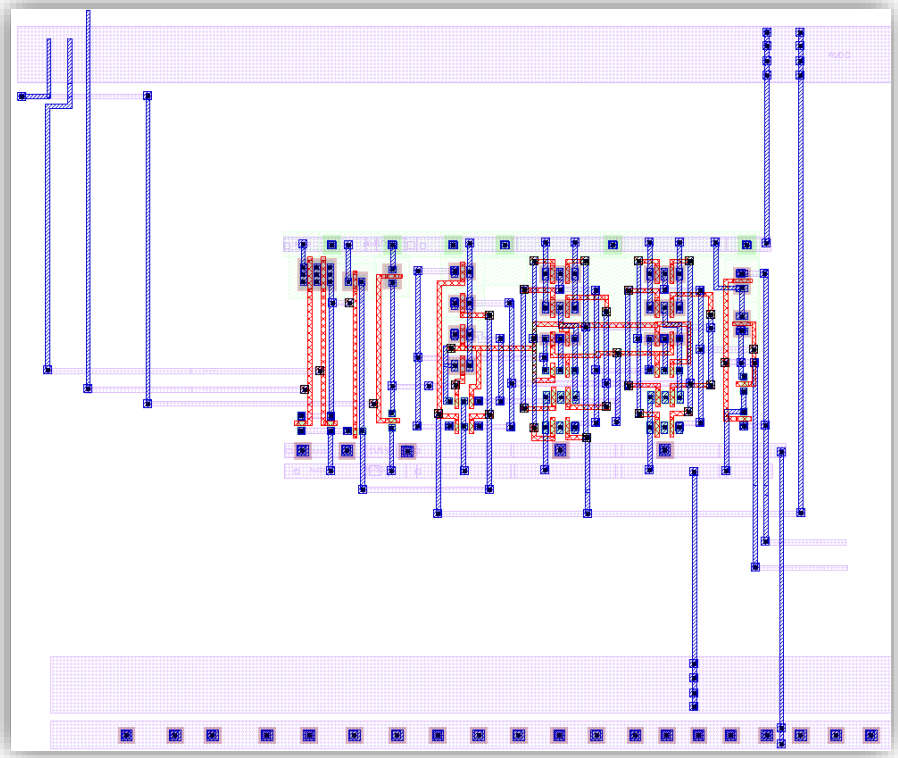




Let's Go in For a Better View!

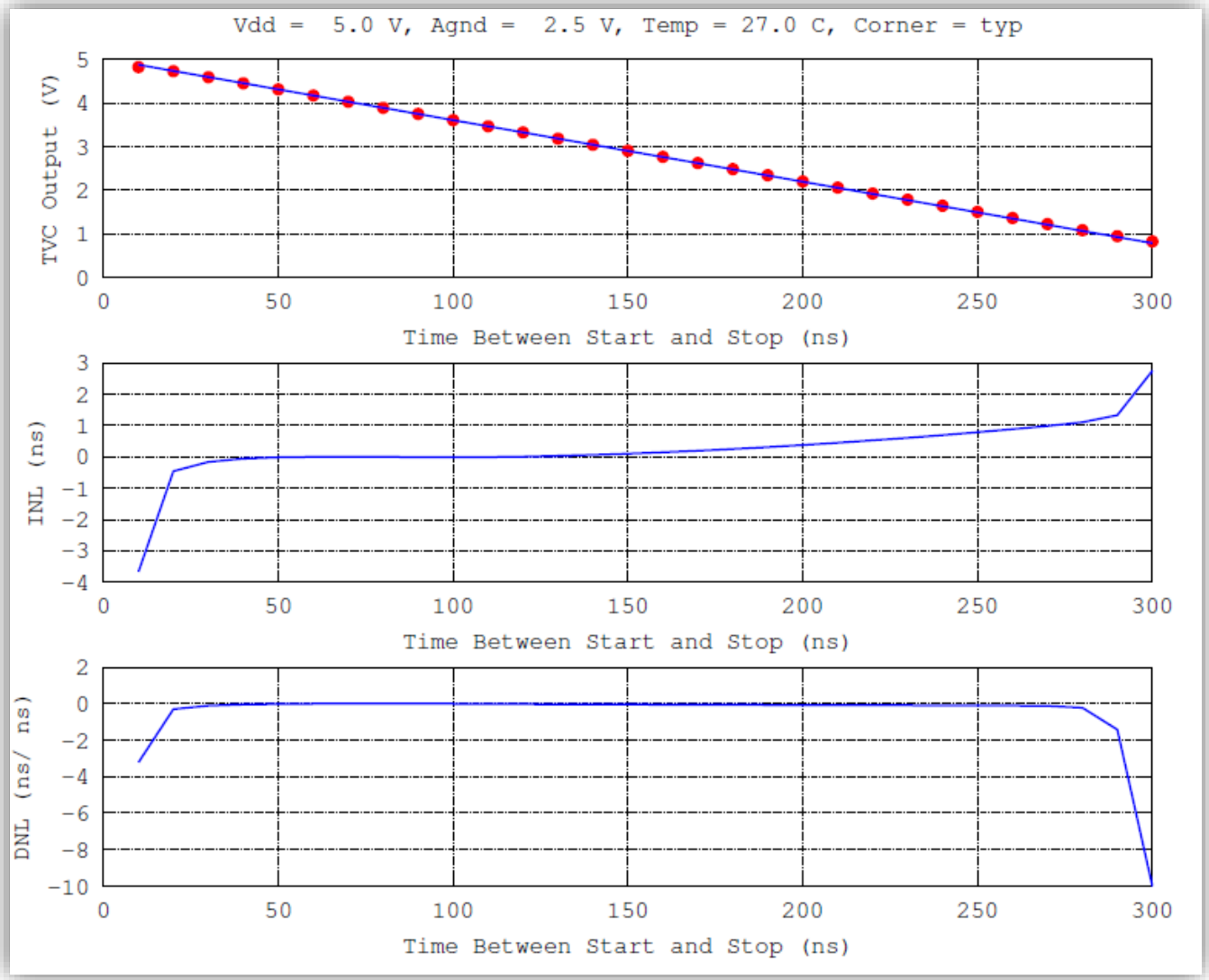


BEFORE

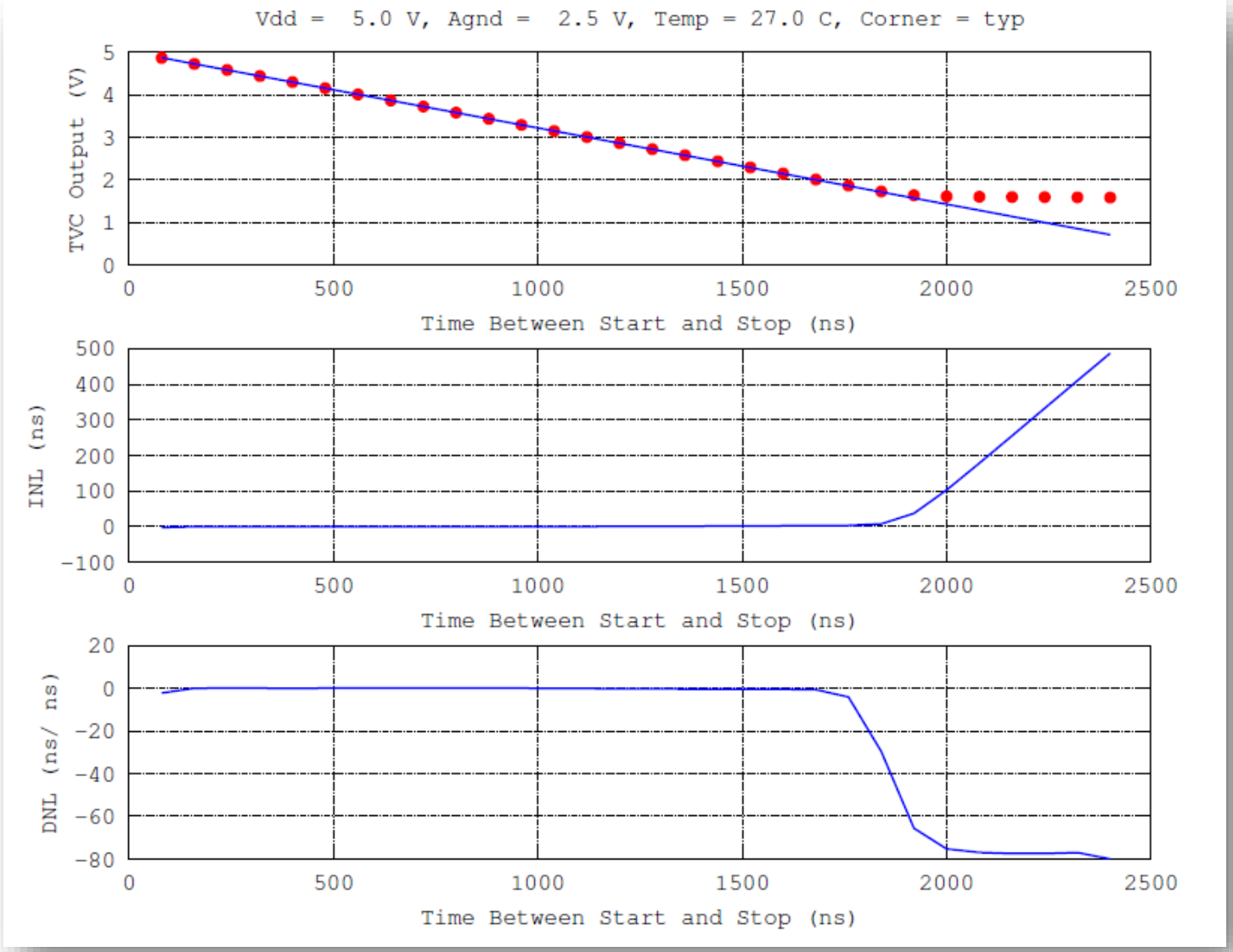


AFTER

TVC Linearity (Typical, 250 ns Range)

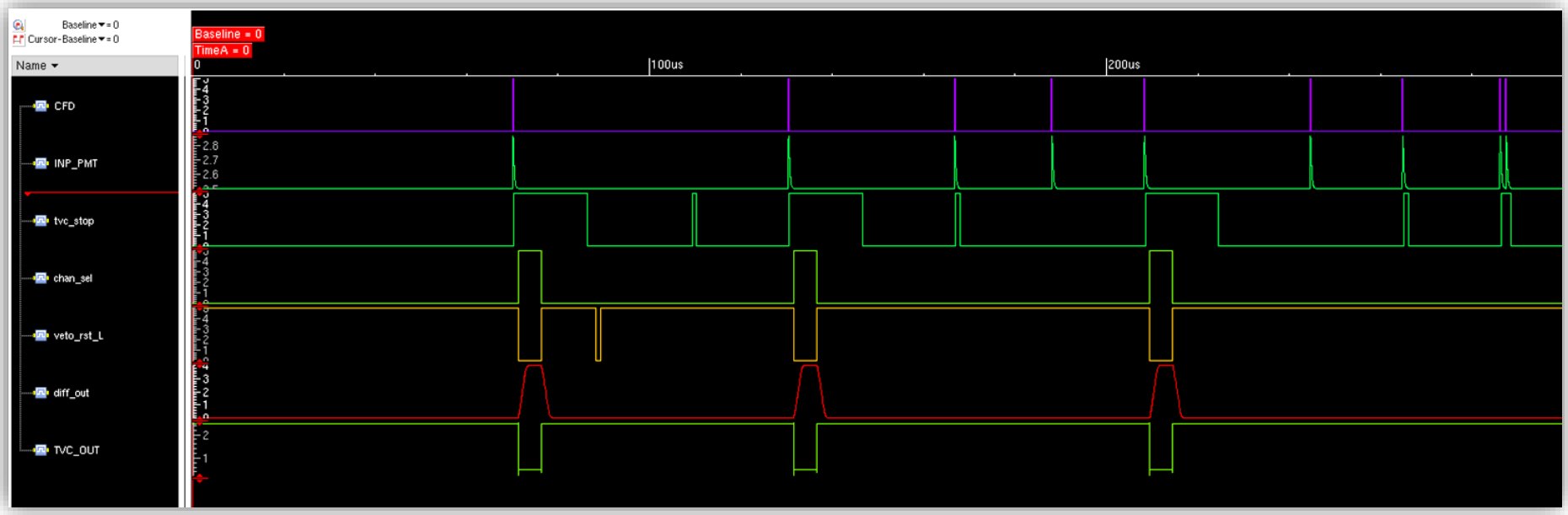


TVC Linearity (Typical, 2000 ns Range)



Functional Test on Single Channel

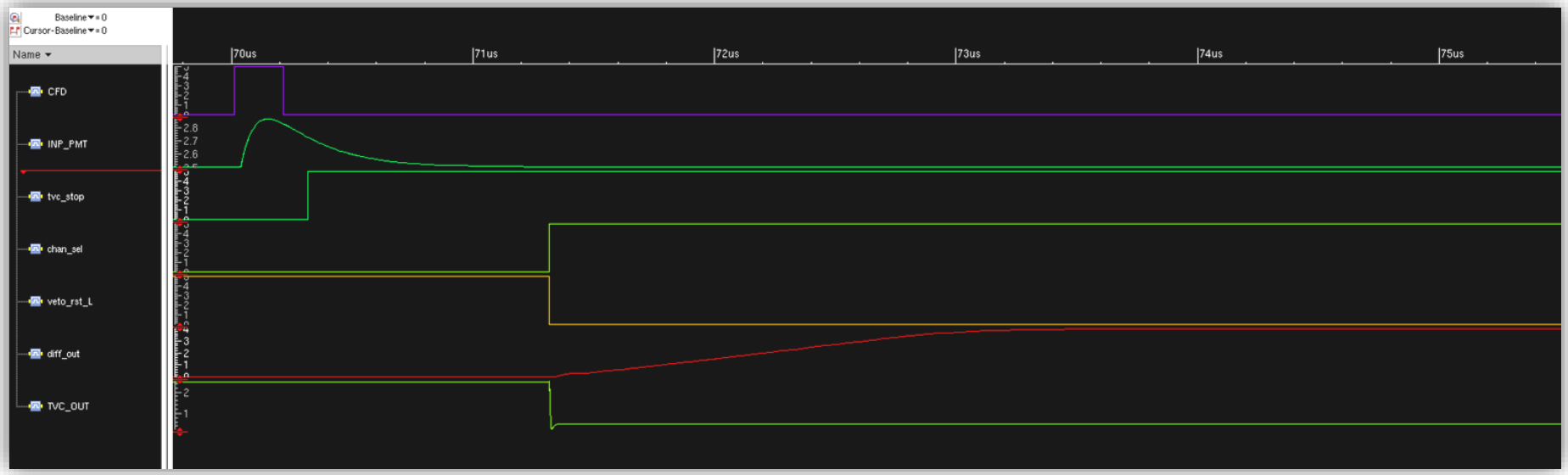
Simulation demonstrates that revised TVC functions correctly!



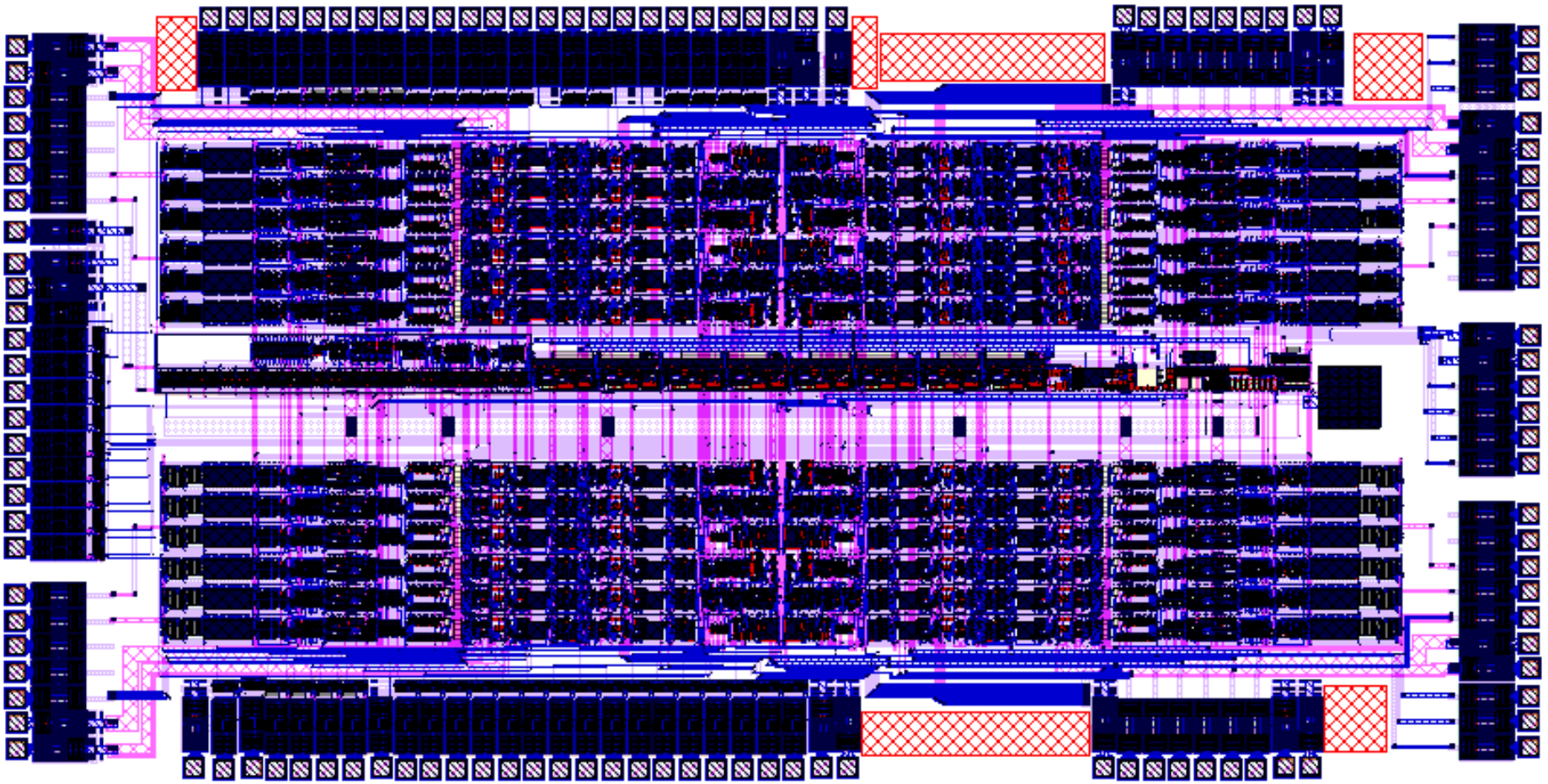
Settling Time Behavior of Buffer

TVC starts on falling edge of CFD signal stops on rising edge of TVC_STOP signal.

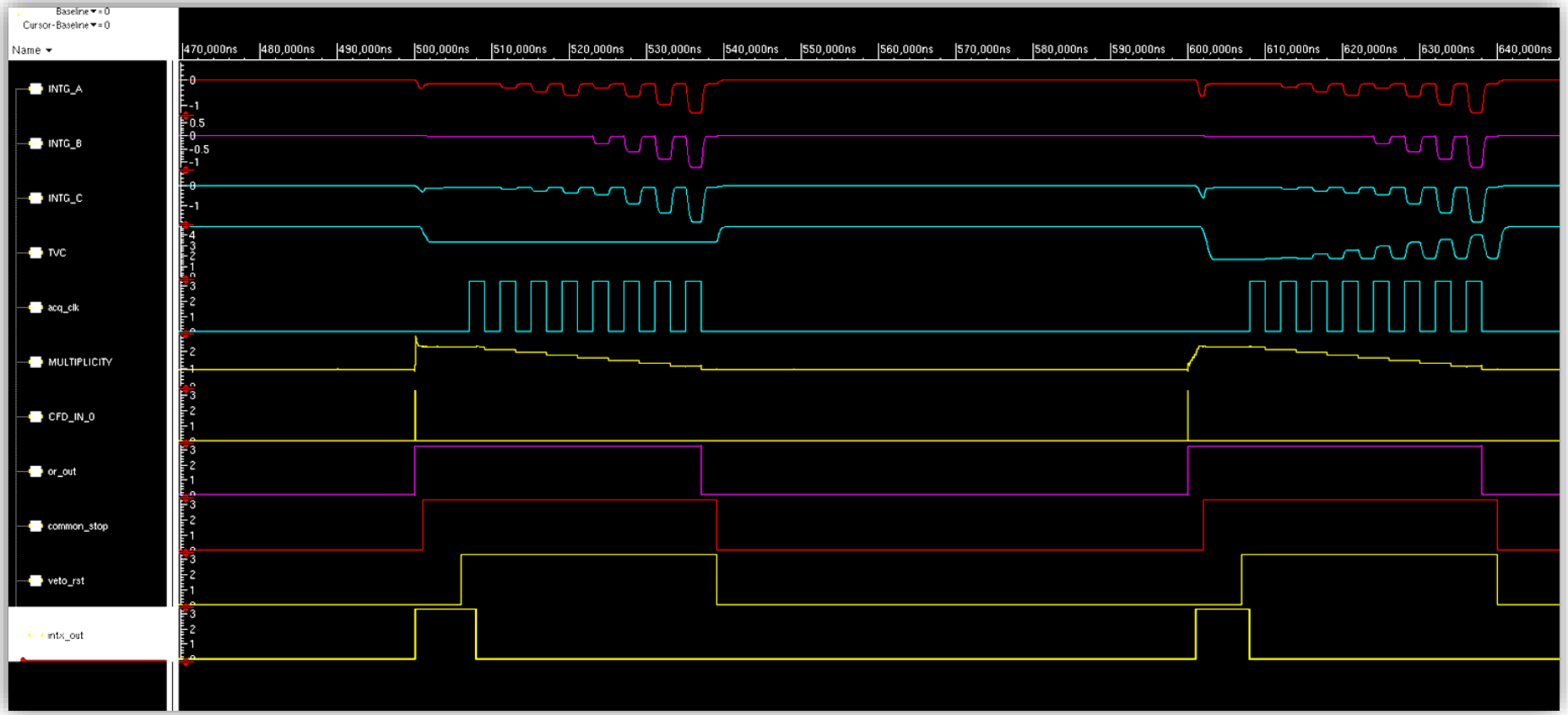
Observe that takes differential signal from output buffer about 4 usec to settle.



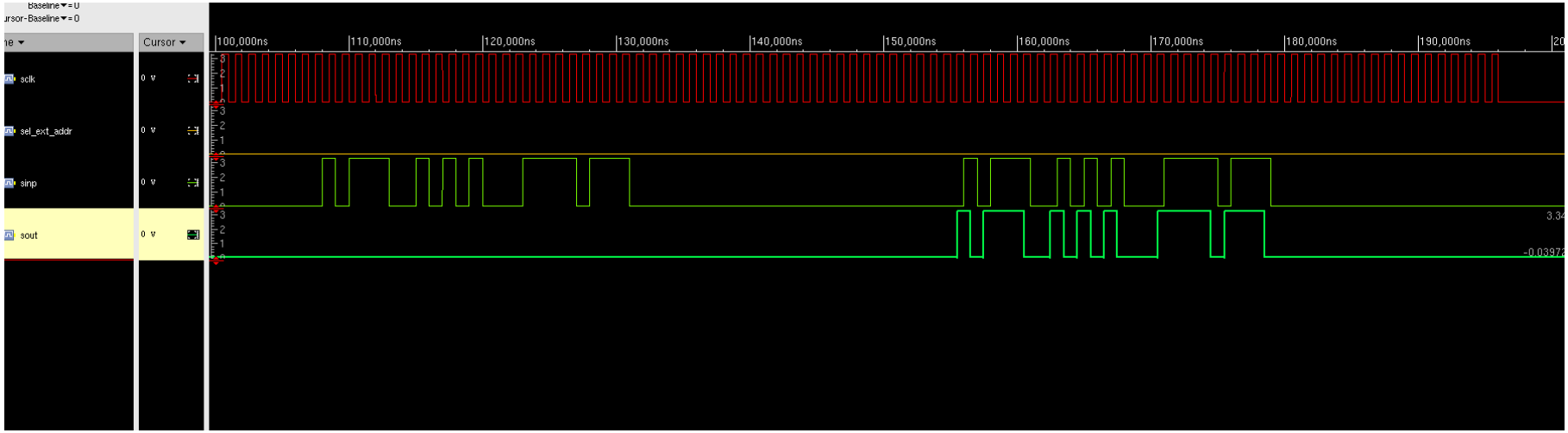
PSD4 Final Layout (5.7 mm x 2.9 mm)



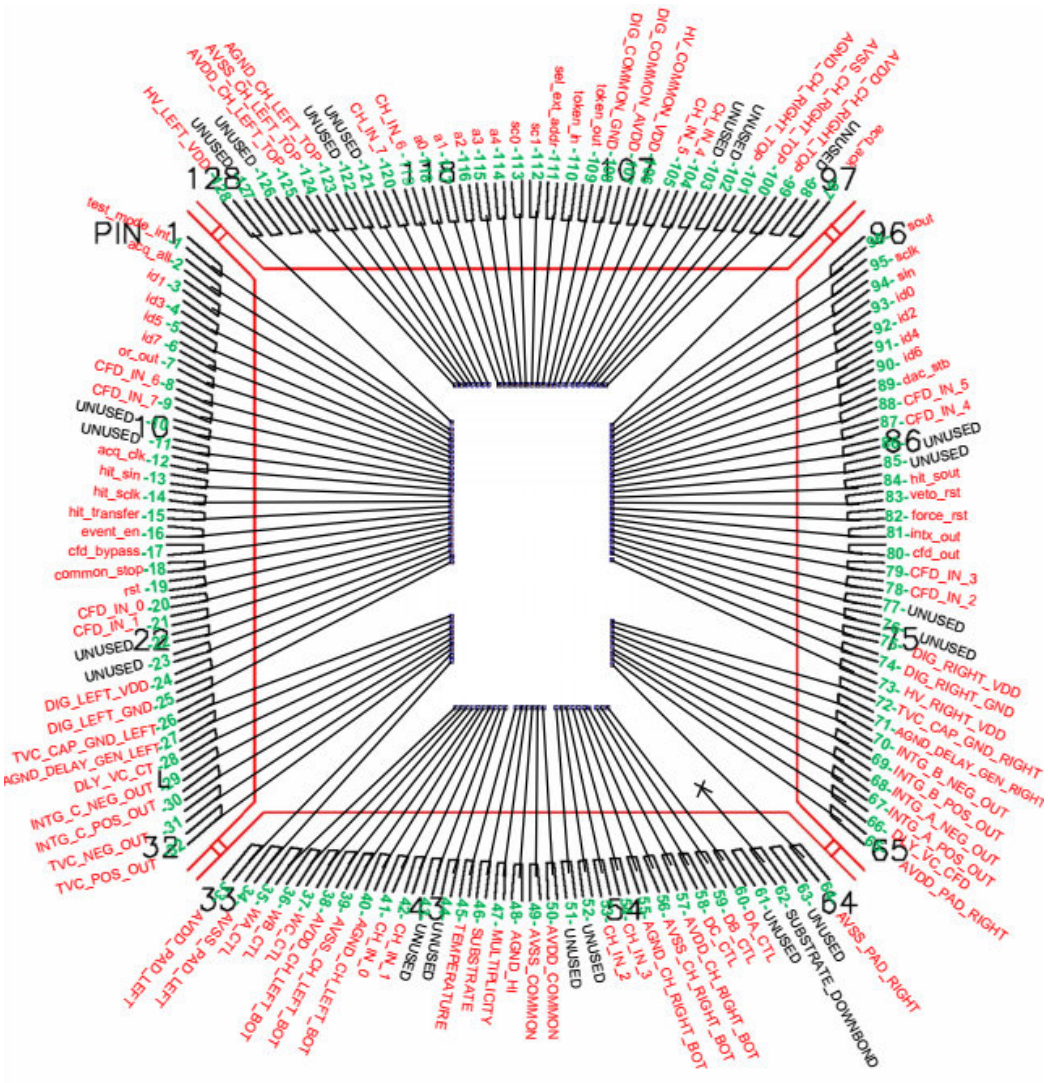
Simulation With Extracted Netlist of Full Chip!!!



Configuration Register Sucessfully Loaded!!!



Bonding Diagram



Summary

- PSD4 addresses issues with current PSD3
- Changes, while not trivial, are “safe”
- Scheduled for fabrication on Dec. 4, 2017
- Current plan is to purchase 160 packaged parts at a total cost of $42,900!