Schematic issues for version 5(latest version) of the chipboard schmatics.

Issue No.	Sheet Name	Symbol Name	Pin Number	Net Name	Status	Remarks
2	Trenz.Sch	J1	12	CFD_OUT	Unresolved	We might want a test pad for the CFD_OUT signal.
4	Trenz.Sch	J1	??	BUSY_OUT_L	Unresolved	Missing output pin assignment for the busy_out_L signal.
5	Trenz.Sch	JB3	26	BUSY_IN	Unresolved	This signal no longer exists. Pin should be no connect.
6	Trenz.Sch	JB1	84	TEST_MODE_INT_0**	Unresolved	The corrected net name is TEST_MODE_INT_1.
7	Trenz.Sch	JB1	90	JTAGSEL	Unresolved	This pin needs to be pulled down to GND.
8	Trenz.Sch	JB1	27	SC_EN1	New	Connect pull up to 3v3
9	Trenz.Sch	JB1	29	SC_PGOOD	New	Output signal from trenz board, can be NC
10	Trenz.Sch	JB1	31	SC_BOOTMODE	New	Connect pull up to 3v3
11	Trenz.Sch	JB2	17	SC_nRST	New	We should use this as a reset. Pull up to 3v3 in normaly open state, momentary switch to gnd.
12	Trenz.Sch	JB2	92	PWR_JTAG	New	Output Pin, for JTAG reference voltage (3.3V) we can leave it NC or expose it via the JTAG port on the board
13	Trenz.Sch	JB2	46	PSD_DAC_STB_1	Unresolved	Should not exist, this should be a NC.
14	Trenz.Sch	JB2	62	PSD_GLBL_ENBL	Unresolved	Should not exist, this should be a NC.
15	Trenz.Sch	JB2	76	DAC_DIN	Unresolved	Should not exist, this should be a NC.
26	Trenz.Sch	PSD2_2	HIT_XFER	HIT_XFER_1	Unresolved	Don't see this net connected to any FPGA pin assignment.
27	Trenz.Sch	PSD2_3	HIT_XFER	HIT_XFER_1	Unresolved	Don't see this net connected to any FPGA pin assignment.
29	Trenz.Sch	JB2	27-28,31-36	LE[0:7]	Unresolved	Should be NC, since we don't plan to use LE signals
32	Trenz.Sch	JB2	27	DELAY_CLK	New	This pin needs to be connected to net DELAY_CLK
33	Trenz.Sch	JB2	28	DELAY_DATA	New	This pin needs to be connected to net DELAY_DATA
34	Trenz.Sch	JB2	31-36	DELAY_EN_L_<0:5>	New	Connect pins to nets DELAY_EN_L_[0:5]
35	Trenz.Sch	JB2	37-38	MUX_SEL_<0:1>	New	Connect pins to nets MUX_SEL_[0:1]
36	Trenz.Sch	JB2	41-42	MUX_SEL_<2:3>	New	Connect pins to nets MUX_SEL_[2:3]
37	Trenz.Sch	JB2	43	MUX_EN	New	Connect pin to net MUX_EN
38	TREnz.Sch	JB1	10,12	VCCIOA	New	The VCCIO bank voltages should be referenced using the onboard 3v3 output reference that is exposed on PWR_M1. Connect to pins JB2-9 and JB2-11
39	TREnz.Sch	JB2	2,4,8,10	VCCIOB, VCCIOD	New	The VCCIO bank voltages should be referenced using the onboard 3v3 output reference that is exposed on PWR_M1. Connect to pins JB2-9 and JB2-11
20	PSD2_3.SCH	PSD4-U5	80	NC	Unresolved	This should not be NC. It should be an output connected to PSD_CFD_OUT_1
21	PSD2_3.SCH	PSD4-U5	1	TEST_INT	Unresolved	Currently pulled up to 3v3. This should be connected to psd_test_mode_int_1
22	PSD2_3.SCH	PSD4-U5	47	SUM2	Unresolved	This should be NC since we plan to use the multiplicity from CFD
23	PSD2_2.SCH	PSD4-U4	80	CFD_OUT	Unresolved	This should not be a testpoint. It should be an output connected to PSD_CFD_OUT_0
24	PSD2_2.SCH	PSD4-U4	1	TEST_INT	Unresolved	Currently pulled up to 3v3. This should be connected to psd_test_mode_int_1
25	PSD2_2.SCH	PSD4-U4	47	SUM1	Unresolved	This should be NC since we plan to use the multiplicity from CFD
31	DELAY.SCH	U8-13	7	CENABLE	Unresolved	The 2015 Datasheet https://www.renesas.com/us/en/document/dst/isl59920-isl59921-isl59922-isl59923-datasheet, recommends a power on delay circuit.
16	CFD.SCH	CFD2-U102	50	AGND_DSBL	Unresolved	Currently Grounded, this should be a jumper to VCC or GND to enable or disable internal AGND generator. Active High to disable.
17	CFD.SCH	CFD2-U102	21,43	AGND	Unresolved	External AGND is generated but is not needed since previous tests show internal AGND is better. We should just keep the C18, C21 caps.
18	CFD.SCH	CFD2-U102	58	TEST_P	Unresolved	TEST_P is an output pin. Current connection is a jumper direct to GND.
19	CFD.SCH	CFD2-U102	40	MULT	Unresolved	Incorrect Net, should be connected to CFD_MULT.