An Improved Pulse Shape Discriminator IC

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Introduction

This paper describes the 4th generation PSD IC which was submitted for fabrication on Dec. 4, 2017.

Description

Conclusions

PIN DESCRIPTIONS

- **NUMBER** 1
  NAME *test_mode_int*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Active HIGH. Places chip into test mode. The selected channel/sub-channel integrator output is routed to the *intx_out* pin (i.e. pin 81).

- **NUMBER** 2
  NAME *acq_all*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Positive going pulse will set the hit register in each of the channels. This is useful if the user want to force the acquisition of **all** channels on the chip.

- **NUMBER** 3
  NAME *id[1]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION Bit 1 of the chip ID bus. When the *sel_ext_addr* is HIGH, the pin is an input. A 10 kΩ pull-down HY-poly resistor ($\frac{5\mu m}{50\mu m}$) is connected internally from the pad to GND.

- **NUMBER** 4
  NAME *id[3]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION Bit 3 of the chip ID bus. When the *sel_ext_addr* is HIGH, the pin is an input. A 10 kΩ pull-down HY-poly resistor ($\frac{5\mu m}{50\mu m}$) is connected internally from the pad to GND.

- **NUMBER** 5
  NAME *id[5]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION Bit 5 of the chip ID bus. When the *sel_ext_addr* is HIGH, the pin is an input. A 10 kΩ pull-down HY-poly resistor ($\frac{5\mu m}{50\mu m}$) is connected internally from the pad to GND.

- **NUMBER** 6
  NAME *id[7]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION Bit 7 of the chip ID bus. When the *sel_ext_addr* is HIGH, the pin is an input. A 10 kΩ pull-down HY-poly resistor ($\frac{5\mu m}{50\mu m}$) is connected internally from the pad to GND.

- **NUMBER** 7
  NAME *or_out*
  TYPE Digital Output Pin (3.3 V Logic Level)
  DESCRIPTION This pin is HIGH if one or more ”hit” registers on the IC are set.

- **NUMBER** 8
  NAME *CFD_IN[6]*
  TYPE Digital Input (3.3 V Logic Level)
  DESCRIPTION CFD input for channel 6.

- **NUMBER** 9
  NAME *CFD_IN[7]*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION CFD input for channel 7.

- **NUMBER** 10
  NAME *UNUSED*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION This is an unused Digital Input pad. It should not be allowed to float. The input pin should be grounded.

- **NUMBER** 11
  NAME *UNUSED*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION This is an unused Digital Input pad. It should not be allowed to float. The input pin should be grounded. Allows for expansion to 16 channels.

- **NUMBER** 12
  NAME *acq_clk*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION This is the clock signal used for data acquisition. The rising edge causes the ”active” register to be set in a channel whose ”hit” register is set AND whose ”token_in” signal is active i.e. LOW. The falling edge of ”acq_clk” in turn causes the ”hit” register to be cleared. This in turn will potentially allow the ”token_out” of the channel to be active i.e. LOW; thereby, enabling the next channel in the chain. The next rising edge of ”acq_clk” will clear the active register.

- **NUMBER** 13
  NAME *hit_sin*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Serial input to the shadow register. Data on the ”hit_sin” pin must be valid on the rising edge of the ”hit_sclk”.

- **NUMBER** 14
  NAME *hit_sclk*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Serial clock for the shadow register. Data on the ”hit_sin” pin must be stable and valid on the rising edge of ”hit_sclk”.

- **NUMBER** 15
  NAME *hit_transfer*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Shadow register transfer signal. A rising edge on this pin will cause the contents of the shadow register to be transferred into the hit register.

- **NUMBER** 16
  NAME *event_en*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION This is an externally generated timing signal. For triggering mode 1 and mode 2, timing is relative to the ”event_en” signal. For triggering mode 3, timing is relative to the CFD_i signal.

- **NUMBER** 17
  NAME *cfd_bypass*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION CFD bypass signal. This pin allows the CFD_i hit signals to be bypassed, allowing the externally generated ”event_en” signal to determine the timing of the sub-channel integrators.

- **NUMBER** 18
  NAME *common_stop*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION When HIGH, halts the time-to-voltage converter in all channels. Once asserted it must remain asserted until channels are reset. If not, the TVCs can re-start. Whenever HIGH, the TVCs can not start.

- **NUMBER** 19
  NAME *rst*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Master reset. Resets all of the digital logic. All bits of the configuration register are cleared. All of the DAC registers on the chip are also cleared.

- **NUMBER** 20
  NAME *CFD_IN[0]*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION CFD input for channel 0.

- **NUMBER** 21
  NAME *CFD_IN[1]*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION CFD input for channel 1.

- **NUMBER** 22
  NAME *UNUSED*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION This is an unused Digital Input pad. It should not be allowed to float. The input pin should be grounded.

- **NUMBER** 23
  NAME *UNUSED*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION This is an unused Digital Input pad. It should NOT be allowed to float. The input pin should be grounded.

- **NUMBER** 24
  NAME *DIG_LEFT_VDD*
  TYPE 3.3 Volt Power Pin
  DESCRIPTION Connect to +3.3 Volts. The pin supplies 3.3 Volts to the digital pads on the left side of the chip.

- **NUMBER** 25
  NAME *DIG_LEFT_GND*
  TYPE Ground Pin
  DESCRIPTION Connect to ground. The pin is ground for the digital pads on the left side of the chip.

- **NUMBER** 26
  NAME *TVC_CAP_GND_LEFT*
  TYPE Analog Pin
  DESCRIPTION This is the signal return line for the capacitors in the TVC circuits (Channels 0, 1, 6, and 7) on the left side of the chip.

- **NUMBER** 27
  NAME *AGND_DELAY_GEN_LEFT*
  TYPE Analog Pin
  DESCRIPTION This is the AGND signal that is used by the gate generators (Channels 0, 1, 6, and 7) on the left side of the chip.

- **NUMBER** 28
  NAME *DLY_VC_CTL*
  TYPE Analog Pin
  DESCRIPTION Control voltage that determines the time delay between a channel being hit and the automatic reset of the time-to-voltage converter, integrators, and the active and hit registers in that channel. This signal is common to all channels on the IC.

- **NUMBER** 29
  NAME *INTEG_C_NEG_OUT*
  TYPE Analog Pin
  DESCRIPTION The C integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is bought off-chip differentially. This is the inverting (-) output. It should be connected to the (-) input on the off-chip ADC.

- **NUMBER** 30
  NAME *INTEG_C_POS_OUT*
  TYPE Analog Pin
  DESCRIPTION The C integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is bought off-chip differentially. This is the non-inverting (+) output. It should be connected to the (+) input on the off-chip ADC.

- **NUMBER** 31
  NAME *TVC_NEG_OUT*
  TYPE Analog Pin
  DESCRIPTION The TVC outputs from the 8 channels are multiplexed to this pin. The integrator output is bought off-chip differentially. This is the inverting (-) output. It should be connected to the (-) input on the off-chip ADC.

- **NUMBER** 32
  NAME *TVC_POS_OUT*
  TYPE Analog Pin
  DESCRIPTION The TVC outputs from the 8 channels are multiplexed to this pin. The integrator output is bought off-chip differentially. This is the non-inverting (+) output. It should be connected to the (+) input on the off-chip ADC.

- **NUMBER** 33
  NAME *AVDD_PAD_LEFT*
  TYPE 5 V Power Pin
  DESCRIPTION Connect to + 5 V. This pin supplies power to analog pads located in lower left of pad frame.

- **NUMBER** 34
  NAME *AVSS_PAD_LEFT*
  TYPE Ground Pin
  DESCRIPTION Connect to ground. This pin supplies ground to analog pads located in lower left of pad frame.

- **NUMBER** 35
  NAME *WA_CTL*
  TYPE Analog Pin
  DESCRIPTION Control voltage used to determine width of integration for the A integrators for all channels on the chip.

- **NUMBER** 36
  NAME *WB_CTL*
  TYPE Analog Pin
  DESCRIPTION Control voltage used to determine width of integration for the B integrators for all channels on the chip.

- **NUMBER** 37
  NAME *WC_CTL*
  TYPE Analog Pin
  DESCRIPTION Control voltage used to determine width of integration for the C integrators for all channels on the chip.

- **NUMBER** 38
  NAME *AVDD_CH_LEFT_BOT*
  TYPE 5 V Power Pin
  DESCRIPTION Connect to +5 V. Supplies power to channels 0 and 1.

- **NUMBER** 39
  NAME *AVSS_CH_LEFT_BOT*
  TYPE Ground Pin
  DESCRIPTION Connect to ground. Supplies ground to channels 0 and 1.

- **NUMBER** 40
  NAME *AGND_CH_LEFT_BOT*
  TYPE Analog Pin
  DESCRIPTION This is the AGND return line for the DACd in channels 0 and 1. There are 6 separate lines from the sub-channels which connect at this pad. This was done to minimize cross-talk.

- **NUMBER** 41
  NAME *CH_IN[0]*
  TYPE Analog Pin
  DESCRIPTION Channel 0 detector input.

- **NUMBER** 42
  NAME *CH_IN[1]*
  TYPE Analog Pin
  DESCRIPTION Channel 1 detector input.

- **NUMBER** 43
  NAME *UNUSED*
  TYPE Analog Pin
  DESCRIPTION This is an unused analog pad and should be connected to ground.

- **NUMBER** 44
  NAME *UNUSED*
  TYPE Analog Pin
  DESCRIPTION This is an unused analog pad and should be connected to ground.

- **NUMBER** 45
  NAME *TEMP*
  TYPE Analog Pin
  DESCRIPTION This pin can be used to infer die temperature. There is a vertical parasitic PNP transistor that is diode-connected on the chip. The user should supply a 25 μA constant current (with a zero tempco) to this pin. The voltage on the pin will display a tempco of approximately $\frac{-2mV}{C}$. Ground if NOT using this feature.

- **NUMBER** 46
  NAME *SUBSTRATE*
  TYPE Analog Pin
  DESCRIPTION Connection to the substrate. Attach to ground.

- **NUMBER** 47
  NAME *MULTIPLICITY*
  TYPE Analog Pin
  DESCRIPTION Analog output voltage proportional to the number of channels whose hit registers are set.

- **NUMBER** 48
  NAME *AGND_HI*
  TYPE Analog Pin
  DESCRIPTION This is analog signal ground for high impedance points so approximately 0 current flows in this line.

- **NUMBER** 49
  NAME *AVSS_COMMON*
  TYPE Ground Pin
  DESCRIPTION This is the ground line for the analog circuits in the center ”common” channel.

- **NUMBER** 50
  NAME *AVDD_COMMON*
  TYPE 5 V Power Pin
  DESCRIPTION Connect to 5 V. The pin provides power for the analog circuits in the center ”common” channel.

- **NUMBER** 51
  NAME *UNUSED*
  TYPE Analog Pin
  DESCRIPTION Connect to ground.

- **NUMBER** 52
  NAME *UNUSED*
  TYPE Analog Pin
  DESCRIPTION Connect to ground.

- **NUMBER** 53
  NAME *CH_IN[2]*
  TYPE Analog Pin
  DESCRIPTION Channel 2 detector input

- **NUMBER** 54
  NAME *CH_IN[3]*
  TYPE Analog Pin
  DESCRIPTION Channel 3 detector input

- **NUMBER** 55
  NAME *AGND_CH_RIGHT_BOT*
  TYPE Analog Pin
  DESCRIPTION This is the AGND return line for the DACs in channels 2 and 3. There are 6 separate lines from the sub-channels which connect at this pad. This was done to minimize cross-talk.

- **NUMBER** 56
  NAME *AVSS_CH_RIGHT_BOT*
  TYPE Ground Pin
  DESCRIPTION Connect to ground. This pin supplies ground to channels 2 and 3.

- **NUMBER** 57
  NAME *AVDD_CH_RIGHT_BOT*
  TYPE 5 V Supply Pin
  DESCRIPTION Connect to +5 V. This pin supplies power for channels 2 and 3.

- **NUMBER** 58
  NAME *DC_CTL*
  TYPE Analog Pin
  DESCRIPTION Control voltage for delay of sub-channel C. For triggering modes 1 and 2, the delay is relative to the "event_en" signal. For triggering mode 3, the delay is relative to the CFD_i signal.

- **NUMBER** 59
  NAME *DB_CTL*
  TYPE Analog Pin
  DESCRIPTION Control voltage for delay of sub-channel B. For triggering modes 1 and 2, the delay is relative to the "event_en" signal. For triggering mode 3, the delay is relative to the CFD_i signal.

- **NUMBER** 60
  NAME *DA_CTL*
  TYPE Analog Pin
  DESCRIPTION Control voltage for delay of sub-channel A. For triggering modes 1 and 2, the delay is relative to the "event_en" signal. For triggering mode 3, the delay is relative to the CFD_i signal.

- **NUMBER** 61
  NAME *UNUSED*
  TYPE NO PAD at this location
  DESCRIPTION We recommend that the pin be grounded but since there is NO pad at the site, connecting the pin to ground is optional.

- **NUMBER** 62
  NAME *DOWNBOND*
  TYPE NO PAD at this location
  DESCRIPTION Connect to ground. This connects the underside of the die to ground. This pin MUST BE GROUNDED!

- **NUMBER** 63
  NAME *UNUSED*
  TYPE NO PAD at this location
  DESCRIPTION We recommend that the pin be grounded but since there is NO pad at the site, connecting the pin to ground is optional.

- **NUMBER** 64
  NAME *AVSS_PAD_RIGHT*
  TYPE Ground Pin
  DESCRIPTION Connect to ground. This pin is the ground for the analog pads located in the lower right of the pad frame.

- **NUMBER** 65
  NAME *AVDD_PAD_RIGHT*
  TYPE 5 V Power Pin
  DESCRIPTION Connect to +5 V. This pin supplies power to the analog pads located in the lower right of the pad frame.

- **NUMBER** 66
  NAME *DLY_VC_CFD*
  TYPE Analog Pin
  DESCRIPTION Control voltage for the one-shot which sets the duration of the reset pulse associated with the automatic reset circuit.

- **NUMBER** 67
  NAME *INTEG_A_POS_OUT*
  TYPE Analog Pin
  DESCRIPTION The A integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off-chip differentially. This is the non-inverting (+) output and should be connected to (+) input on off-chip ADC.

- **NUMBER** 68
  NAME *INTEG_A_NEG_OUT*
  TYPE Analog Pin
  DESCRIPTION The A integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off-chip differentially. This is the inverting (-) output and should be connected to (-) input on off-chip ADC.

- **NUMBER** 69
  NAME *INTEG_B_POS_OUT*
  TYPE Analog Pin
  DESCRIPTION The B integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off-chip differentially. This is the non-inverting (+) output and should be connected to (+) input on off-chip ADC.

- **NUMBER** 70
  NAME *INTEG_B_NEG_OUT*
  TYPE Analog Pin
  DESCRIPTION The B integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off-chip differentially. This is the inverting (-) output and should be connected to (-) input on off-chip ADC.

- **NUMBER** 71
  NAME *AGND_DELAY_GEN_RIGHT*
  TYPE Analog Pin
  DESCRIPTION This is the AGND signal that is used by the gate generators in the channels (2, 3, 4, and 5) on the right side of the IC.

- **NUMBER** 72
  NAME *TVC_CAP_GND_RIGHT*
  TYPE Analog Pin
  DESCRIPTION This is the ground return line for the capacitors in the TVC circuits on the right side of the chip (channels 2, 3, 4, and 5).

- **NUMBER** 73
  NAME *HV_RIGHT_VDD*
  TYPE 5 V Power Pin
  DESCRIPTION Connect to +5 V. This is the power connection for the level translation circuits.

- **NUMBER** 74
  NAME *DIG_RIGHT_GND*
  TYPE Ground Pin
  DESCRIPTION Connect to ground. This is the ground connection for the digital pads on the right-side of the chip.

- **NUMBER** 75
  NAME *DIG_RIGHT_VDD*
  TYPE 3.3 V Power Pin
  DESCRIPTION Connect to +3.3 V. This is the power connection for the digital pads on the right-side of the chip.

- **NUMBER** 76
  NAME *UNUSED*
  TYPE Digital Input Pin
  DESCRIPTION Connect to ground.

- **NUMBER** 77
  NAME *UNUSED*
  TYPE Digital Input Pin
  DESCRIPTION Connect to ground.

- **NUMBER** 78
  NAME *CFD_IN[2]*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION CFD input for channel 2.

- **NUMBER** 79
  NAME *CFD_IN[3]*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION CFD input for channel 3.

- **NUMBER** 80
  NAME *cfd_out*
  TYPE Digital Output Pin (3.3 V Logic Level)
  DESCRIPTION This is the output (for the selected channel) of the 100 ns one-shot that is triggered by the narrow output pulse from the CFD. The CFD outputs from all 8 channels are multiplexed to this pin.

- **NUMBER** 81
  NAME *intx_out*
  TYPE Digital Output Pin (3.3 V Logic Level)
  DESCRIPTION When the ”test_mode_int” (pin 1) is HIGH, the integration region of the channel/sub-channel currently selected is routed out to this pin. The user should trigger their oscilloscope using either the ”event_en” or CFD_i signal (applied to channel 1 of the scope) and then observe the ”intx_out” signal on channel 2 of the scope.

- **NUMBER** 82
  NAME *force_rst*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION A positive-going pulse on this line will reset the time-to-voltage converter and integrators as well as the hit and active registers in ALL channels.

- **NUMBER** 83
  NAME *veto_rst*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION After a channel has been hit, the time-to-voltage converter and the the integrators as well as the his and active registers will be automatically reset **UNLESS** ”veto_rst” is asserted (brought HIGH). The ”veto_rst” signal must continue to be asserted until the time when the automatic reset would have taken place.

- **NUMBER** 84
  NAME *hit_sout*
  TYPE Digital Output Pin (3.3 V Logic Level)
  DESCRIPTION Serial output of the shadow register.

- **NUMBER** 85
  NAME *UNUSED*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Connect to ground.

- **NUMBER** 86
  NAME *UNUSED*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Connect to ground.

- **NUMBER** 87
  NAME *CFD_IN[4]*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION CFD input for channel 4.

- **NUMBER** 88
  NAME *CFD_IN[5]*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION CFD input for channel 5.

- **NUMBER** 89
  NAME *dac_stb*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Data on the address pins ($a_0 - a_5$) are latched into an internal address latch on the rising edge of "dac_stb". When "dac_stb" is HIGH, data on the address lines will alter the DAC output whose channel is selected by the address stored in the internal address latch. On the falling edge, the data on the address pins will be latched into the DAC latch. **IMPORTANT**: Data on the address lines must be stable and valid on both rising and falling edge of "dac_stb".

- **NUMBER** 90
  NAME *id[6]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION Bit 6 of the chip ID bus. When the *sel_ext_addr* is HIGH, the pin is an input. A 10 kΩ pull-down HY-poly resistor ($\frac{5\mu m}{50\mu m}$) is connected internally from the pad to GND.

- **NUMBER** 91
  NAME *id[4]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION Bit 4 of the chip ID bus. When the *sel_ext_addr* is HIGH, the pin is an input. A 10 kΩ pull-down HY-poly resistor ($\frac{5\mu m}{50\mu m}$) is connected internally from the pad to GND.

- **NUMBER** 92
  NAME *id[2]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION Bit 2 of the chip ID bus. When the *sel_ext_addr* is HIGH, the pin is an input. A 10 kΩ pull-down HY-poly resistor ($\frac{5\mu m}{50\mu m}$) is connected internally from the pad to GND.

- **NUMBER** 93
  NAME *id[0]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION Bit 0 of the chip ID bus. When the *sel_ext_addr* is HIGH, the pin is an input. A 10 kΩ pull-down HY-poly resistor ($\frac{5\mu m}{50\mu m}$) is connected internally from the pad to GND.

- **NUMBER** 94
  NAME *sin*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Serial input to the 48-bit on-chip configuration register. Data on the ”sin” pin must be stable and valid on the rising edge of ”sclk”.

- **NUMBER** 95
  NAME *sclk*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION Serial clock to the 48-bit on-chip configuration register. Data on the ”sin” pin must be stable and valid on the rising edge of ”sclk”.

- **NUMBER** 96
  NAME *sout*
  TYPE Digital Output Pin (3.3 V Logic Level)
  DESCRIPTION Serial output of the 48-bit configuration register.

- **NUMBER** 97
  NAME *acq_ack*
  TYPE Digital Output Pin (3.3 V Logic Level)
  DESCRIPTION The ”acq_ack” pin will be HIGH during the acquisition process and will go LOW once all channels have been acquired.

- **NUMBER** 98
  NAME *UNUSED*
  TYPE NO PAD at this location
  DESCRIPTION There is NO pad at this location but we still recommend grounding the pin.

- **NUMBER** 99
  NAME *AVDD_CH_RIGHT_TOP*
  TYPE 5 V Power Pin
  DESCRIPTION Connect to 5 V. This pin provides power to channels 4 and 5.

- **NUMBER** 100
  NAME *AVSS_CH_RIGHT_TOP*
  TYPE Ground Pin
  DESCRIPTION Connect to ground. This pin provides power to channels 4 and 5.

- **NUMBER** 101
  NAME *AGND_CH_RIGHT_TOP*
  TYPE Analog Pin
  DESCRIPTION This is the AGND return line for the DACs in channels 4 and 5.

- **NUMBER** 102
  NAME *UNUSED*
  TYPE Analog Pin
  DESCRIPTION We recommend that this unused pin be connected to ground.

- **NUMBER** 103
  NAME *UNUSED*
  TYPE Analog Pin
  DESCRIPTION We recommend that this unused pin be connected to ground.

- **NUMBER** 104
  NAME *CH_IN[4]*
  TYPE Analog Pin
  DESCRIPTION Channel 4 detector input..

- **NUMBER** 105
  NAME *CH_IN[5]*
  TYPE Analog Pin
  DESCRIPTION Channel 5 detector input.

- **NUMBER** 106
  NAME *HV_COMMON_VDD*
  TYPE 5 V Power Pin
  DESCRIPTION Connect to +5 V. This pin powers all digital circuits in the ”common” channel. It also supplies power to the level translators in digital pads on top side of IC

- **NUMBER** 107
  NAME *DIG_COMMON_VDD*
  TYPE 3.3 V Power Pin
  DESCRIPTION Connect to +3.3 V. This pin supplies power to digital pads along top of IC.

- **NUMBER** 108
  NAME *DIG_COMMON_GND*
  TYPE Ground Pin
  DESCRIPTION Connect to ground. This pin supplies ground to digital pads along top of IC.

- **NUMBER** 109
  NAME *token_out*
  TYPE Digital Output Pin(3.3 V Logic Level)
  DESCRIPTION This is the token out of the chip. It is active LOW. When the line is HIGH, an acquisition is in progress.

- **NUMBER** 110
  NAME *token_in*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION This is the token into the chip. It is active LOW.

- **NUMBER** 111
  NAME *sel_ext_addr*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION When HIGH, this signal selects the externally supplied address as input to the decoder used for selecting on of the 8 channels. When HIGH, makes $a_0 - a_4$ as well as $id_0 - id_7$ inputs to the IC.

- **NUMBER** 112
  NAME *sc[1]*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION This is external sub-address line sc_1. This is the most significant bit of the sub-channel address the user would like to select.

- **NUMBER** 113
  NAME *sc[0]*
  TYPE Digital Input Pin (3.3 V Logic Level)
  DESCRIPTION This is external sub-address line sc_0. This is the least significant bit of the sub-channel address the user would like to select.

- **NUMBER** 114
  NAME *a[4]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION This is external address line a_4.

- **NUMBER** 115
  NAME *a[3]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION This is external address line a_3.

- **NUMBER** 116
  NAME *a[2]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION This is external address line a_2.

- **NUMBER** 117
  NAME *a[1]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION This is external address line a_1.

- **NUMBER** 118
  NAME *a[0]*
  TYPE Bi-Directional Pin (3.3 V Logic Level)
  DESCRIPTION This is external address line a_0.

- **NUMBER** 119
  NAME *CH_IN[6]*
  TYPE Analog Pin
  DESCRIPTION Channel 6 detector input.

- **NUMBER** 120
  NAME *CH_IN[7]*
  TYPE Analog Pin
  DESCRIPTION Channel 7 detector input.

- **NUMBER** 121
  NAME *UNUSED*
  TYPE Analog Pin
  DESCRIPTION We recommend that this unused pad be connected to ground.

- **NUMBER** 122
  NAME *UNUSED*
  TYPE Analog Pin
  DESCRIPTION We recommend that this unused pad be connected to ground.

- **NUMBER** 123
  NAME *AGND_CH_LEFT_TOP*
  TYPE Analog Pin
  DESCRIPTION This is the AGND return line for the DACs in channels 6 and 7.

- **NUMBER** 124
  NAME *AVSS_CH_LEFT_TOP*
  TYPE Ground Pin
  DESCRIPTION Connect to ground. The pin supplies ground to channels 6 and 7.

- **NUMBER** 124
  NAME *AVDD_CH_LEFT_TOP*
  TYPE +5 V Supply Pin
  DESCRIPTION Connect to +5 V. The pin supplies power to channels 6 and 7.

- **NUMBER** 125
  NAME *UNUSED*
  TYPE NO PAD at this location
  DESCRIPTION While not absolutely necessary, we recommend grounding the pin.

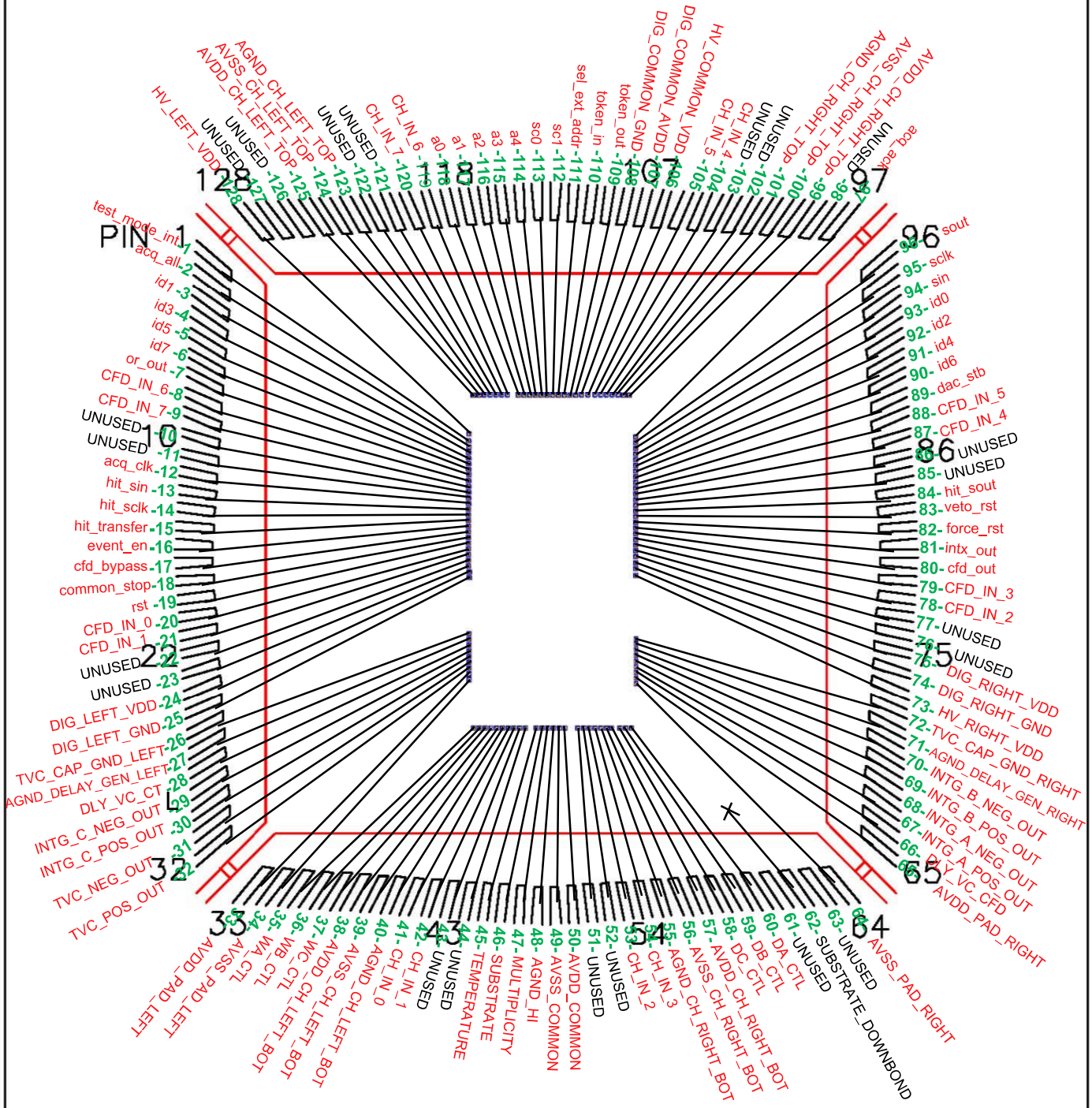
- **NUMBER** 126
  NAME *UNUSED*
  TYPE NO PAD at this location
  DESCRIPTION While not absolutely necessary, we recommend grounding the pin.

- **NUMBER** 127
  NAME *UNUSED*
  TYPE NO PAD at this location
  DESCRIPTION While not absolutely necessary, we recommend grounding the pin.

- **NUMBER** 128
  NAME *HV_LEFT_VDD*
  TYPE +5 V Supply Pin
  DESCRIPTION Connect to +5 V. The pin supplies power to the level translators on the left side of the IC.

TOP

PSDRev4_11/17/2017



LEFT

RIGHT

BOTTOM

√ CHECK PIN 1 DIE ORIENTATION WITH RESPECT TO WAFER FLAT

LEADFRAME:	LF1-H128-201
D/A PAD SIZE:	9.5mm X 9.5mm
SCALE:	DO NOT SCALE DRAWING

ECN#	REV.	DESCRIPTION	DATE		
98-101	A	NEW RELEASE	10/28/98	DRAWN: Laure Rezonable	DATE: 08/09/2000
00-148	B	CHANGED SCALE TO NC	08/04/00	CHECKED: George Fujimoto	DATE: 08/09/2000
				APPROVED:	DATE
				APPROVED:	DATE
				DWG. NUMBER: QFP-EDO-14SQ-128-01	
				ACAD FILENAME: B1281401.DWG	

TITLE:

BOND SHELL - 14X14X1.4/2.0 QFP, 128 LD

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