APPENDIX B

PSD8C Pin Descriptions (Final Pinout for PSD4)

8 – June - 2017

Pin number: 1
Pin name: test_mode_int
Pin type: digital input
Description: When test_mode_int (pin 128) is HIGH the integration region of the channel/sub-channel currently selected is routed to this pin. The user should trigger their oscilloscope using either the EventEn or CFD_i signal (applied to channel 1 of the scope) and then observe the intx_out signal on channel 2.

Pin number: 2
Pin name: acq_all
Pin type: digital input
Description: A positive going pulse will set the "hit" register in each of the channels. This can be useful if one wants to force the acquisition of **all** channels on the chip.

Pin number: 3
Pin name: id1
Pin type: bi-directional
Description: Bit 1 of the chip identification code. When "sel_ext_addr" is HIGH, id1 is an input.

Pin number: 4
Pin name: id3
Pin type: bi-directional
Description: Bit 3 of the chip identification code. When "sel_ext_addr" is HIGH, id3 is an input.

Pin number: 5
Pin name: id5
Pin type: bi-directional
Description: Bit 5 of the chip identification code. When "sel_ext_addr" is HIGH, id5 is an input.

Pin number: 6
Pin name: id7
Pin type: bi-directional
Description: Bit 7 of the chip identification code. When "sel_ext_addr" is HIGH, id5 is an input.

Pin number: 7
Pin name: or_out
Pin type: digital output
Description: The "or_out" pin will be HIGH if any hit register on the chip is set. A LOW on this pin indicates that NONE of the "hit" registers are set.

Pin number: 8
Pin name: CFD_IN_6
Pin type: digital input
Description: CFD input for channel 6

Pin number: 9
Pin name: CFD_IN_7
Pin type: digital input
Description: CFD input for channel 7

Pin number: 10
Pin name: N/A
Pin type: N/A
Description: UNUSED (Will be used for CFD input if we expand to 16 channels.)

Pin number: 11
Pin name: N/A
Pin type: N/A
Description: UNUSED (Will be used for CFD input if we expand to 16 channels.)

Pin number: 12
Pin name: acq_clk
Pin type: digital input
Description: This is the clock signal used for acquisition. The rising edge of "ack_clk" causes the active register to be set in a channel whose "hit" register is set AND whose "token_in" is active i.e. LOW. The falling edge of "acq_clk" in turn causes the "hit" register to be cleared. This in turn will potentially allow the "token_out" of the channel to be active i.e. LOW; thereby, enabling the next channel in the chain. The next rising edge of "acq_clk" will clear the active register.

Pin number: 13
Pin name: hit_sin
Pin type: digital input
Description: Serial input to the shadow register. Data on "hit_sin" pin must be valid on rising edge of "hit_sclk".

Pin number: 14
Pin name: hit_sclk
Pin type: digital input
Description: Serial clock for the shadow register. Data on "hit_sin" pin must be valid on rising edge of "hit_sclk".

Pin number: 15
Pin name: hit_transfer
Pin type: digital input
Description: Shadow register transfer signal. A rising edge on this pin will cause the contents of the shadow register to be transferred into the hit register.

Pin number: 16
Pin name: event_en
Pin type: digital input
Description: This is externally generated timing signal. For triggering mode 1 and 2, timing is relative to the EventEn signal. For triggering mode 3, timing is relative to the CFD_i signal.

Pin number: 17
Pin name: cfd_bypass
Pin type: digital input
Description: CFD bypass signal. This pin allows the CFD hit signals to be bypassed, allowing the externally generated EventEn signal to determine the timing of the sub-channel integrators.

Pin number: 18
Pin name: common_stop
Pin type: digital input
Description: When HIGH, halts the time-to-voltage converter in every channel. The time-to-voltage conversions will STOP even if the start conversion signal is still asserted.

Pin number: 19
Pin name: rst
Pin type: digital input
Description: Master reset. Resets all of the digital logic. All bits of the configuration register are cleared. All of the DAC registers on chip are also cleared.

Pin number: 20
Pin name: CFD_IN_0
Pin type: digital input
Description: CFD input for channel 0

Pin number: 21
Pin name: CFD_IN_1
Pin type: digital input
Description: CFD input for channel 1

Pin number: 22
Pin name: N/A
Pin type: N/A
Description: UNUSED (Will be used for CFD input if we expand to 16 channels.)

Pin number: 23
Pin name: N/A
Pin type: N/A
Description: UNUSED (Will be used for CFD input if we expand to 16 channels.)

Pin number: 24
Pin name: DIG_LEFT_VDD
Pin type: 3.3 Volt power pin
Description: Connect to +3.3 volts. This pin supplies power only to the digital pads on the left side of the chip.

Pin number: 25
Pin name: DIG_LEFT_GND
Pin type: Ground pin
Description: Connect to gnd. This pin supplies gnd only to the digital pads on the left side of the chip.

Pin number: 26
Pin name: TVC_CAP_GND_LEFT
Pin type: analog
Description: This is the return line for the capacitors in the TVC circuits on left side of the chip (channels 0, 1, 6, and 7).

Pin number: 27
Pin name: AGND_DELAY_GEN_LEFT
Pin type: analog
Description: This is the AGND signal that is used by the gate generators on left side of the IC *i.e.* channels 0, 1, 6, and 7.

Pin number: 28
Pin name: DLY_VC_CTL
Pin type: analog
Description: Control voltage that determines the time delay between a channel being hit and the automatic reset of the time-to-voltage converter, integrators, and the active and hit registers in that channel. This signal is common to all channels on the IC.

Pin number: 29
Pin name: INTG_C_POS_OUT
Pin type: analog
Description: The C integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off chip differentially. This is the (+) output.

Pin number: 30
Pin name: INTG_C_NEG_OUT
Pin type: analog
Description: The C integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off chip differentially. This is the (-) output.

Pin number: 31
Pin name: TVC_POS_OUT
Pin type: analog
Description: The TVC outputs from the 8 channels are multiplexed to this pin. The TVC output is brought off chip differentially. This is the (+) output.

Pin number: 32
Pin name: TVC_NEG_OUT
Pin type: analog
Description: The TVC outputs from the 8 channels are multiplexed to this pin. The TVC output is brought off chip differentially. This is the (-) output.

Pin number: 33
Pin name: AVDD_PAD_LEFT
Pin type: 5 Volt power pin
Description: Connect to +5V. This pin supplies power to just the analog pads located in lower left of pad frame.

Pin number: 34
Pin name: AVSS_PAD_LEFT
Pin type: Ground pin
Description: Connect to gnd. This pin supplies gnd to just the analog pads located in lower left of pad frame.

Pin number: 35

Pin name: WA_CTL
Pin type: analog
Description: Control voltage for width of integration for the A integrators for all channels on the chip.

Pin number: 36
Pin name: WB_CTL
Pin type: analog
Description: Control voltage for width of integration for the B integrators for all channels on the chip.

Pin number: 37
Pin name: WC_CTL
Pin type: analog
Description: Control voltage for width of integration for the C integrators for all channels on the chip.

Pin number: 38
Pin name: AVDD_CH_LEFT_BOT
Pin type: 5 Volt power pin
Description: Connect to +5 Volt. This supplies power to channels 0 and 1.

Pin number: 39
Pin name: AVSS_CH_LEFT_BOT
Pin type: Ground pin
Description: Connect to gnd. This supplies gnd to channels 0 and 1.

Pin number: 40
Pin name: AGND_CH_LEFT_BOT
Pin type: analog
Description: This is the AGND return line for the DACs in channel 0 and channel 1. There are 6 separate lines from sub-channels and they only connect at the pad. This was done to minimize cross-talk.

Pin number: 41
Pin name: CH_IN_0
Pin type: analog
Description: Channel 0 detector input

Pin number: 42
Pin name: CH_IN_1
Pin type: analog
Description: Channel 1 detector input

Pin number: 43
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 44
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 45
Pin name: TEMPERATURE
Pin type: analog
Description: This output can be used to infer die temperature. There is vertical parasitic PNP transistor that is diode connected on the chip. The user should supply a temperature–independent (10 - 100 □A) constant current to this pin. The voltage at this pin may then be measured prior to applying power to the chip. The voltage will display a temperature coefficient of -2 mV/C. For example, if after some time the voltage on this pin decreased by 20 mV, then one could infer that the die was at a temperature of 10 degrees celsius above ambient.

Pin number: 46
Pin name: SUBSTRATE
Pin type: analog
Description: This is our connection to the top-side of the global substrate. Connect the pin to gnd.

Pin number: 47
Pin name: MULTIPLICITY
Pin type: analog
Description: Analog output voltage proportional to the number of channels in which the hit registers are set.

Pin number: 48
Pin name: AGND_HI
Pin type: analog
Description: This is a high-impedance AGND line (no currents flow in it). Since the output buffers have both an NFET and a PFET input stage, the stage NOT used (as determined by the polarity bit in the configuration register) has its inputs connected to this AGND pin.

Pin number: 49

Pin name: AVSS_COMMON
Pin type: Ground pin
Description: Connect to gnd. This pin supplies gnd to the analog circuits in the “common” channel.

Pin number: 50
Pin name: AVDD_COMMON
Pin type: 5 Volt power pin
Description: Connect to +5 Volts. This pin powers the analog circuits in the “common” channel.

Pin number: 51
Pin name: N/A
Pin type: N/A
Description: Currently unused. This pin is reserved for future expansion.

Pin number: 52
Pin name: N/A
Pin type: N/A
Description: Current unused. This pin is reserved for future expansion.

Pin number: 53
Pin name: CH_IN_2
Pin type: analog
Description: Channel 2 detector input.

Pin number: 54
Pin name: CH_IN_3
Pin type: analog
Description: Channel 3 detector input.

Pin number: 55
Pin name: AGND_CH_RIGHT_BOT
Pin type: analog
Description: This is the AGND return line for the DACs in channel 2 and channel 3. There are 6 separate lines from the sub-channels and they only connect at this pad. This was done to minimize cross-talk.

Pin number: 56
Pin name: AVSS_CH_RIGHT_BOT
Pin type: Ground pin
Description: Connect to gnd. This supplies gnd to channels 2 and 3.

Pin number: 57

Pin name: AVDD_CH_RIGHT_BOT
Pin type: +5 Volt supply pin
Description: Connect to +5 Volts. This supplies power to channels 2 and 3.

Pin number: 58
Pin name: DC_CTL
Pin type: analog
Description: Control voltage for delay of subchannel C. For triggering mode 1 and 2, this is relative to the EventEn signal. For triggering mode 3, this is relative to the CFD hit signal.

Pin number: 59
Pin name: DB_CTL
Pin type: analog
Description: Control voltage for delay of subchannel B. For triggering mode 1 and 2, this is relative to the EventEn signal. For triggering mode 3, this is relative to the CFD hit signal.

Pin number: 60
Pin name: DA_CTL
Pin type: analog
Description: Control voltage for delay of subchannel A. For triggering mode 1 and 2, this is relative to the EventEn signal. For triggering mode 3, this is relative to the CFD hit signal.

Pin number: 61
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 62
Pin name: No pad.
Pin type: No pad.
Description: SUBSTRATE DOWNBOND. Connect to gnd.

Pin number: 63
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 64
Pin name: DLY_VC_CFD
Pin type: analog
Description: Control voltage for one-shot which set the duration of reset pluse. For avoiding channels being hited again while doing reset.

Pin number: 65

Pin name: AVSS_PAD_RIGHT
Pin type: Ground Pin
Description: Connect to gnd. This pin supplies gnd to just the analog pads located in lower right of pad frame.

Pin number: 66
Pin name: AVDD_PAD_RIGHT
Pin type: 5 Volt power pin
Description: Connect to +5V. This pin supplies power to just the analog pads located in lower right of pad frame.

Pin number: 67
Pin name: INTG_A_POS_OUT
Pin type: analog
Description: The A integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off chip differentially. This is the (+) output.

Pin number: 68
Pin name: INTG_A_NEG_OUT
Pin type: analog
Description: The A integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off chip differentially. This is the (-) output.

Pin number: 69
Pin name: INTG_B_POS_OUT
Pin type: analog
Description: The B integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off chip differentially. This is the (+) output.

Pin number: 70
Pin name: INTG_B_NEG_OUT
Pin type: analog
Description: The B integrator outputs from the 8 channels are multiplexed to this pin. The integrator output is brought off chip differentially. This is the (-) output.

Pin number: 71
Pin name: AGND_DELAY_GEN_RIGHT
Pin type: analog
Description: This is the AGND signal that is used by the gate generators on right side of the IC *i.e.* channels 2, 3, 4, and 5.

Pin number: 72
Pin name: TVC_CAP_GND_RIGHT
Pin type: analog
Description: This is the return line for the capacitors in the TVC circuits on right side of the chip (channels 2, 3, 4, and 5).

Pin number: 73
Pin name: HV_RIGHT_VDD
Pin type: 5 Volt power pin
Description: Connect to +5 Volts. This is the power connection for the digital pads on the right-side of the chip.

Pin number: 74
Pin name: DIG_RIGHT_GND
Pin type: Ground Pin
Description: Connect to gnd. This is the gnd connection for the digital pads on the right-side of the chip.

Pin number: 75
Pin name: DIG_RIGHT_VDD
Pin type: 3.3 Volt power pin
Description: Connect to +3.3 Volts. This is the power connection for the digital pads on the right-side of the chip

Pin number: 76
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 77
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 78
Pin name: CFD_IN_2
Pin type: digital input
Description: CFD input for channel 2

Pin number: 79
Pin name: CFD_IN_3
Pin type: digital input
Description: CFD input for channel 3

Pin number: 80

Pin name: cfd_out
Pin type: digital output
Description: This is the output (for the selected channel) of the 100 ns one-shot that is triggered by the narrow output pulse from the CFD. The CFD outputs from all 8 channels are multiplexed. This is the output of the multiplexer.

Pin number: 81
Pin name: intx_out
Pin type: digital output
Description: When test_mode_int (pin 128) is HIGH the integration region of the channel/sub-channel currently selected is routed to this pin. The user should trigger their oscilloscope using either the EventEn or CFD_i signal (applied to channel 1 of the scope) and then observe the intx_out signal on channel 2.

Pin number: 82
Pin name: force_rst
Pin type: digital input
Description: A positive going pulse on this line will reset the time-to-voltage and integrators as well as the hit and active registers in ALL channels.

Pin number: 83
Pin name: veto_rst
Pin type: digital input
Description: After a channel has been hit, the time-to-voltage and integrators as well as the hit and active registers will automatically be reset UNLESS "veto_rst" is asserted (HIGH). The "veto_rst" signal must continue to be asserted until the time when the automatic reset would have taken place.

Pin number: 84
Pin name: hit_sout
Pin type: digital output
Description: Serial output of the shadow register.

Pin number: 85
Pin name: N/A
Pin type: N/A
Description: UNUSED (Will be used for CFD input if we expand to 16 channels.)

Pin number: 86
Pin name: N/A
Pin type: N/A
Description: UNUSED (Will be used for CFD input if we expand to 16 channels.)

Pin number: 87
Pin name: CFD_IN_4
Pin type: digital input
Description: CFD input for channel 4

Pin number: 88
Pin name: CFD_IN_5
Pin type: digital input
Description: CFD input for channel 5

Pin number: 89
Pin name: dac_stb
Pin type: digital input
Description: Data on the address pins (a0-a5) are latched into an internal address latch on the rising edge of dac_stb. When dac_stb is high, data on the ext_addr lines will alter the DAC output whose channel is selected by the address stored in the internal address latch. On the falling edge the data on the address pins will be latched into the DAC register. IMPORTANT NOTE: Data on address lines a0-a5 must be stable and valid on both rising and falling edge of "dac_stb".

Pin number: 90
Pin name: id6
Pin type: bidirectional
Description: Bit 6 of the chip identification code. When "sel_ext_addr" is HIGH, id6 is an input.

Pin number: 91
Pin name: id4
Pin type: bidirectional
Description: Bit 4 of the chip identification code. When "sel_ext_addr" is HIGH, id4 is an input.

Pin number: 92
Pin name: id2
Pin type: bidirectional
Description: Bit 2 of the chip identification code. When "sel_ext_addr" is HIGH, id2 is an input.

Pin number: 93

Pin name: id0
Pin type: bidirectional
Description: Bit 0 of the chip identification code. When "sel_ext_addr" is HIGH, id0 is an input.

Pin number: 94
Pin name: sin
Pin type: digital input
Description: Serial input to 48-bit configuration register. Data on "sin" pin must be valid on rising edge of "sclk".

Pin number: 95
Pin name: sclk
Pin type: digital input
Description: Serial clock for 48-bit configuration register. Data on "sin" pin must be valid on rising edge of "sclk".

Pin number: 96
Pin name: sout
Pin type: digital output
Description: Serial output from 48-bit configuration register.

Pin number: 97
Pin name: acq_ack
Pin type: digital output
Description: The "acq_ack" pin will be HIGH during the acquisition process and will go LOW once all channels have been acquired.

Pin number: 98
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 99
Pin name: AVDD_CH_RIGHT_TOP
Pin type: +5 V supply pin
Description: Connect to +5 Volts. This supplies power to channels 4 and 5.

Pin number: 100

Pin name: AVSS_CH_RIGHT_TOP
Pin type: Ground pin
Description: Connect to gnd. This supplies gnd to channels 4 and 5.

Pin number: 101
Pin name: AGND_CH_RIGHT_TOP
Pin type: analog
Description: This is the AGND return line for the DACs in channel 4 and channel 5. There are 6 separate lines from the sub-channels and they only connect at this pad. This was done to minimize cross-talk.

Pin number: 102
Pin name: N/A
Pin type: analog
Description: UNUSED (Will be used for a channel input if we expand to 16 channels.)

Pin number: 103
Pin name: N/A
Pin type: analog
Description: UNUSED (Will be used for a channel input if we expand to 16 channels.)

Pin number: 104
Pin name: CH_IN_4
Pin type: analog input
Description: Channel 4 detector input

Pin number: 105
Pin name: CH_IN_5
Pin type: analog input
Description: Channel 5 detector input

Pin number: 106
Pin name: HV_COMMON_VDD
Pin type: +5 Volt power
Description: Connect to +5 Volts. This pin is used to power all digital circuits in the “common” channel.

Pin number: 107
Pin name: DIG_COMMON_AVDD
Pin type: +3.3 Volt power
Description: Connect to +3.3 Volts. This pin is used to power all digital circuits in the “common” channel.

Pin number: 108

Pin name: DIG_COMMON_GND
Pin type: Ground
Description: Connect to gnd. This pin is used to supply gnd to all digital circuits in the “common” channel.

Pin number: 109
Pin name: token_out
Pin type: digital output
Description: This is the token out of the chip. It is active LOW. When the line is high, an acquisition is in progress.

Pin number: 110
Pin name: token_in
Pin type: digital input
Description: This is the token into the chip. It is active LOW.

Pin number: 111
Pin name: sel_ext_addr
Pin type: digital input
Description: When HIGH, this signal selects the external address as input to the decoder used for selecting one of the 8 channels. When HIGH, makes a0-a4 lines as well as id0-id7 lines inputs.

Pin number: 112
Pin name: sc1
Pin type: digital input
Description: This is external address line sc0. This is the most significant bit of the address of the subchannel which the user wishes to select.

Pin number: 113
Pin name: sc0
Pin type: digital input
Description: This is external address line sc0. This is the least significant bit of the address of the subchannel which the user wishes to select. Sub-channel address 00 selects the A integrator, 01 selects the B integrator, and 10 selects the C integrator. The code 11 is currently unused.

Pin number: 114
Pin name: a4
Pin type: bidirectional
Description: This is external address line a4. See description for address line a0.

Pin number: 115

Pin name: a3
Pin type: bidirectional
Description: This is external address line a3. See description for address line a0.

Pin number: 116
Pin name: a2
Pin type: bidirectional
Description: This is external address line a2. See description for address line a0.

Pin number: 117
Pin name: a1
Pin type: bidirectional
Description: This is external address line a1. See description for address line a0.

Pin number: 118
Pin name: a0
Pin type: bidirectional
Description: This is external address line a0. When the "sel_ext_addr" pin is HIGH, this line will be a DIGITAL INPUT and is the least significant bit of the address of the channel the user wishes to select. When the "sel_ext_addr" pin is LOW, this line will be a DIGITAL OUTPUT and will be the least significant bit of the address of the channel that is currently in need of attention.

Pin number: 119
Pin name: CH_IN_6
Pin type: analog input
Description: Channel 6 detector input

Pin number: 120
Pin name: CH_IN_7
Pin type: analog input
Description: Channel 7 detector input

Pin number: 121
Pin name: N/A
Pin type: N/A
Description: UNUSED.

Pin number: 122
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 123

Pin name: AGND_CH_LEFT_TOP
Pin type: analog
Description: This is the AGND return line for the DACs in channel 6 and channel 7. There are 6 separate lines from the sub-channels and they only connect at this pad. This was done to minimize cross-talk.

Pin number: 124
Pin name: AVSS_CH_LEFT_TOP
Pin type: Ground pin
Description: Connect to gnd. This supplies gnd to channels 6 and 7.

Pin number: 125
Pin name: AVDD_CH_LEFT_TOP
Pin type: +5 Volt supply pin
Description: Connect to +5 Volts. This supplies power to channels 6 and 7.

Pin number: 126
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 127
Pin name: N/A
Pin type: N/A
Description: UNUSED

Pin number: 128
Pin name: HV_LEFT_VDD
Pin type: +5 Volt power
Description: Connect to +5 Volts. This is the power connection for the digital pads on the left-side of the chip.