GPIO	Dir	Bit	Nickname	Verilog Signal
0	in	0	>	board_id[0]
0	in	1	>	board_id[1]
0	in	2	>	board_id[2]
0	in	3	>	board_id[3]
0	in	4	>	board_id[4]
0	in	5	>	board_id[5]
0	in	6	>	common_stop
0	in	7	glob_ena	glob_ena_micro
0	in	8	event_ena	event_ena_micro
0	in	9	force_reset	force_reset_micro
0	in	10	take_event	take_event_micro
0	in	11	?	0
0	in	12	?	0
0	in	13	?	0
0	in	14	?	0
0	in	15	?	0
0	in	16	?	0
0	in	17	?	0
0	in	18	?	0
0	in	19	?	0
0	in	20	?	0
0	in	21	?	0
0	in	22	?	0
0	in	23	?	0
0	in	24	?	0
0	in	25	?	0
0	in	26	?	0
0	in	27	?	0
0	in	28	?	0
0	in	29	?	0
0	in	30	?	0
0	in	31	?	0
0	out	0	>	or_sel[0]
0	out	1	>	or_sel[1]
0	out	2	>	cfd_out_sel
0	out	3	>	psd_intx_out_sel
1	in	0	psd0_chan_addr_in_0	0
1	in	1	psd0_chan_addr_in_1	0
1	in	2	psd0_chan_addr_in_2	0
1	in	3	psd0_chan_addr_in_3	0
1	in	4	psd0_chan_addr_in_4	0
1	in	5	psd1_chan_addr_in_0	0
1	in	6	psd1_chan_addr_in_1	0
1	in	7	psd1_chan_addr_in_2	0
1	in	8	psd1_chan_addr_in_3	0
1	in	9	psd1_chan_addr_in_4	0

1	in	10	?	0
1	in	11	?	0
1	in	12	?	0
1	in	13	?	0
1	in	14	?	0
1	in	15	?	0
1	in	16	?	0
1	in	17	?	0
1	in	18	?	0
1	in	19	?	0
1	in	20	?	0
1	in	21	?	0
1	in	22	?	0
1	in	23	?	0
1	in	24	?	0
1	in	25	?	0
1	in	26	?	0
1	in	27	?	0
1	in	28	?	0
1	in	29	?	0
1	in	30	?	0
1	in	31	?	0
1	out	0	psd0_chan_addr_out_0	psd_addr_in_0_from_micro[0]
1	out	1	psd0_chan_addr_out_1	psd_addr_in_0_from_micro[1]
1	out	2	psd0_chan_addr_out_2	psd_addr_in_0_from_micro[2]
1	out	3	psd0_chan_addr_out_3	psd_addr_in_0_from_micro[3]
1	out	4	psd0_chan_addr_out_4	psd_addr_in_0_from_micro[4]
1	out	5	psd1_chan_addr_out_0	psd_addr_in_1_from_micro[0]
1	out	6	psd1_chan_addr_out_1	psd_addr_in_1_from_micro[1]
1	out	7	psd1_chan_addr_out_2	psd_addr_in_1_from_micro[2]
1	out	8	psd1_chan_addr_out_3	psd_addr_in_1_from_micro[3]
1	out	9	psd1_chan_addr_out_4	psd_addr_in_1_from_micro[4]
1	out	10	>	psd_global_enable_override
1	out	11	psd_force_rst	psd_force_reset_from_micro
1	out	12	psd_veto_reset	psd_veto_reset_from_micro
1	out	13	psd_reset	psd_reset_from_micro
2	in	0	>	psd_sout
2	in	1	?	0
2	in	2	?	0
2	in	3	?	0
2	in	4	?	0
2	in	5	?	0
2	in	6	?	0
2	in	7	?	0
2	in	8	?	0
2	in	9	?	0
2	in	10	?	0
2	in	11	?	0
2	in	12	?	0

2	in	13	?	0
2	in	14	?	0
2	in	15	?	0
2	in	16	?	0
2	in	17	?	0
2	in	18	?	0
2	in	19	?	0
2	in	20	?	0
2	in	21	?	0
2	in	22	?	0
2	in	23	?	0
2	in	24	?	0
2	in	25	?	0
2	in	26	?	0
2	in	27	?	0
2	in	28	?	0
2	in	29	?	0
2	in	30	?	0
2	in	31	?	0
2	out	0	busy_out	busy_out_micro
2	out	1	>	delay_data
2	out	2	>	delay_clk
2	out	3	>	delay_en_l[0]
2	out	4	>	delay_en_l[1]
2	out	5	>	delay_en_l[2]
2	out	6	>	delay_en_l[3]
2	out	7	>	delay_en_l[4]
2	out	8	>	delay_en_l[5]
2	out	9	>	mux_en
2	out	10	>	mux_sel[0]
2	out	11	>	mux_sel[1]
2	out	12	>	mux_sel[2]
2	out	13	>	mux_sel[3]
2	out	14	>	dac_ld
2	out	15	>	dac_sclk
2	out	16	>	dac_din
2	out	17	>	psd_dac_stb_0
2	out	18	>	psd_dac_stb_1
2	out	19	>	psd_acq_all
2	out	20	>	psd_cfd_bypass
2	out	21	>	psd_sin
2	out	22	>	psd_sclk
2	out	23	psd_sel_ext_addr_0	psd_sel_ext_addr_0_from_micro
2	out	24	psd_sel_ext_addr_1	psd_sel_ext_addr_1_from_micro
2	out	25	psd_sc0_0	psd_sc_addr_0_from_micro[0]
2	out	26	psd_sc1_0	psd_sc_addr_0_from_micro[1]
2	out	27	psd_sc0_1	psd_sc_addr_1_from_micro[0]
2	out	28	psd_sc1_1	psd_sc_addr_1_from_micro[1]
2	out	29	>	psd_test_mode_int_0
2	out	30	>	psd_test_mode_int_1

```
3    in    0            >                    cfd_ad_in[0]
3    in    1            >                    cfd_ad_in[1]
3    in    2            >                    cfd_ad_in[2]
3    in    3            >                    cfd_ad_in[3]
3    in    4            >                    cfd_ad_in[4]
3    in    5            >                    cfd_ad_in[5]
3    in    6            >                    cfd_ad_in[6]
3    in    7            >                    cfd_ad_in[7]
3    in    8            ?                          0
3    in    9            ?                          0
3    in   10            ?                          0
3    in   11            ?                          0
3    in   12            ?                          0
3    in   13            ?                          0
3    in   14            ?                          0
3    in   15            ?                          0
3    in   16            ?                          0
3    in   17            ?                          0
3    in   18            ?                          0
3    in   19            ?                          0
3    in   20            ?                          0
3    in   21            ?                          0
3    in   22            ?                          0
3    in   23            ?                          0
3    in   24            ?                          0
3    in   25            ?                          0
3    in   26            ?                          0
3    in   27            ?                          0
3    in   28            ?                          0
3    in   29            ?                          0
3    in   30            ?                          0
3    in   31            ?                          0

3   out    0            >                   cfd_ad_out[0]
3   out    1            >                   cfd_ad_out[1]
3   out    2            >                   cfd_ad_out[2]
3   out    3            >                   cfd_ad_out[3]
3   out    4            >                   cfd_ad_out[4]
3   out    5            >                   cfd_ad_out[5]
3   out    6            >                   cfd_ad_out[6]
3   out    7            >                   cfd_ad_out[7]
3   out    8            >                      cfd_stb
3   out    9            >                    cfd_write
3   out   10            >                   cfd_neg_pol
3   out   11            >                    cfd_reset
3   out   12            >                 cfd_global_ena
```