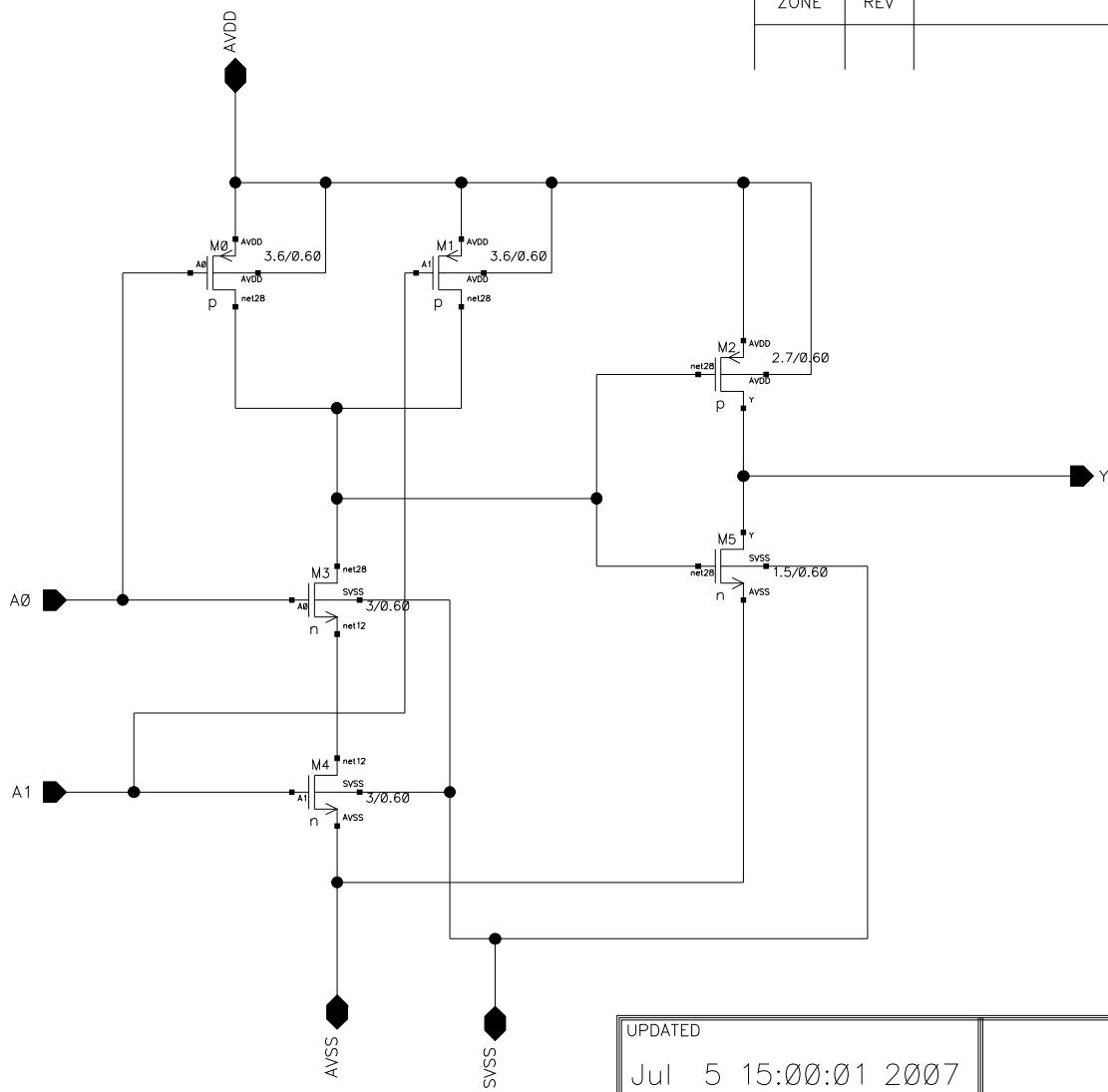


CAGE NO. DWG NO. SH 1 REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Jul 5 15:00:01 2007

and

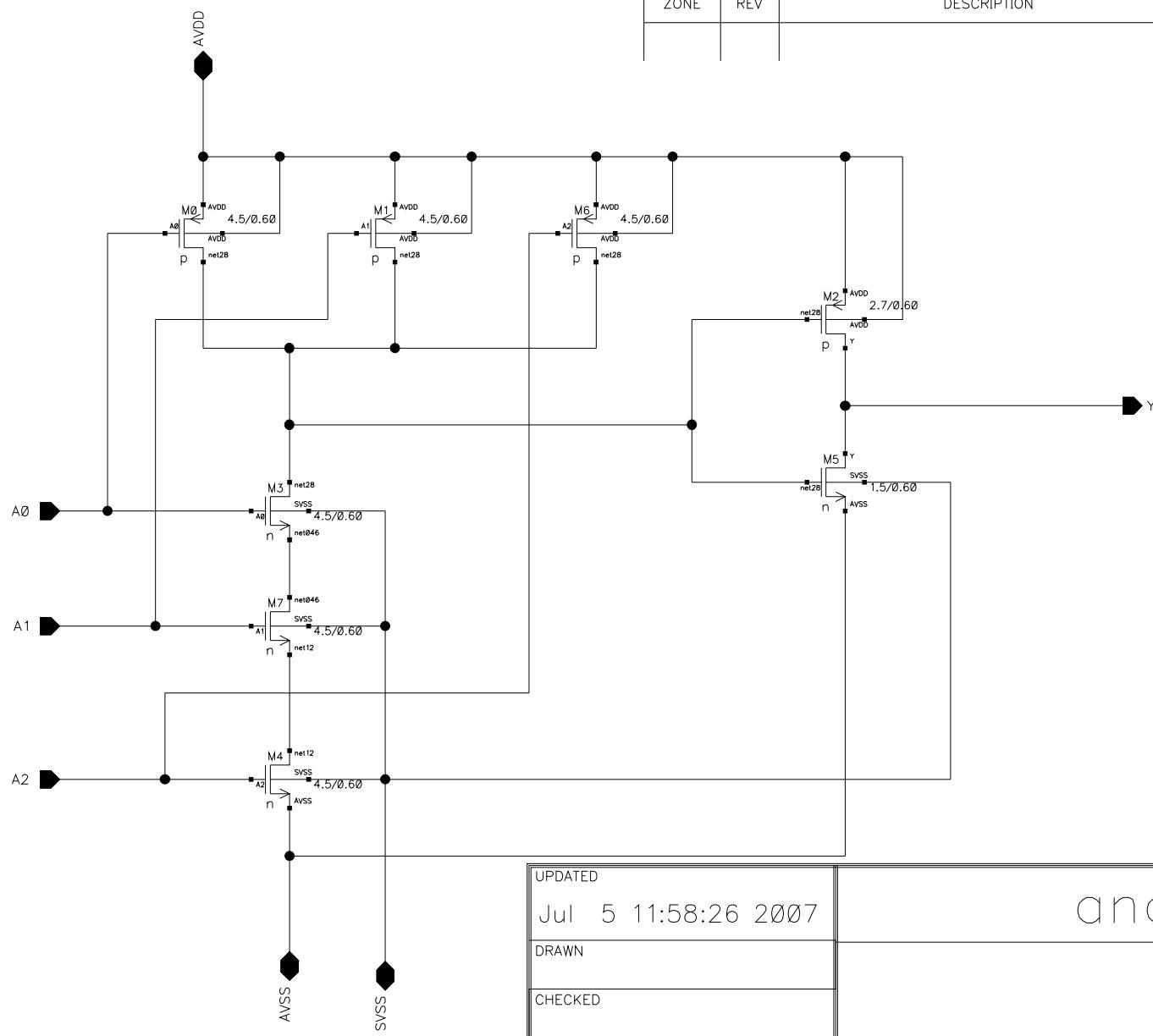
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SIZE	CAGE NO.	DWG NO.	REV
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SHEET		1 OF 1	



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Jul 5 11:58:26 2007  
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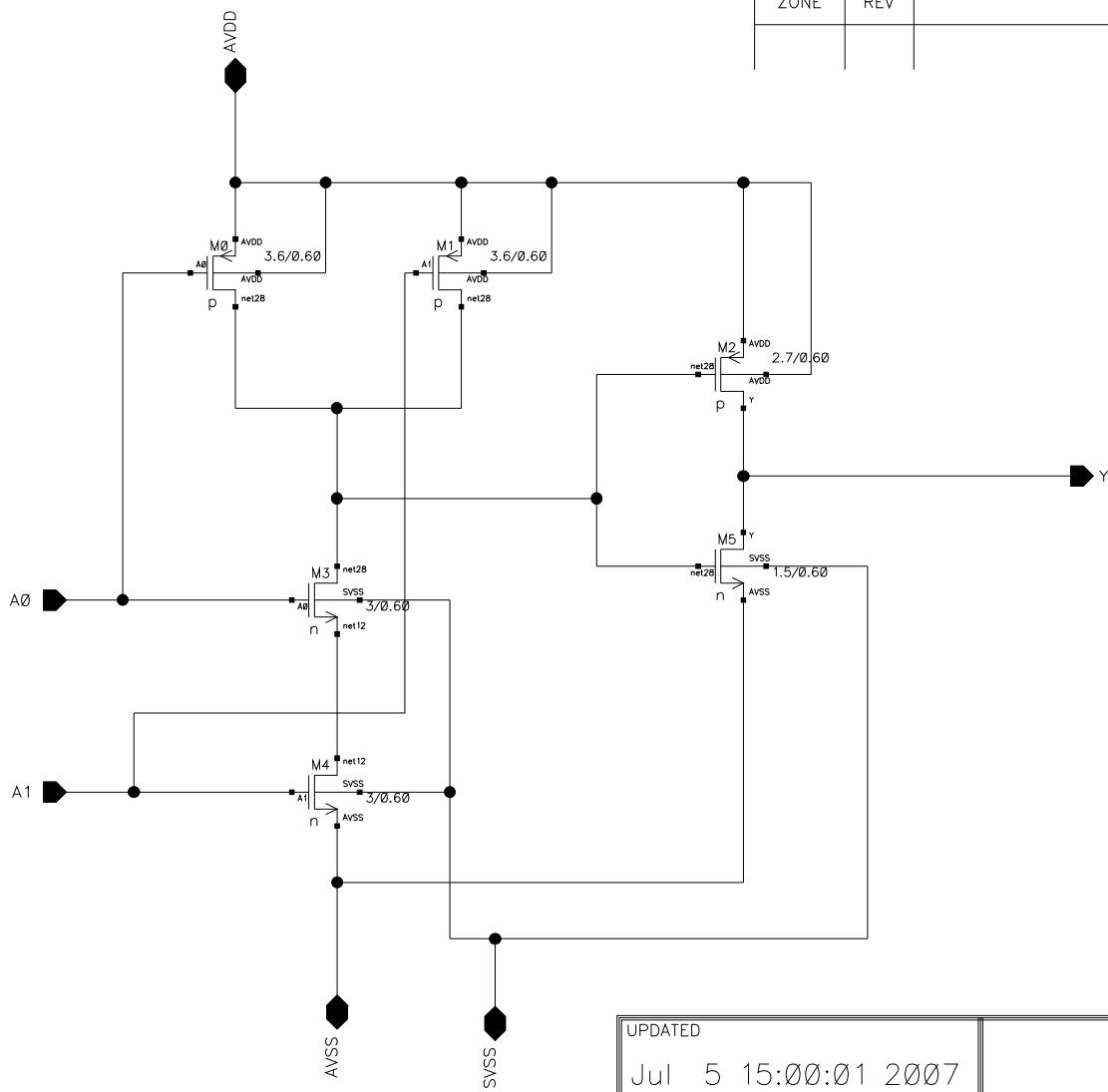
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CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	Jul 5 15:00:01 2007
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SIZE	CAGE NO.	DWG NO.	REV
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SHEET 1 OF 1

CAGE NO. DWG NO. SH 1 REV

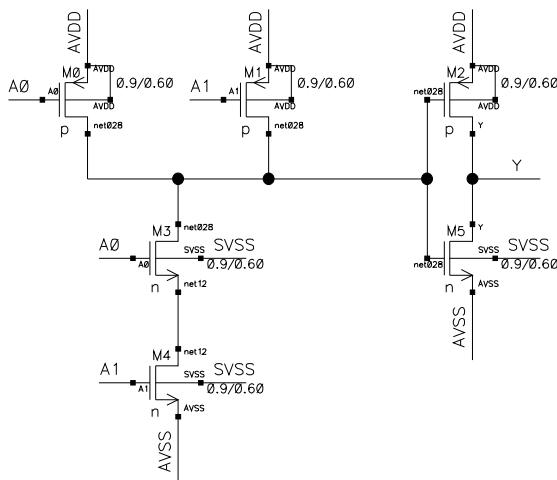
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

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UPDATED  
Aug 8 14:14:18 2007

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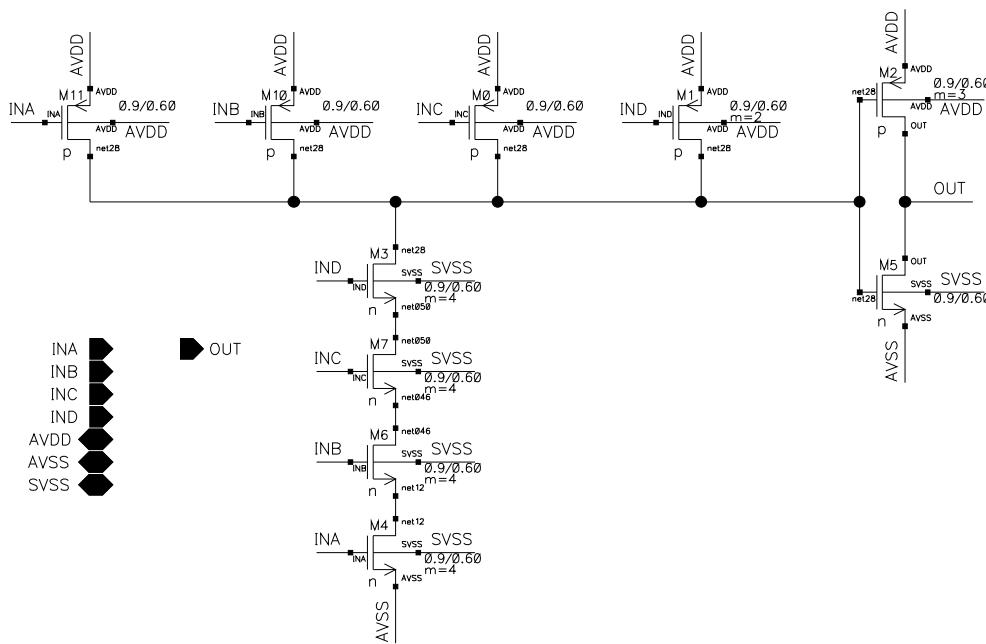
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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Feb 20 16:35:34 2007

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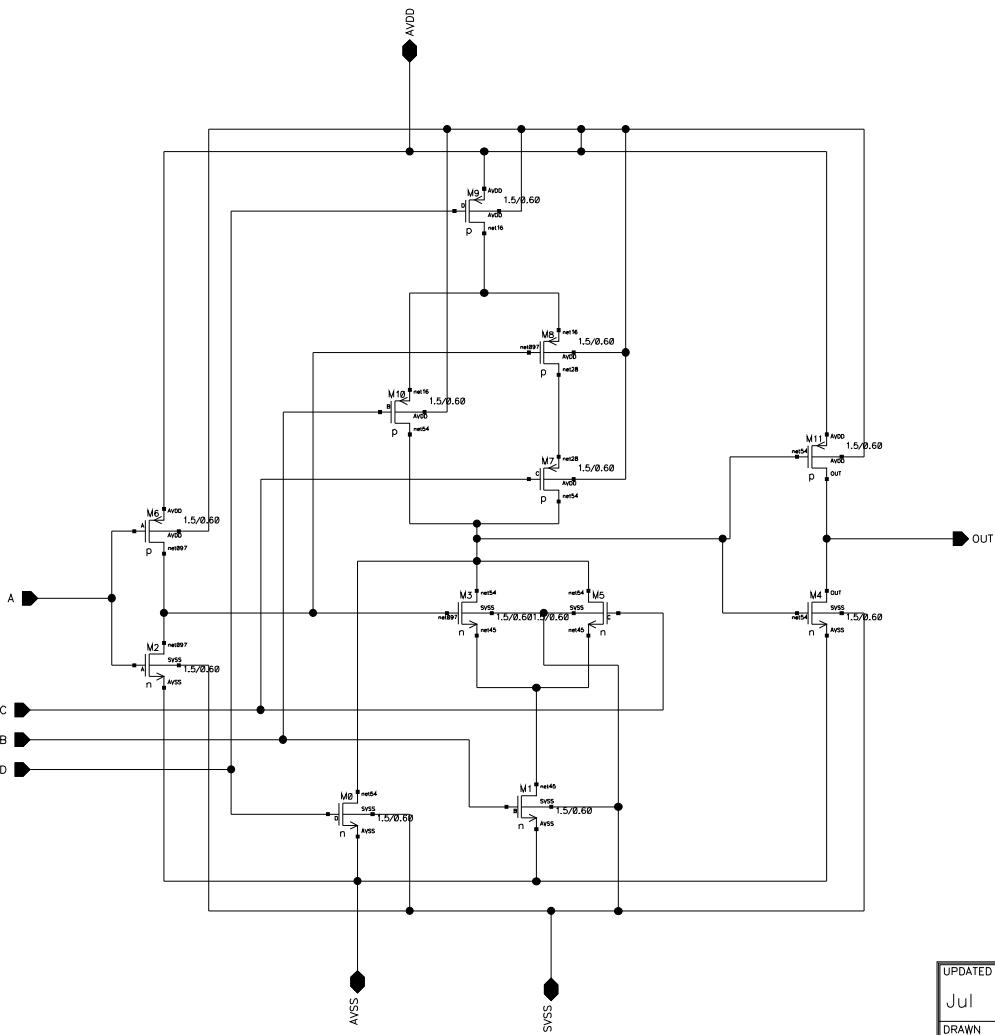
SCALE

SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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**REVISIONS**

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Jul 9 11:16:30 2007

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SIZE	CAGE NO.	DWG NO.	REV
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1 OF 1			

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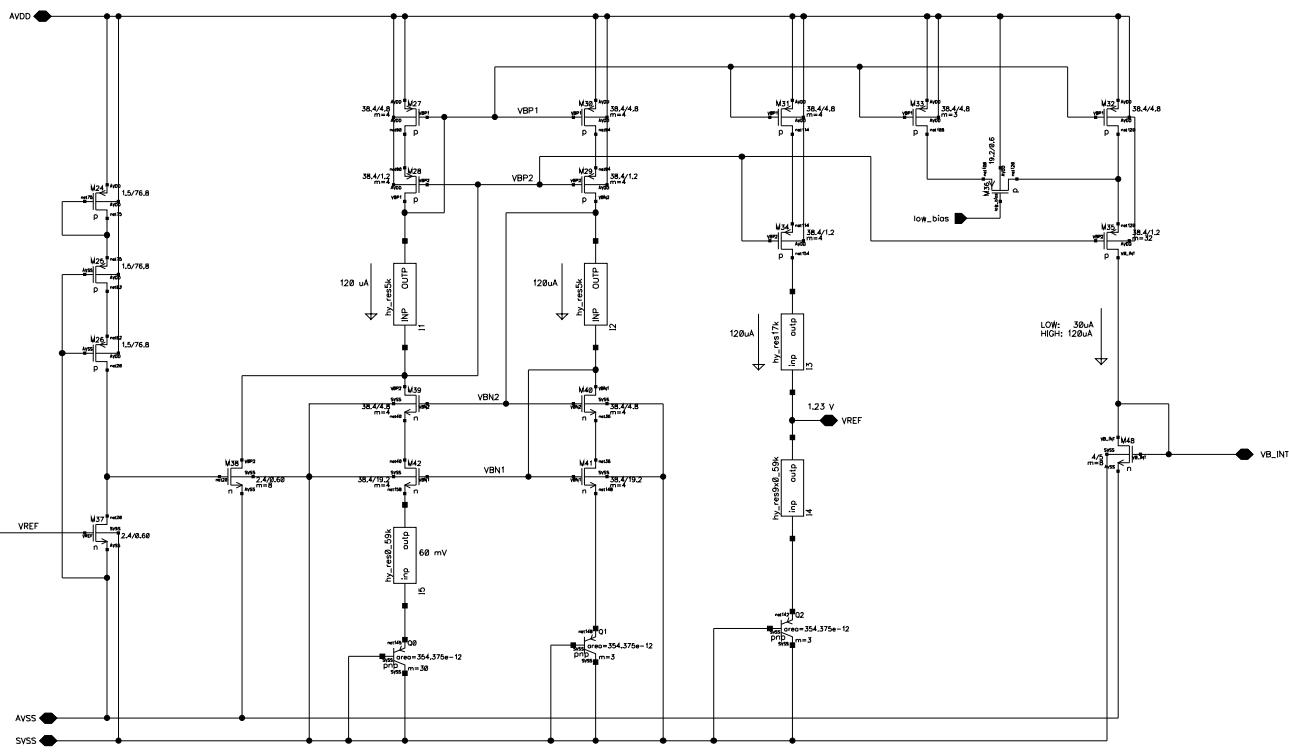
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REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

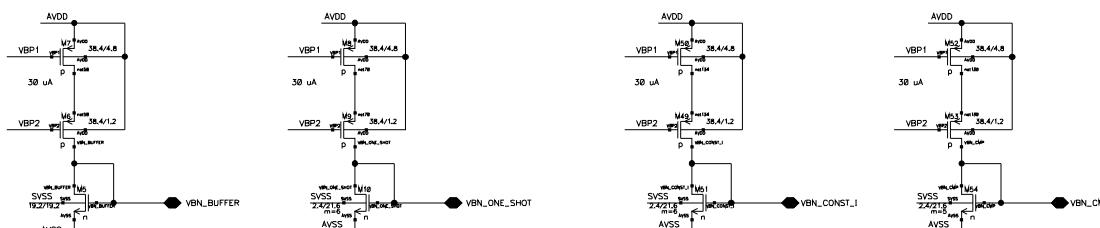
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UPDATED Oct 30 14:23:38 2007	bias		
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## REVISIONS

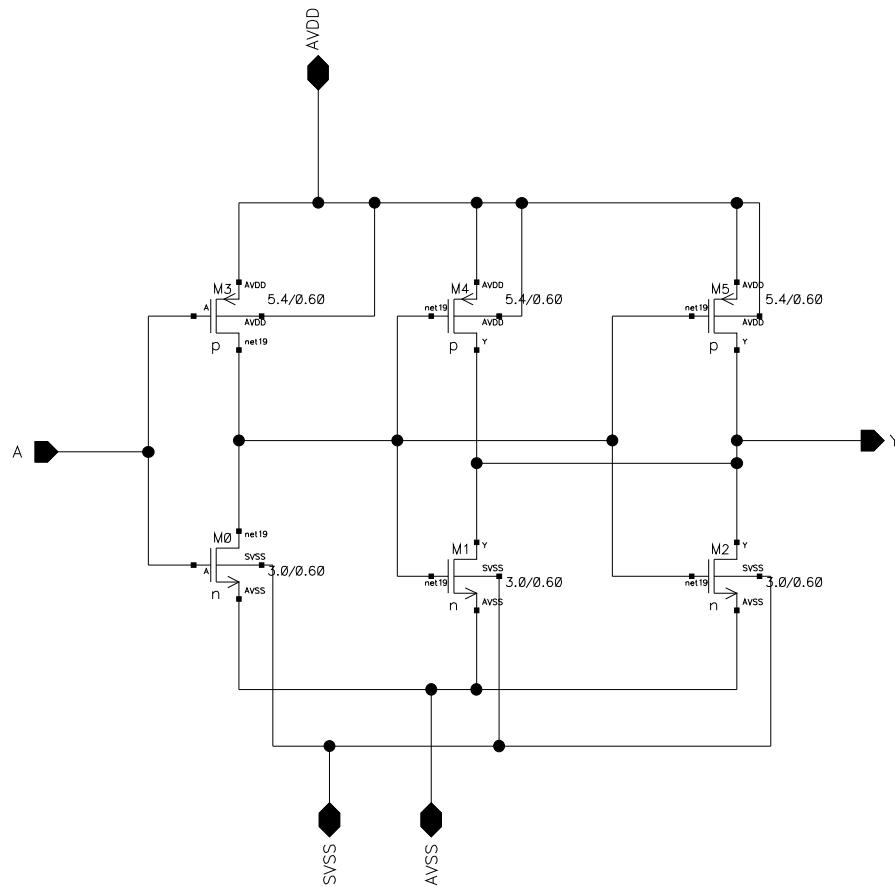
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Jun 15 14:49:33 2007

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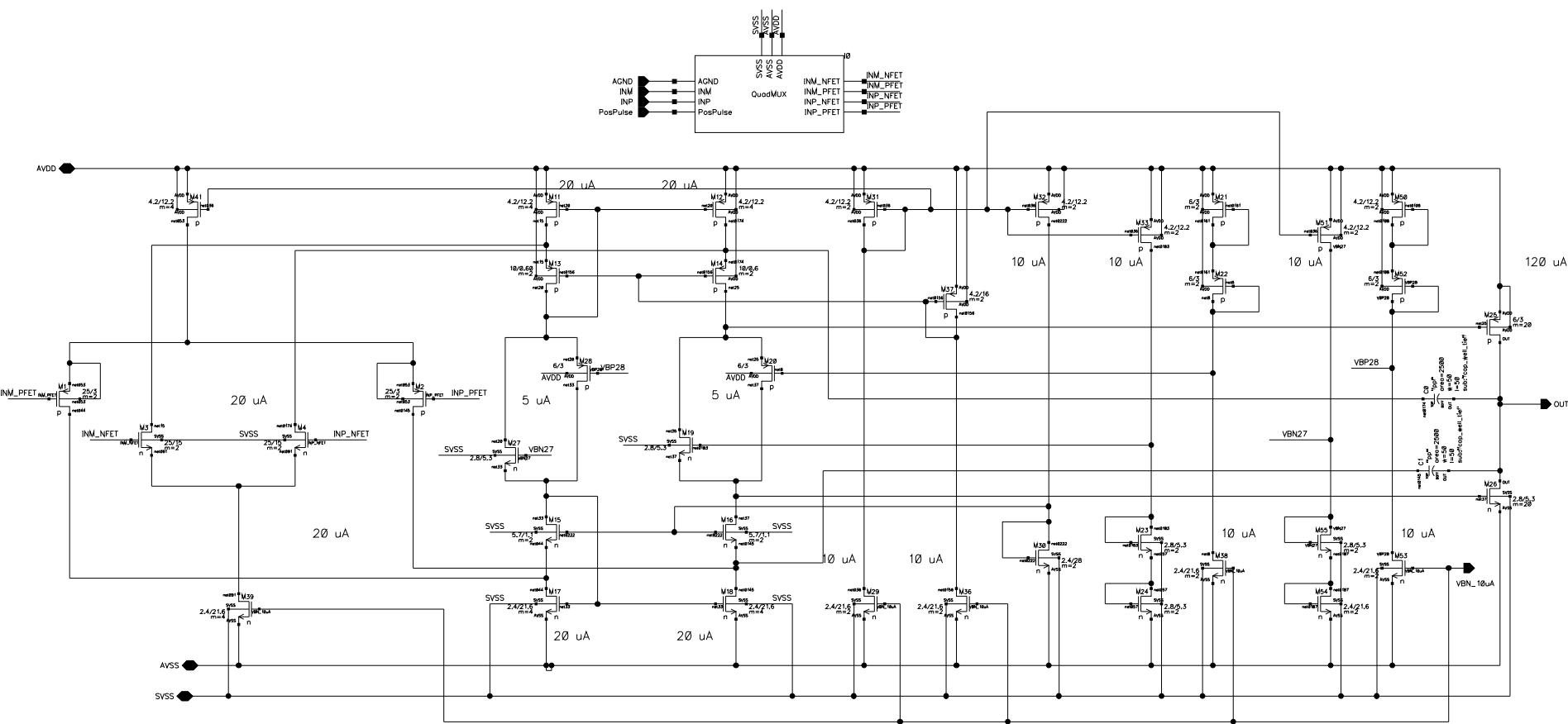
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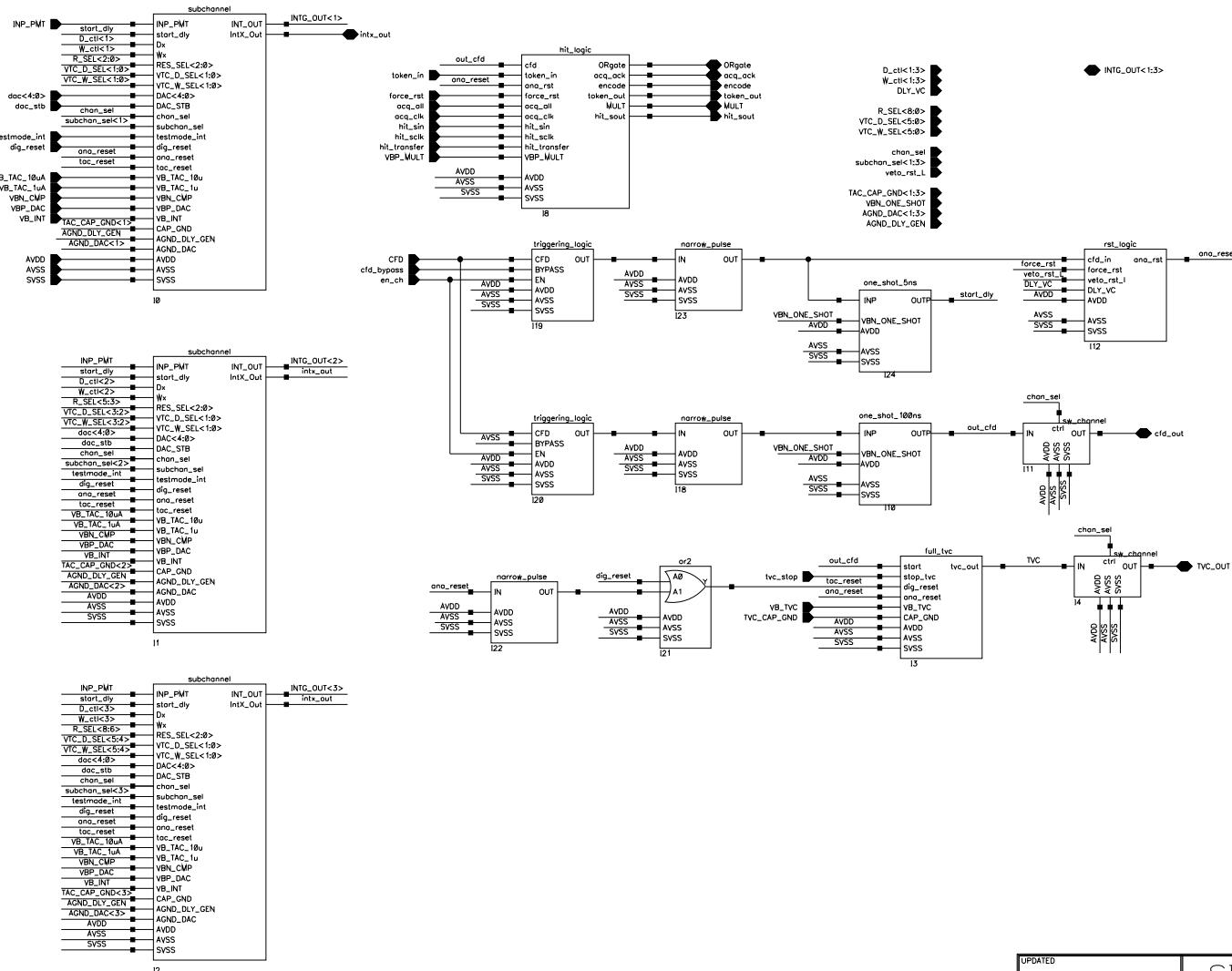
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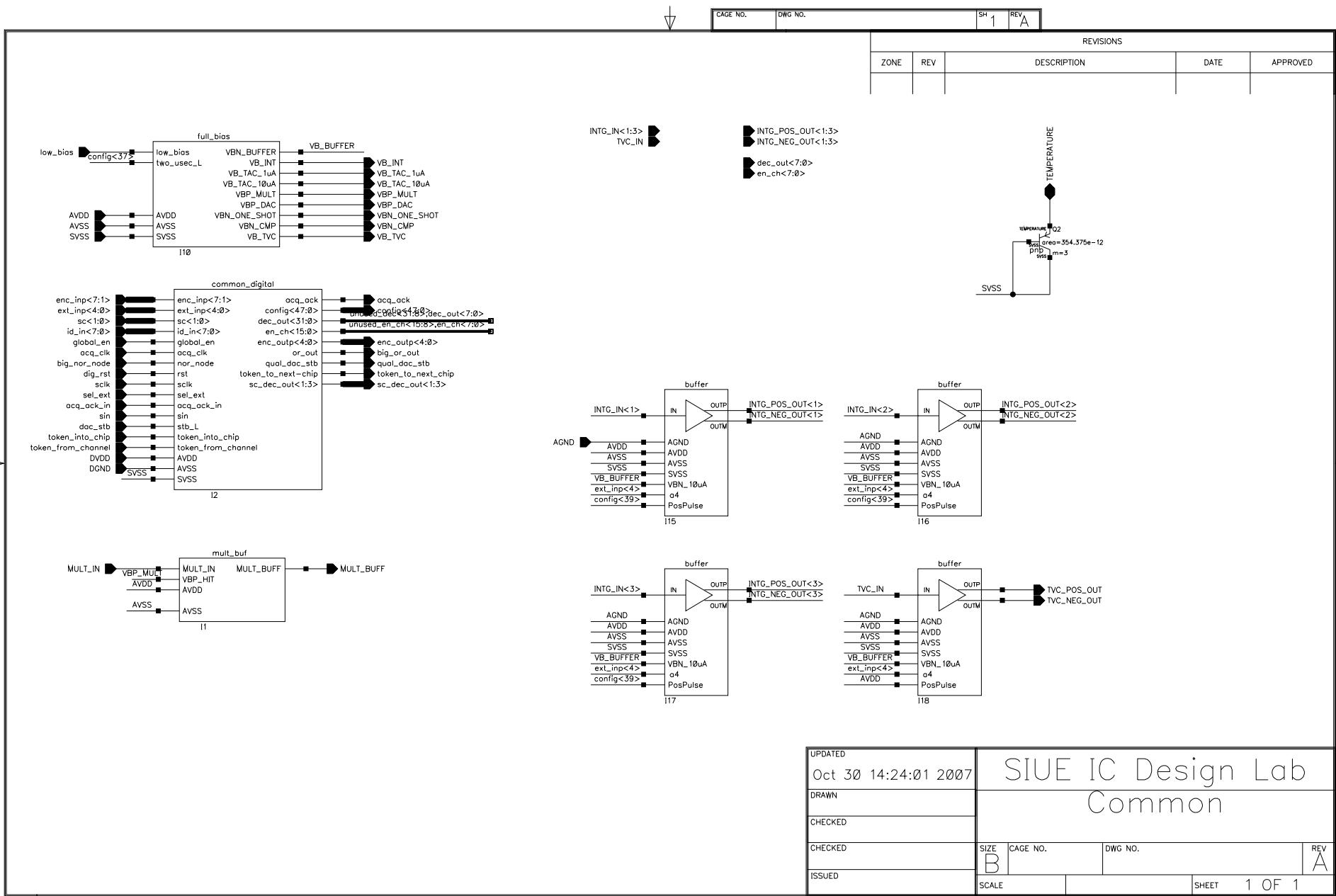
SHEET 1 OF 1



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

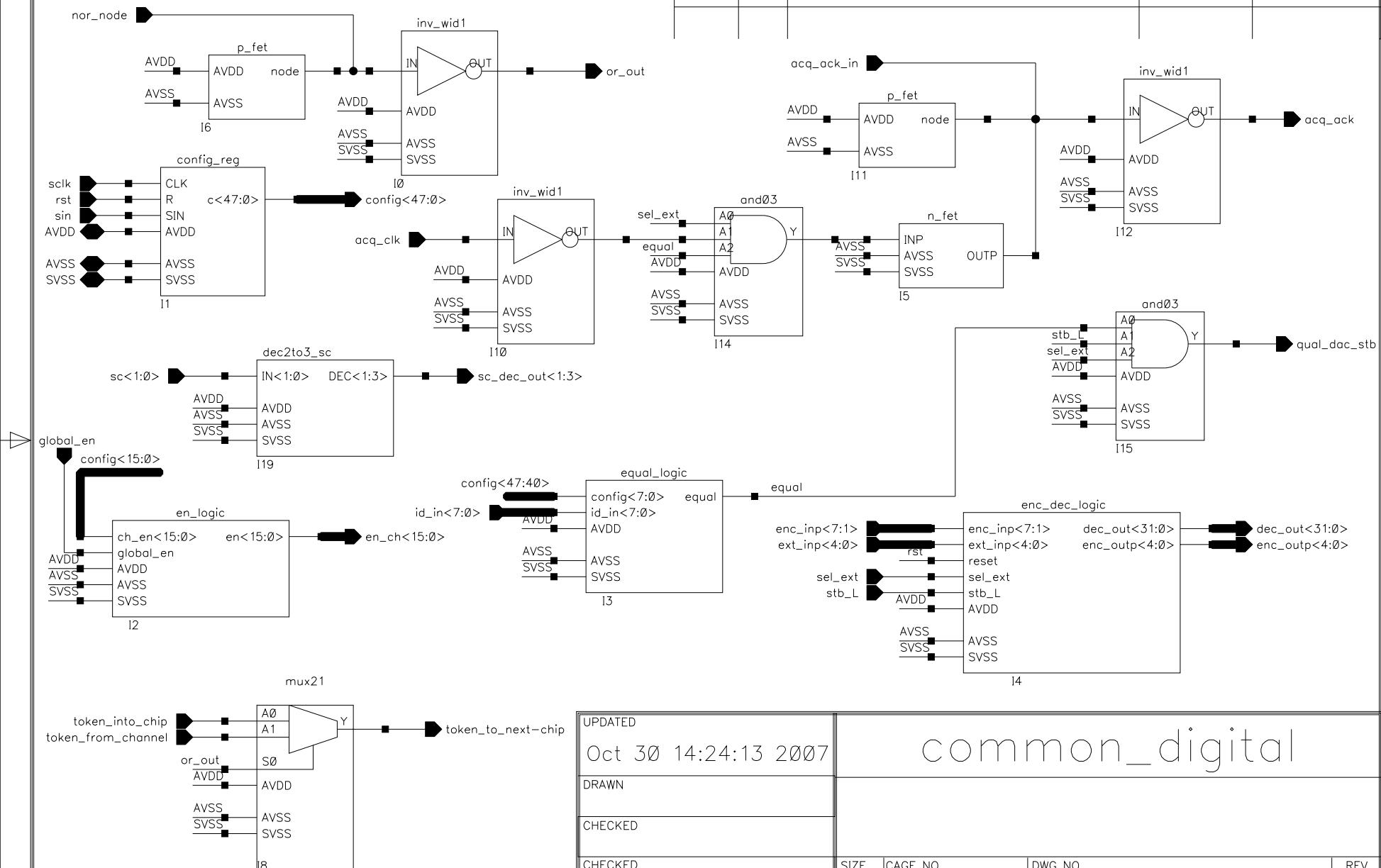


UPDATED Oct 31 16:02:20 2007	SIUE IC Design Lab Channel		
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## REVISIONS

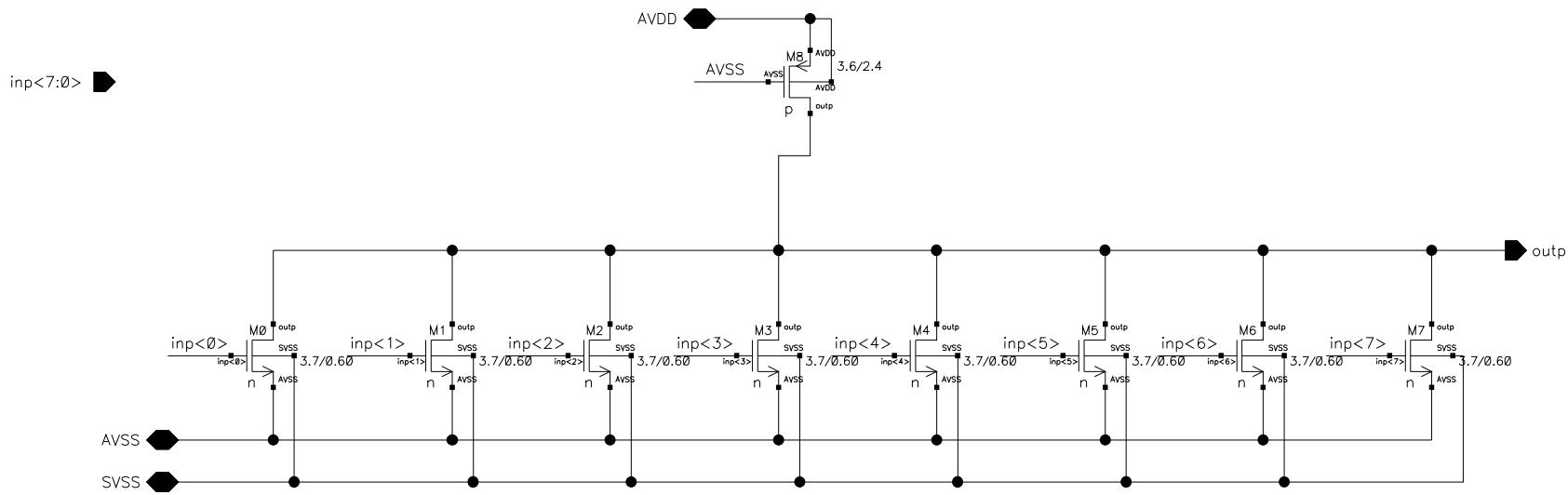
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CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

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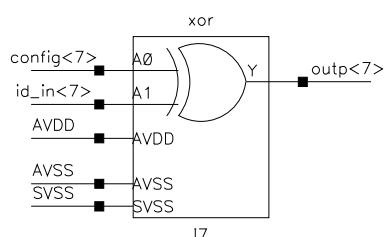
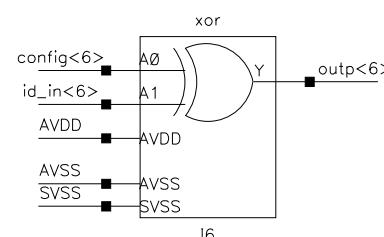
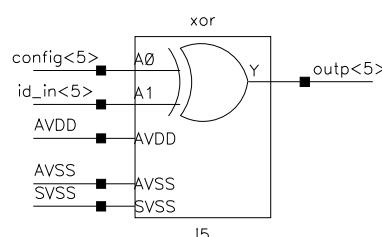
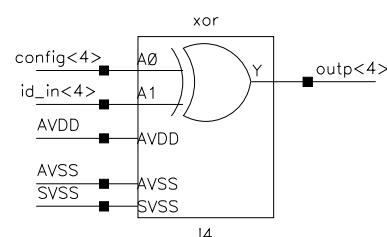
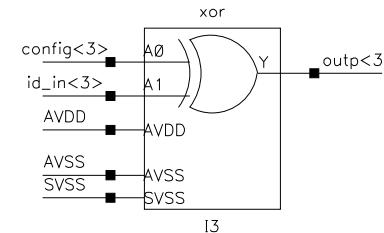
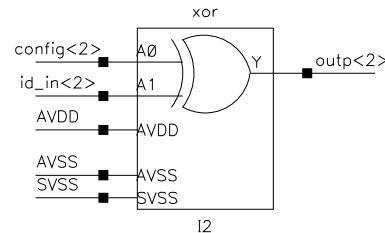
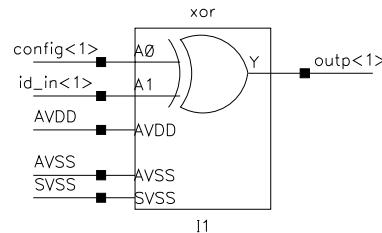
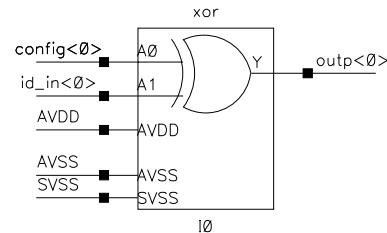


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CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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UPDATED  
Jul 9 14:04:08 2007

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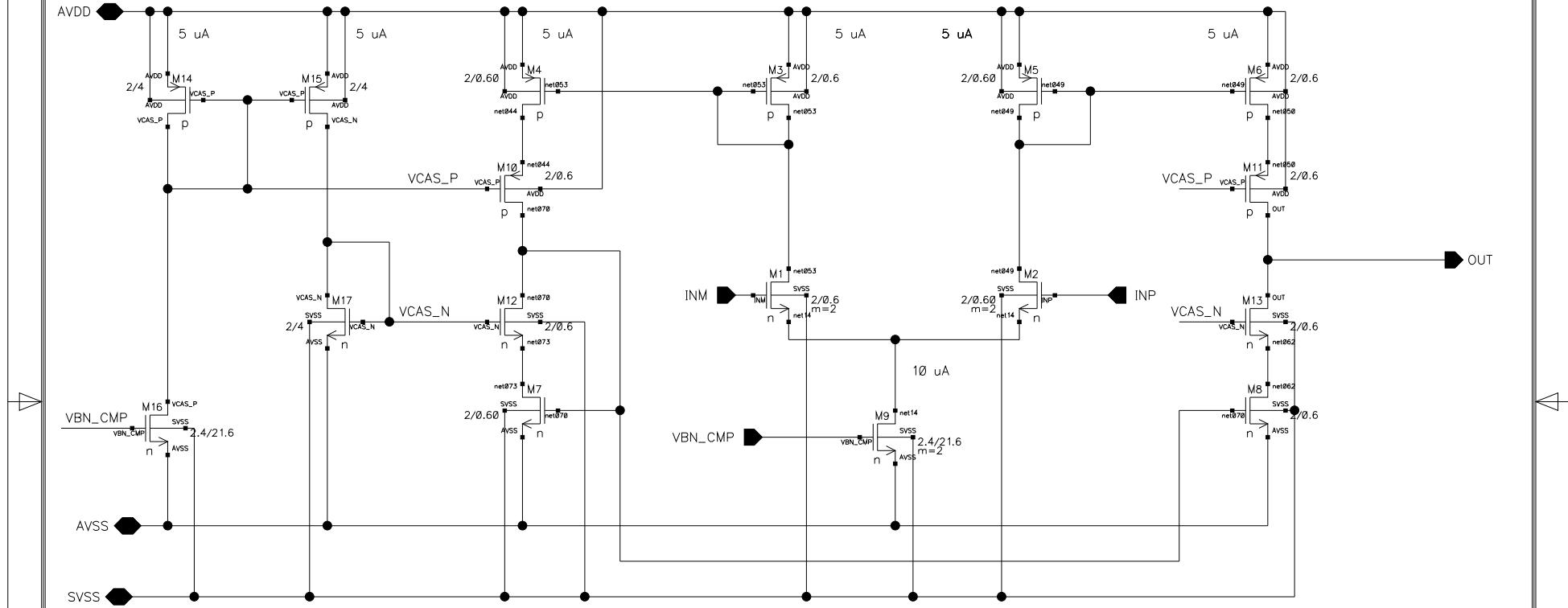
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1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	Jul 9 10:40:35 2007
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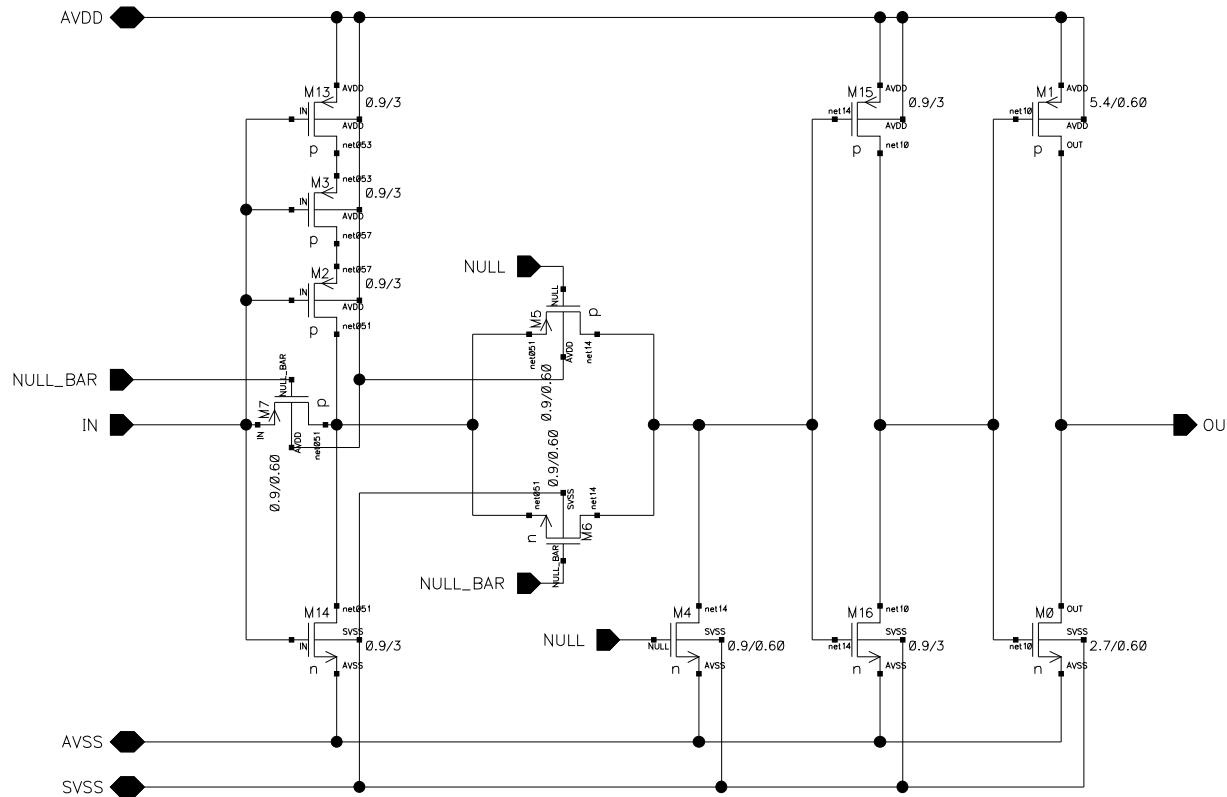
SIUE IC Design Lab  
Comparator

SIZE	CAGE NO.	DWG NO.	REV
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SCALE		SHEET	1 OF 1
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED

Jul 10 13:06:58 2007

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SHEET 1 OF 1

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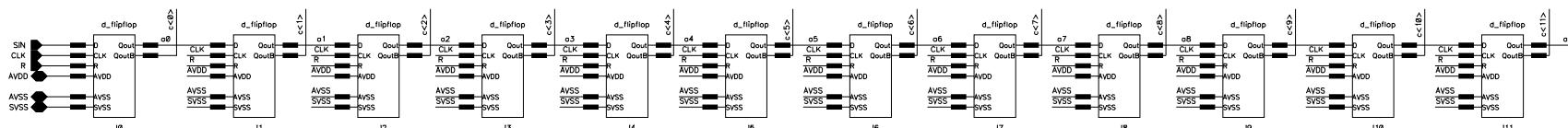
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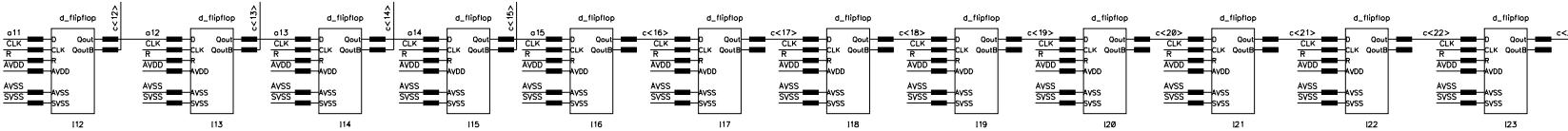
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
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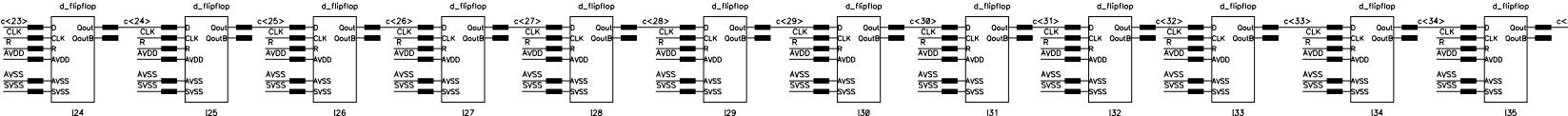
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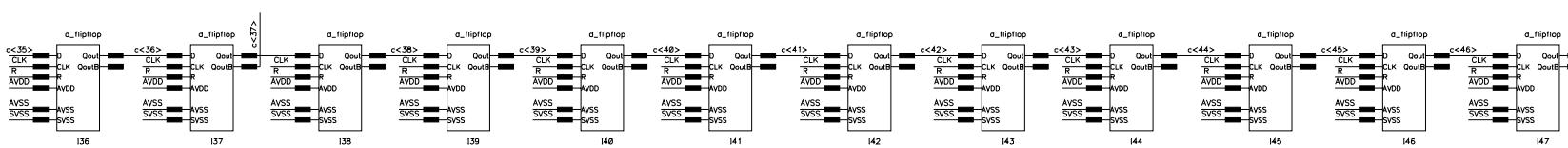
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	SHEET 1 OF 1		

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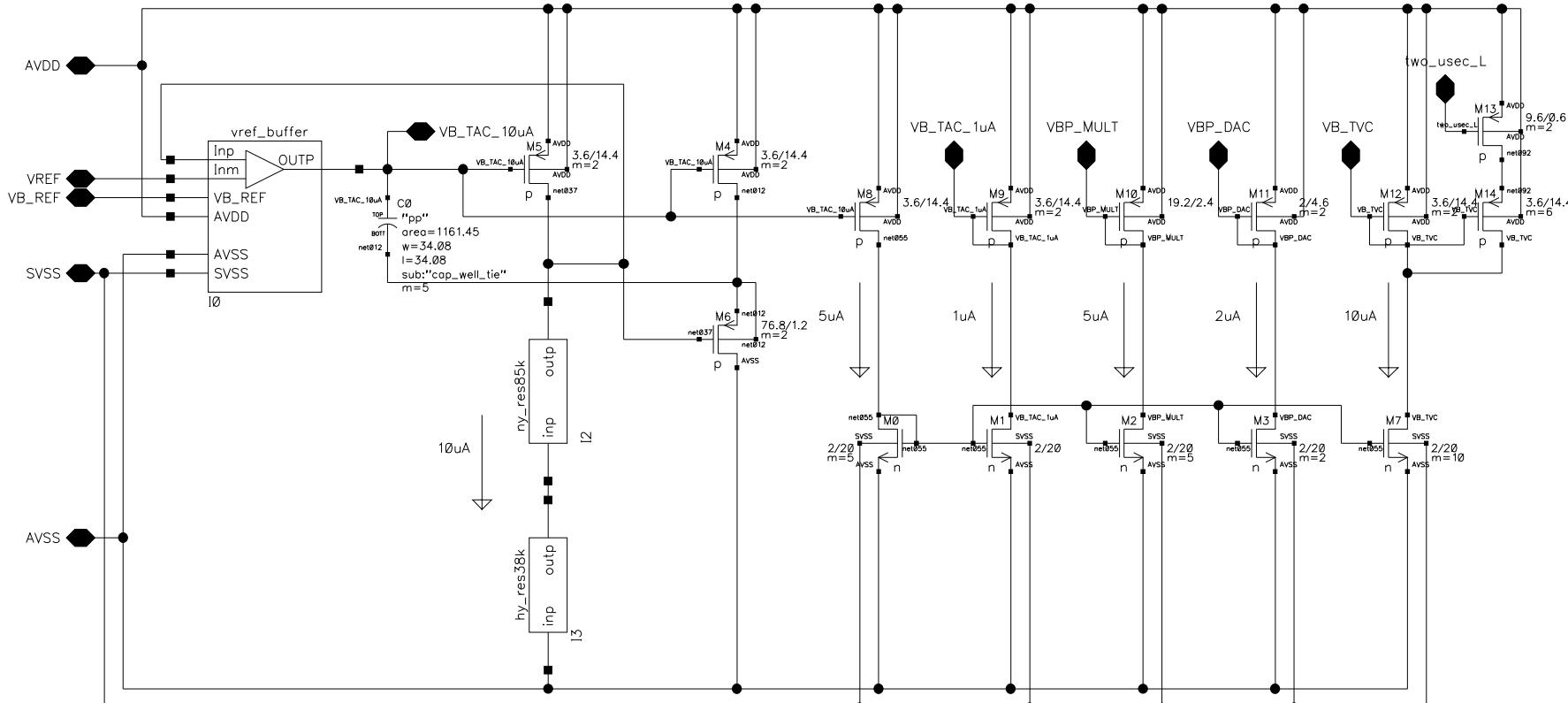
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REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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Oct 30 14:23:53 2007

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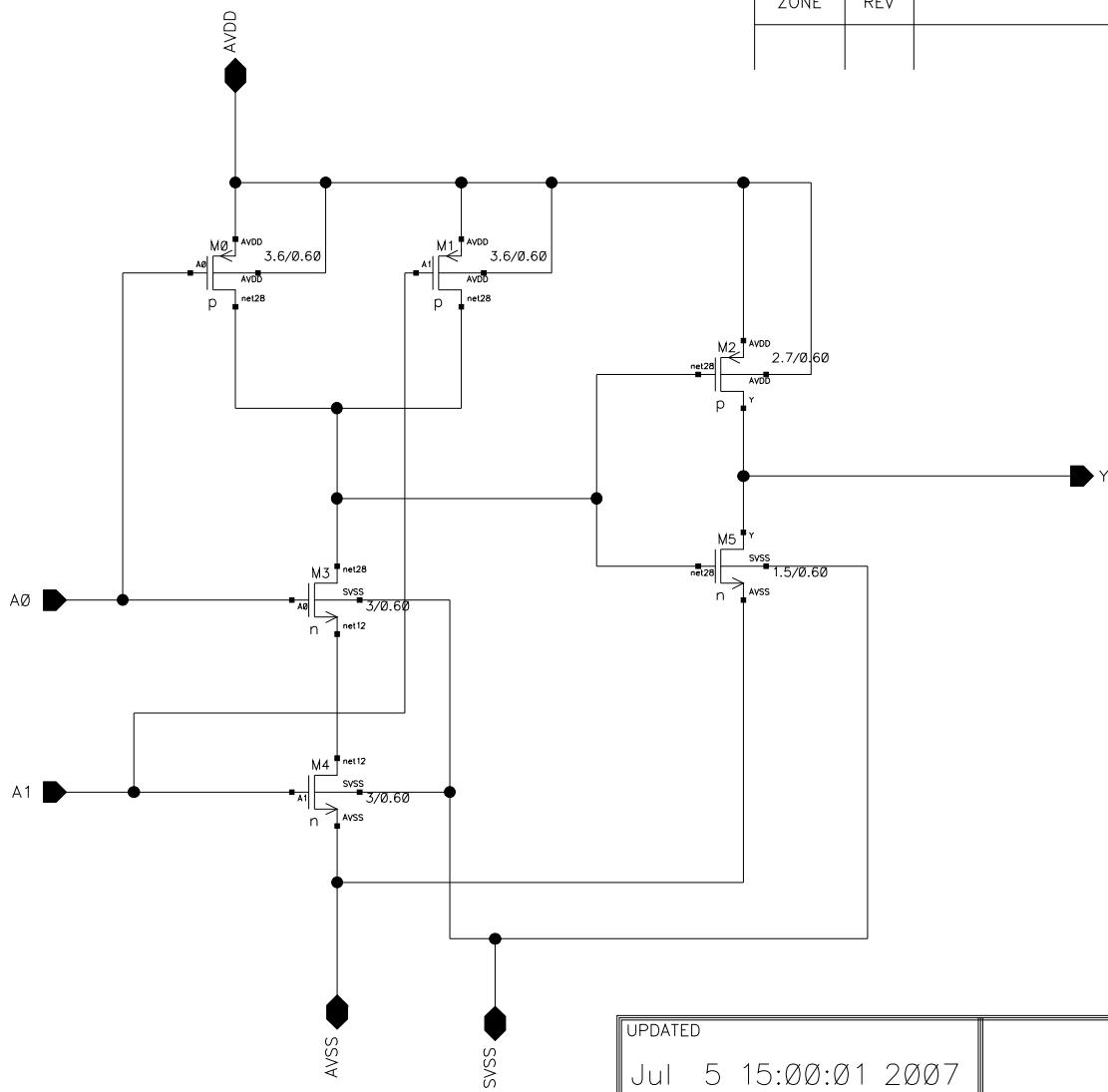
SCALE

SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

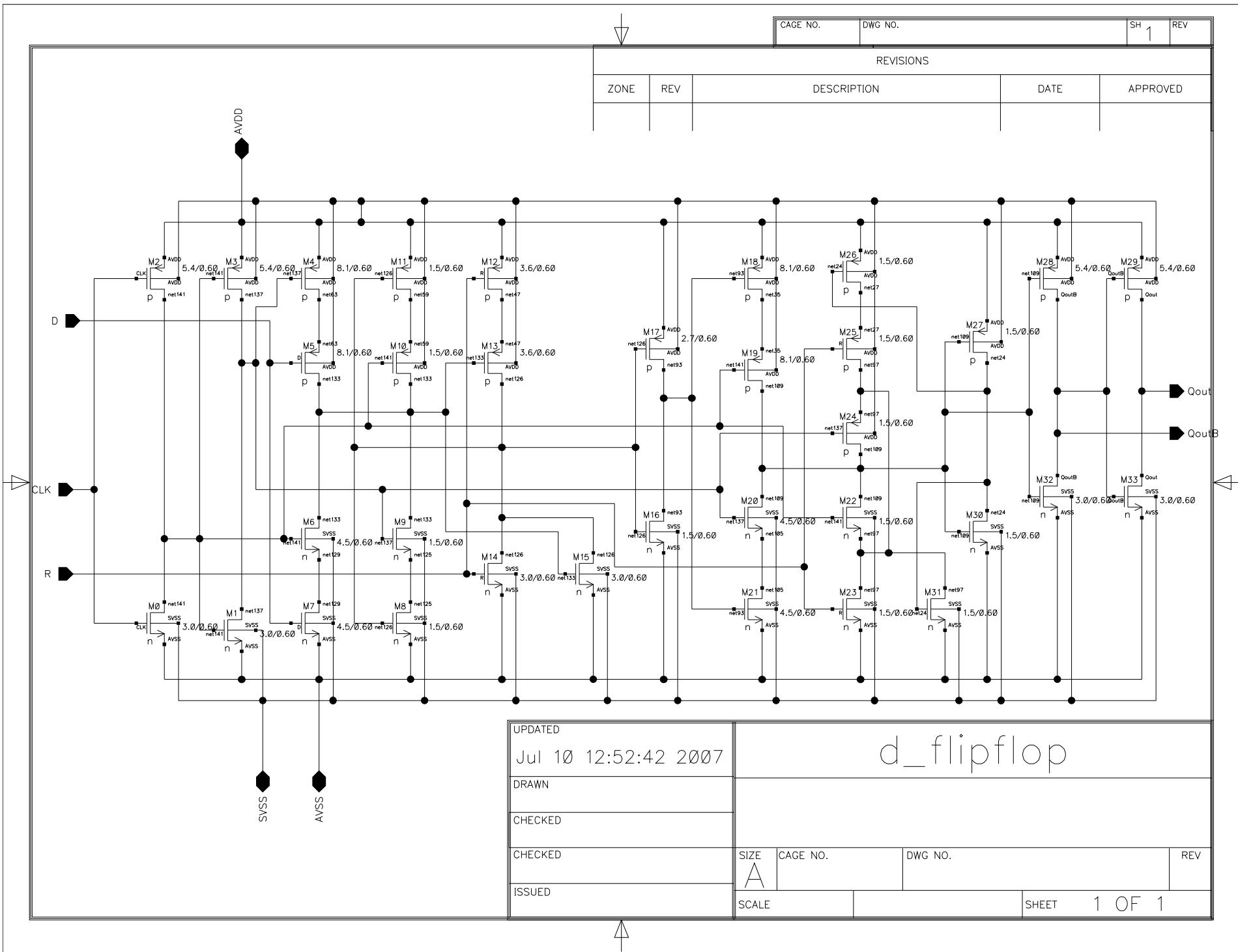


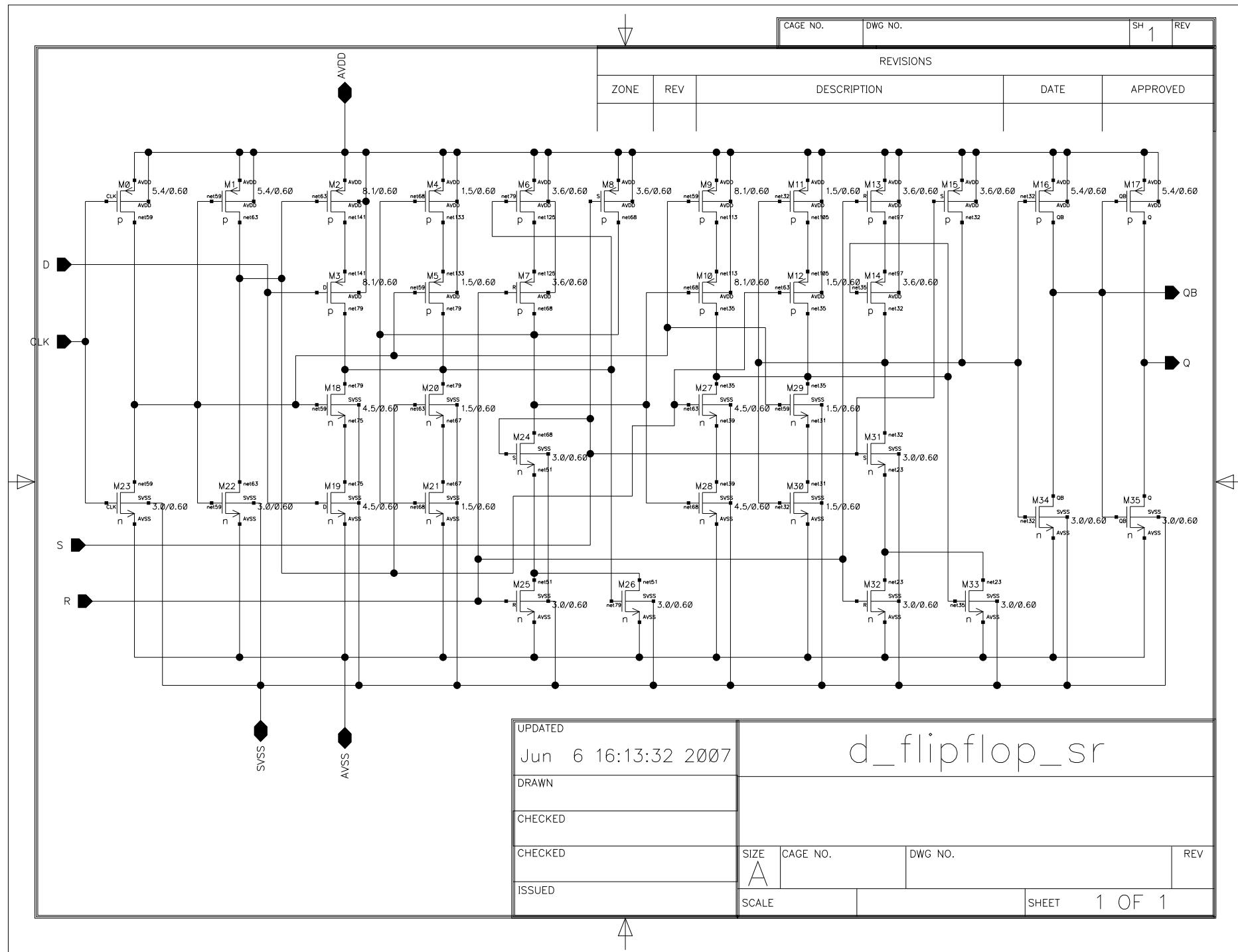
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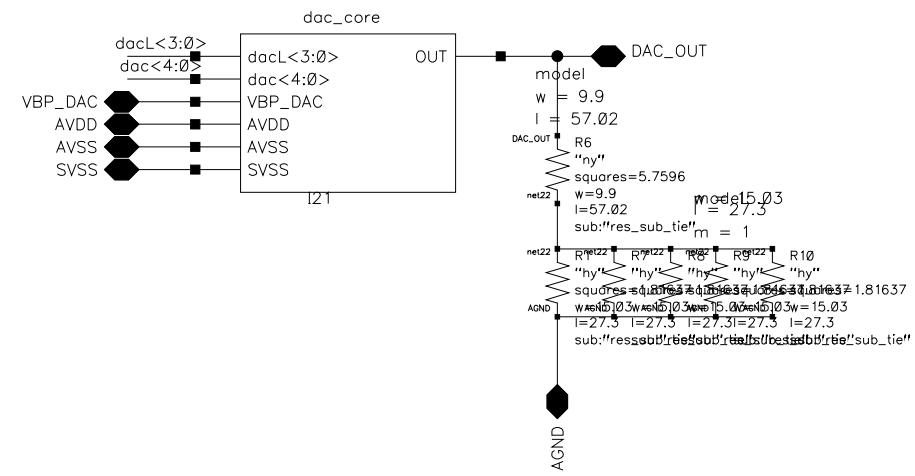
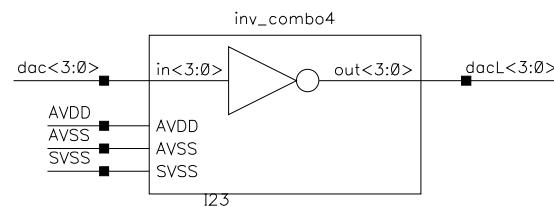
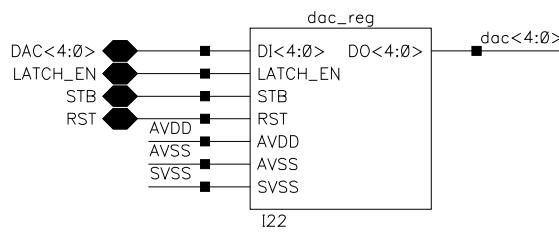
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SHEET 1 OF 1





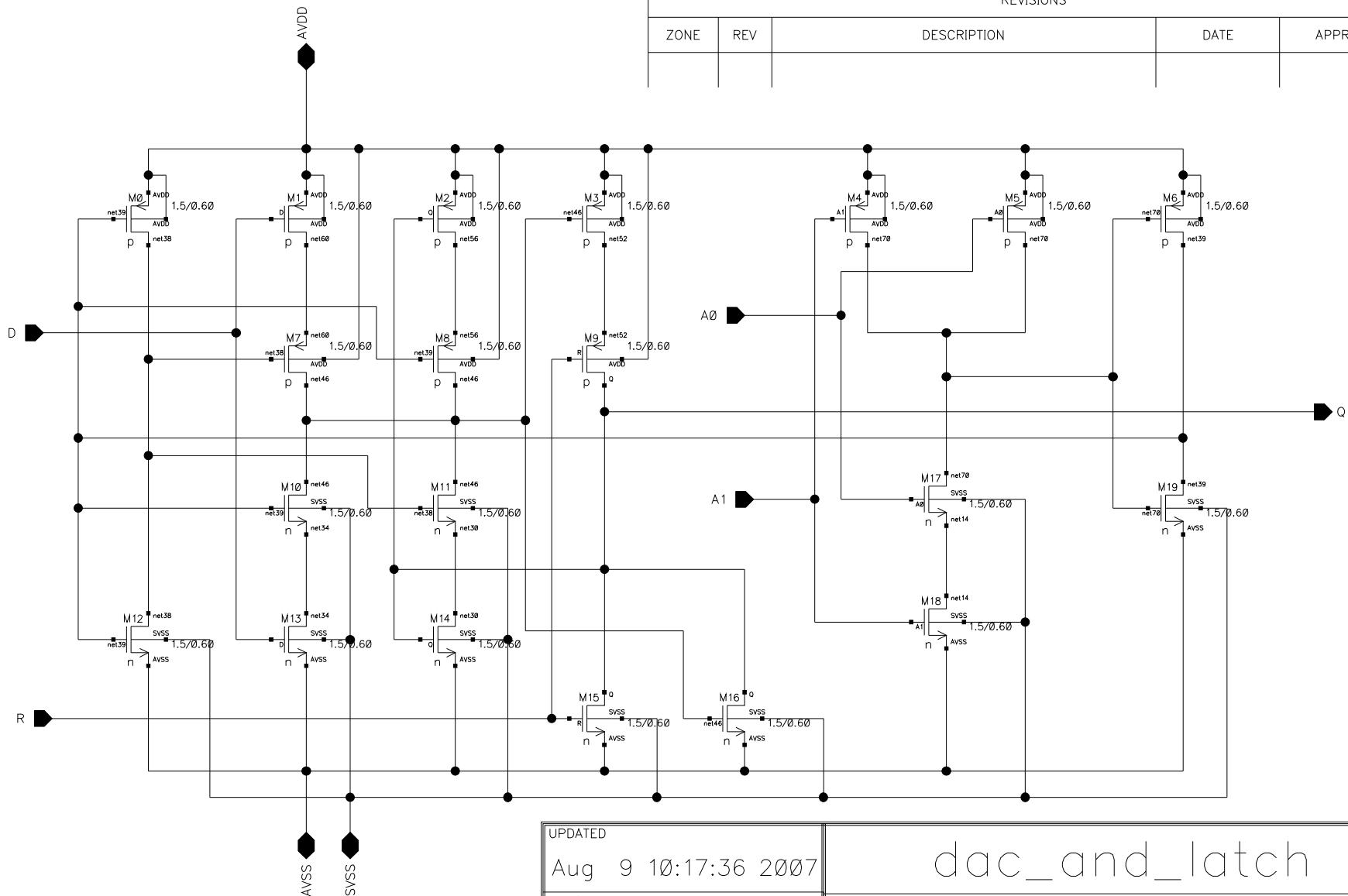


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CAGE NO.	DWG NO.	SH 1	REV
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### REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Aug 9 10:17:36 2007

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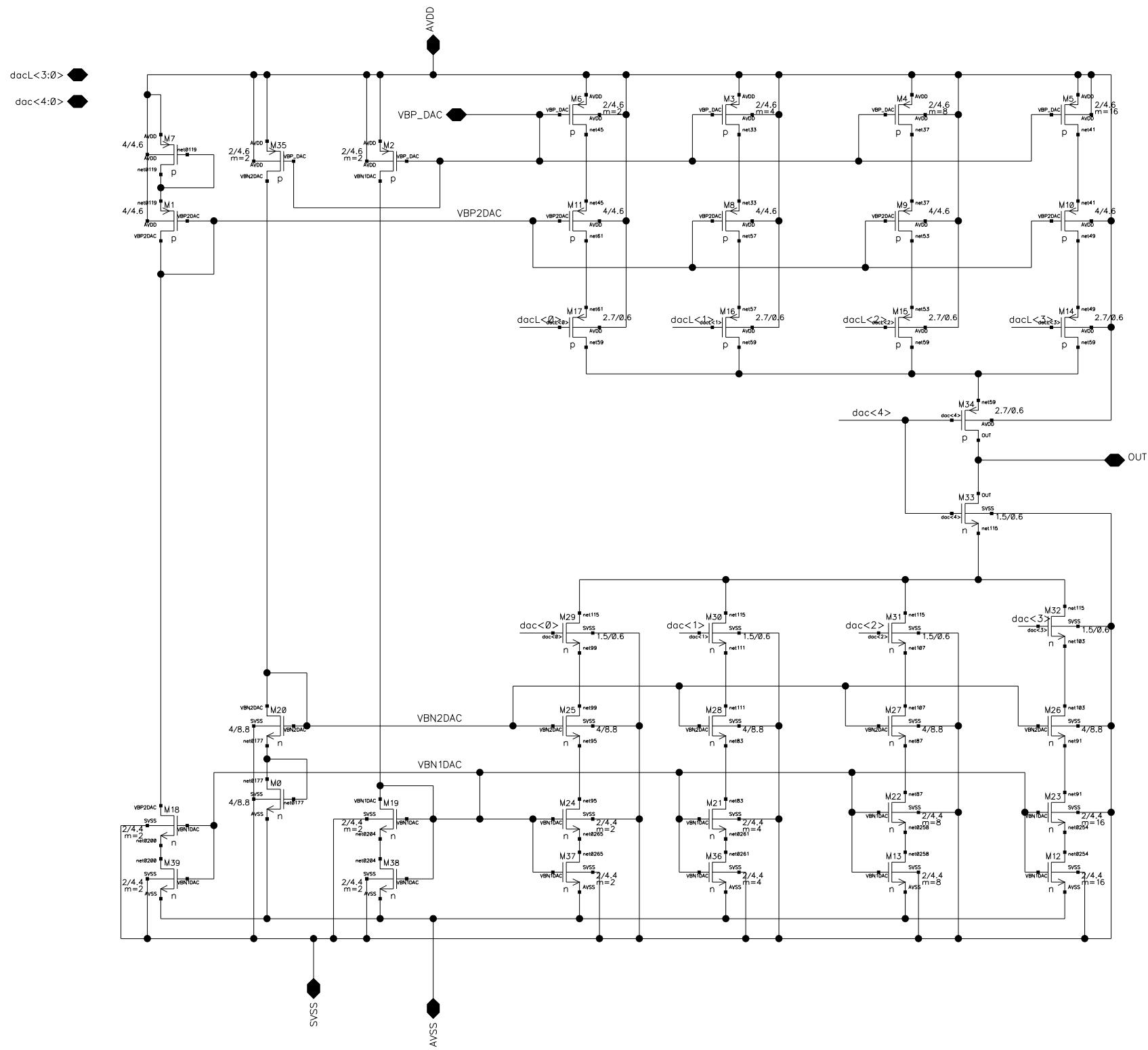
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SIZE	CAGE NO.	DWG NO.	REV
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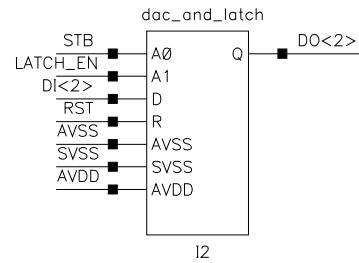
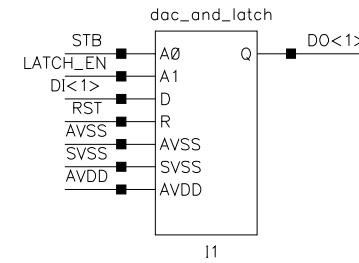
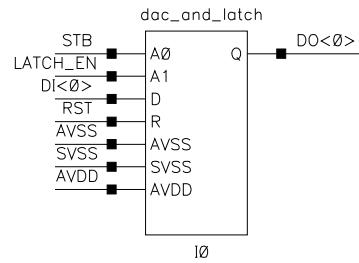
SHEET 1 OF 1



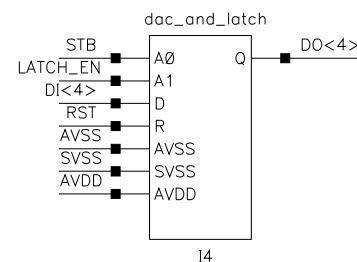
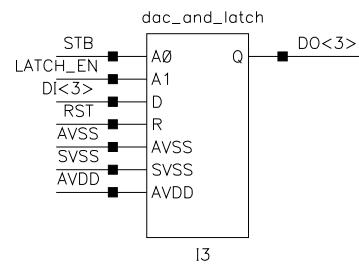
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ZONE	REV	DESCRIPTION	DATE	APPROVED

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LATCH\_EN ◆  
RST ◆  
AVDD ◆



AVSS ◆  
SVSS ◆  
◆ DO<4:0>



UPDATED  
Oct 30 14:27:07 2007

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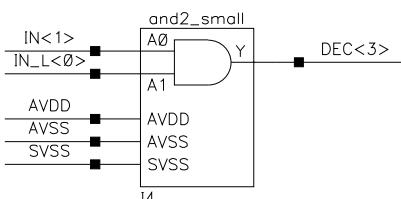
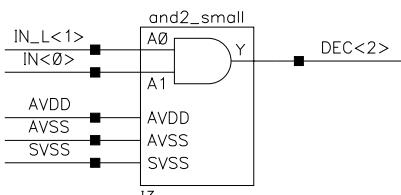
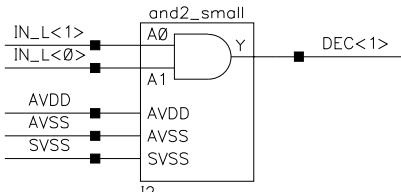
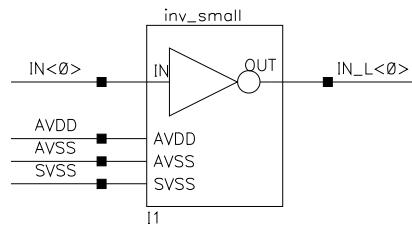
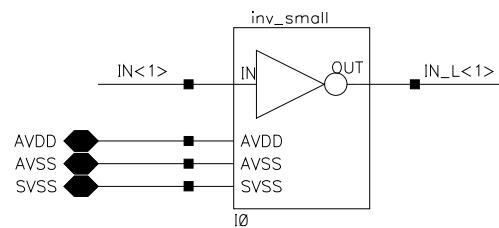
SIZE	CAGE NO.	DWG NO.	REV
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

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UPDATED  
Sep 5 11:36:39 2007

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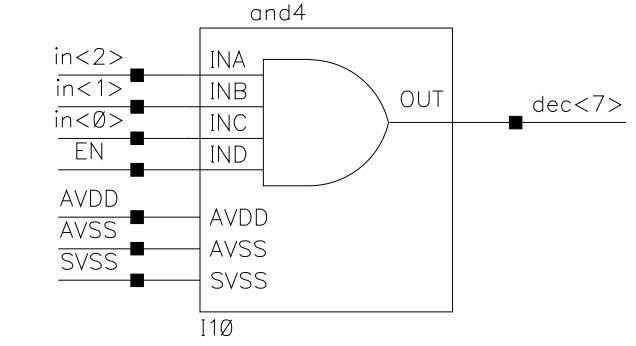
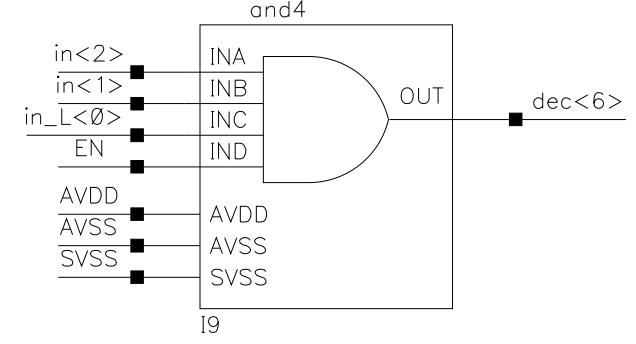
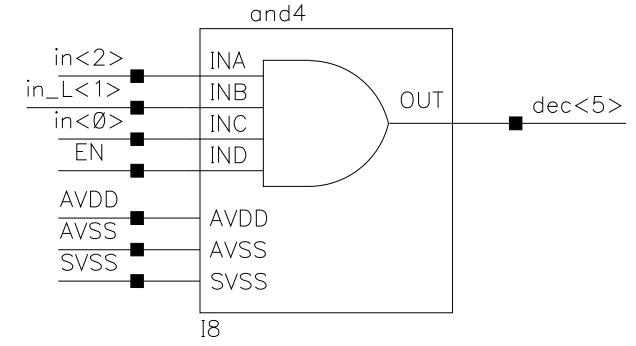
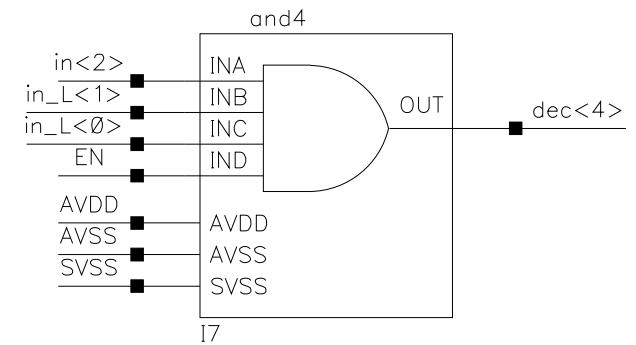
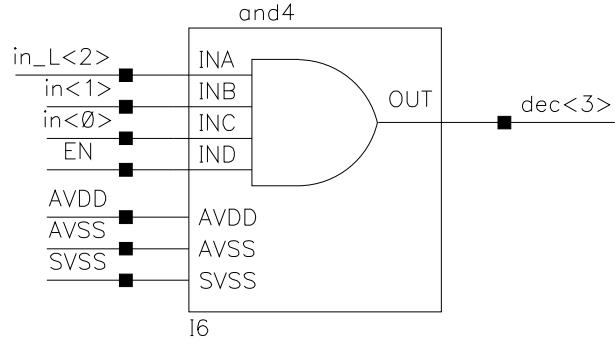
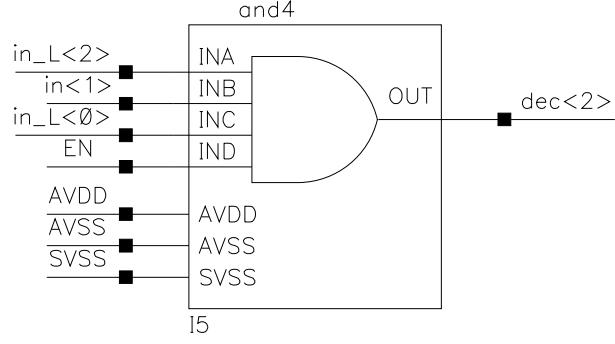
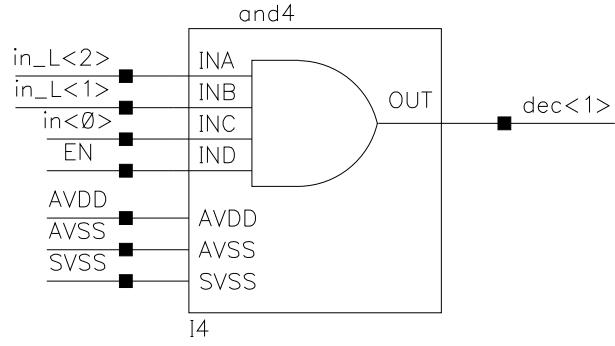
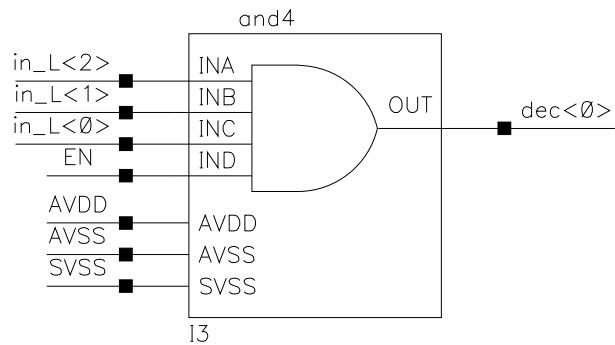
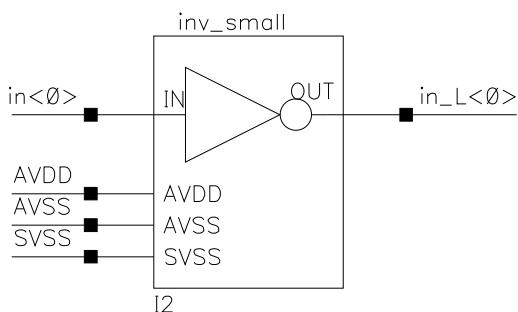
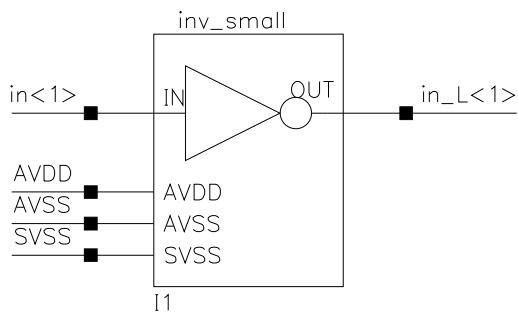
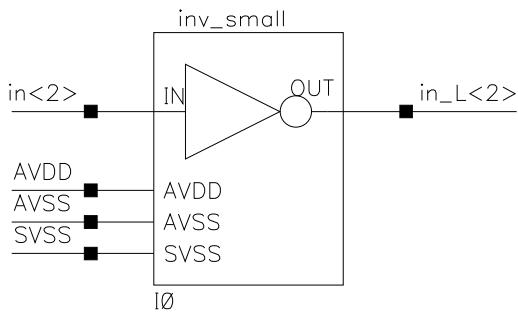
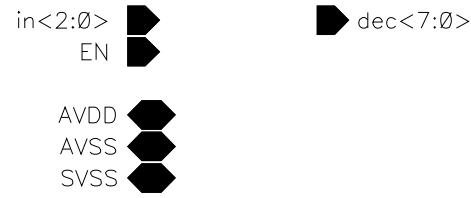
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SIUE IC Design Lab  
Decoder 2 to 3  
Subchannel Selects

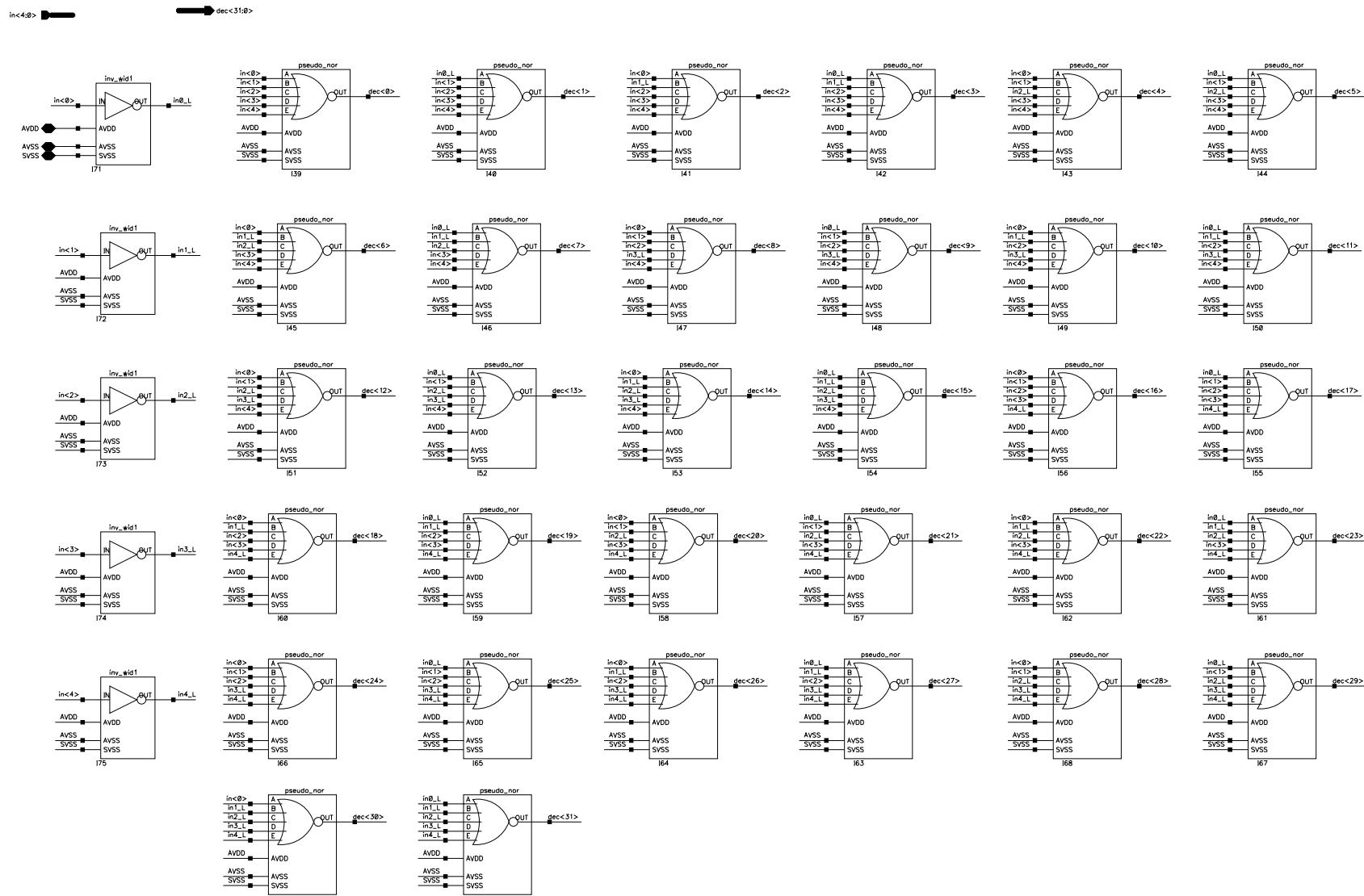
SIZE A CAGE NO. DWG NO.

REV A

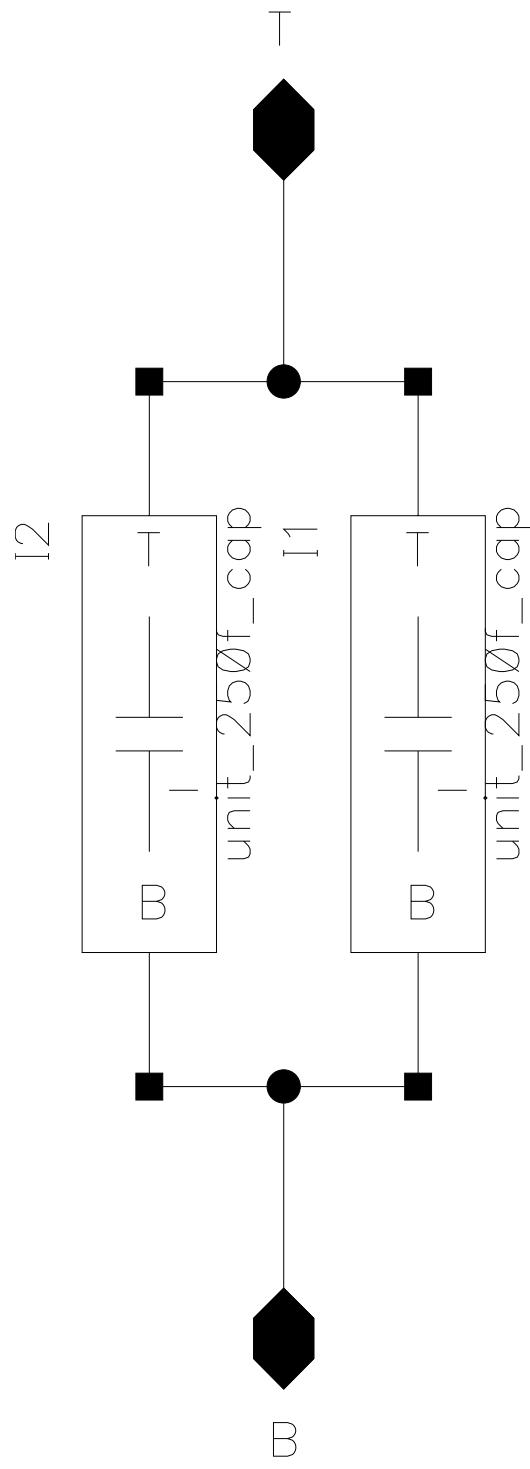
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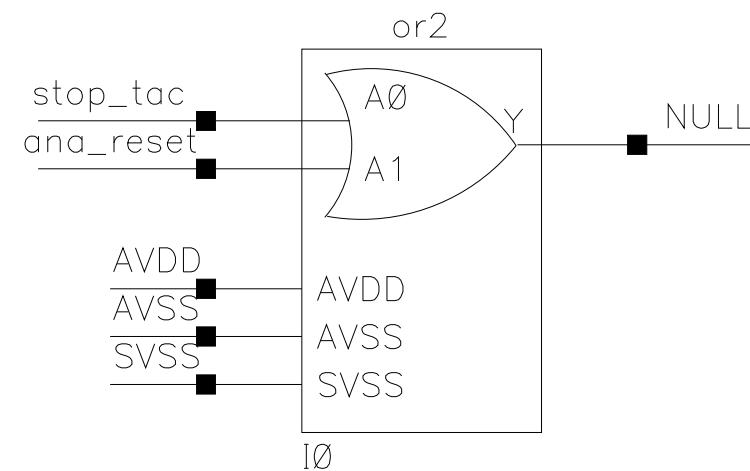
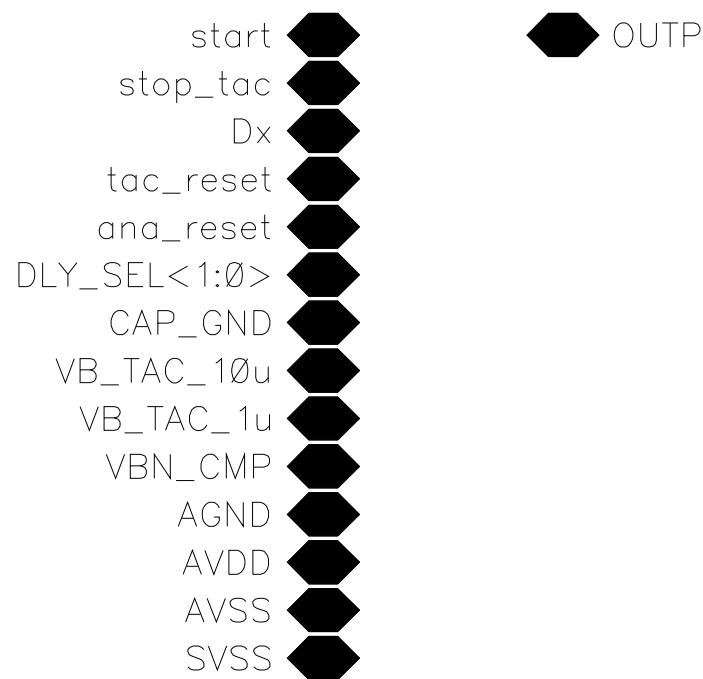
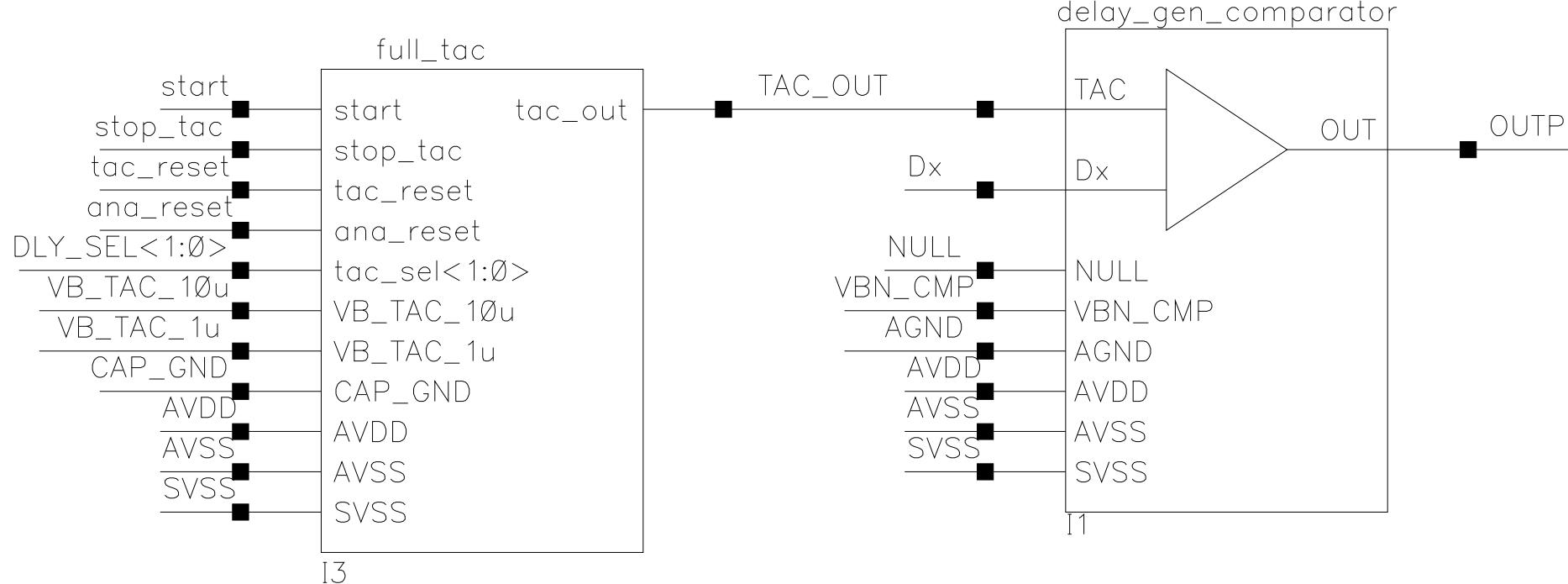


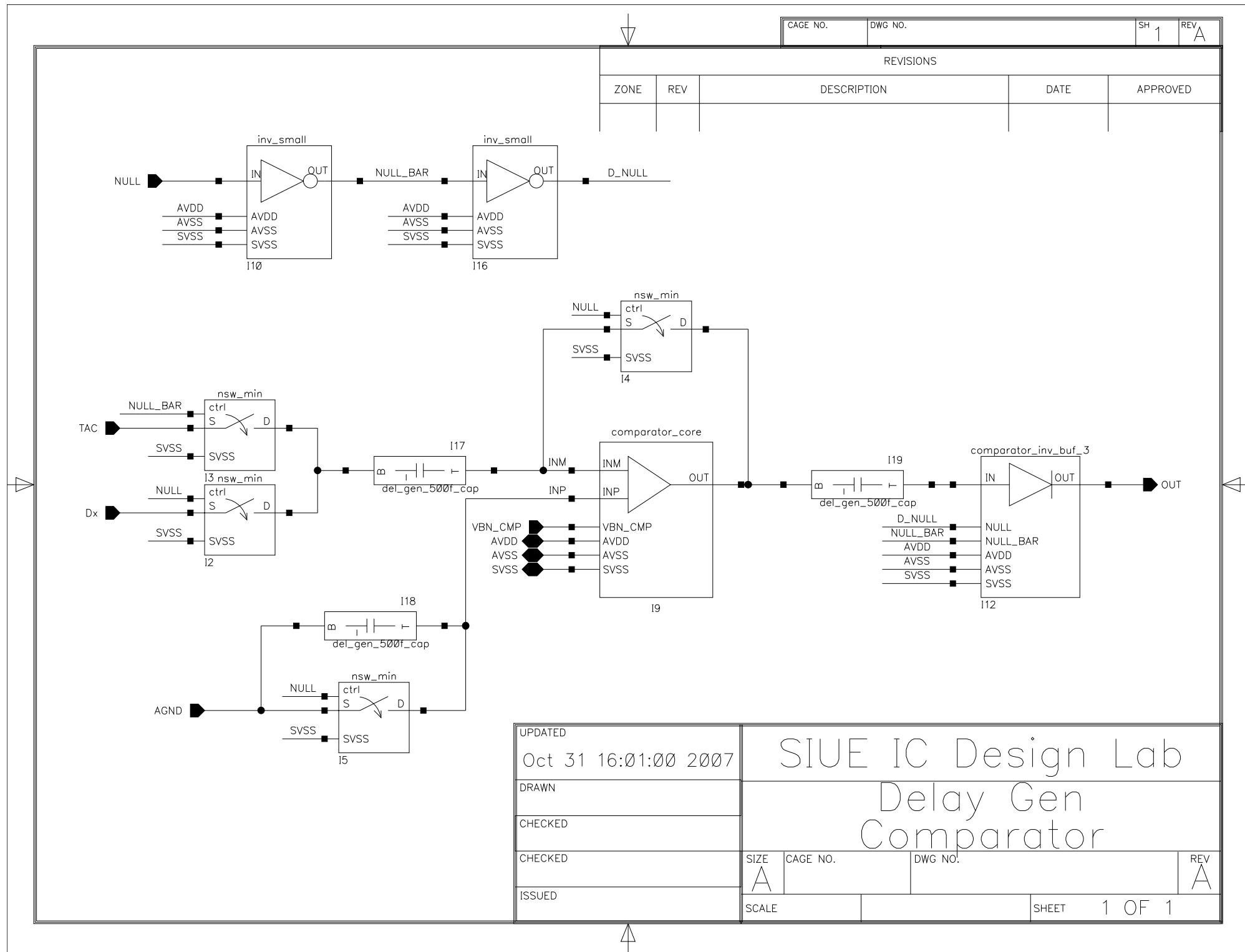
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Aug 1 12:15:27 2007	dec5to32		
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ISSUED	SCALE		SHEET 1 OF 1



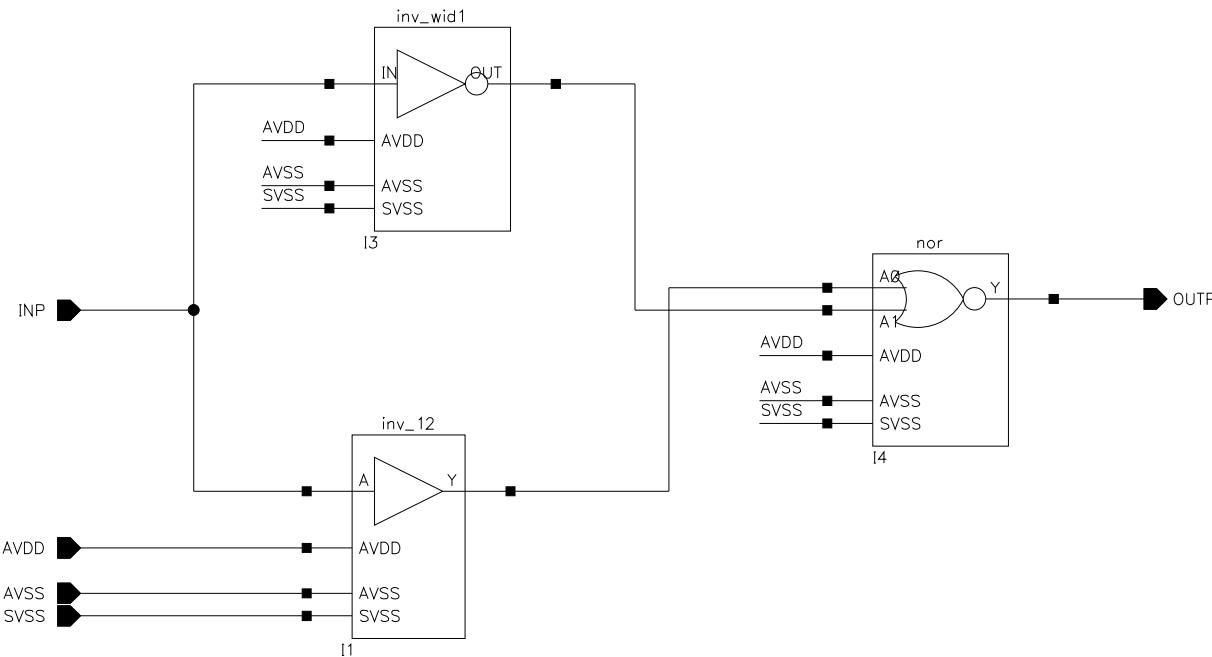




CAGE NO. DWG NO. SH 1 REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Jun 13 14:00:49 2007

edge\_det\_pos

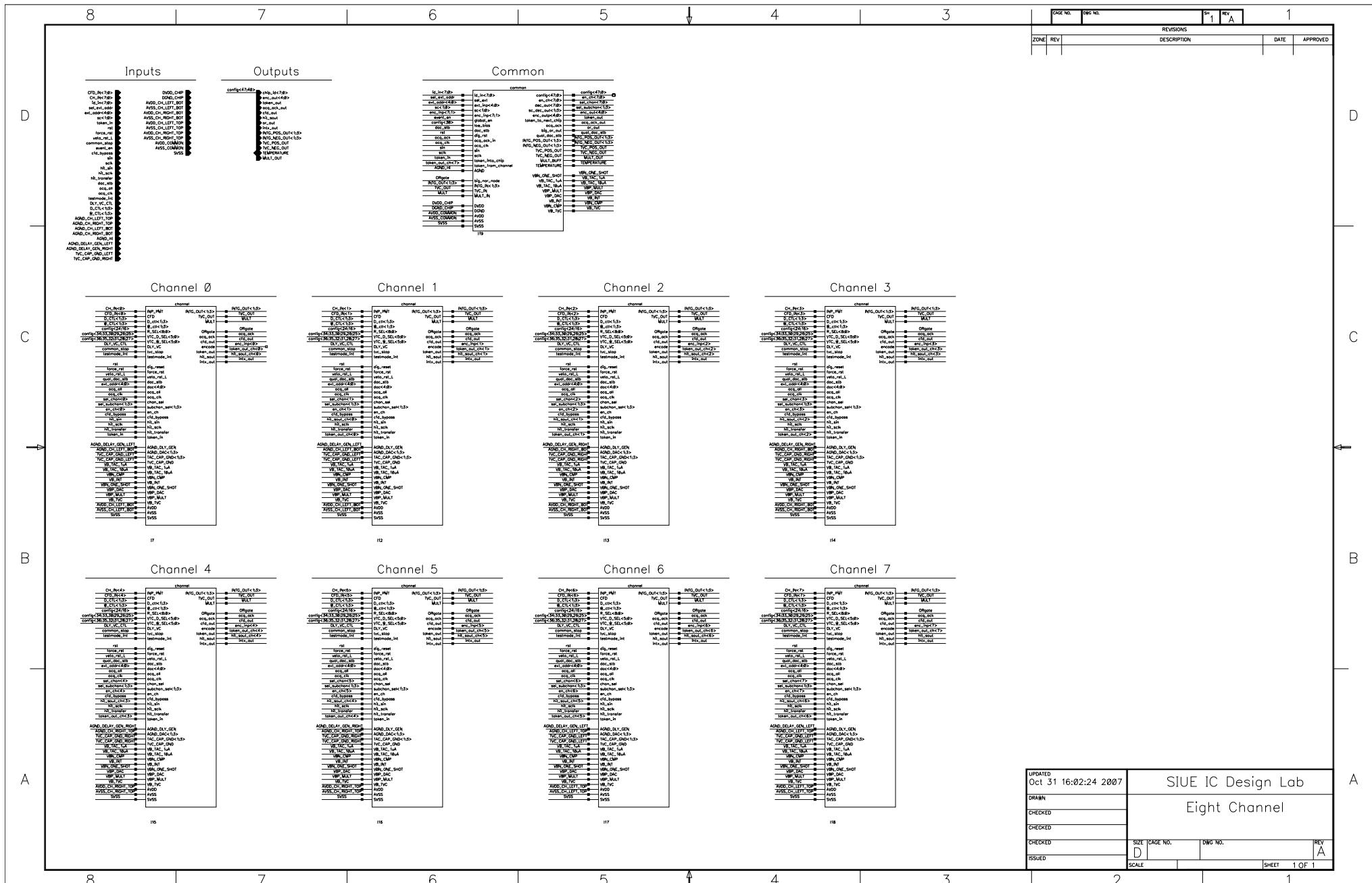
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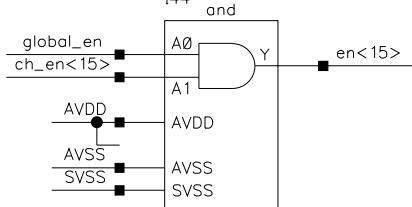
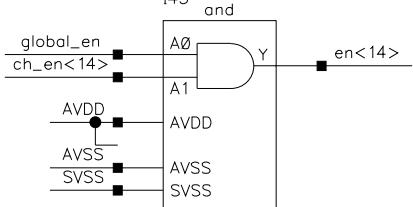
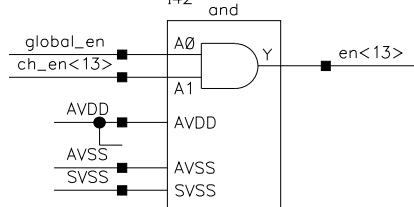
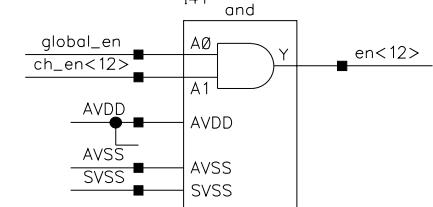
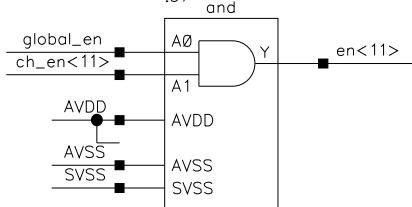
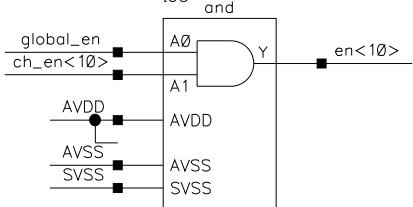
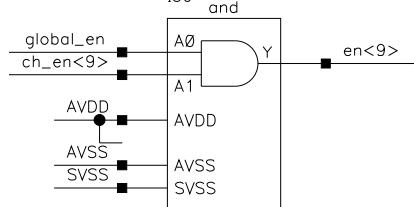
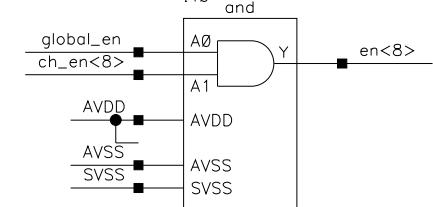
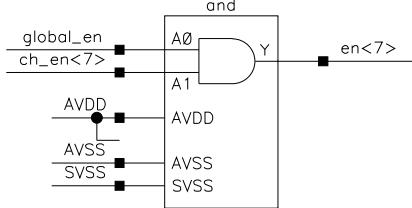
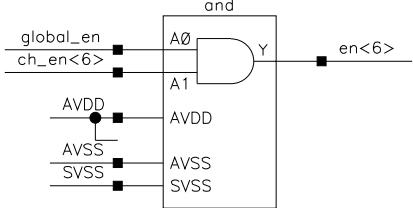
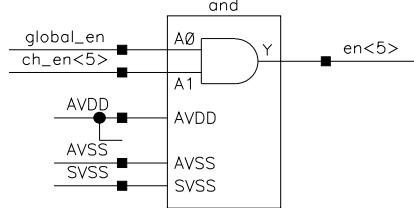
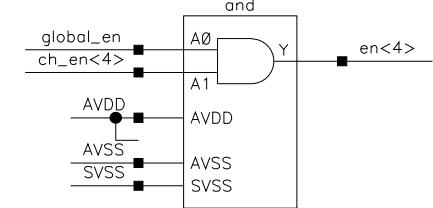
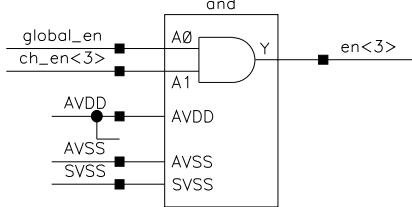
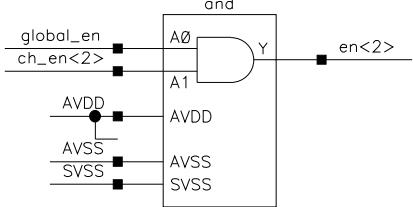
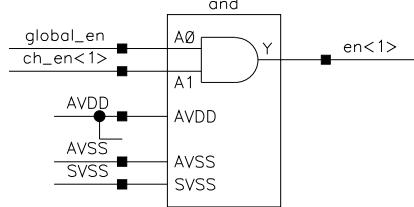
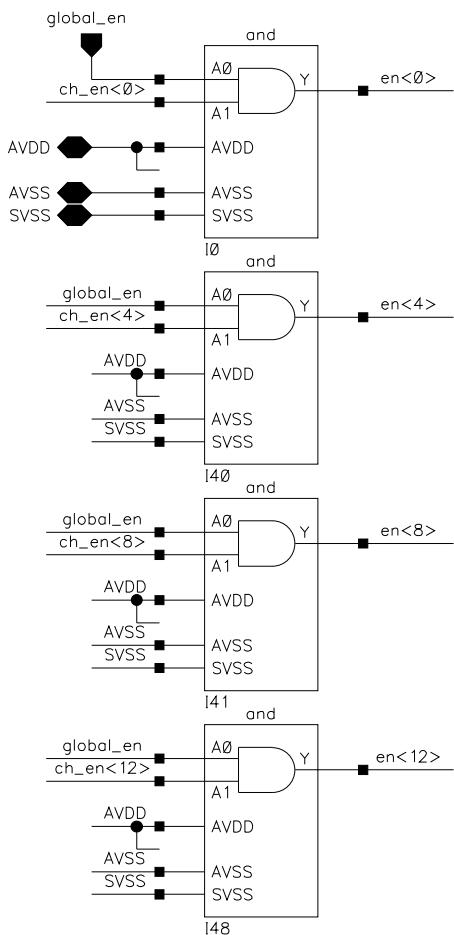
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SCALE				
SHEET	1 OF 1			



CAGE NO.	DWG NO.	SH 1	REV A
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



ch\_en&lt;15:0&gt; ➤

➤ en&lt;15:0&gt;

UPDATED

Jul 11 11:05:28 2007

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SIUE IC Design Lab  
Enable Logic

SIZE A

CAGE NO.

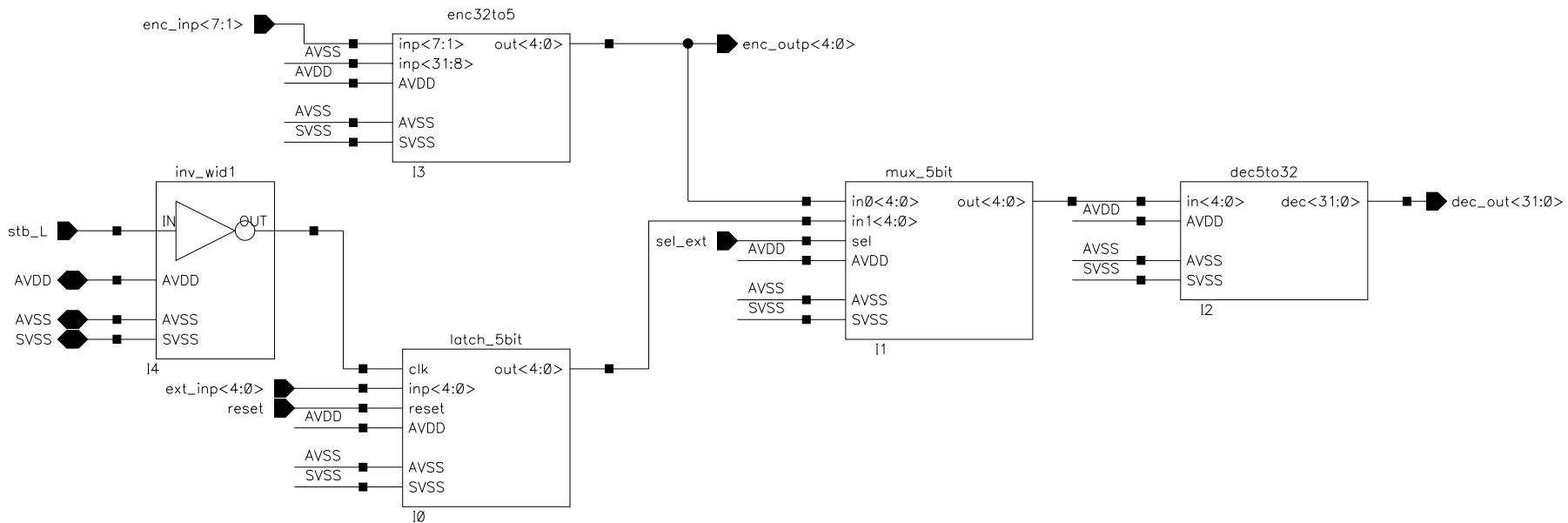
DWG NO.

REV A

SCALE

SHEET

1 OF 1



UPDATED  
Aug 2 14:16:39 2007

## enc\_dec\_logic

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SIZE | CAGE NO.

DWG NO

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REV

SCALE

SHEET 1 OF 1

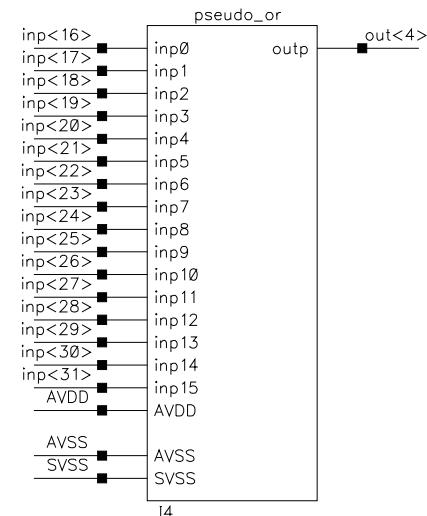
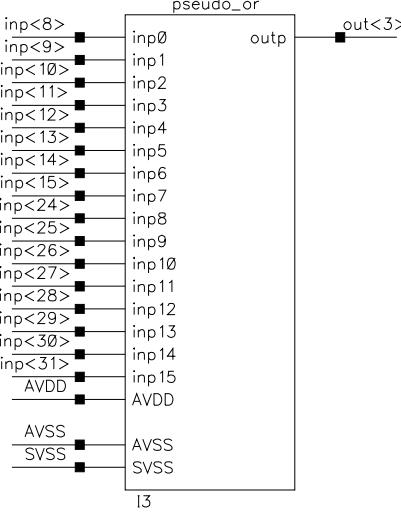
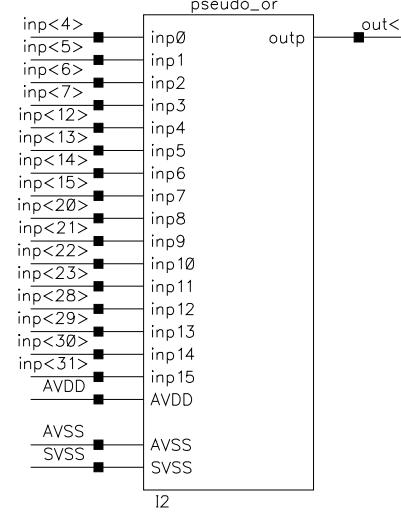
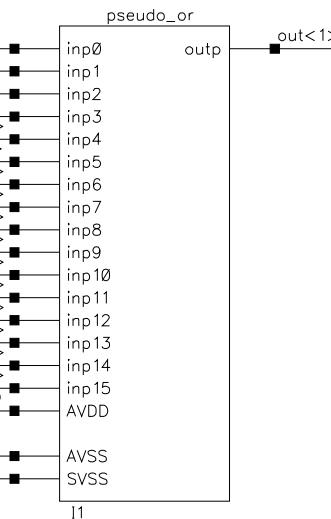
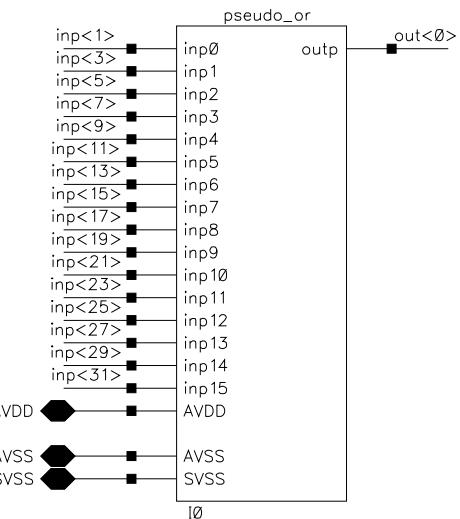
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

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out<4:0>

inp<31:8>



UPDATED

Jul 31 11:15:11 2007

enc32to5

DRAWN

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CHECKED

ISSUED

SIZE

A

CAGE NO.

DWG NO.

REV

SCALE

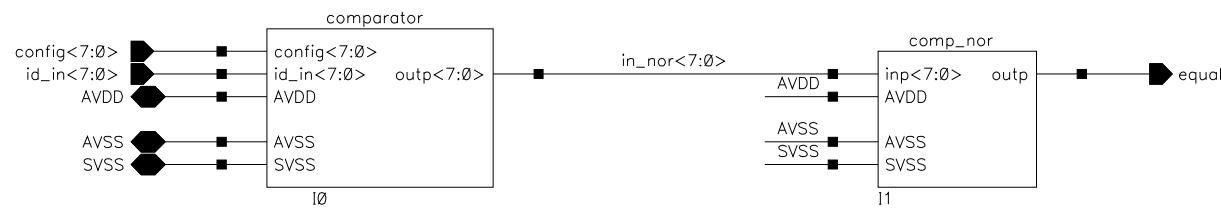
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1 OF 1

CAGE NO. DWG NO. SH 1 REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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ISSUED	SCALE		REV
			SHEET 1 OF 1

CAGE NO.

DWG NO.

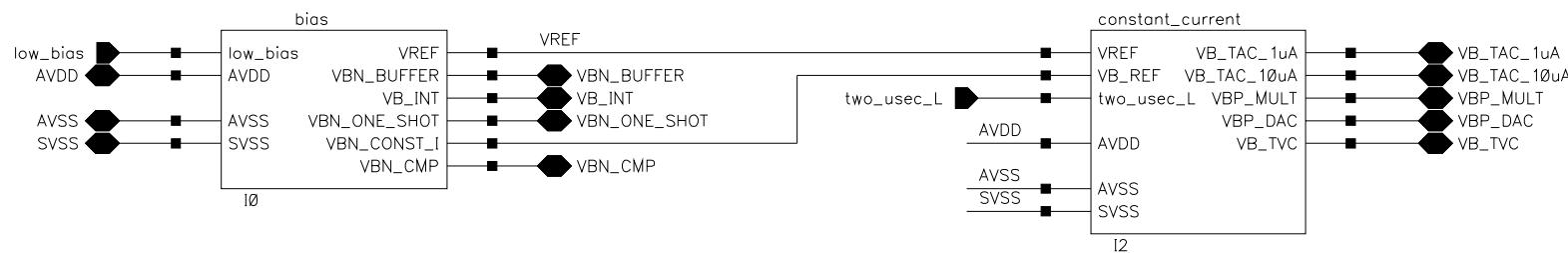
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1

REV

## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Oct 30 14:17:59 2007

full\_bias

DRAWN

CHECKED

CHECKED

ISSUED

SIZE

A

CAGE NO.

DWG NO.

REV

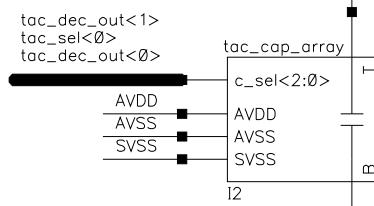
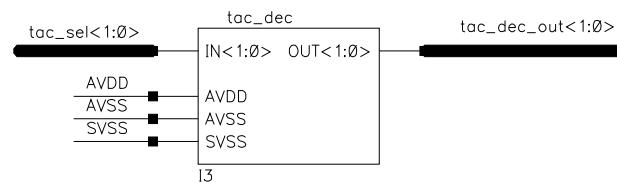
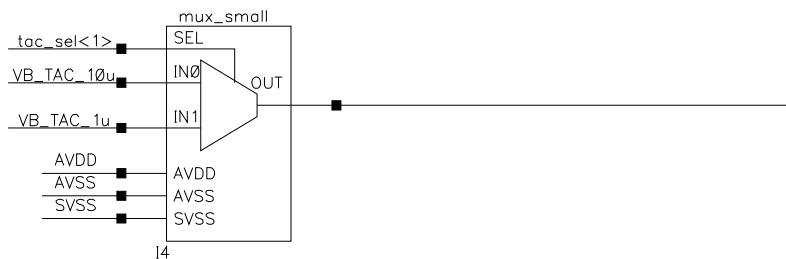
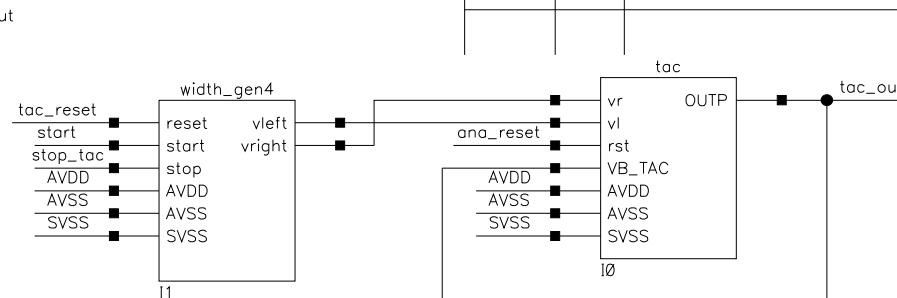
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SHEET 1 OF 1

## REVISIONS

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 stop\_tac  
 tac\_reset  
 ana\_reset  
 tac\_sel<1:0>  
 VB\_TAC\_10u  
 VB\_TAC\_1u  
 CAP\_GND  
 AVDD  
 AVSS  
 SVSS



CAP\_GND

tac_sel	I (uA)	C (pf)	T max (ns)	T min (ns)
00	10	0.2	50	5
01	10	1.0	250	25
10	1	0.6	1500	150
11	1	4.0	10000	1000

Note: Assume Vmax = 2.5 and Vmin = 0.25

UPDATED  
Oct 31 16:02:09 2007

full\_tac

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SIZE	CAGE NO.	DWG NO.	REV
A			

SCALE SHEET 1 OF 1

CAGE NO.

DWG NO.

SH 1

REV

## REVISIONS

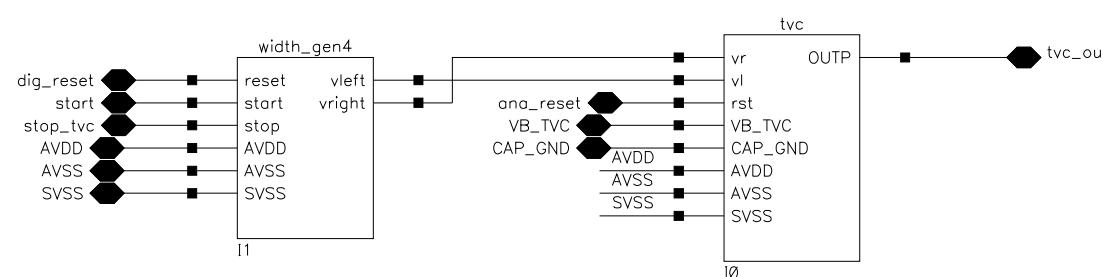
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REV

DESCRIPTION

DATE

APPROVED



UPDATED

Jul 9 11:21:55 2007

full\_tvc

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ISSUED

SIZE

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CAGE NO.

DWG NO.

REV

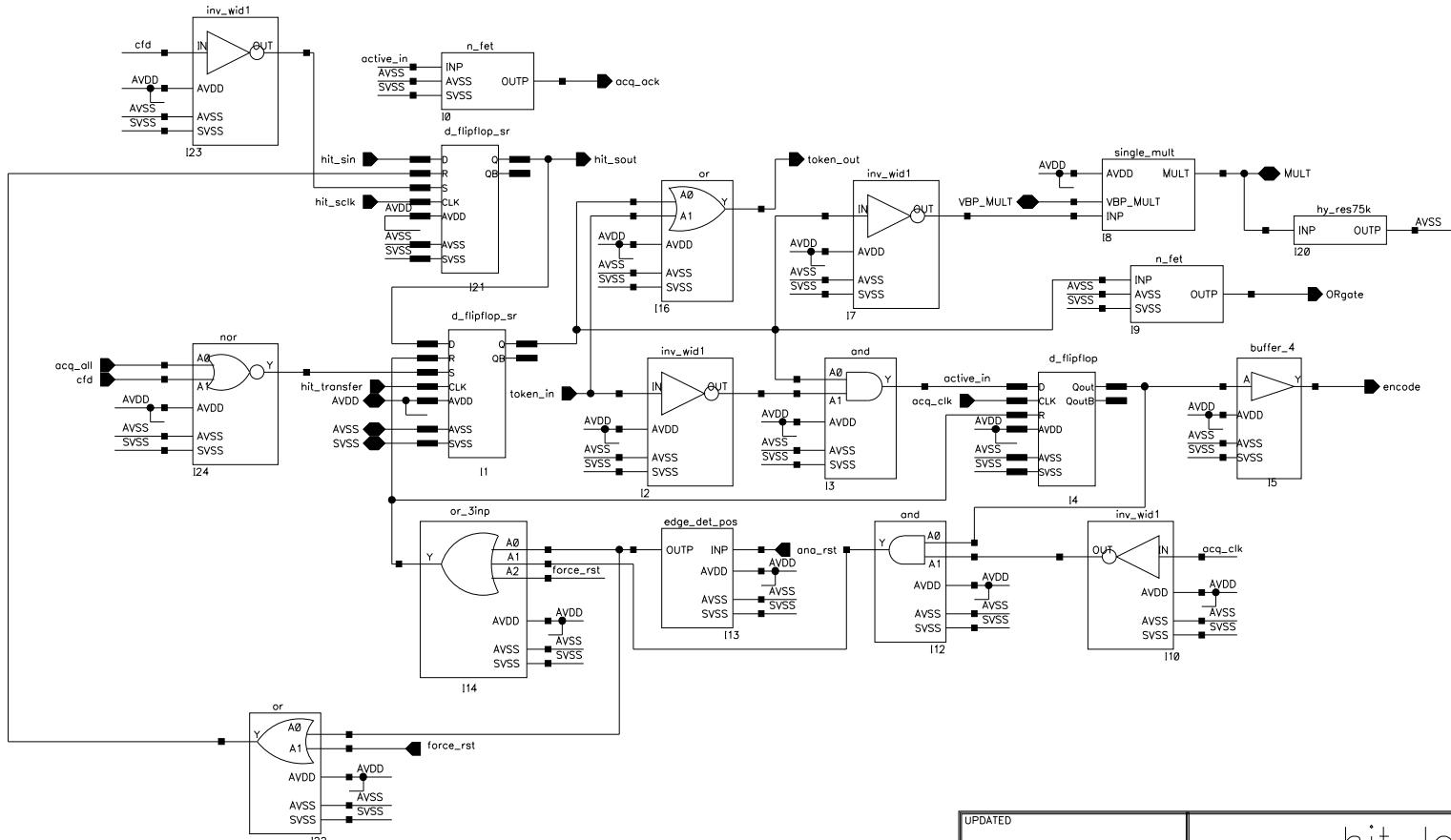
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SHEET 1 OF 1

CAGE NO. DWG NO. SH 1 REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Aug 9 16:00:35 2007

hit\_logic

DRAWN

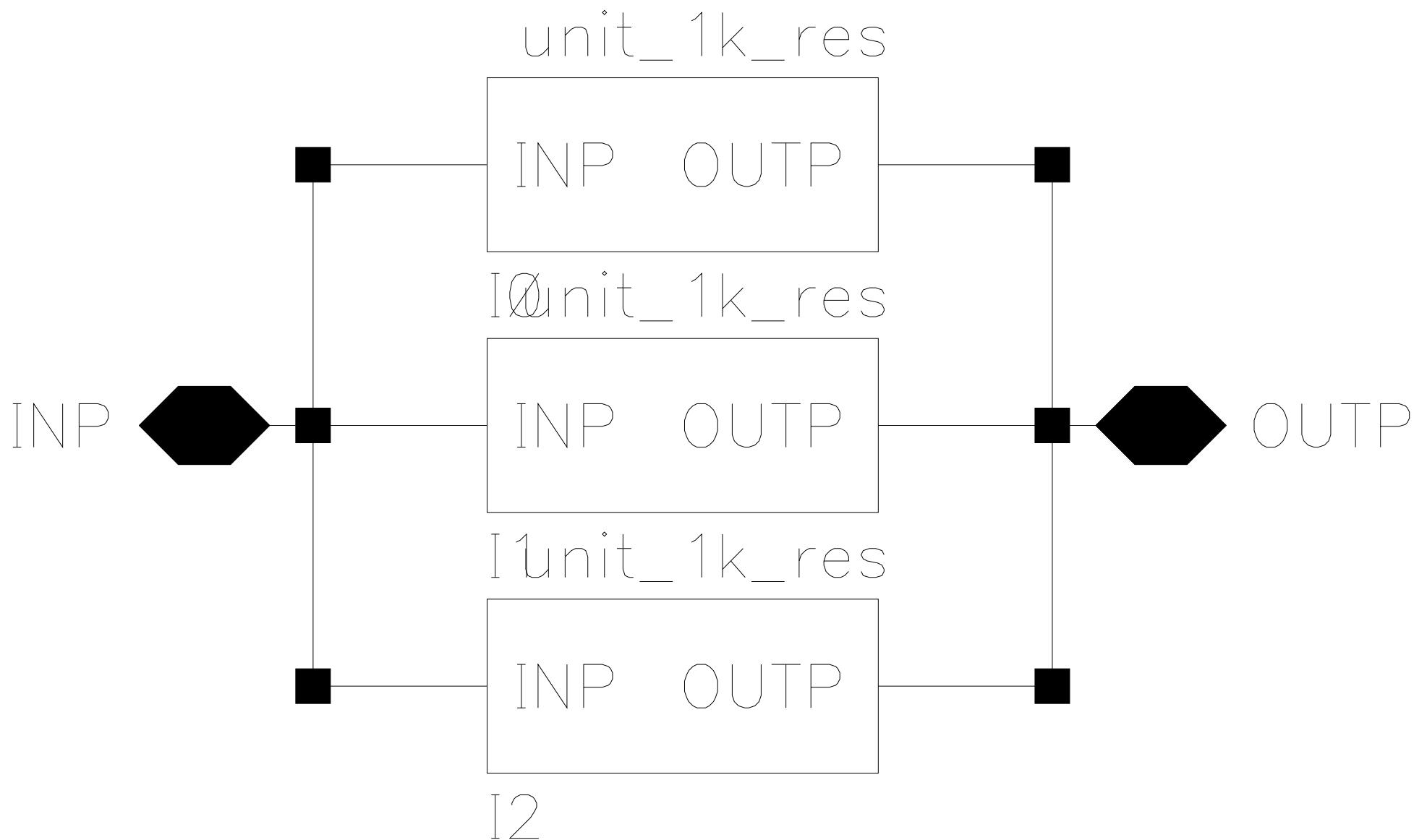
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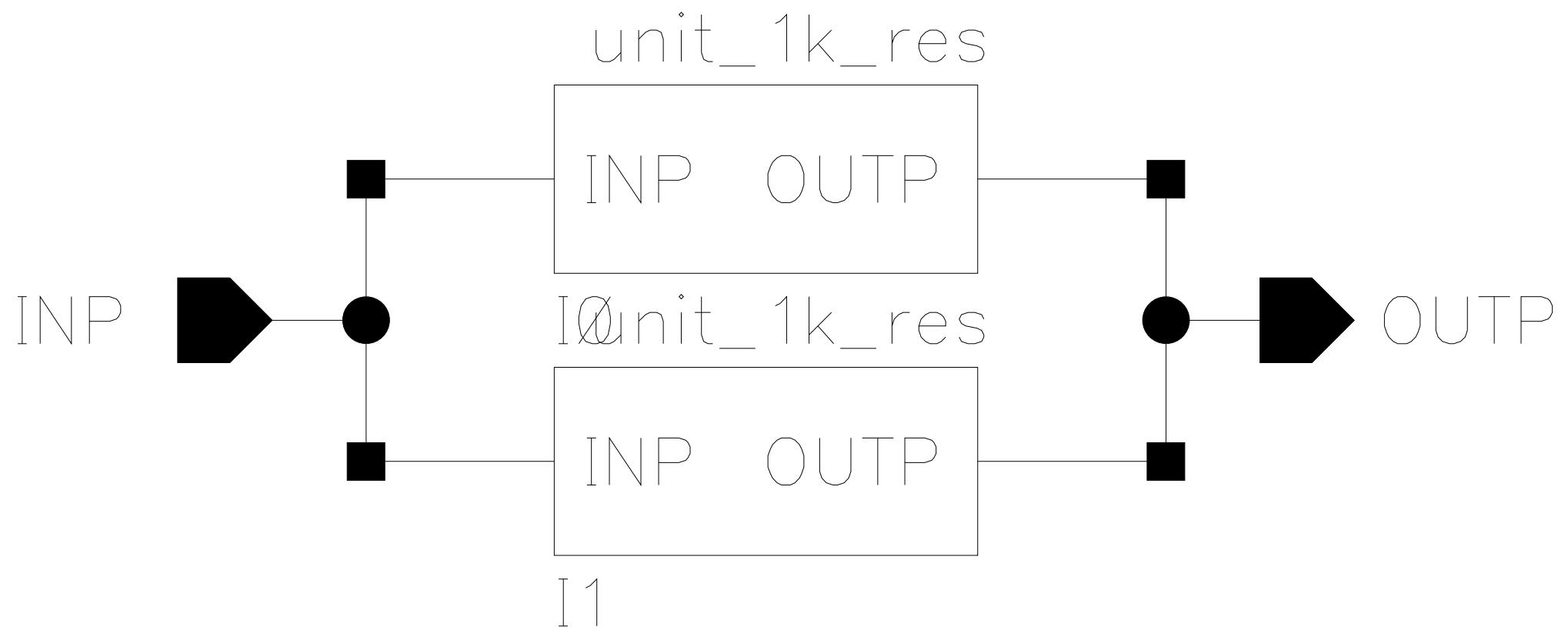
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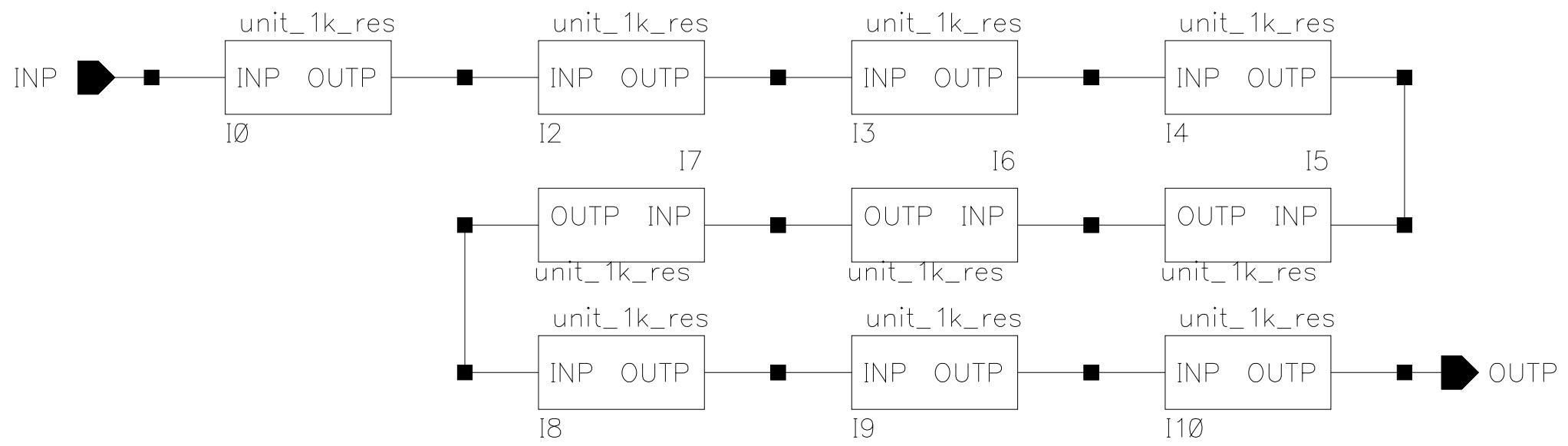
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SIZE B CAGE NO. DWG NO. REV

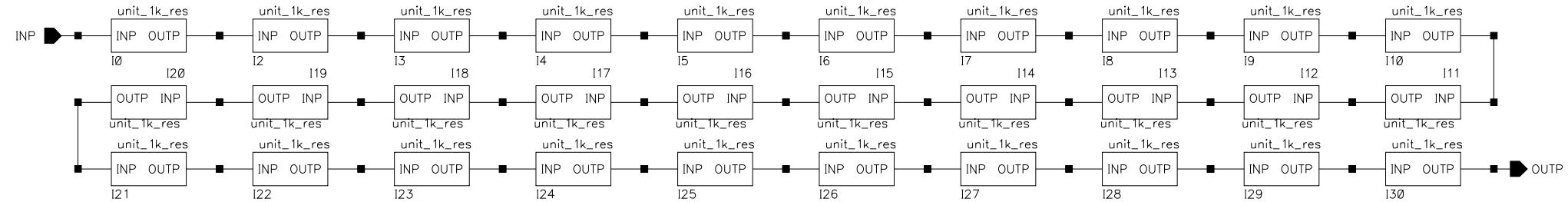
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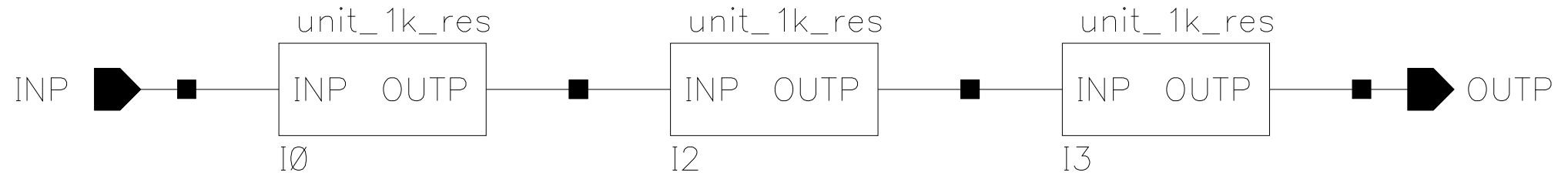


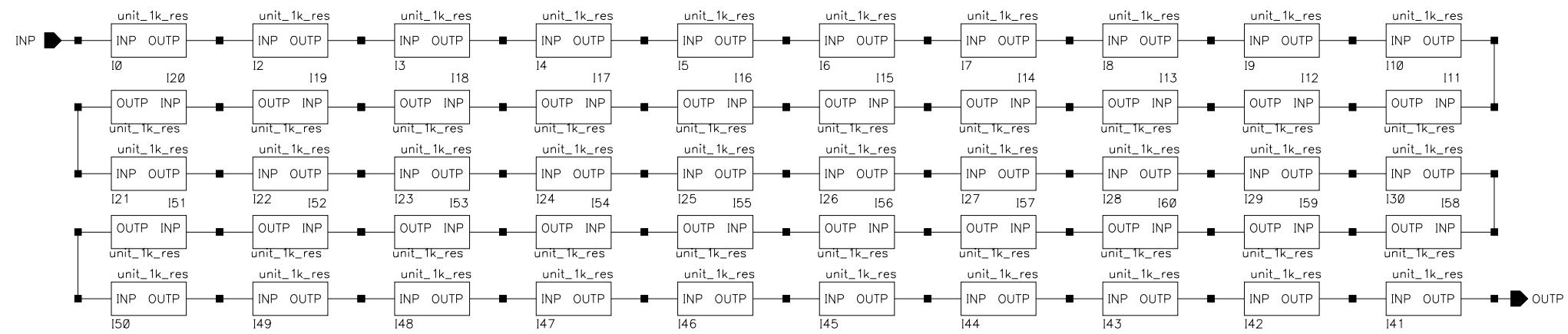


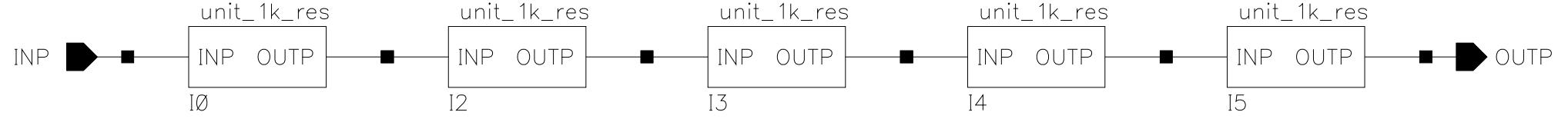












CAGE NO.

DWG NO.

SH

1

REV

## REVISIONS

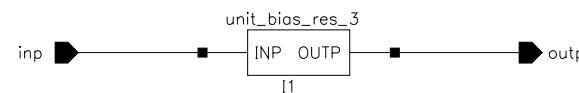
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REV

DESCRIPTION

DATE

APPROVED



UPDATED

Oct 30 15:50:11 2007

hy\_resØ\_59k

DRAWN

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SIZE

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CAGE NO.

DWG NO.

REV

SCALE

SHEET 1 OF 1

CAGE NO.

DWG NO.

SH 1

REV

## REVISIONS

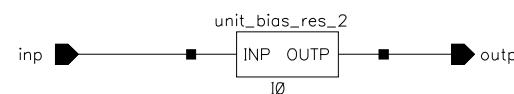
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DATE

APPROVED



UPDATED  
Oct 30 15:36:28 2007

hy\_res17k

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DWG NO.

REV

SCALE

SHEET 1 OF 1



CAGE NO.

DWG NO.

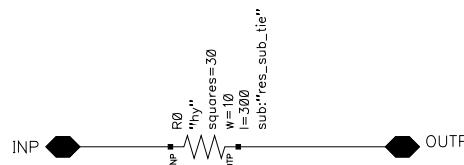
SH

1

REV

## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Aug 16 14:34:22 2007

hy\_res30k

DRAWN

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SIZE  
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DWG NO.

REV

SCALE

SHEET 1 OF 1



CAGE NO.

DWG NO.

SH

1

REV

## REVISIONS

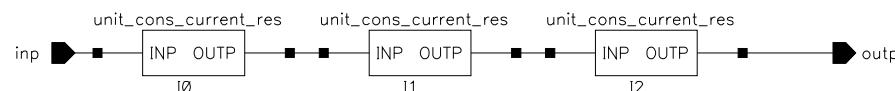
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REV

DESCRIPTION

DATE

APPROVED



UPDATED  
Oct 30 15:34:02 2007

hy\_res38k

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ISSUED

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CAGE NO.

DWG NO.

REV

SCALE

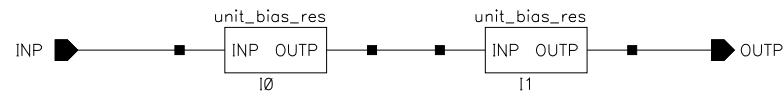
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1 OF 1

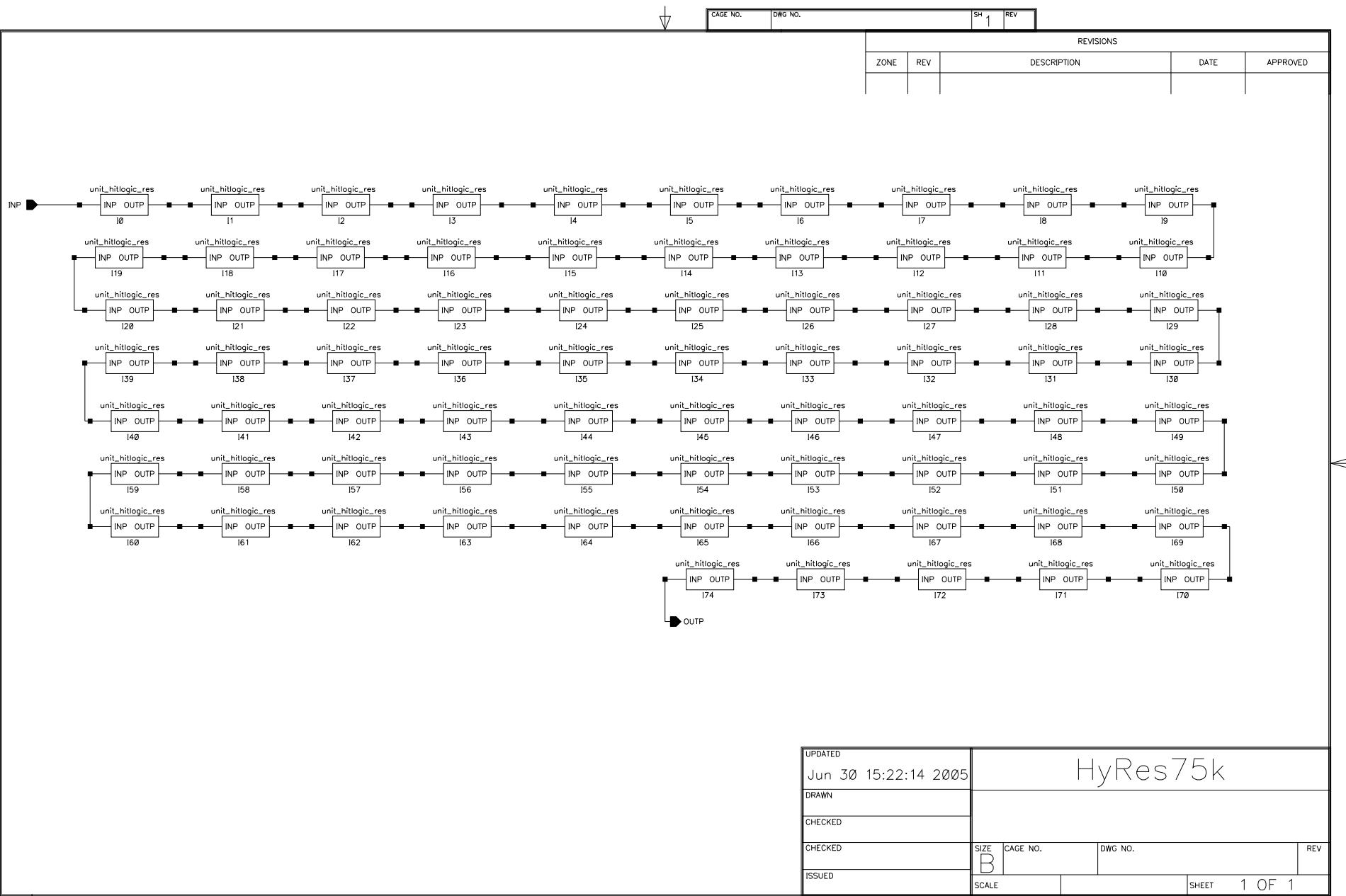
CAGE NO.	DWG NO.	SH 1	REV
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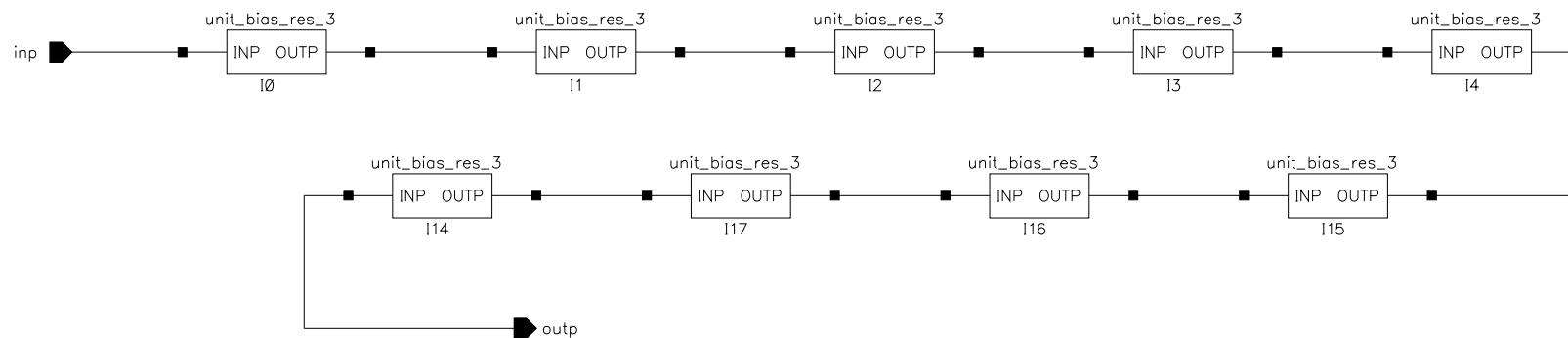
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ISSUED	SCALE		REV
			SHEET 1 OF 1



CAGE NO. DWG NO. SH 1 REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Oct 30 15:37:15 2007

hy\_res9x0\_59k

DRAWN

CHECKED

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SIZE  
A

CAGE NO.

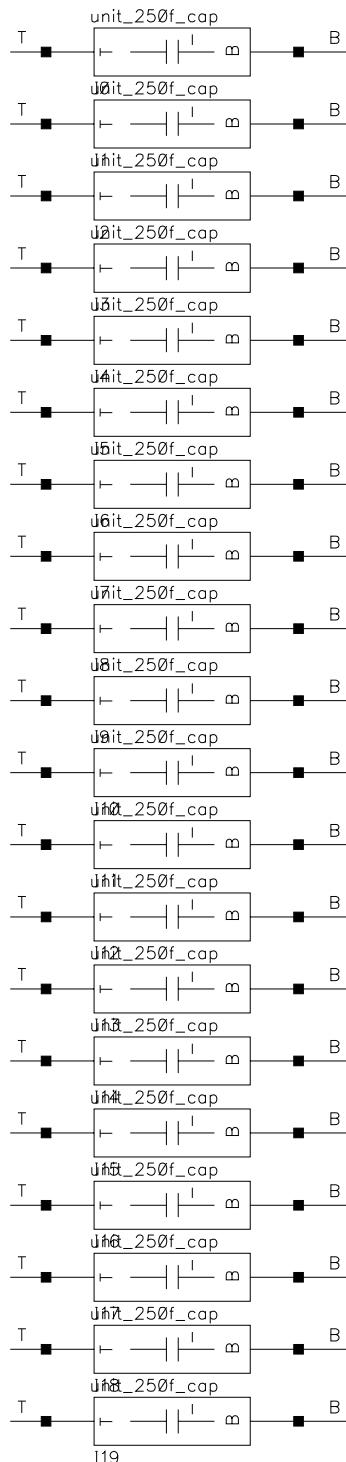
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REV

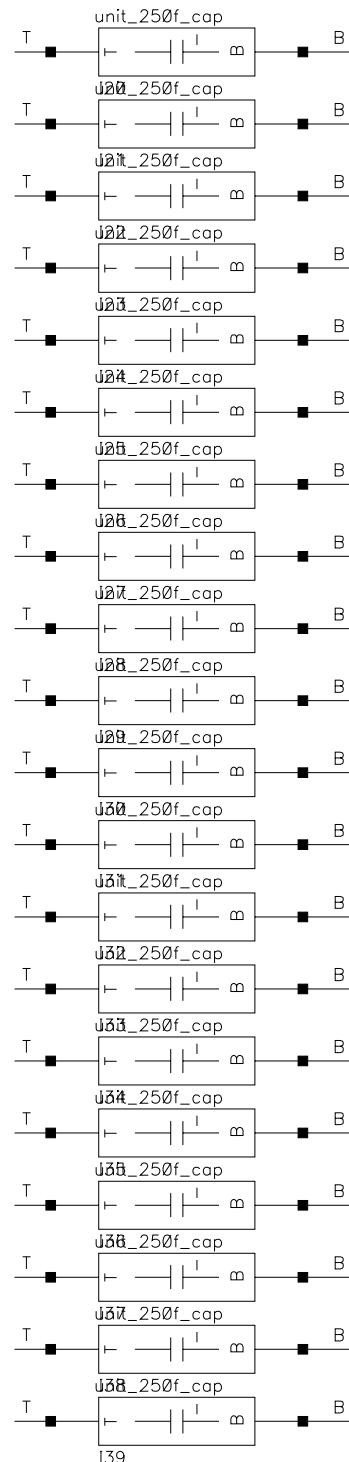
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SHEET 1 OF 1

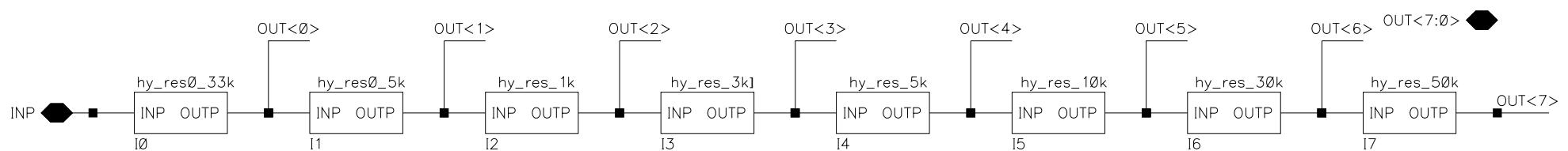
T ◆◆ B ◆◆



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Output	Resistance
OUT<0>	0.5 K
OUT<1>	1 K
OUT<2>	2 K
OUT<3>	5 K
OUT<4>	10 K
OUT<5>	20 K
OUT<6>	50 K
OUT<7>	100 K

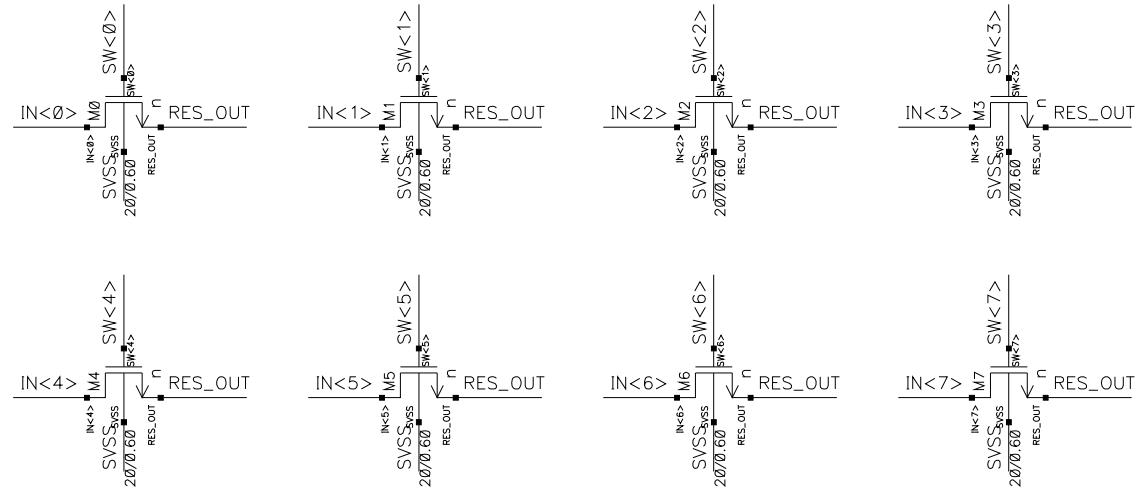
Resistances include the switch resistance following the resistor array.

IN<7:0>  
SW<7:0>  
chan\_sel  
DUMP  
AVDD  
AVSS  
SVSS

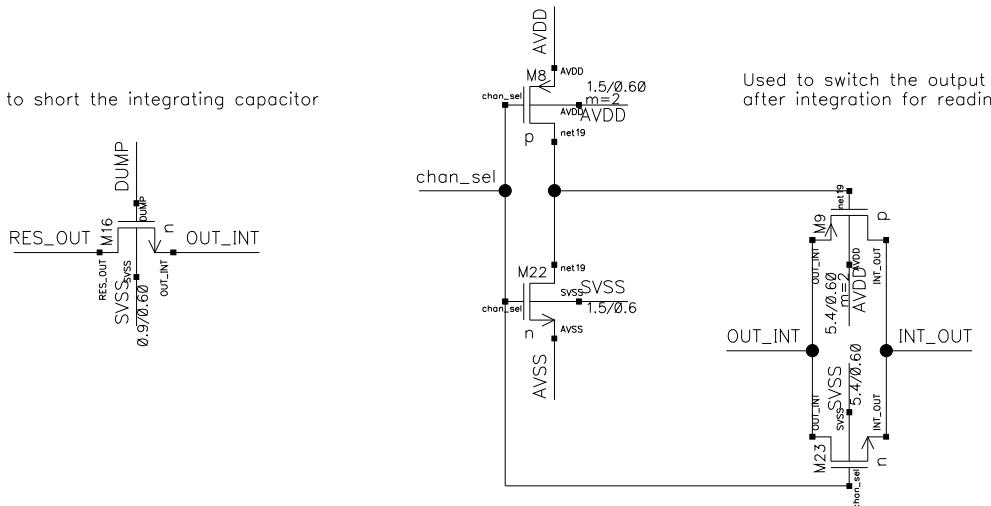
OUT\_INT  
RES\_OUT  
INT\_OUT

Switch	Resistance
SW<0>	0.5 K
SW<1>	1 K
SW<2>	2 K
SW<3>	5 K
SW<4>	10 K
SW<5>	20 K
SW<6>	50 K
SW<7>	100 K

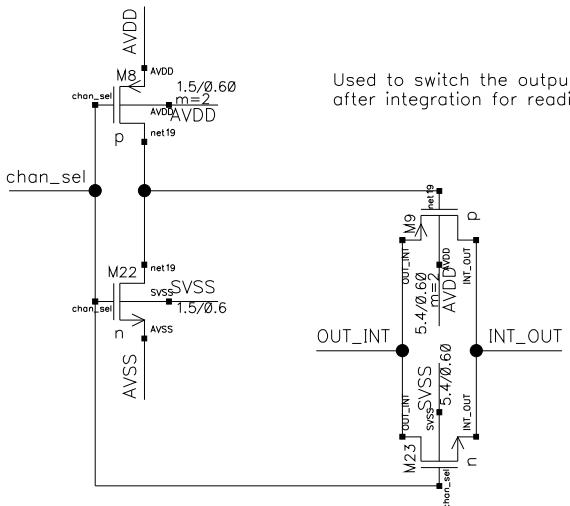
Resistances include the switch resistance  
and the resistor array preceding the switch.

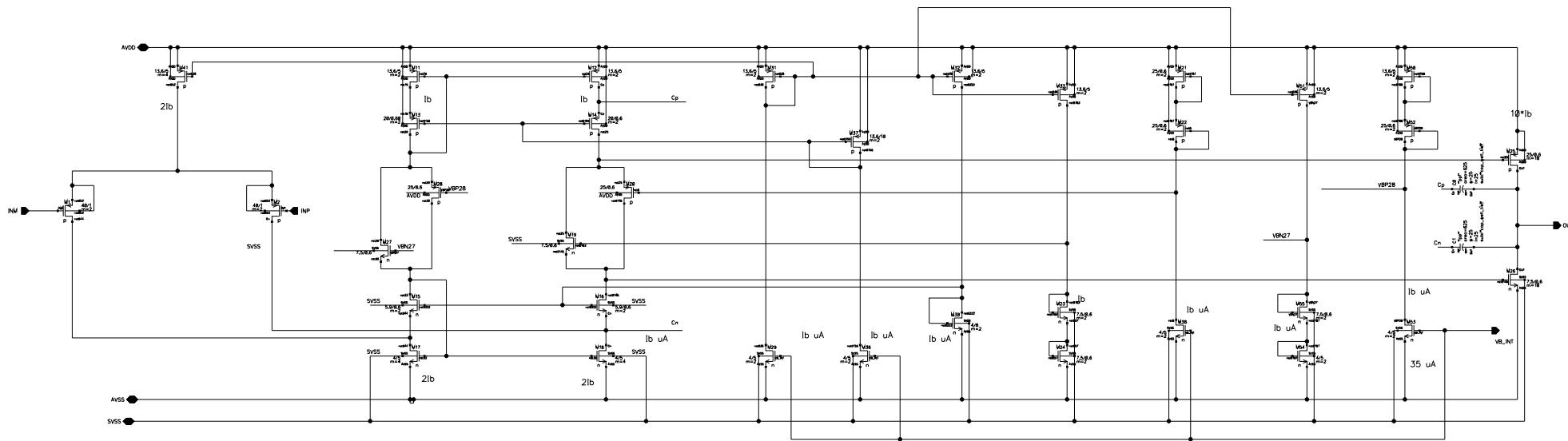


Used to short the integrating capacitor



Used to switch the output of the OTA  
after integration for reading purposes.

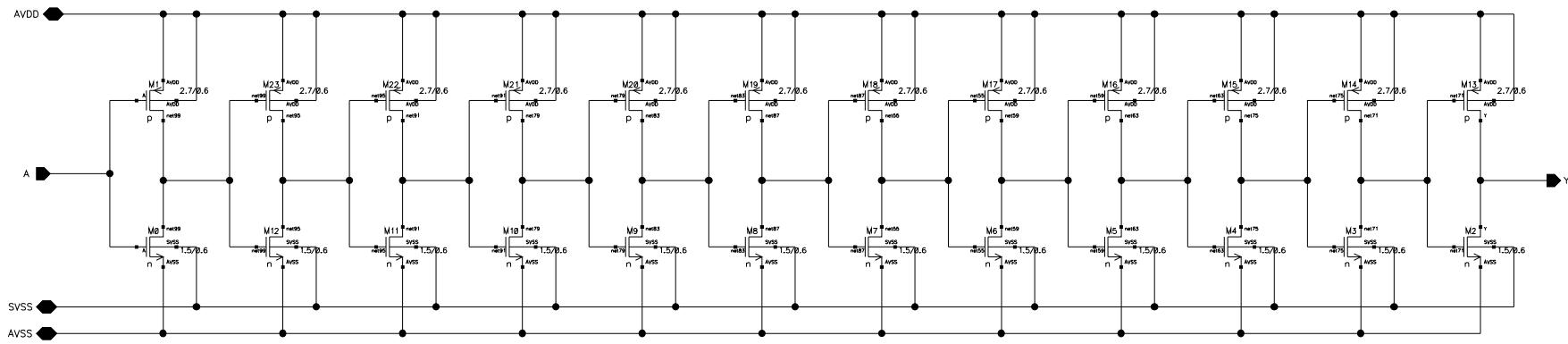




CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

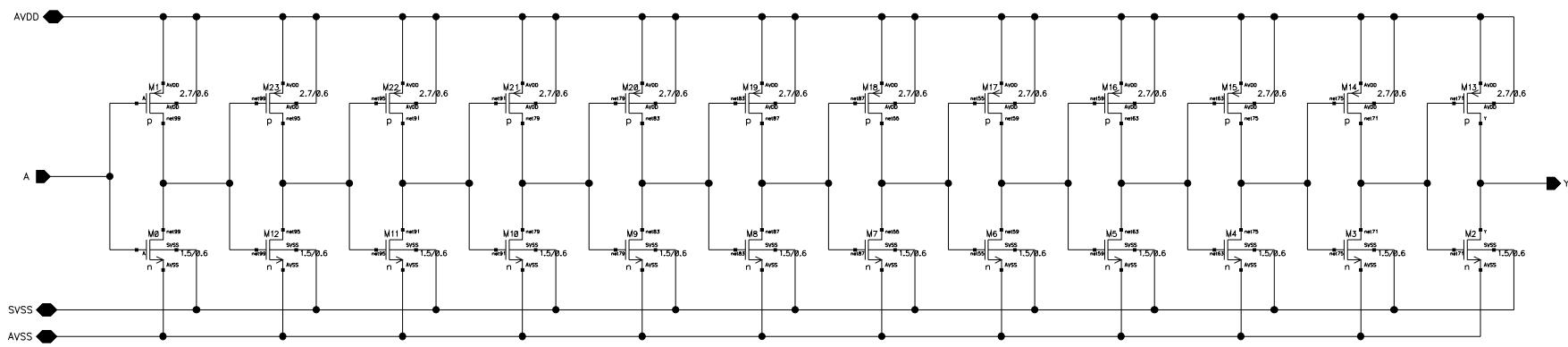


UPDATED Jun 11 12:04:17 2007	inv_12		
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ISSUED	SCALE		REV
		SHEET 1 OF 1	

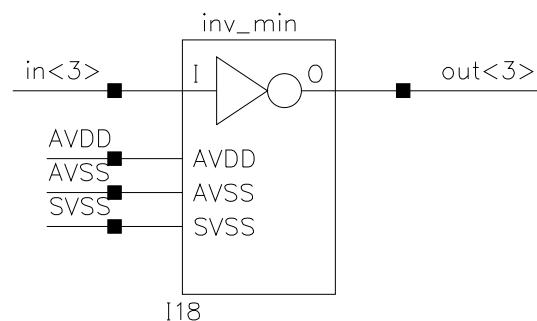
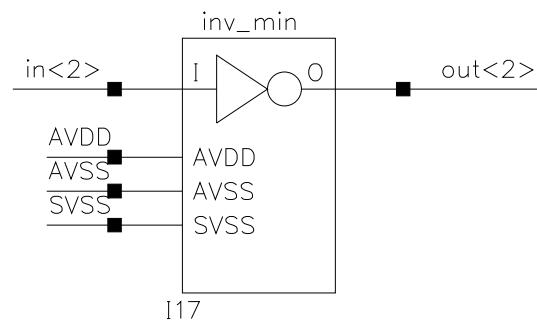
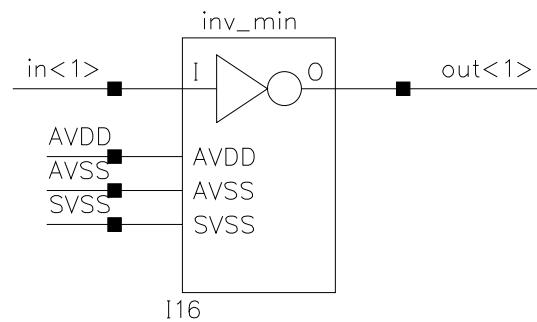
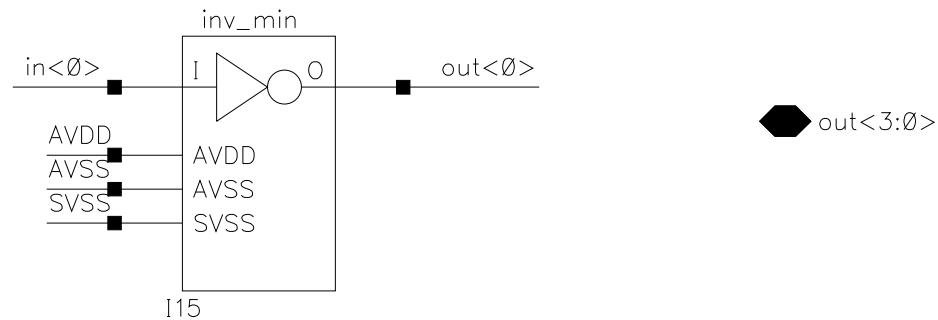
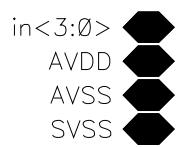
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REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



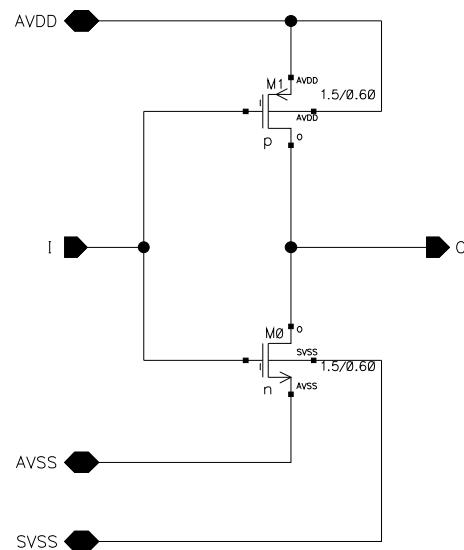
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CHECKED	SIZE B	CAGE NO.	DWG NO.
ISSUED	SCALE		REV
		SHEET 1 OF 1	



CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Jul 9 15:23:25 2007

inv\_min

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SIZE A	CAGE NO.	DWG NO.	REV
	SCALE		SHEET 1 OF 1

CAGE NO.

DWG NO.

SH 1

REV

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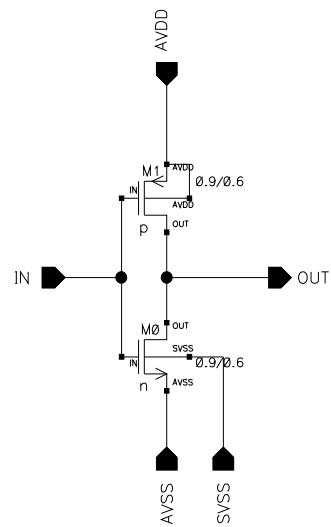
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REV

DESCRIPTION

DATE

APPROVED



UPDATED  
Aug 15 11:38:53 2007

inverter

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CAGE NO.

DWG NO.

REV

SCALE

SHEET 1 OF 1

CAGE NO.

DWG NO.

SH 1

REV

## REVISIONS

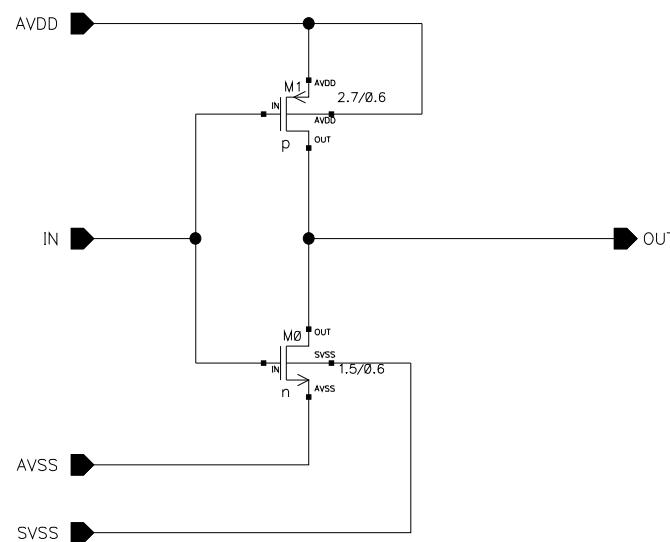
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REV

DESCRIPTION

DATE

APPROVED



UPDATED

Jul 5 15:27:12 2007

inv\_wid1

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A

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REV

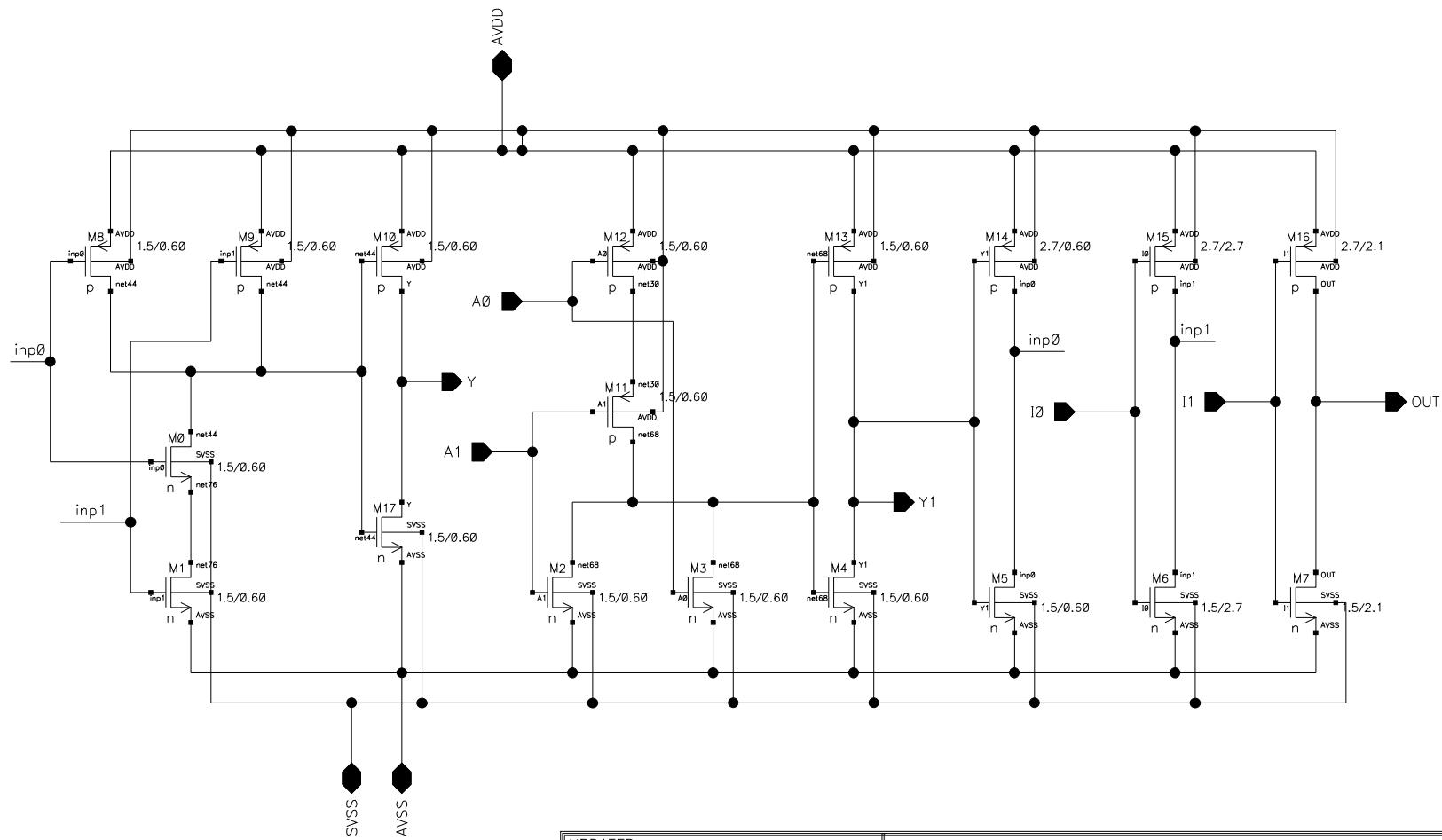
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SHEET

1 OF 1

## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED

Jul 9 10:40:23 2007

DRAWN

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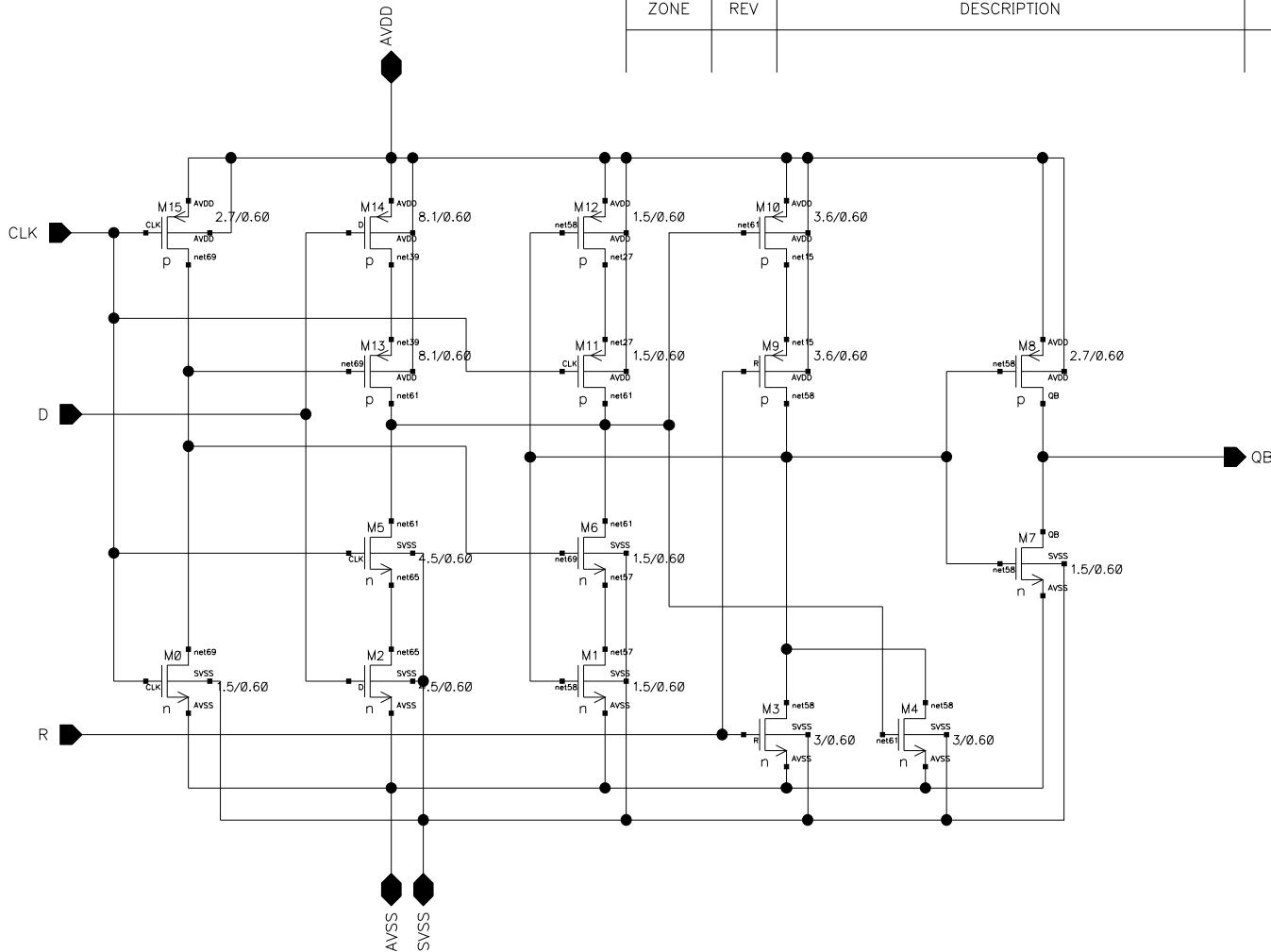
CHECKED

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SIZE	CAGE NO.	DWG NO.	REV
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SCALE			SHEET 1 OF 1

## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Jul 9 10:44:29 2007

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SIZE	CAGE NO.	DWG NO.	REV
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SCALE SHEET 1 OF 1

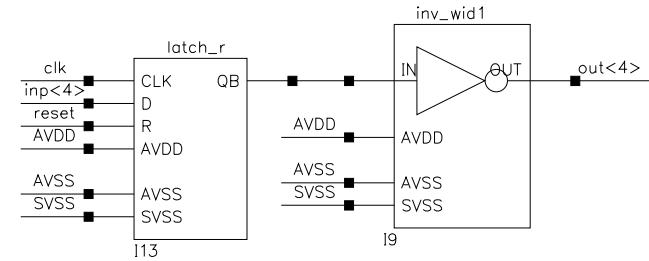
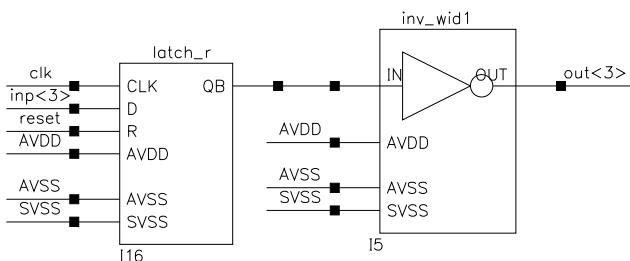
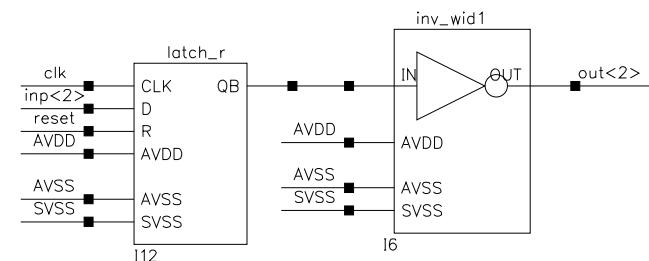
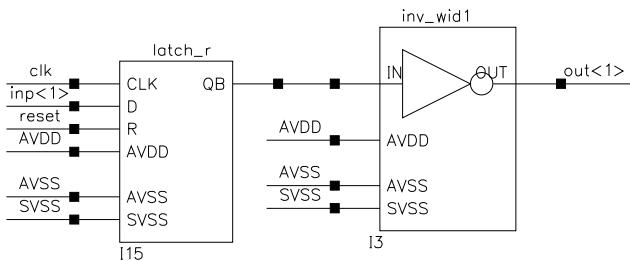
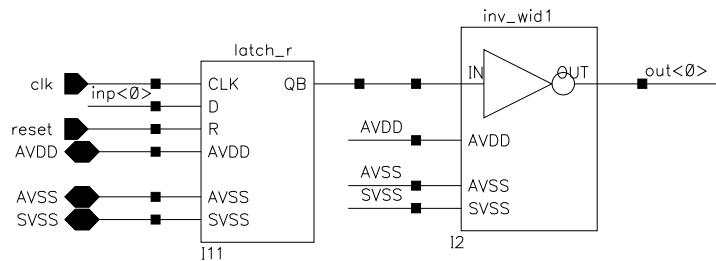
CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

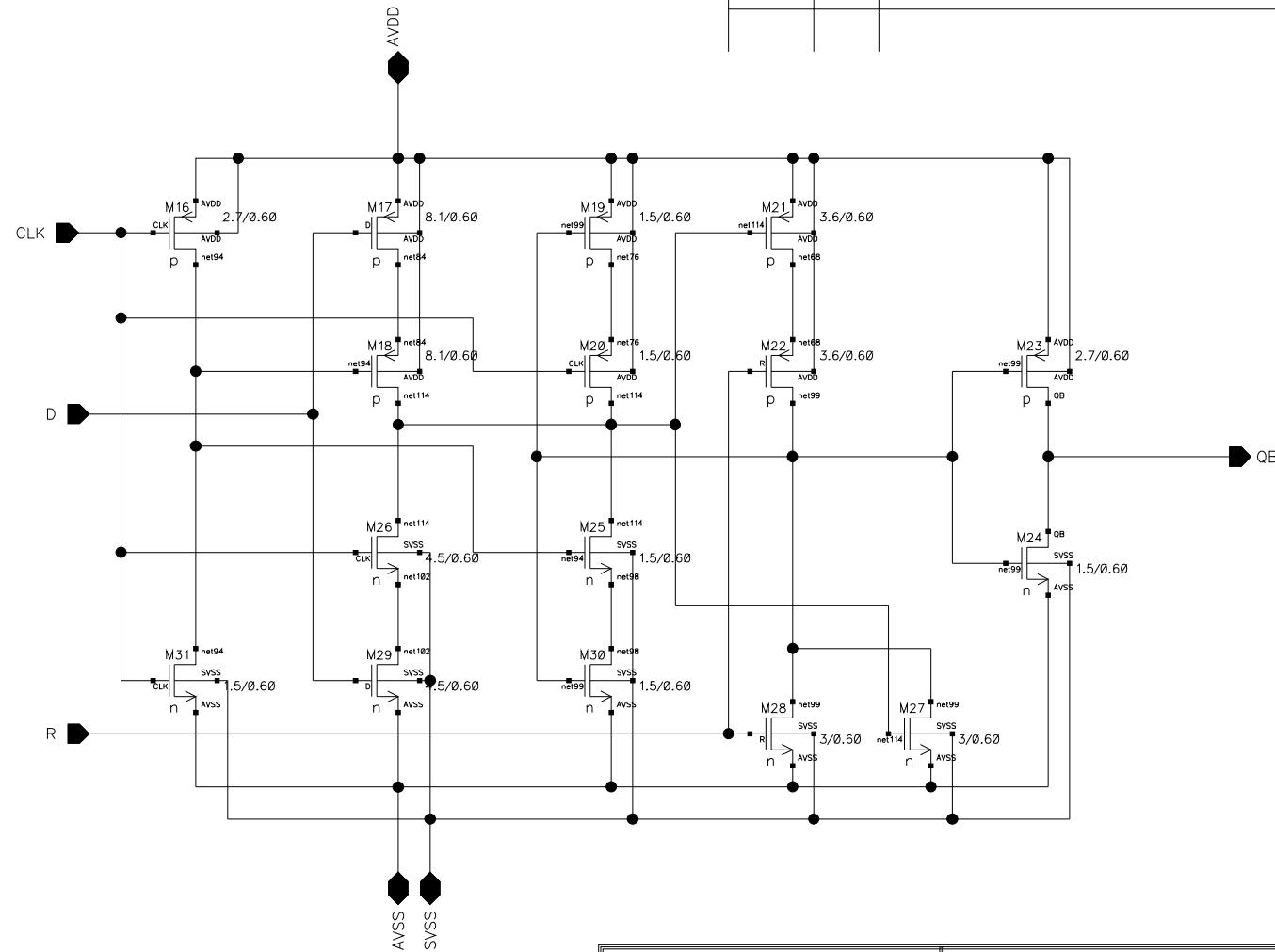
ZONE	REV	DESCRIPTION	DATE	APPROVED

inp&lt;4:0&gt;

out&lt;4:0&gt;



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	SHEET	1 OF 1	



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Jul 11 12:19:31 2007

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SHEET 1 OF 1

CAGE NO.

DWG NO.

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## REVISIONS

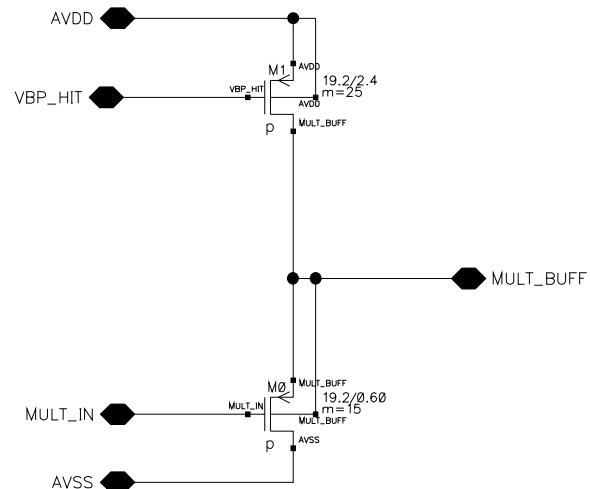
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Sep 12 17:19:01 2007

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SHEET 1 OF 1

REVISIONS

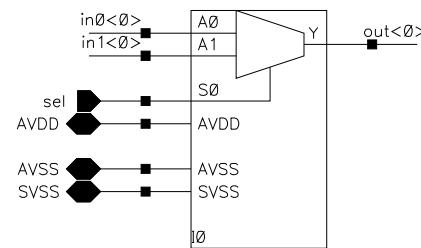
ZONE	REV	DESCRIPTION	DATE	APPROVED

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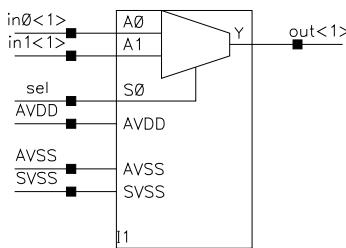
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in1<4:0>

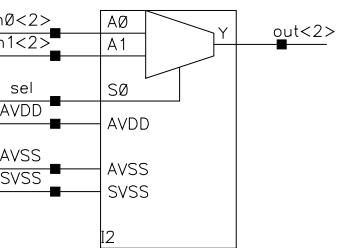
mux21



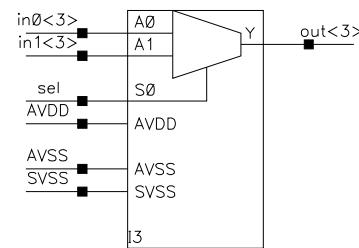
mux21



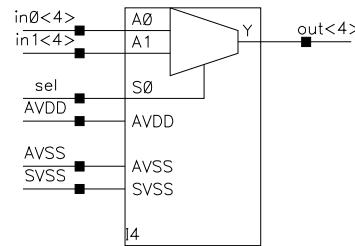
mux21



mux21



mux21



UPDATED  
Jul 11 12:02:37 2007

mux\_5bit

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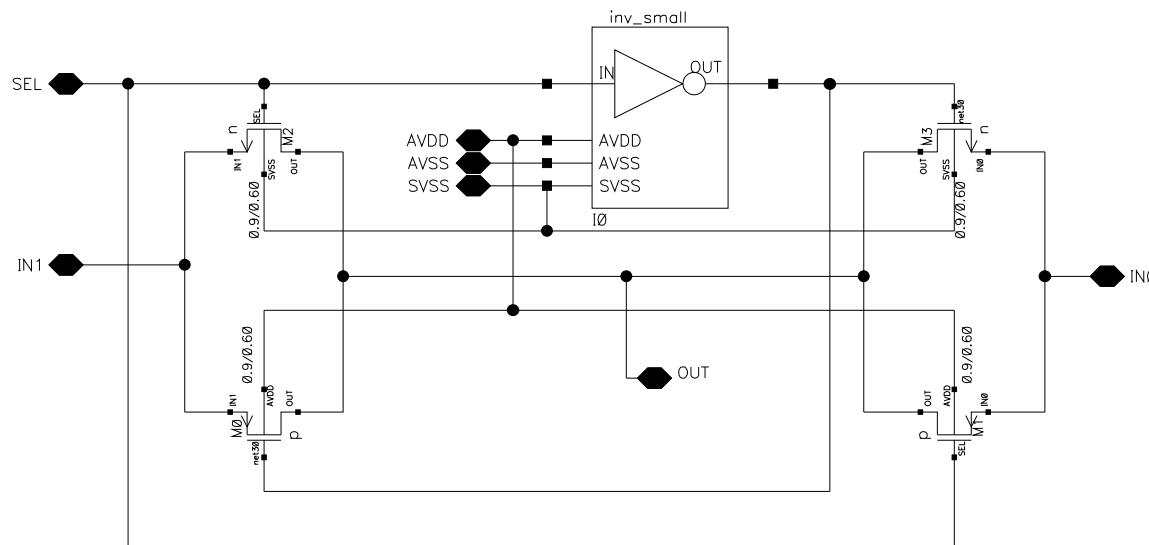
SHEET

1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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Oct 31 16:06:54 2007

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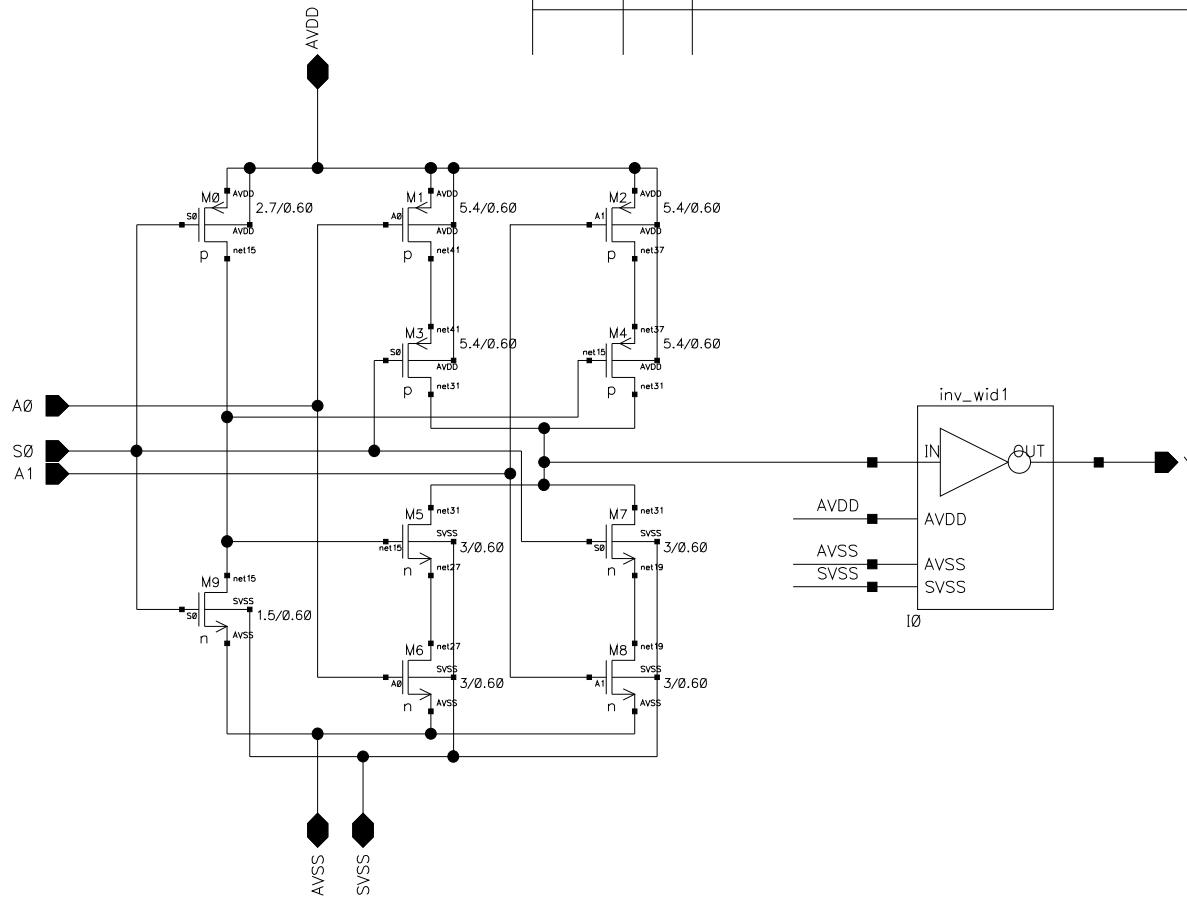
SCALE

SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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### REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED

Jul 5 15:27:21 2007

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SHEET 1 OF 1

CAGE NO.

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## REVISIONS

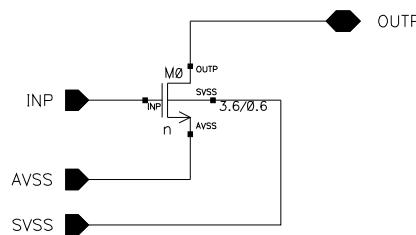
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Jul 24 14:51:53 2003

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SHEET 1 OF 1

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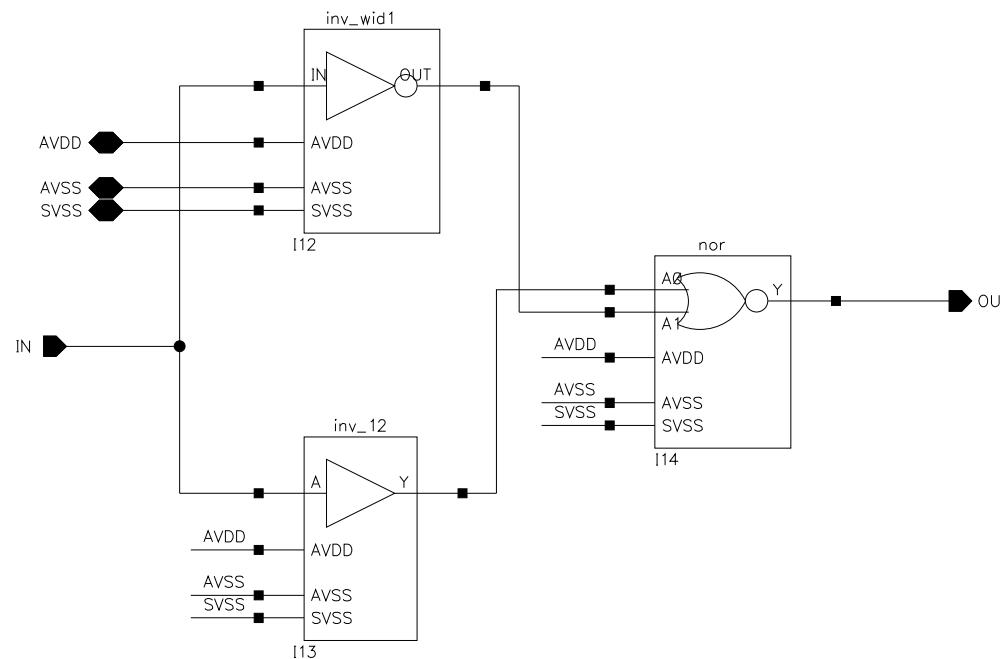
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Aug 13 15:53:22 2007

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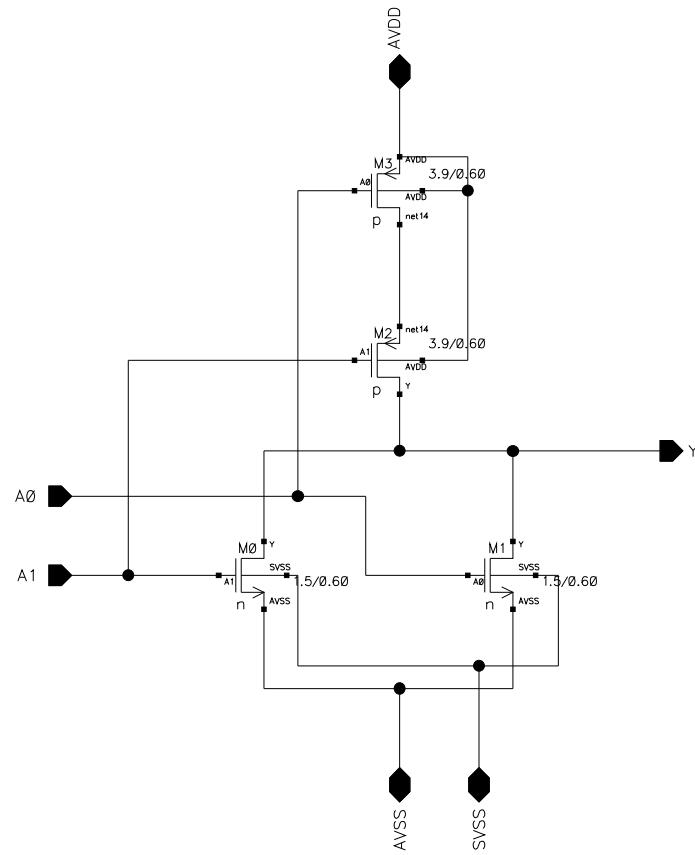
SCALE

SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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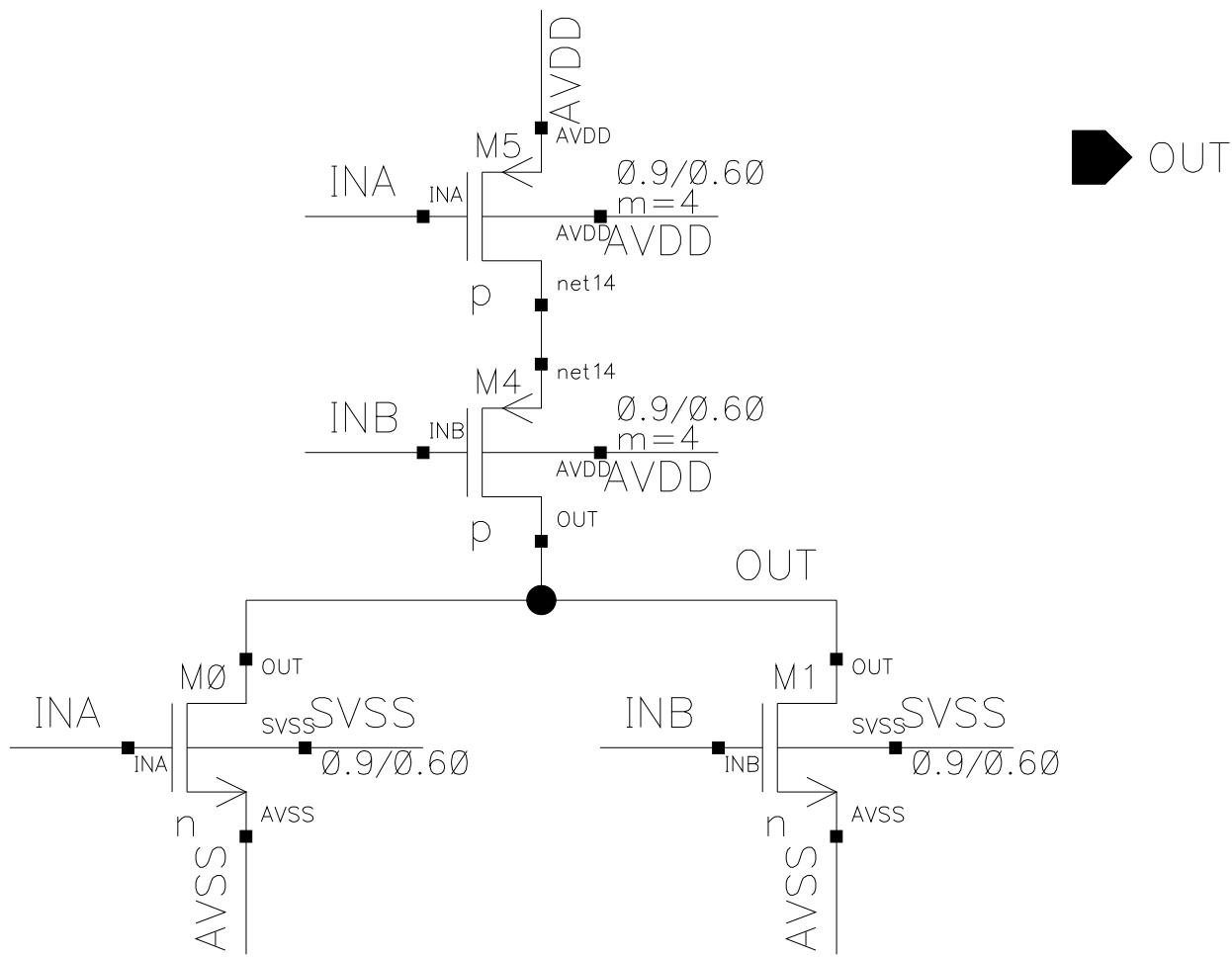
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SIZE	CAGE NO.	DWG NO.	REV
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SHEET		1 OF 1	

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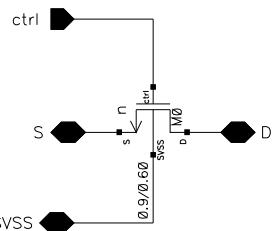
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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Apr 1 21:23:24 2007

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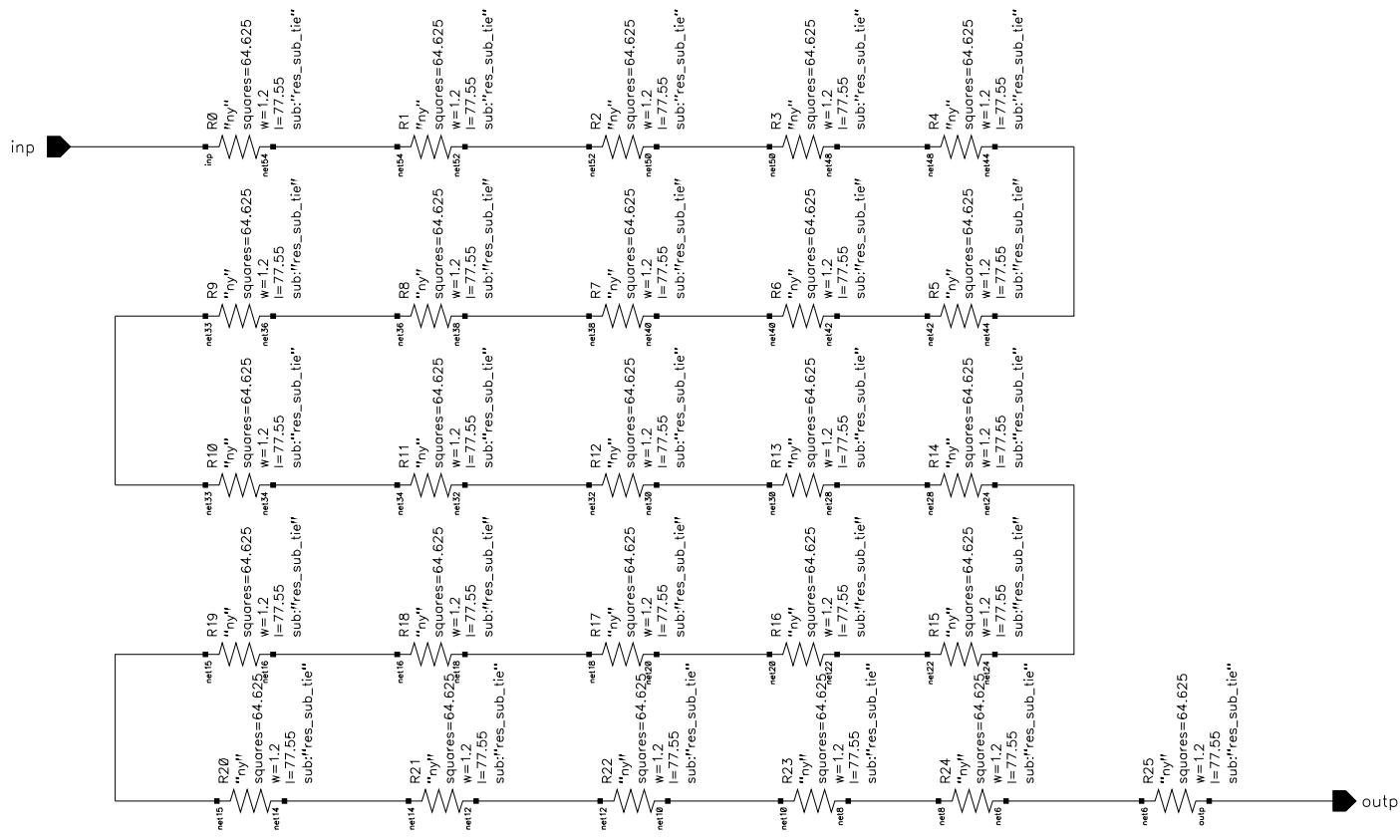
CAGE NO.

DWG NO.

REV A

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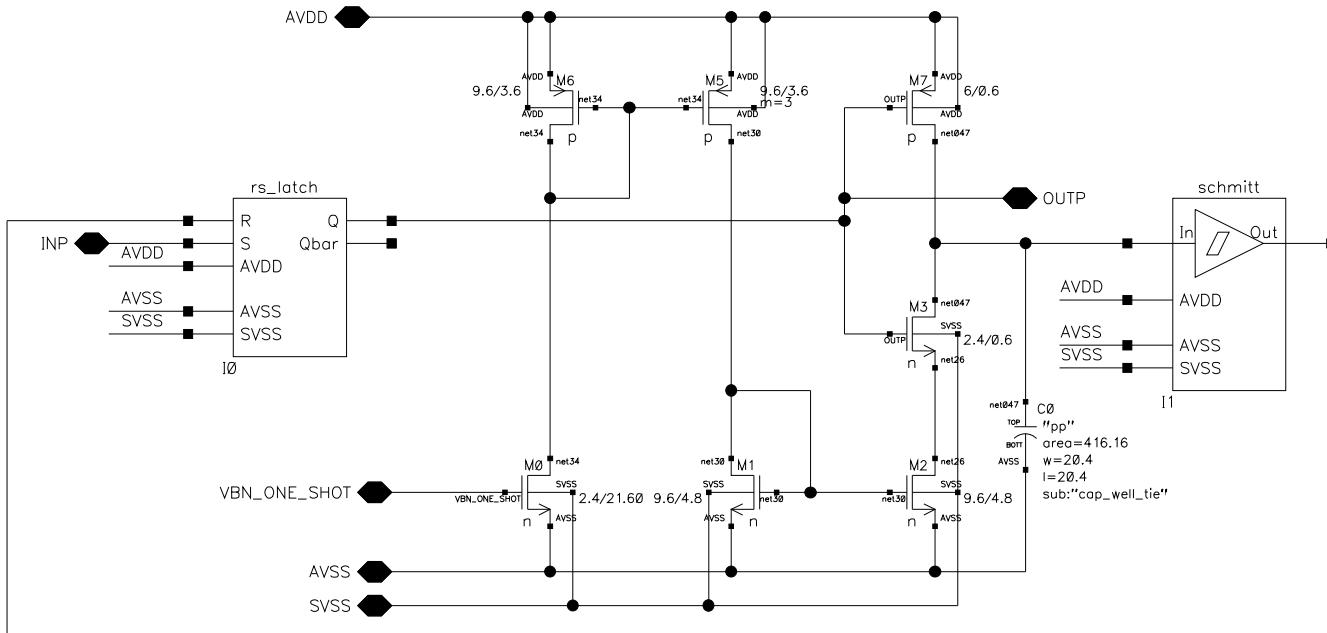
SHEET 1 OF 1



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Sep 6 14:10:53 2002	ny_res85k			
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CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
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## REVISIONS

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Aug 27 12:57:37 2007

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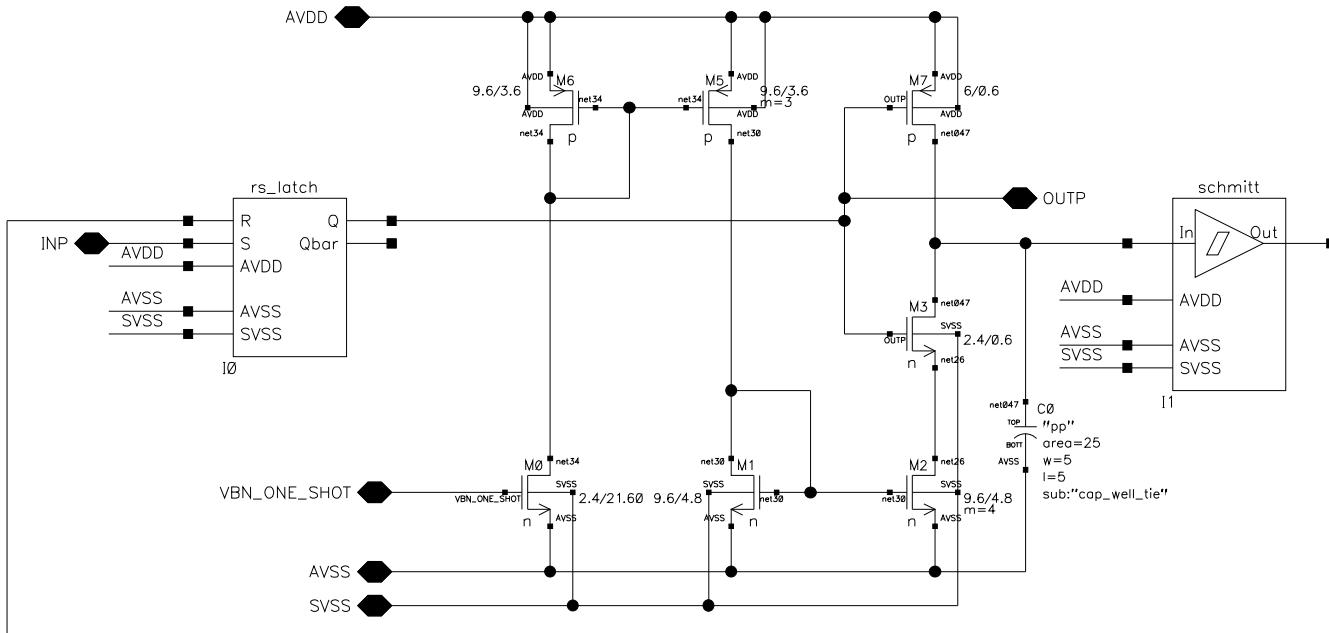
ISSUED

SIZE	CAGE NO.	DWG NO.	REV
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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Aug 27 12:57:37 2007

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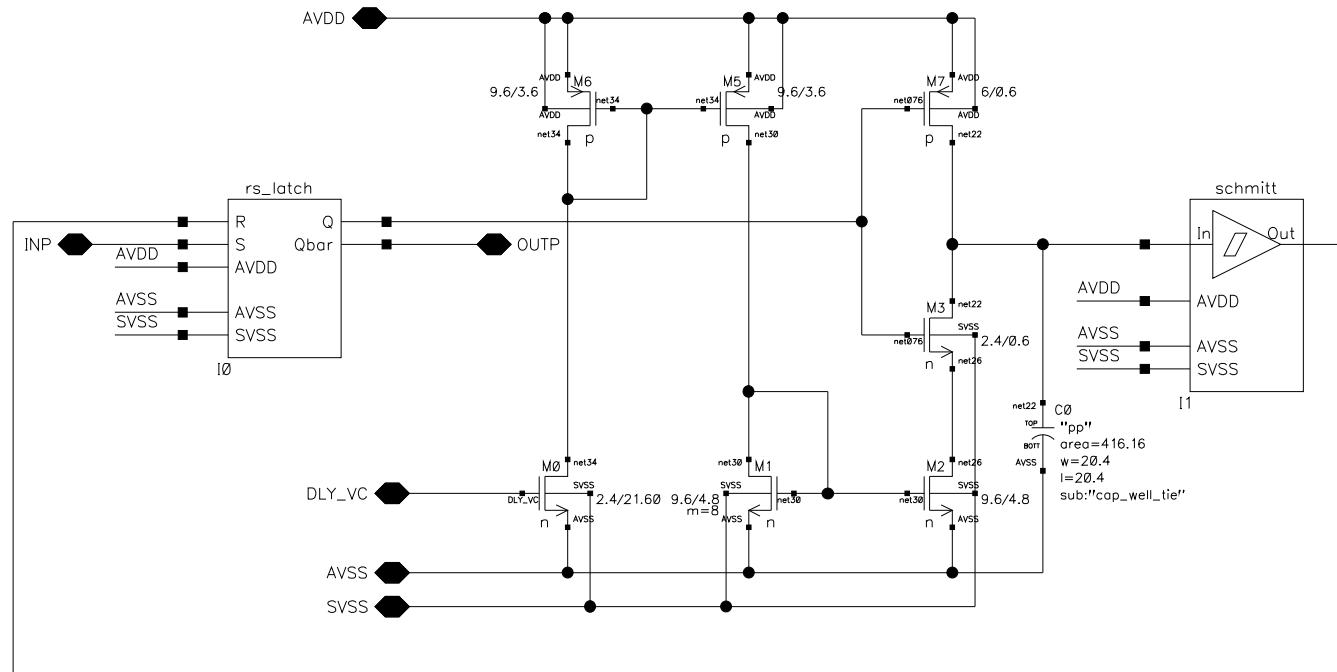
SIZE	CAGE NO.	DWG NO.	REV
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SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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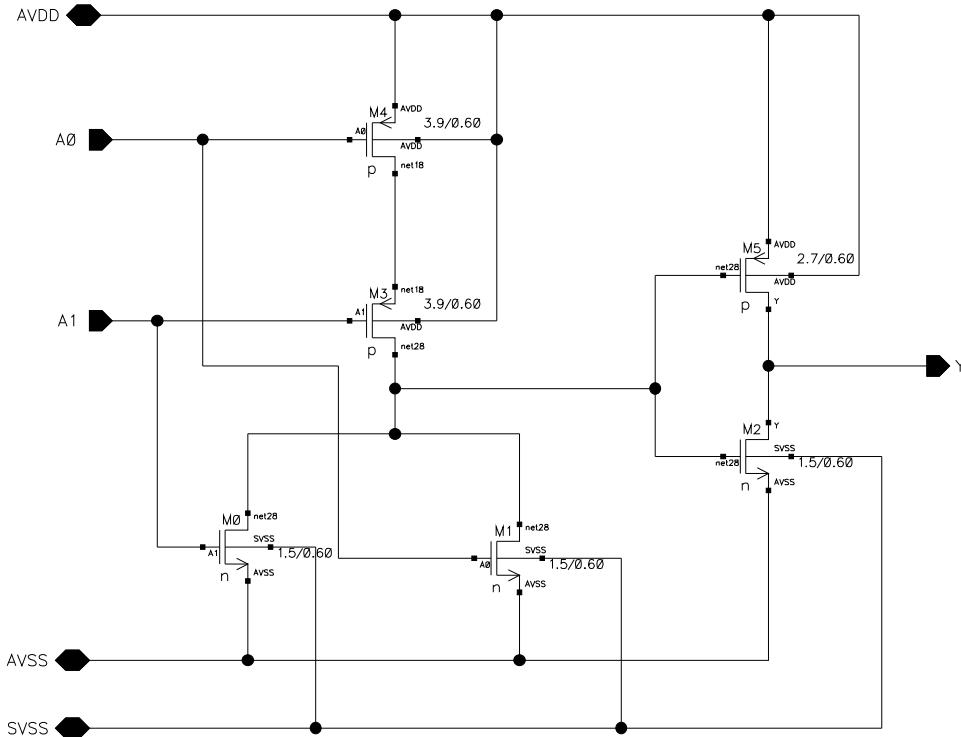
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SHEET 1 OF 1

CAGE NO. DWG NO. SH 1 REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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Jun 11 15:23:02 2007

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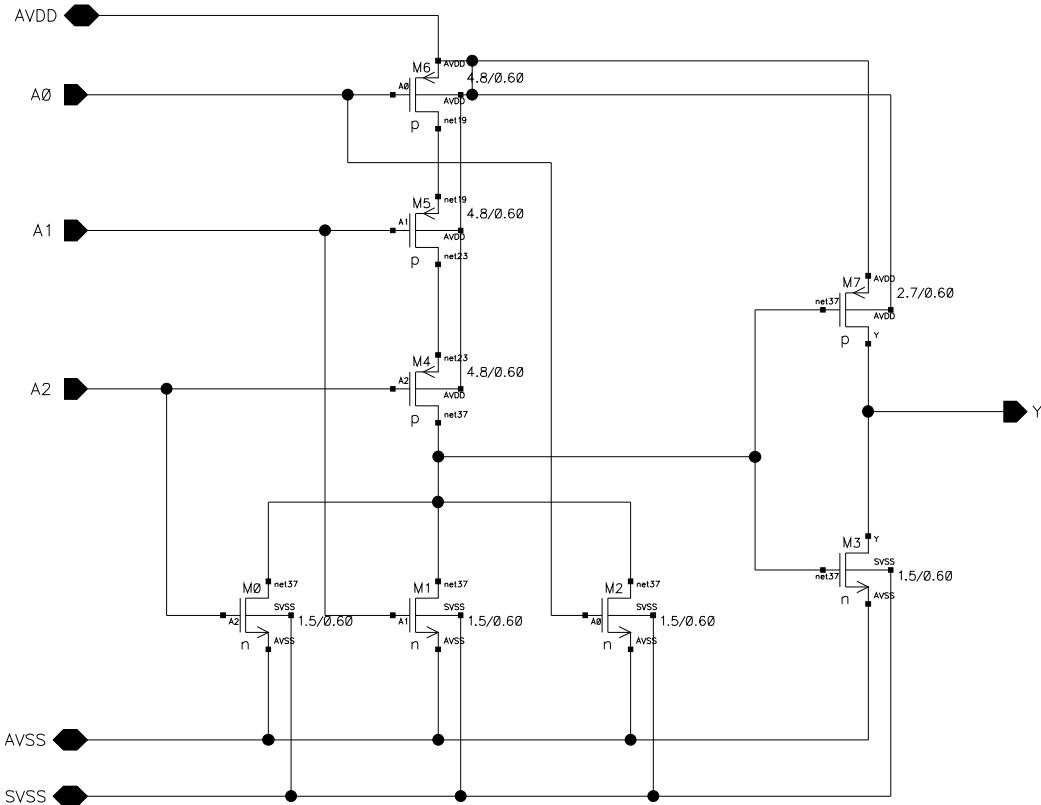
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CAGE NO. DWG NO. SH 1 REV

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ZONE	REV	DESCRIPTION	DATE	APPROVED



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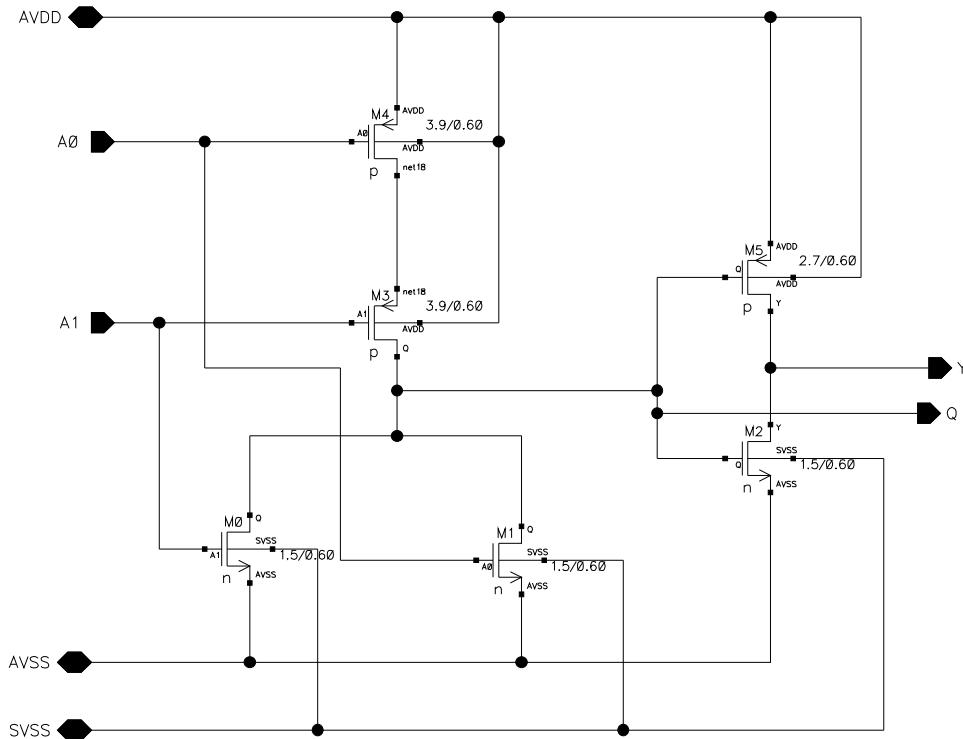
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CAGE NO. DWG NO. SH 1 REV

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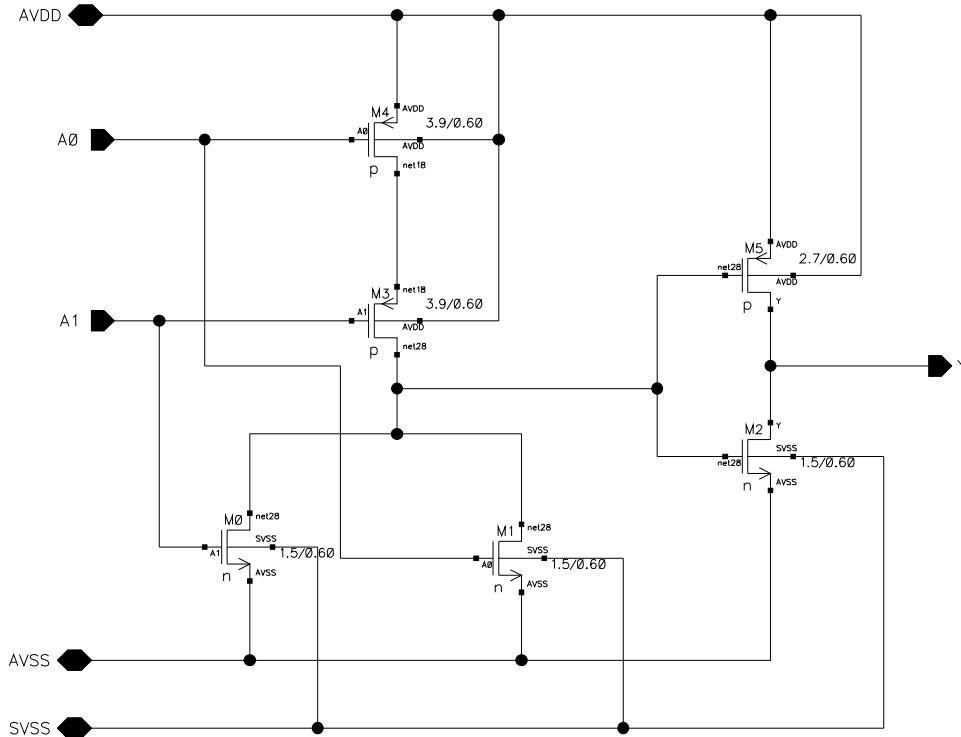
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SIZE	CAGE NO.	DWG NO.	REV
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SHEET 1 OF 1			

CAGE NO.	DWG NO.	SH 1	REV
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## REVISIONS

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Jun 5 12:02:59 2007

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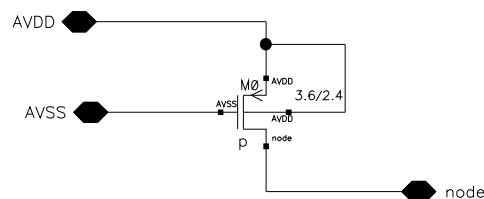
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Aug 3 14:33:16 2007

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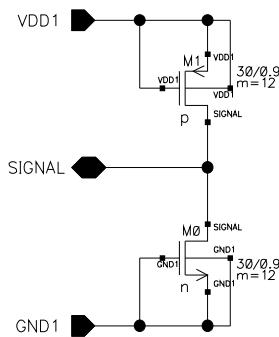
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CAGE NO. DWG NO. SH 1 REV

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ZONE	REV	DESCRIPTION	DATE	APPROVED



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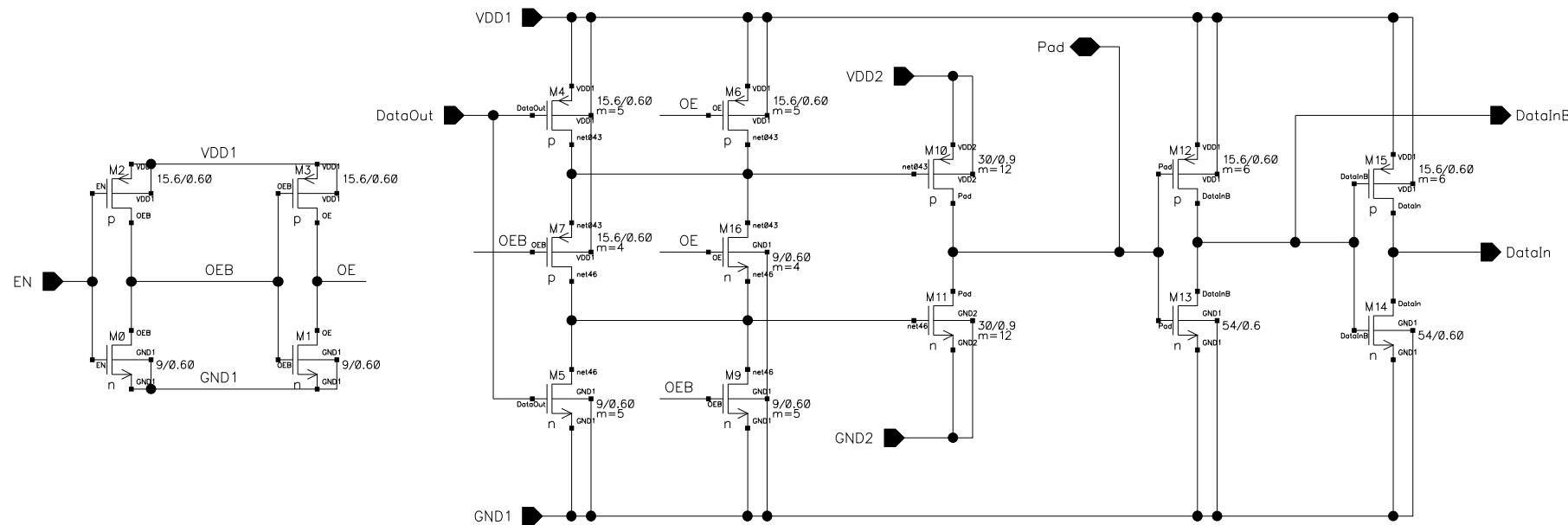
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## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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## REVISIONS

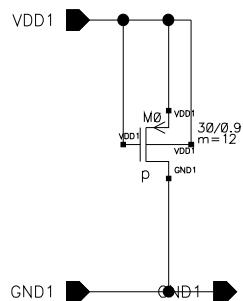
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## REVISIONS

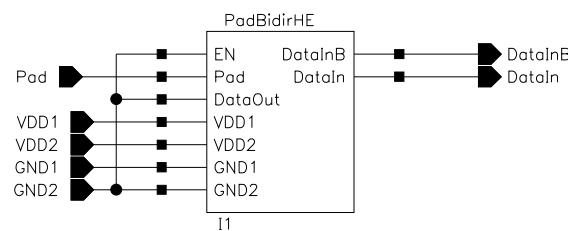
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Jul 9 16:11:27 2003

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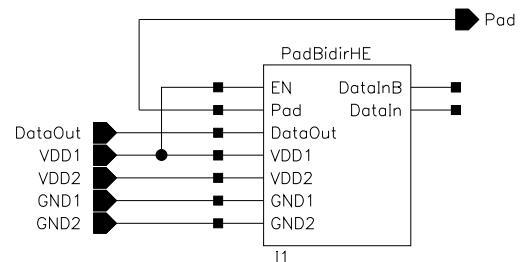
SHEET

1 OF 1

CAGE NO. DWG NO. SH 1 REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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			SHEET 1 OF 1

CAGE NO.

DWG NO.

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## REVISIONS

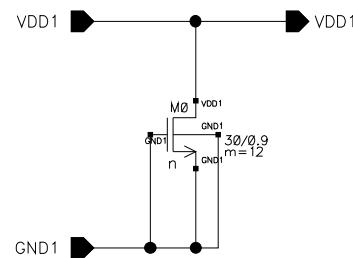
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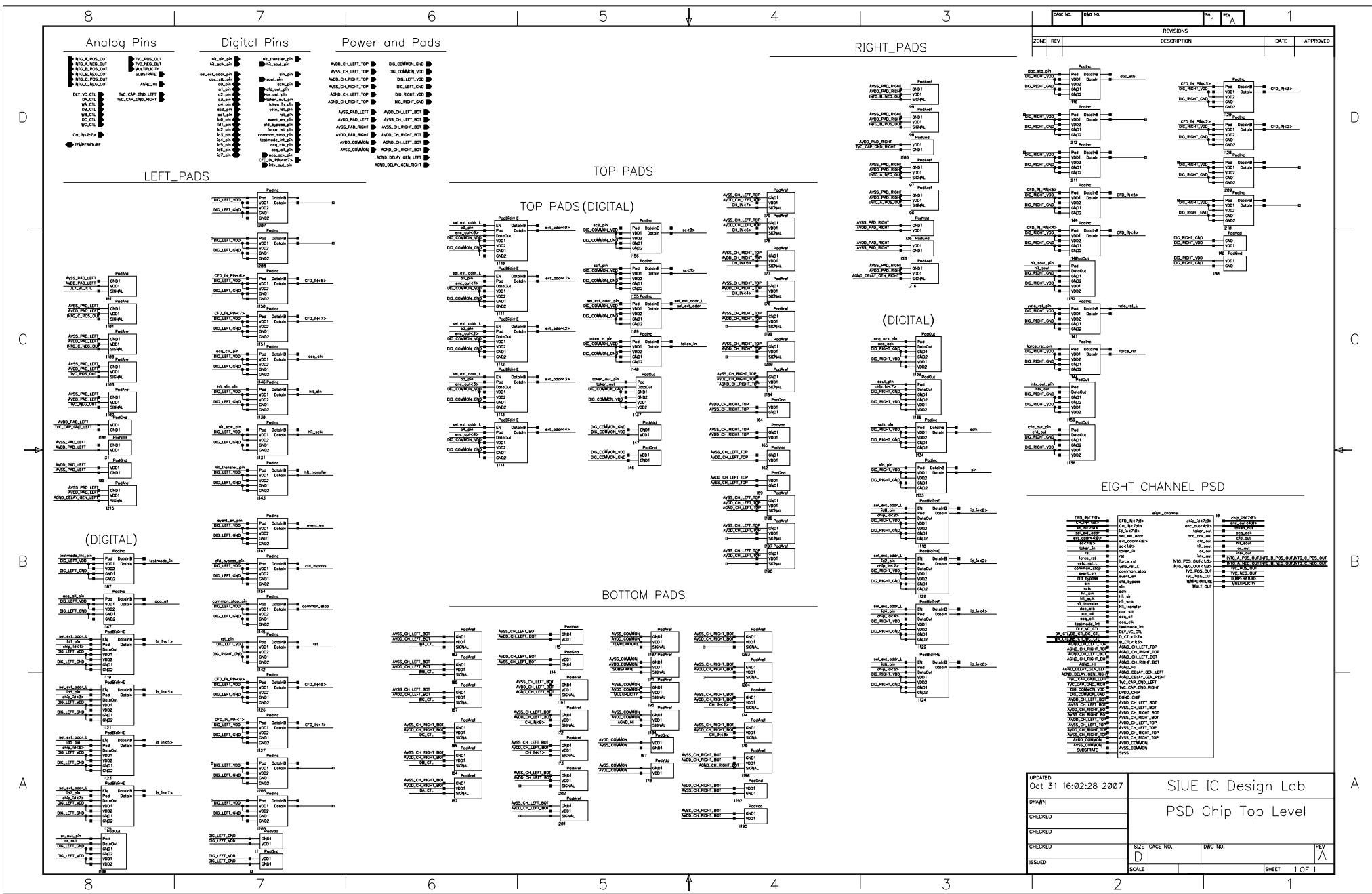
CAGE NO.

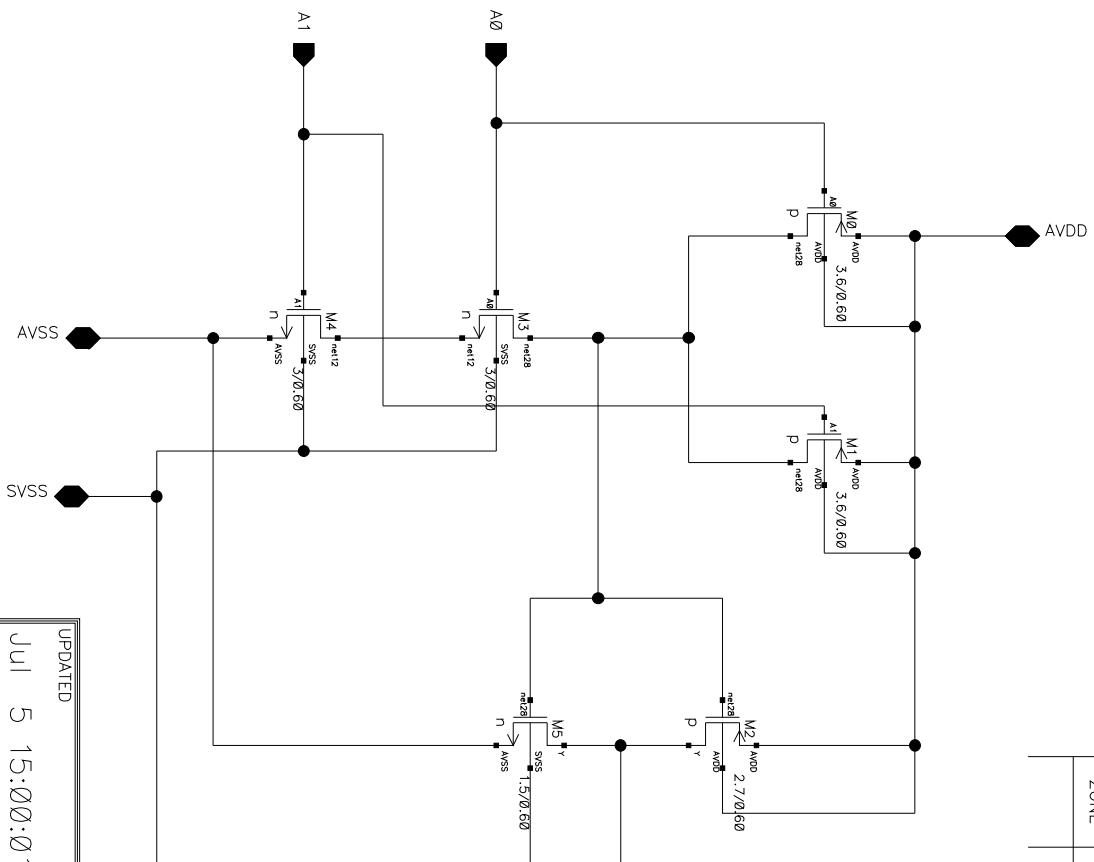
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SHEET 1 OF 1



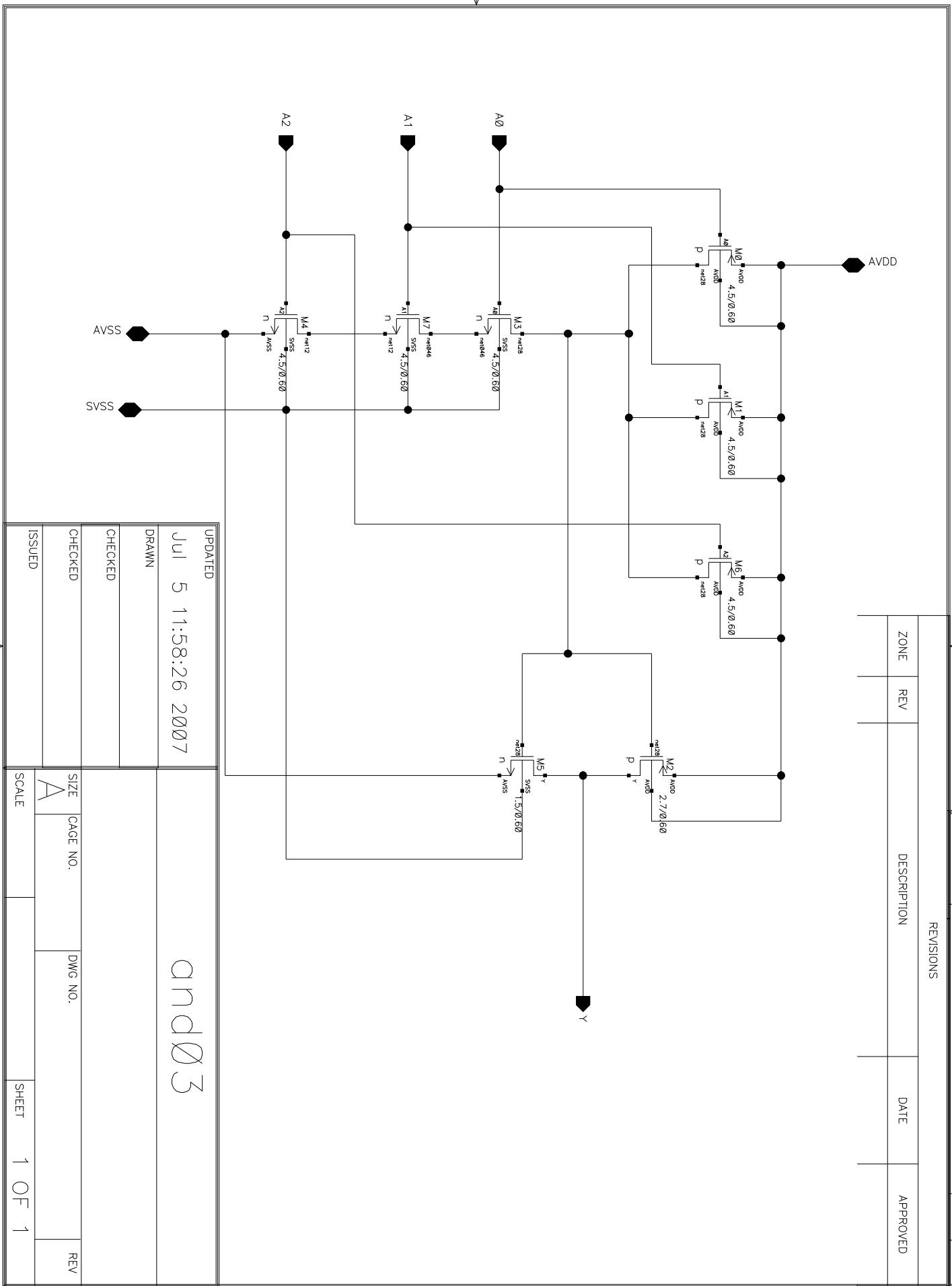


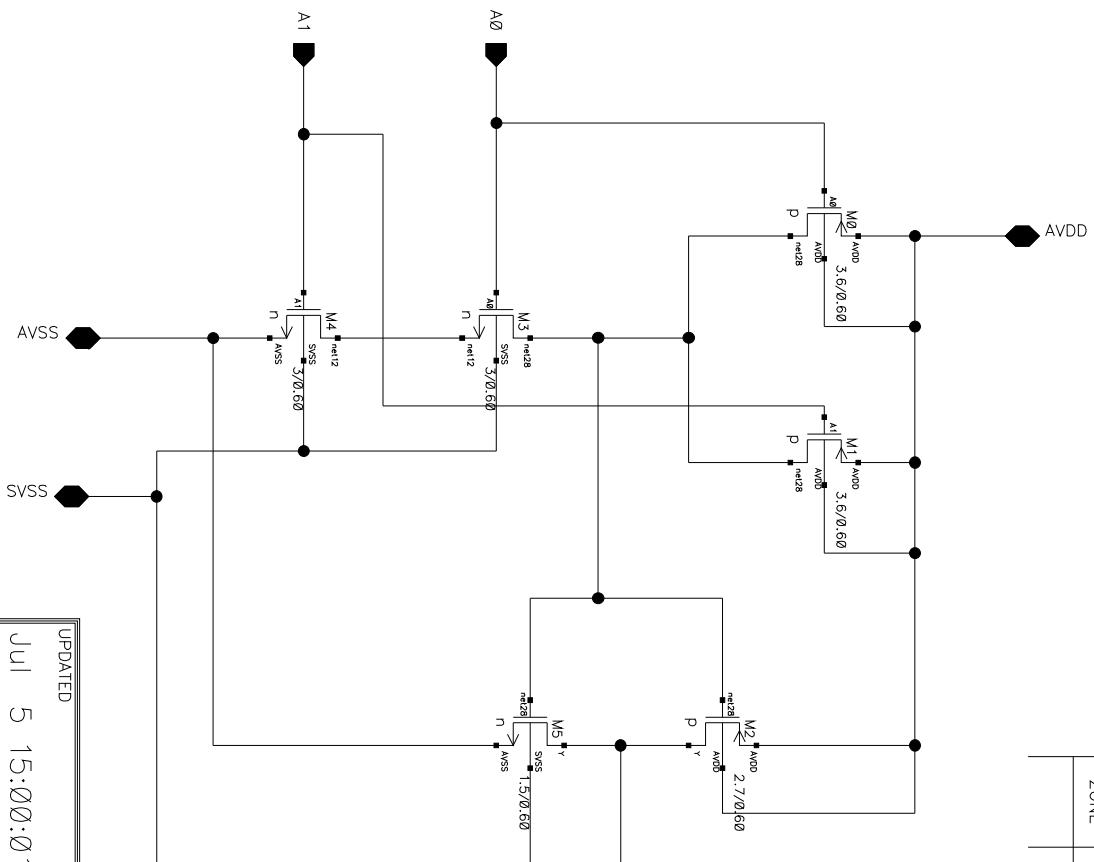
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ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

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ISSUED	<div style="display: flex; align-items: center; justify-content: space-between;"> <div style="flex: 1;"> <div style="display: flex; align-items: center;"> <span style="font-size: 2em; margin-right: 10px;">A</span> <span style="border: 1px solid black; padding: 2px 10px; margin-right: 10px;">SIZE</span> <span style="border: 1px solid black; padding: 2px 10px; margin-right: 10px;">CAGE NO.</span> <span style="border: 1px solid black; padding: 2px 10px; margin-right: 10px;">DWG NO.</span> <span style="border: 1px solid black; padding: 2px 10px; margin-right: 10px;">REV</span> </div> <div style="flex: 1; text-align: right;"> <span style="border: 1px solid black; padding: 2px 10px; margin-right: 10px;">SCALE</span> <span style="border: 1px solid black; padding: 2px 10px; margin-right: 10px;">SHEET</span> <span style="border: 1px solid black; padding: 2px 10px; margin-right: 10px;">1</span> <span style="border: 1px solid black; padding: 2px 10px; margin-right: 10px;">OF</span> <span style="border: 1px solid black; padding: 2px 10px; margin-right: 10px;">1</span> </div> </div> </div>		

CAGE NO.	DWG NO.	REV	SH 1	REV
DESCRIPTION		DATE	APPROVED	
ZONE	REV			



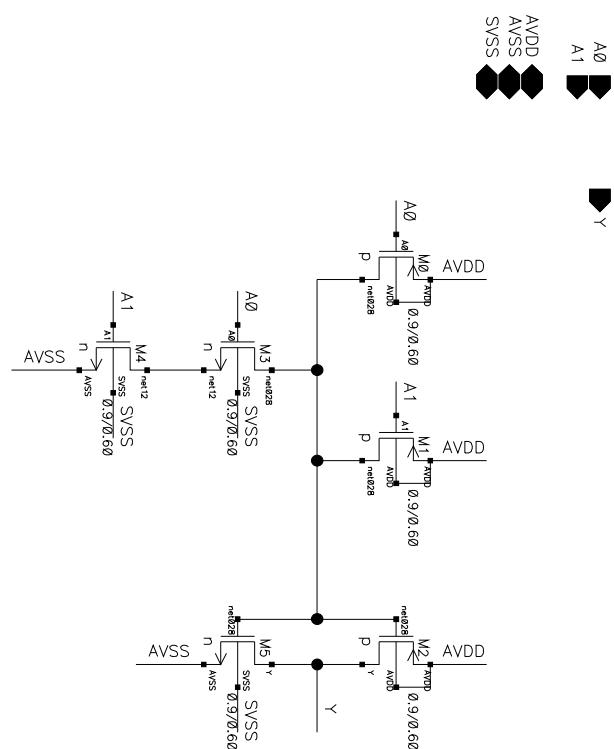


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ZONE	REV	DESCRIPTION	DATE	APPROVED

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Three small circles are arranged vertically. The top and bottom circles have a horizontal line extending to the right from their right side, while the middle circle is a simple outline.

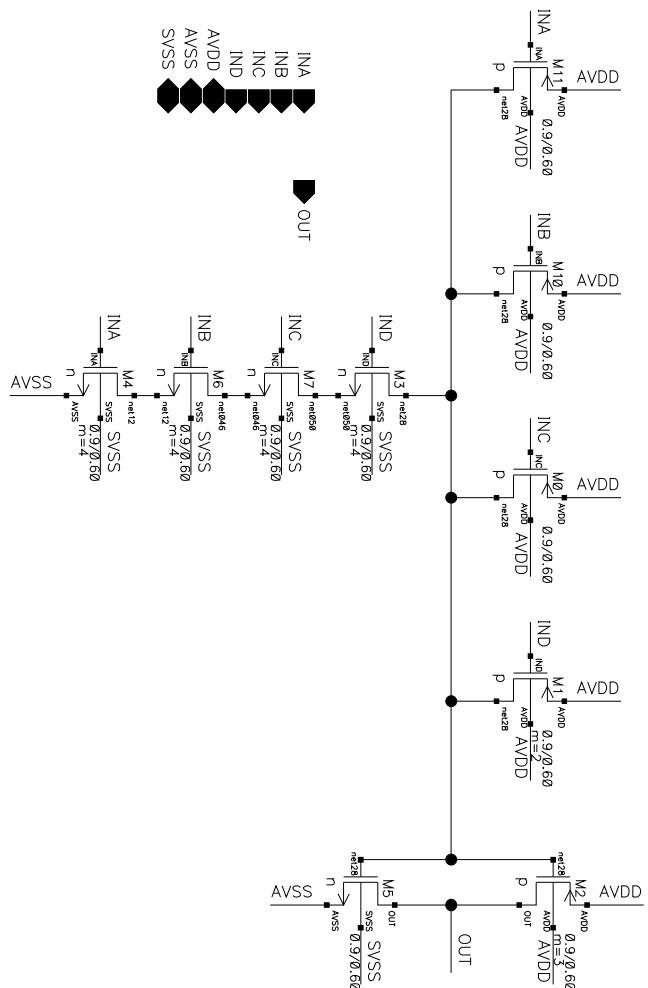
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	SIZE A SCALE	CAGE NO. DWG NO.	REV SHEET 1 OF 1



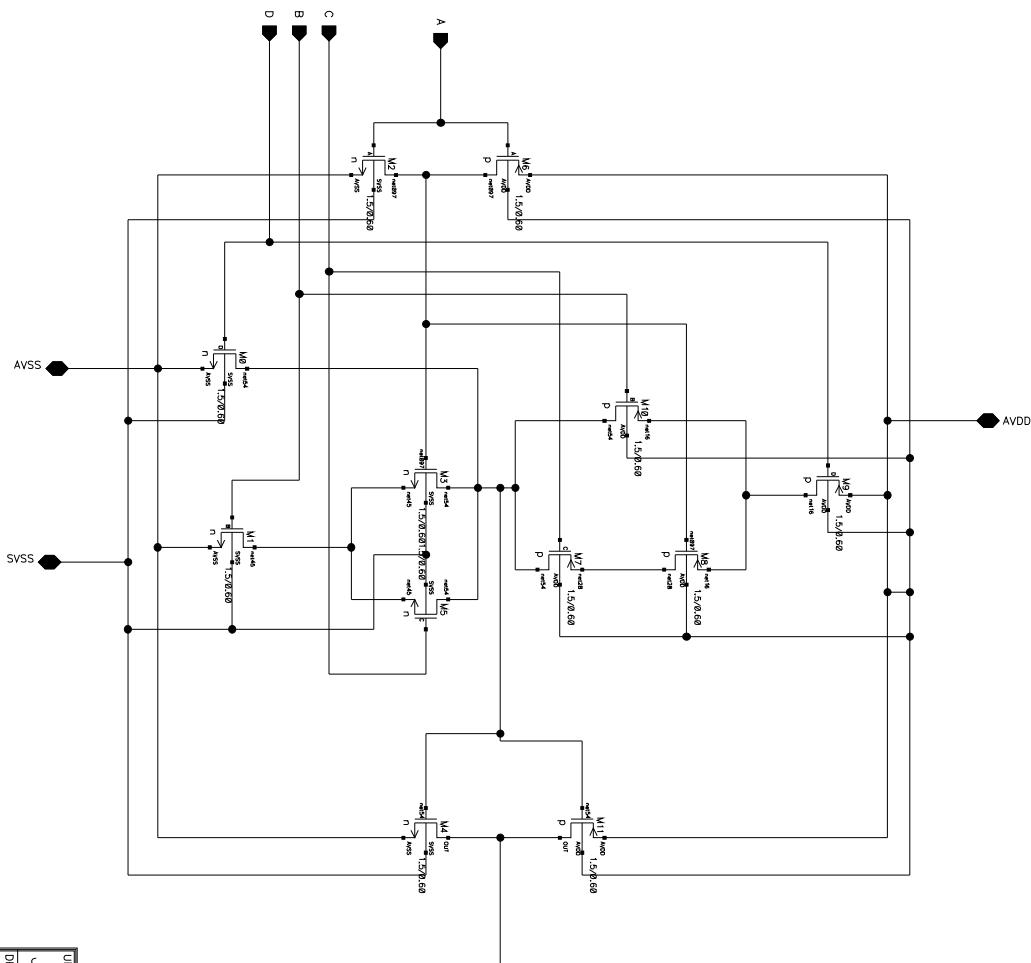
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ZONE	REV	DESCRIPTION	DATE
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			SH 1 REV

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Aug 8 14:14:18 2007	and		
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	SIZE A	CAGE NO.	DWG NO.
	SCALE		
			SHEET 1 OF 1 REV

CAGE NO.	DWG NO.	REV	SH 1	REV
DESCRIPTION		DATE	APPROVED	



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Feb 20 16:35:34 2007			
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CAGE NO. / DWG NO.		REV		DESCRIPTION	DATE	APPROVED
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	SHEET 1 OF 1	

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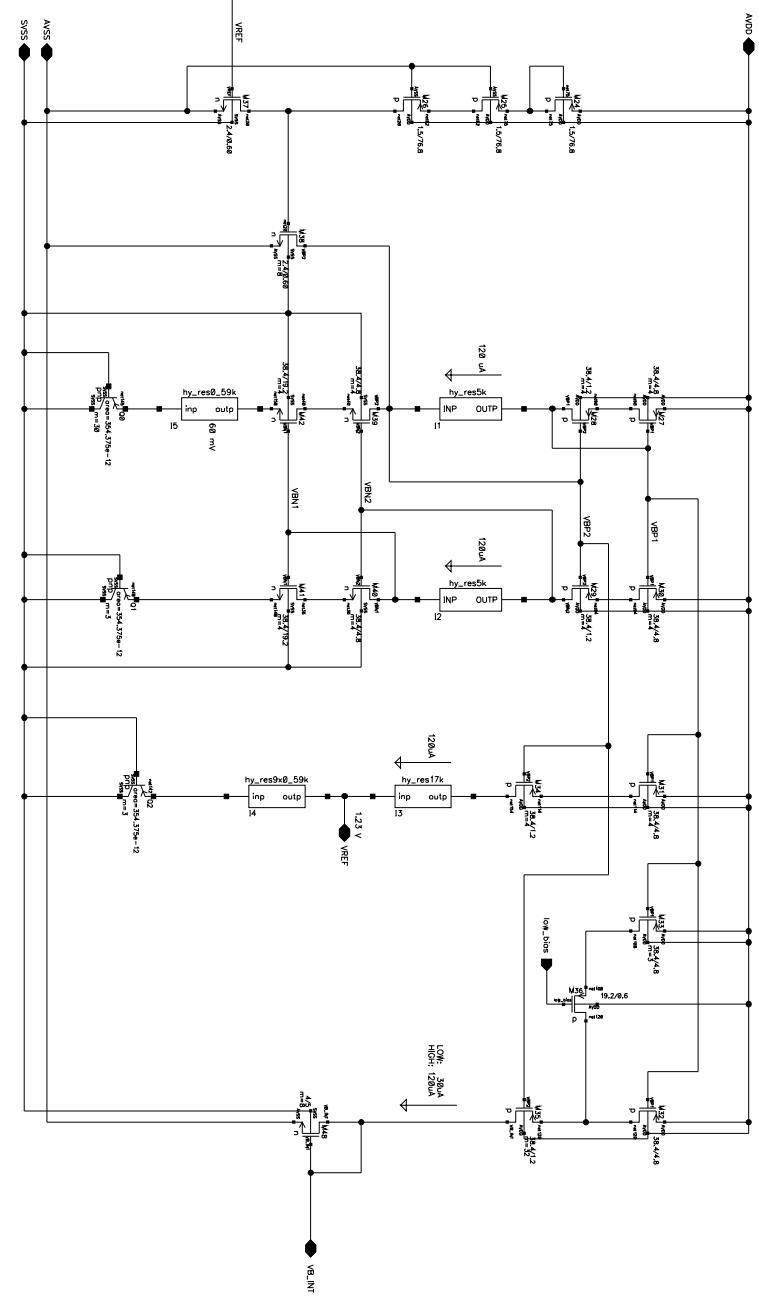
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REVISIONS			
ZONE	REV	DESCRIPTION	DATE
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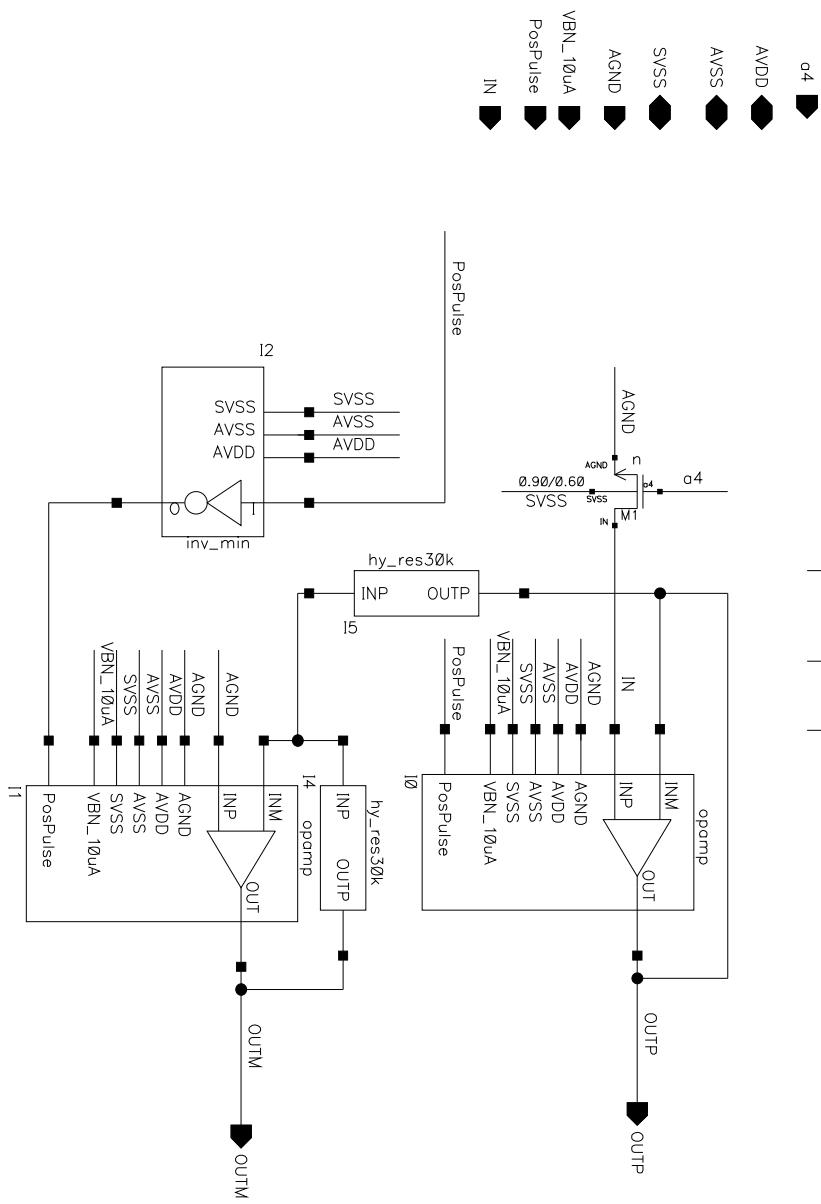
UPDATED  
Oct 30 14:23:38 2000

89

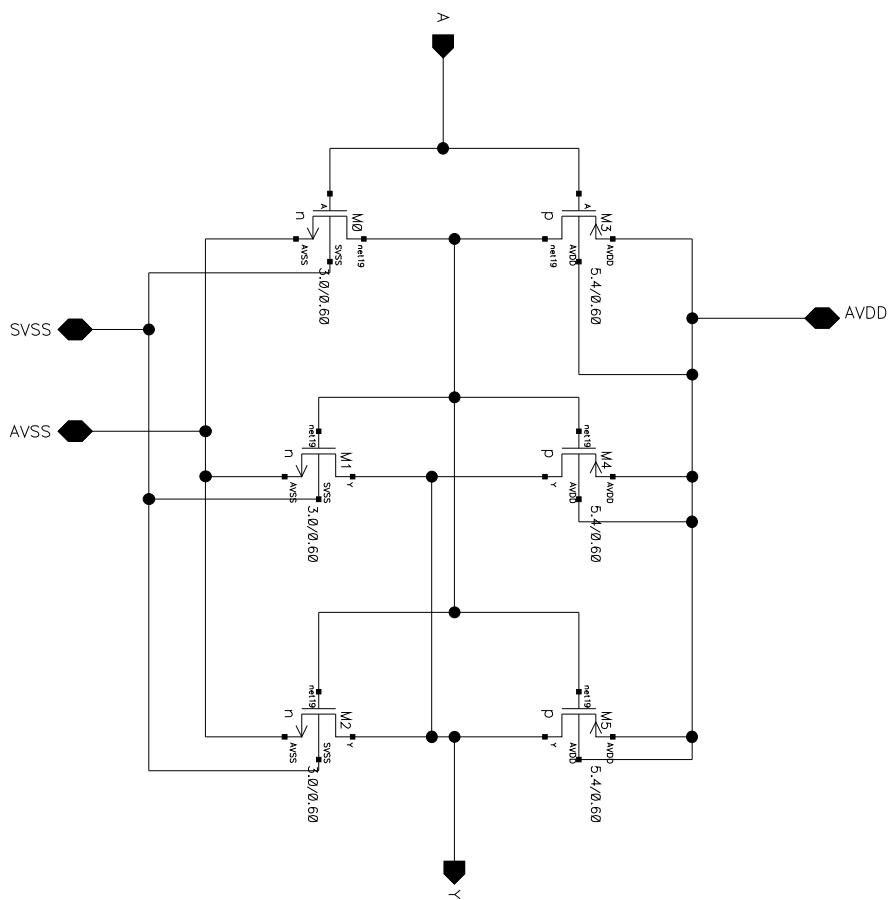
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Oct 30 14:23:38 2007	bias		
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CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS			
ZONE	REV	DESCRIPTION	DATE
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Jun 15 14:49:33 2007

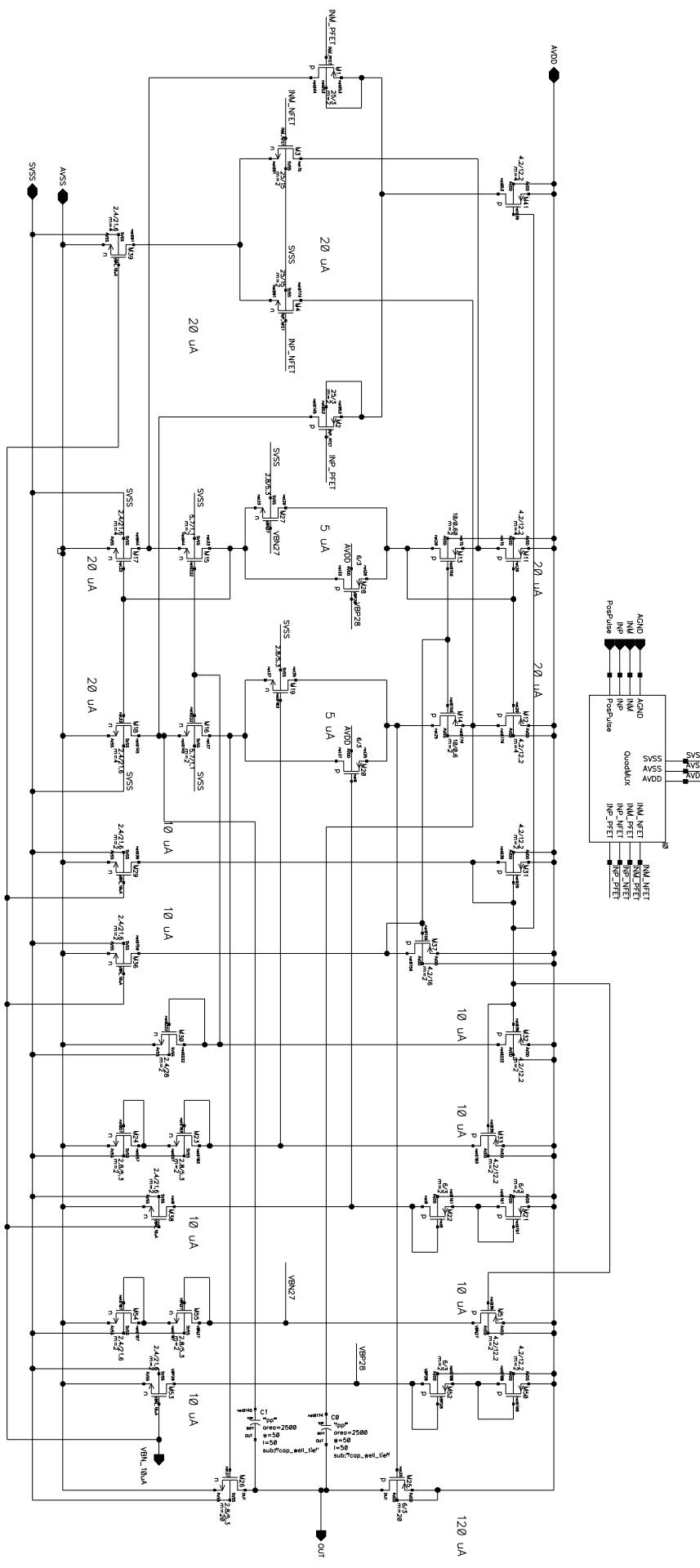
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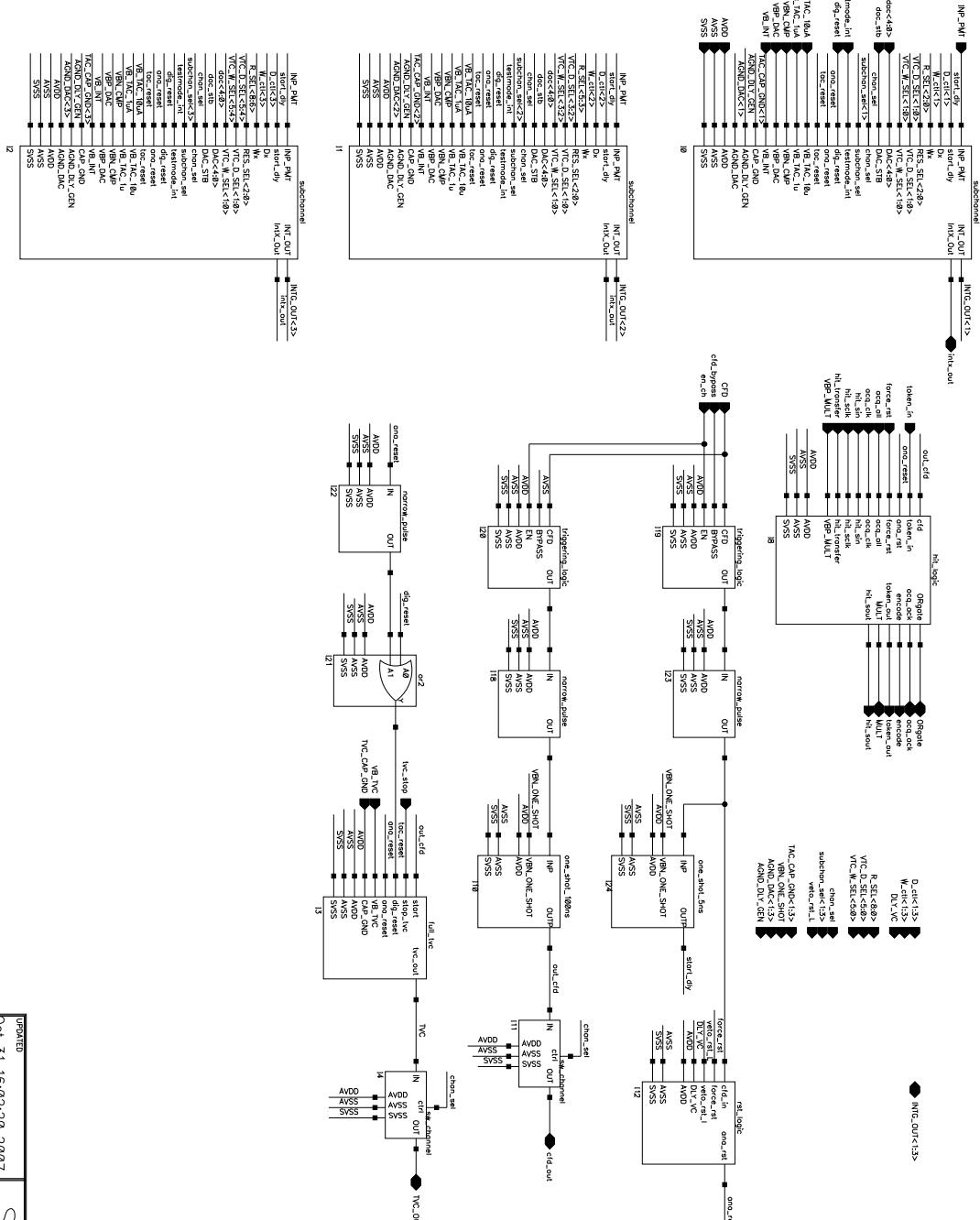
DRAWN	SIZE	CAGE NO.	DWG NO.	REV
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ISSUED	SCALE			
			SHEET 1 OF 1	

ZONE	REV	DESCRIPTION	DATE	APPROVED

CAGE NO. DWG NO. SH 1 REV

REVISIONS



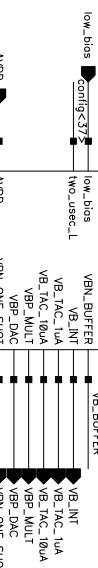


REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED

CAGE NO.	DWG NO.	REV	REVISIONS	DATE	APPROVED
		1	REV A		

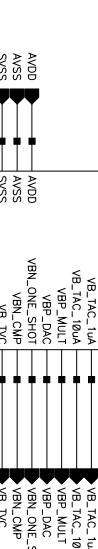
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110

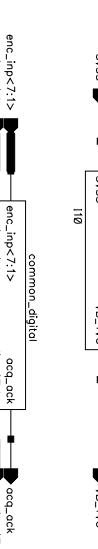
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111

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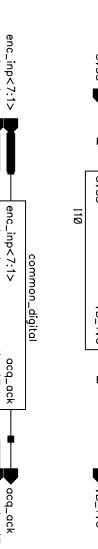
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112

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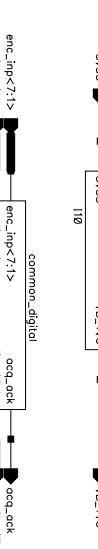
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113

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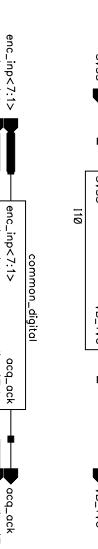
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114

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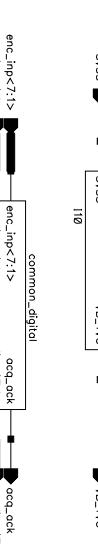
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115

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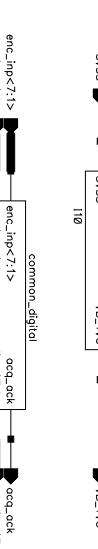
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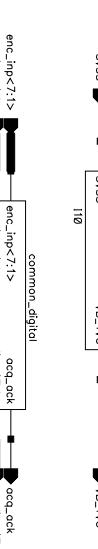
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117

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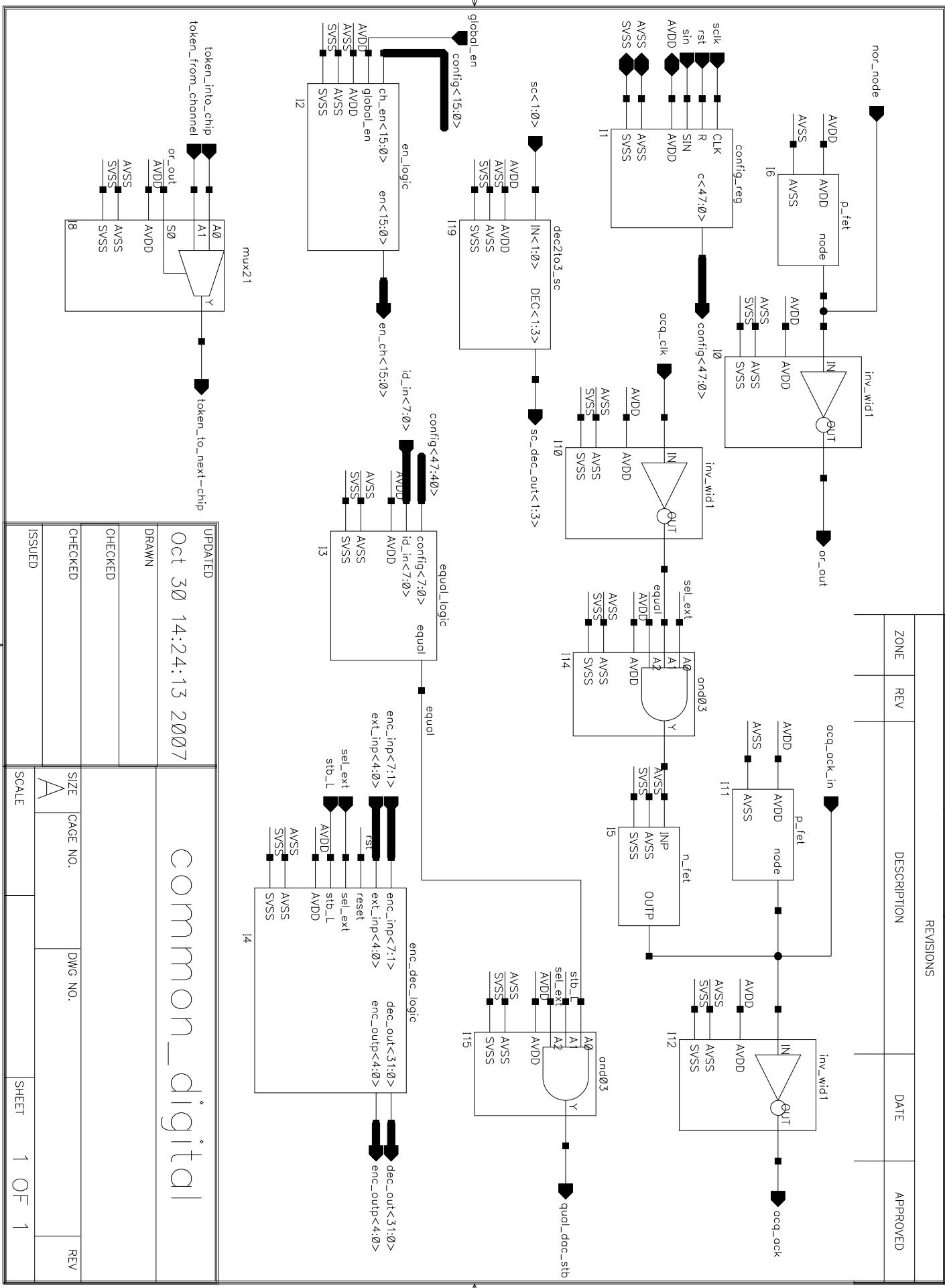
118

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Oct 30 14:24:01 2007  
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ISSUED  
SIUE IC Design Lab  
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SCALE  
SIZE CAGE NO. DWG NO.  
B

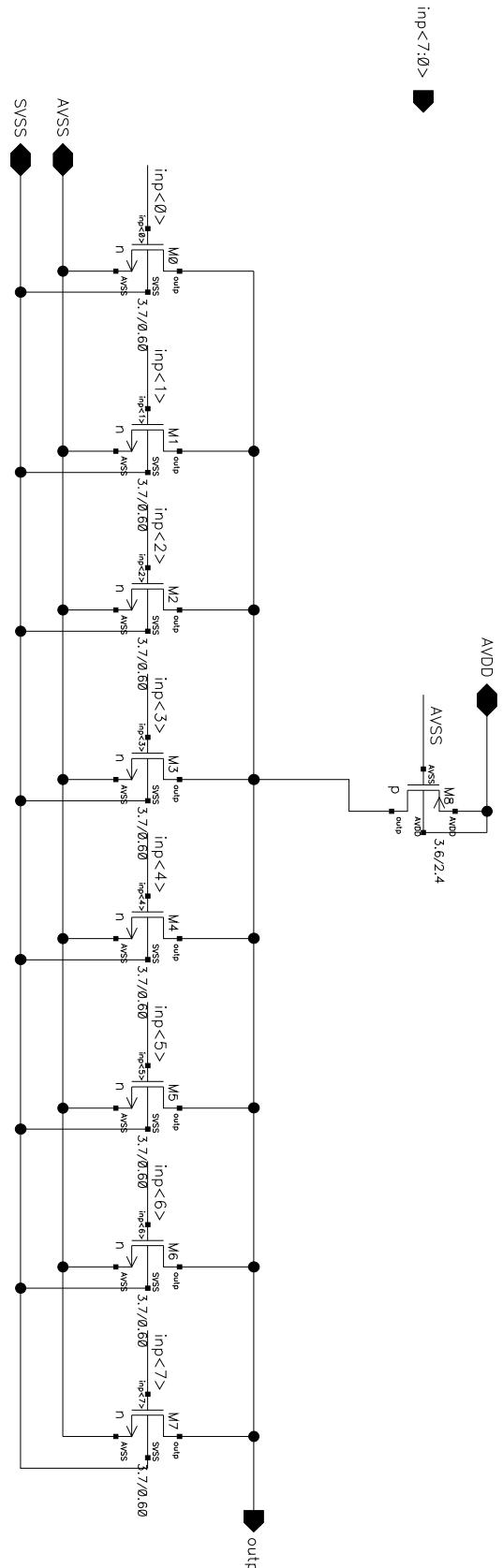
REV A

SHEET 1 OF 1



CAGE NO.	DWG NO.	SH	1	REV

CAGE NO.	DWG NO.	SH 1	REV
DESCRIPTION		DATE	APPROVED
REV			



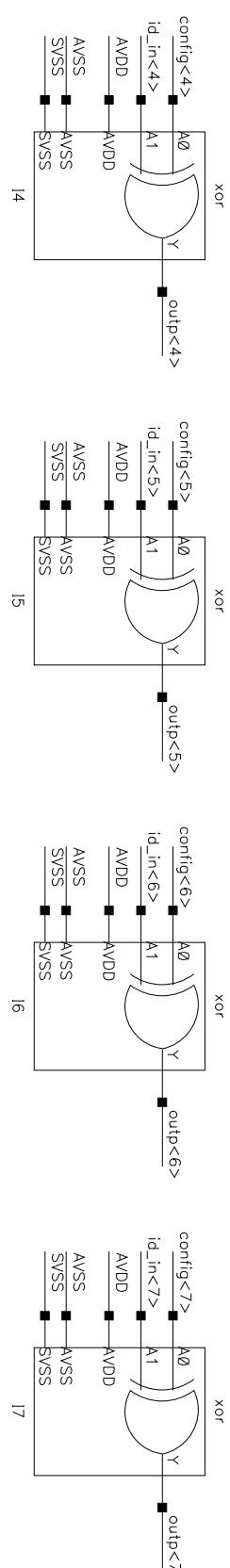
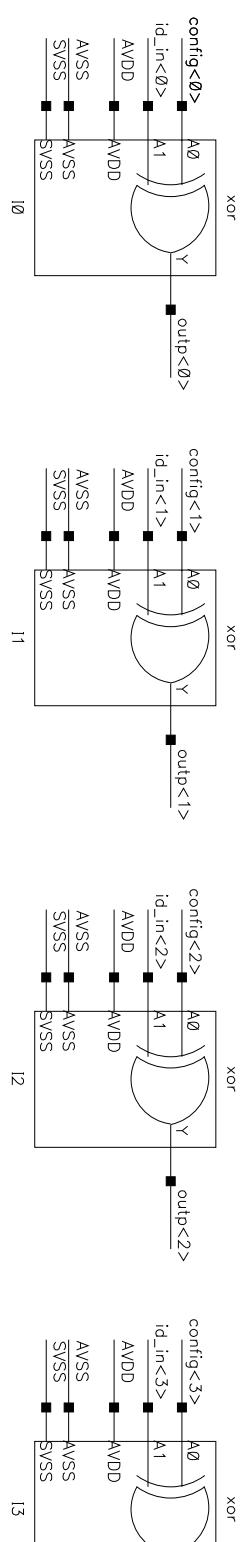
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JUL 6 10:56:07 2007			
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SIZE	CAGE NO.	DWG NO.	REV
SCALE			
		SHEET 1 OF 1	



CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



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AVSS  
SVSSUPDATED  
JUL 9 14:04:08 2007

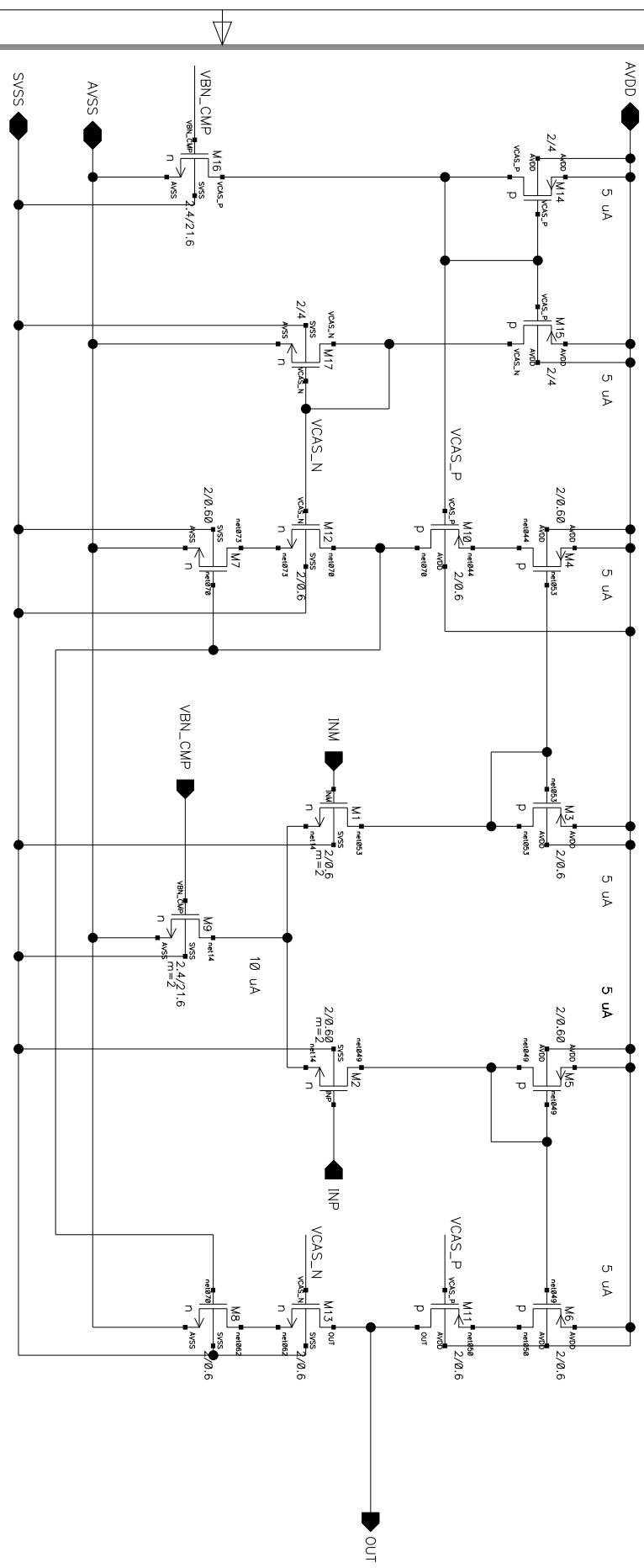
## comparator

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ISSUED

SIZE	CAGE NO.	DWG NO.	SHEET	1 OF 1
SCALE				

REV

CAGE NO.		DWG NO.		SH 1	REV		
ZONE	REV	DESCRIPTION					
REVISIONS							



UPDATED

Jul 9 10:40:35 2007

# SiUE IC Design Lab

## Comparator

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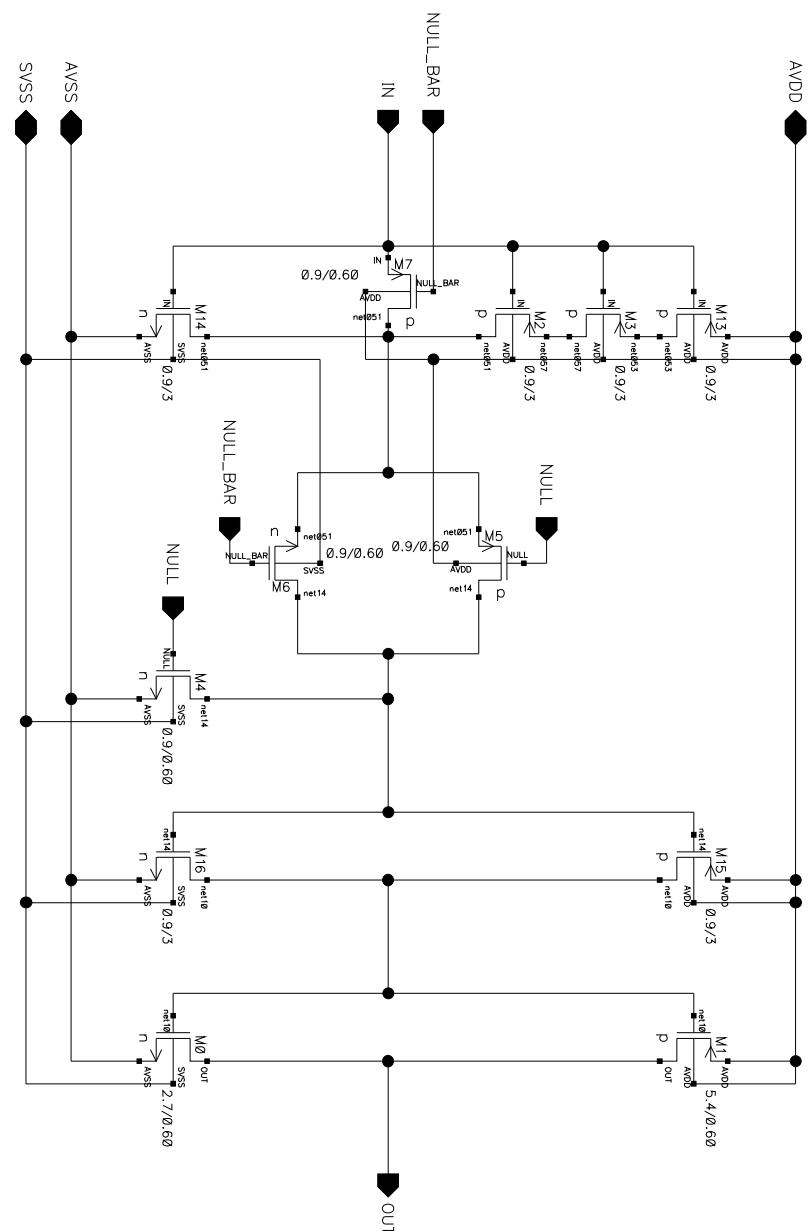
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SCALE

REV

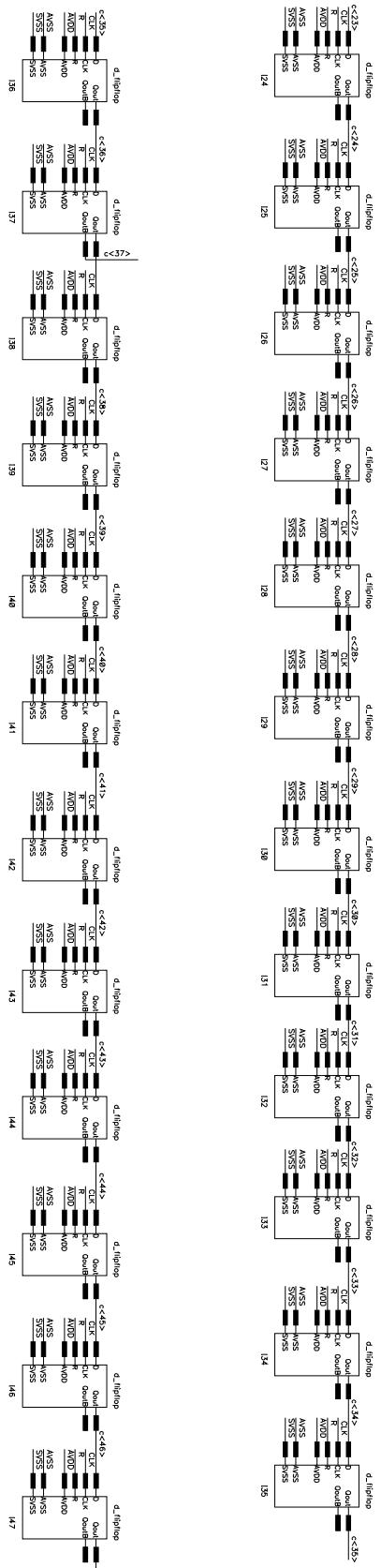
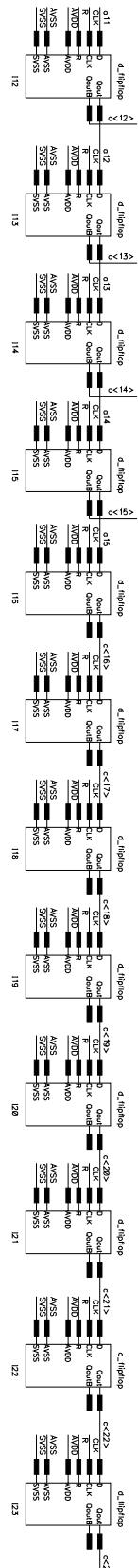
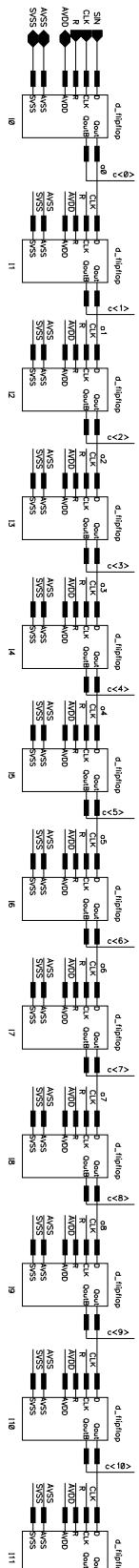
SHEET 1 OF 1

ZONE	REV	DESCRIPTION	DATE	APPROVED
			SH 1	REV A

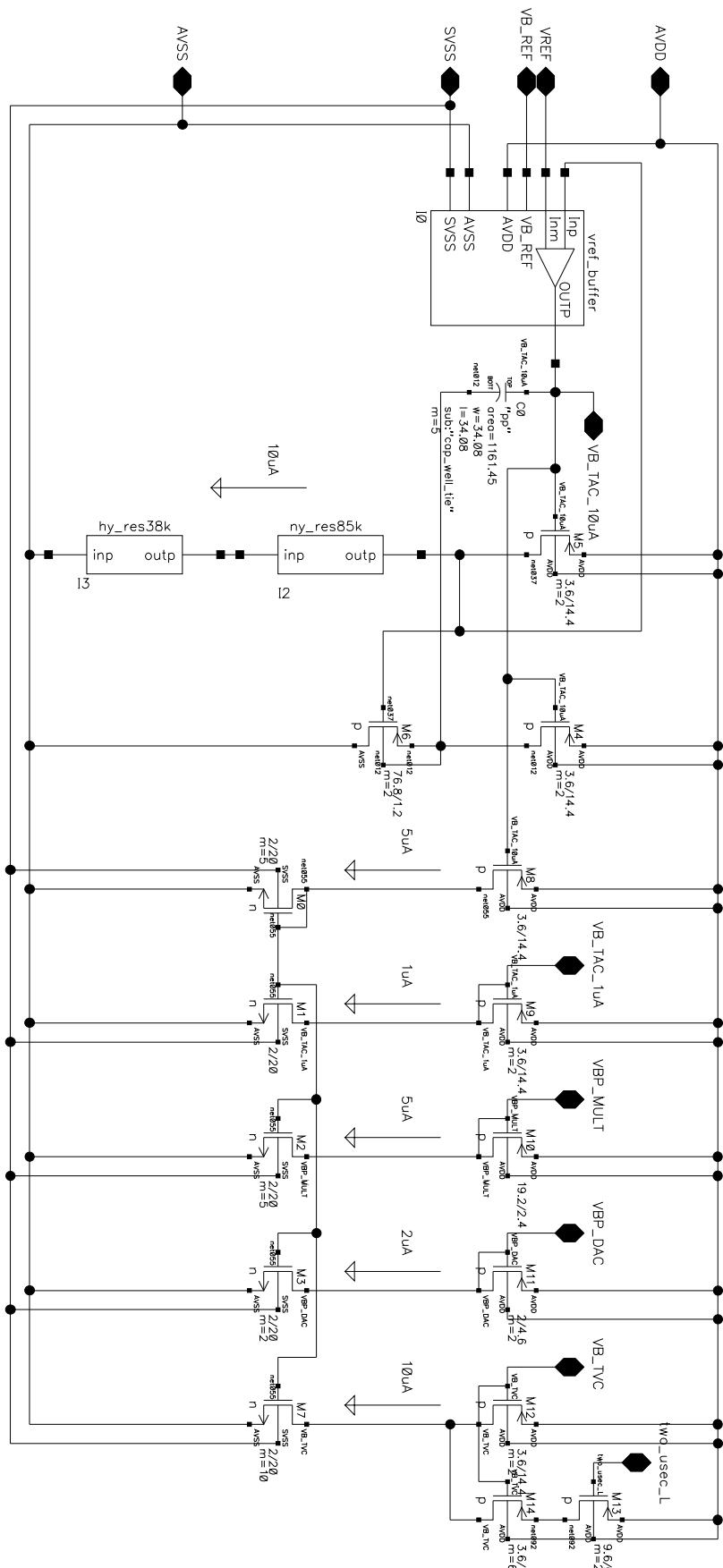


UPDATED Jul 10 13:06:58 2007	SIUE IC Design Lab		
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SIZE A	CAGE NO.	DWG NO.	SHEET 1 OF 1
SCALE			REV A

ZONE	REV	DESCRIPTION	DATE	APPROVED
REVISONS				



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	REV	REV	REV



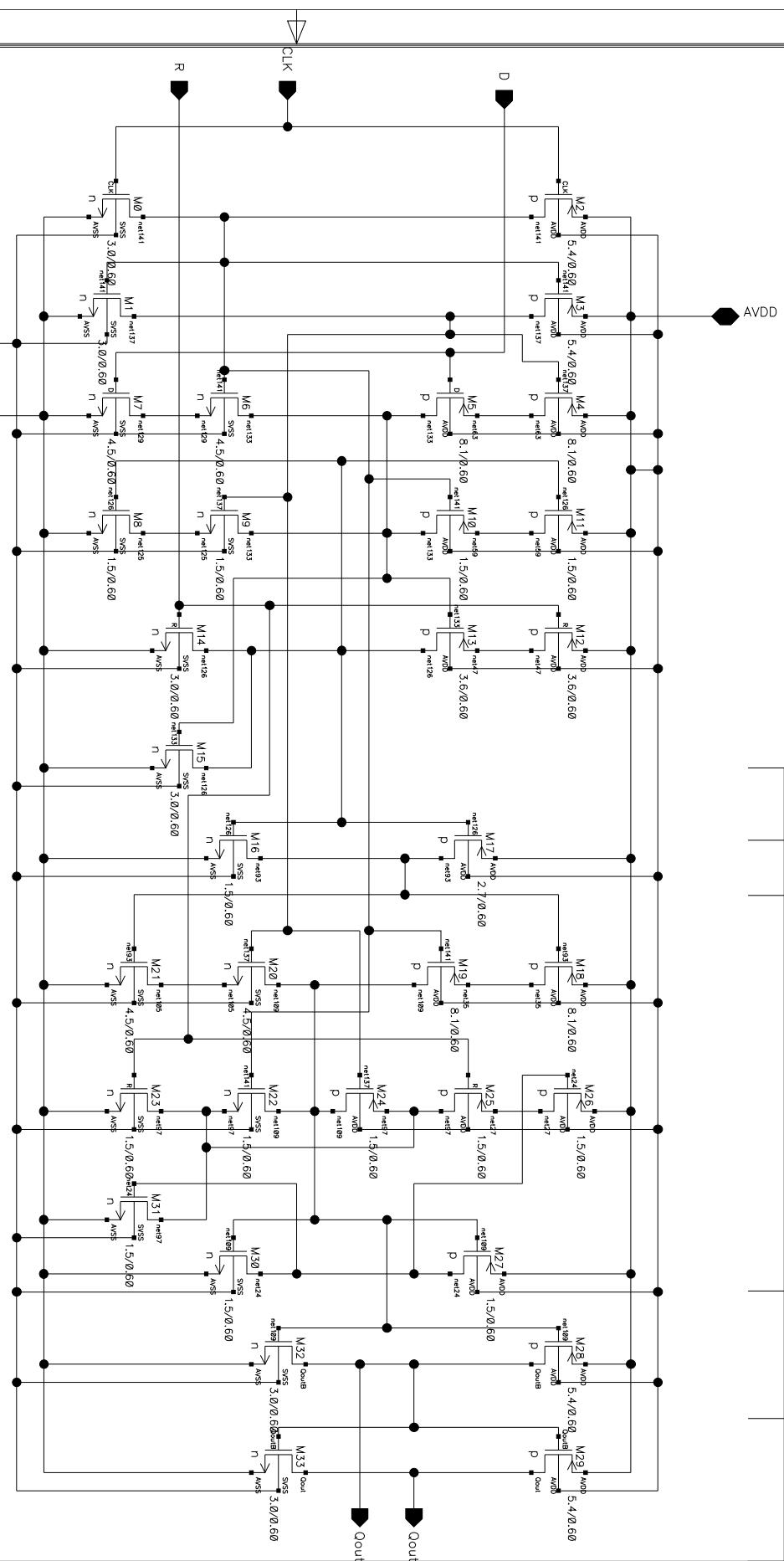
REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV A

UPDAIED

Oct 30 14:23:53 2007  
DRAWN  
SIUE IC Design Lab  
Constant Current

ISSUED	SCALE	SIZE	CAGE NO.	DWG NO.
			SHEET	1 OF 1
				REV A

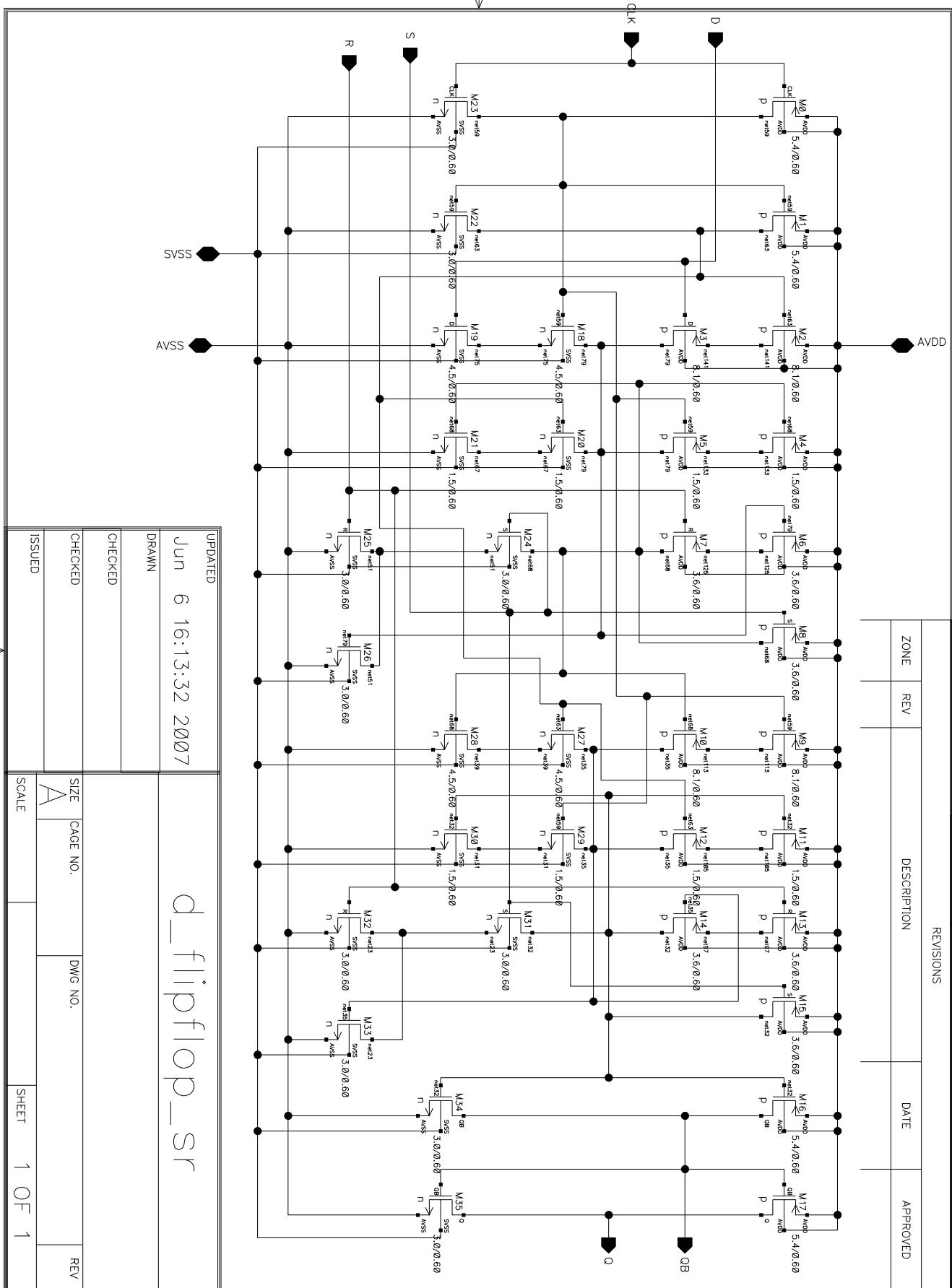
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REVISIONS				



UPDATED  
JUL 10 12:52:42 2007

C — f | P f | O P

DRAWN	SIZE	CAGE NO.	DWG NO.	SHEET	1 OF 1
CHECKED					
ISSUED	SCALE				
			REV		



CAGE NO.	DWG NO.	SH	REV
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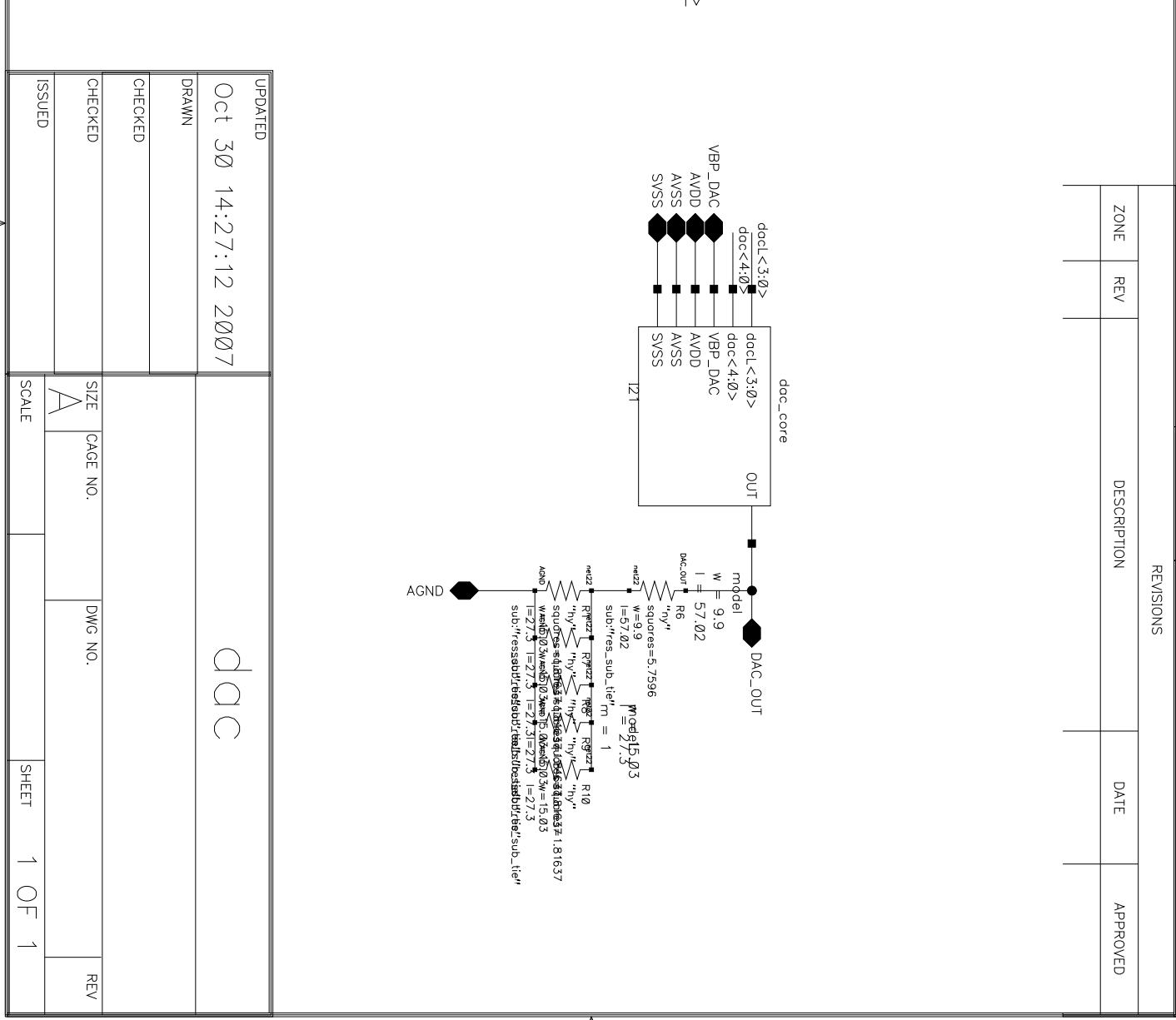
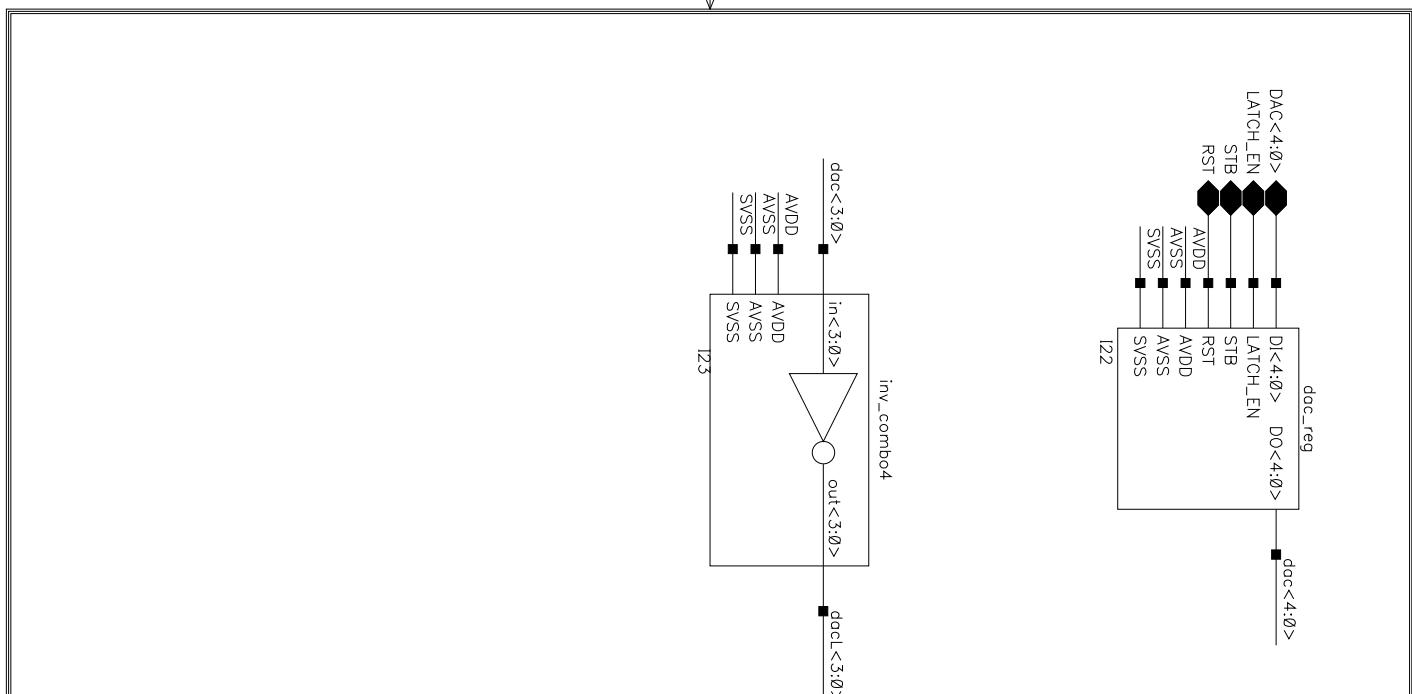
ZONE	REV	DESCRIPTION	DATE	APPROVED
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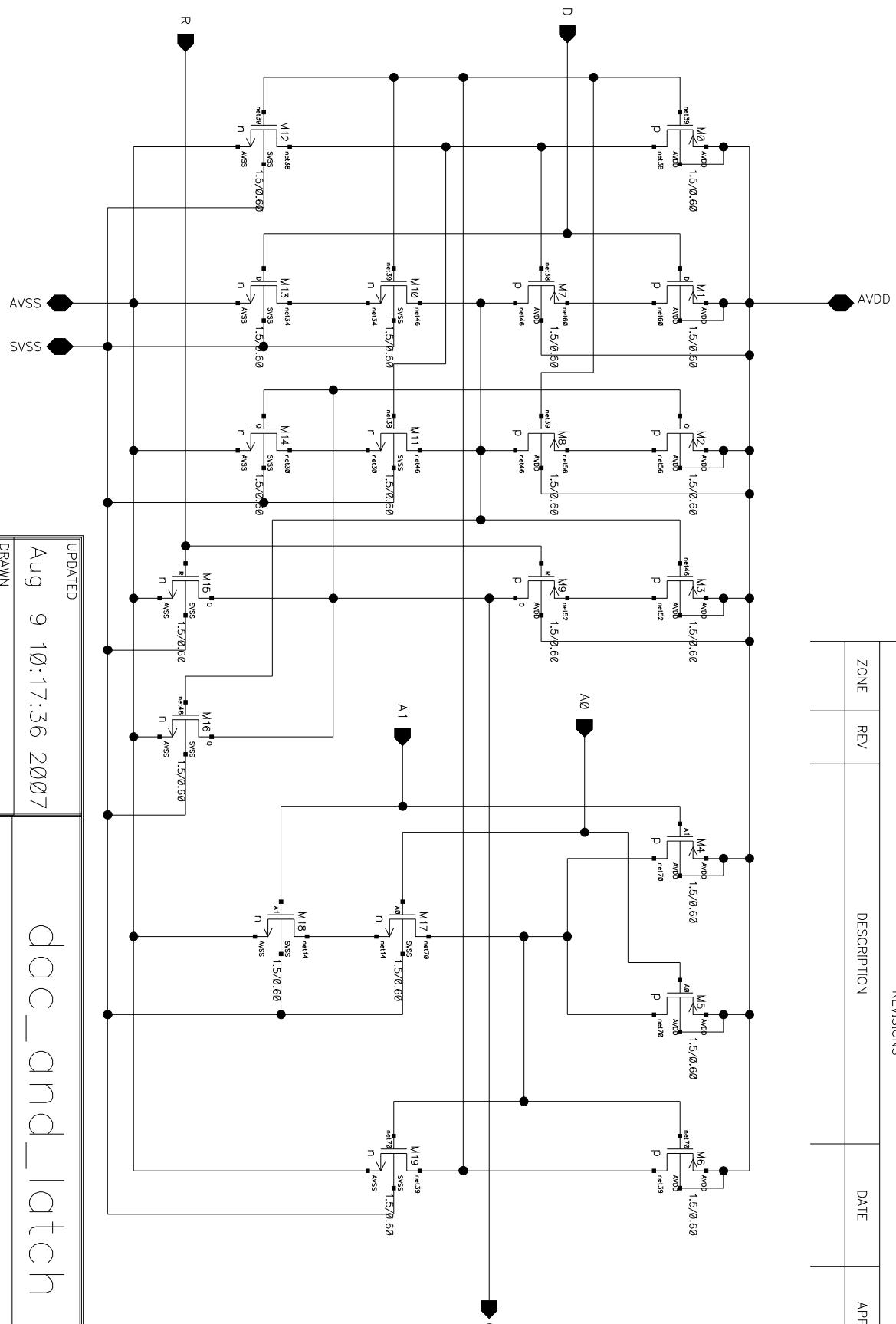
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JUN 6 16:13:32 2007

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CHECKED  
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	SCALE			1 OF 1

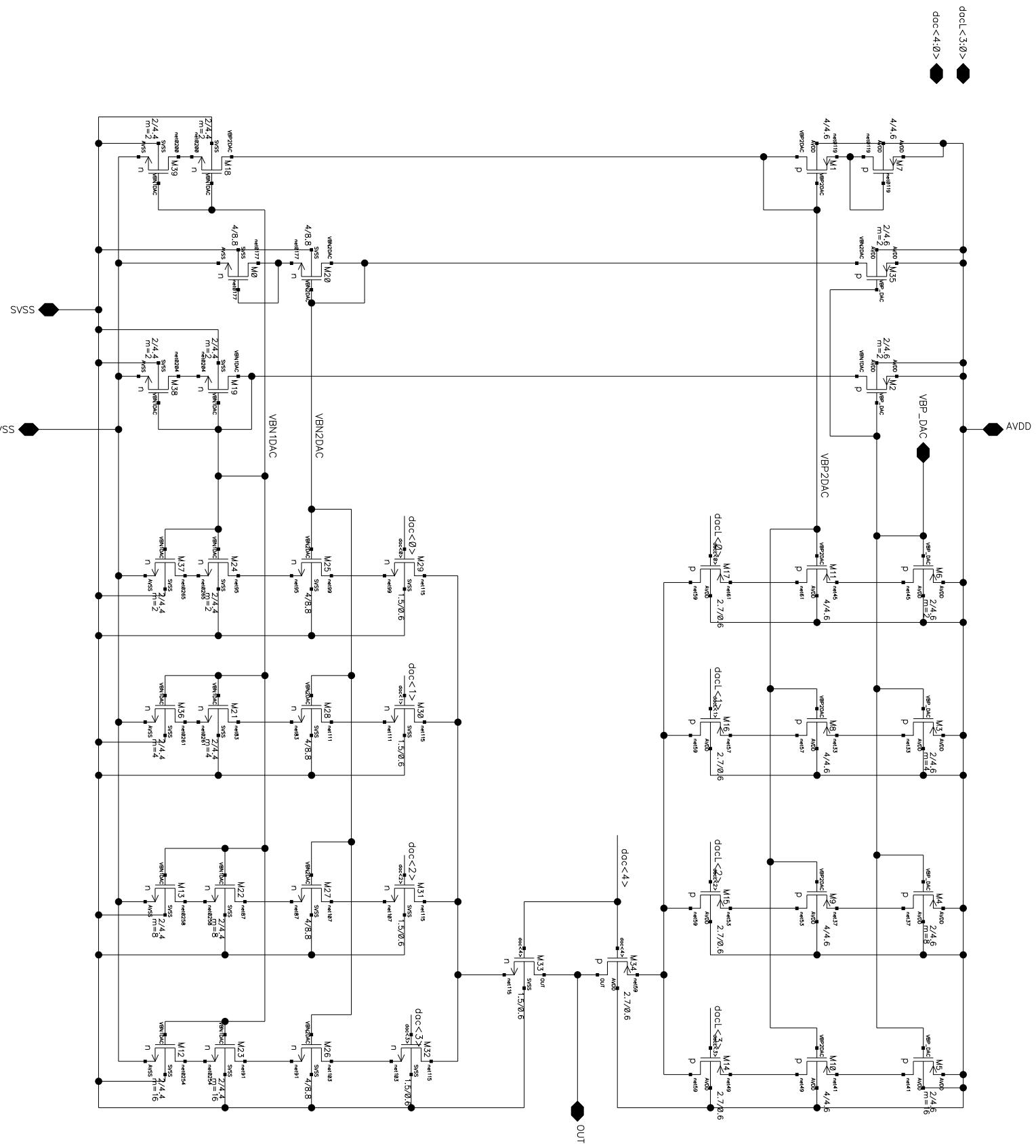




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REVISI						
ZONE	REV	DESCRIPTION	DATE	APPROVED		

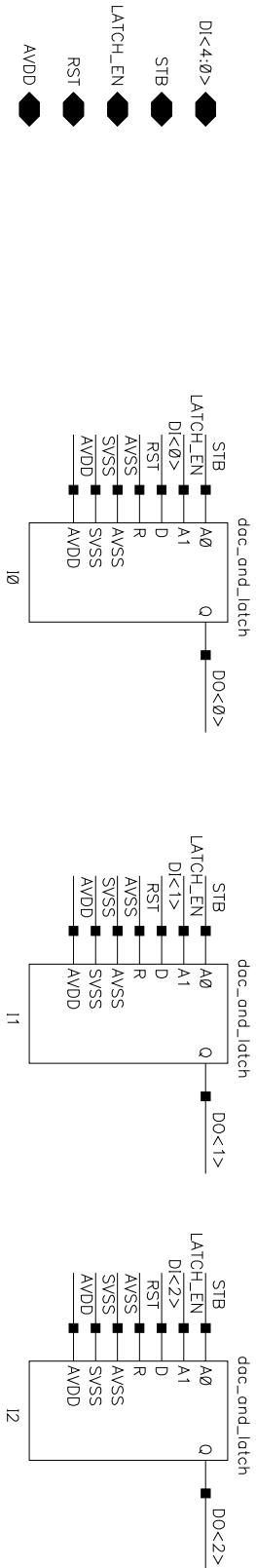
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	SCALE				



ZONE	REV	DESCRIPTION	DATE	APPROVED

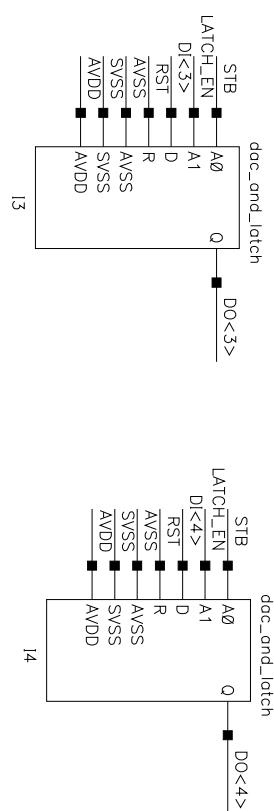
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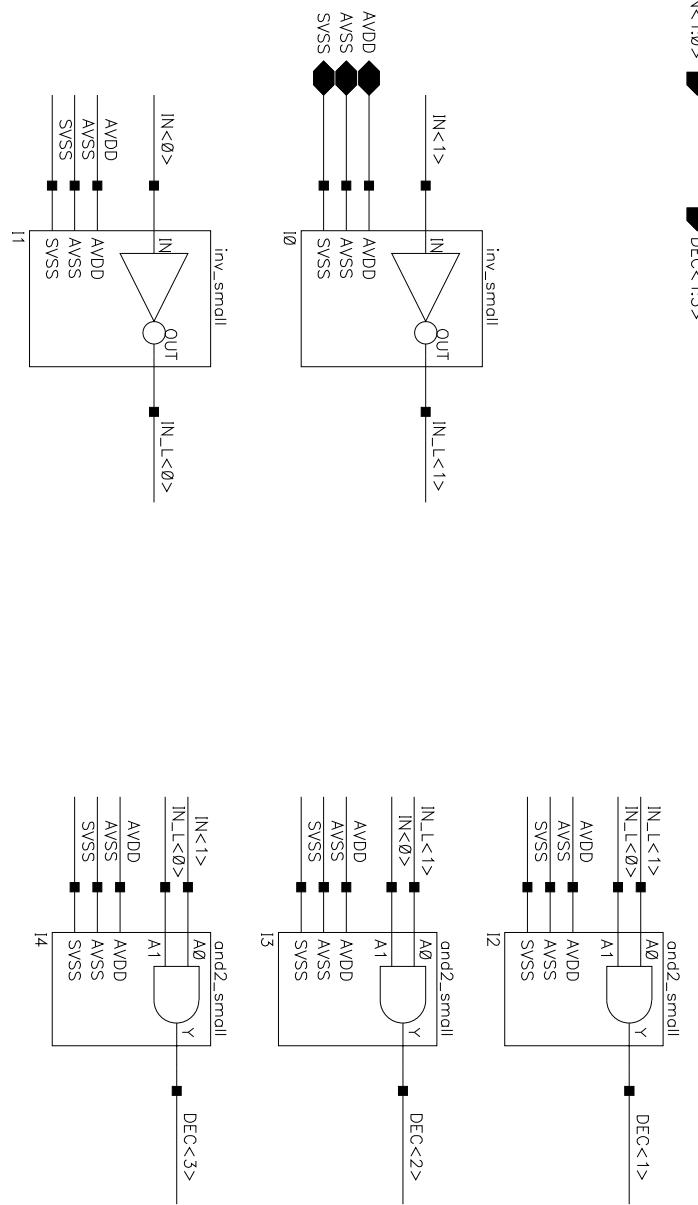


13

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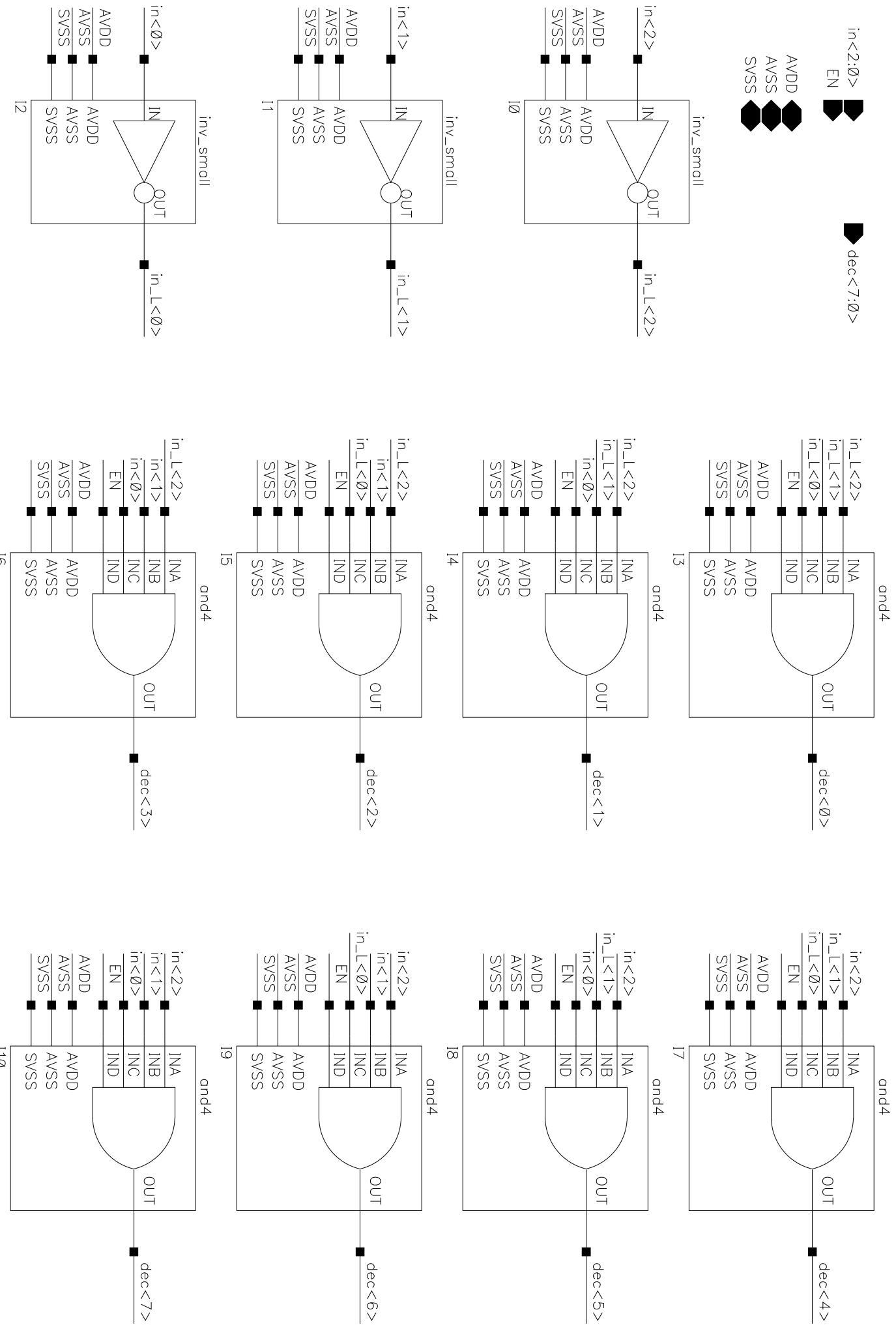
lē\_dac\_reg

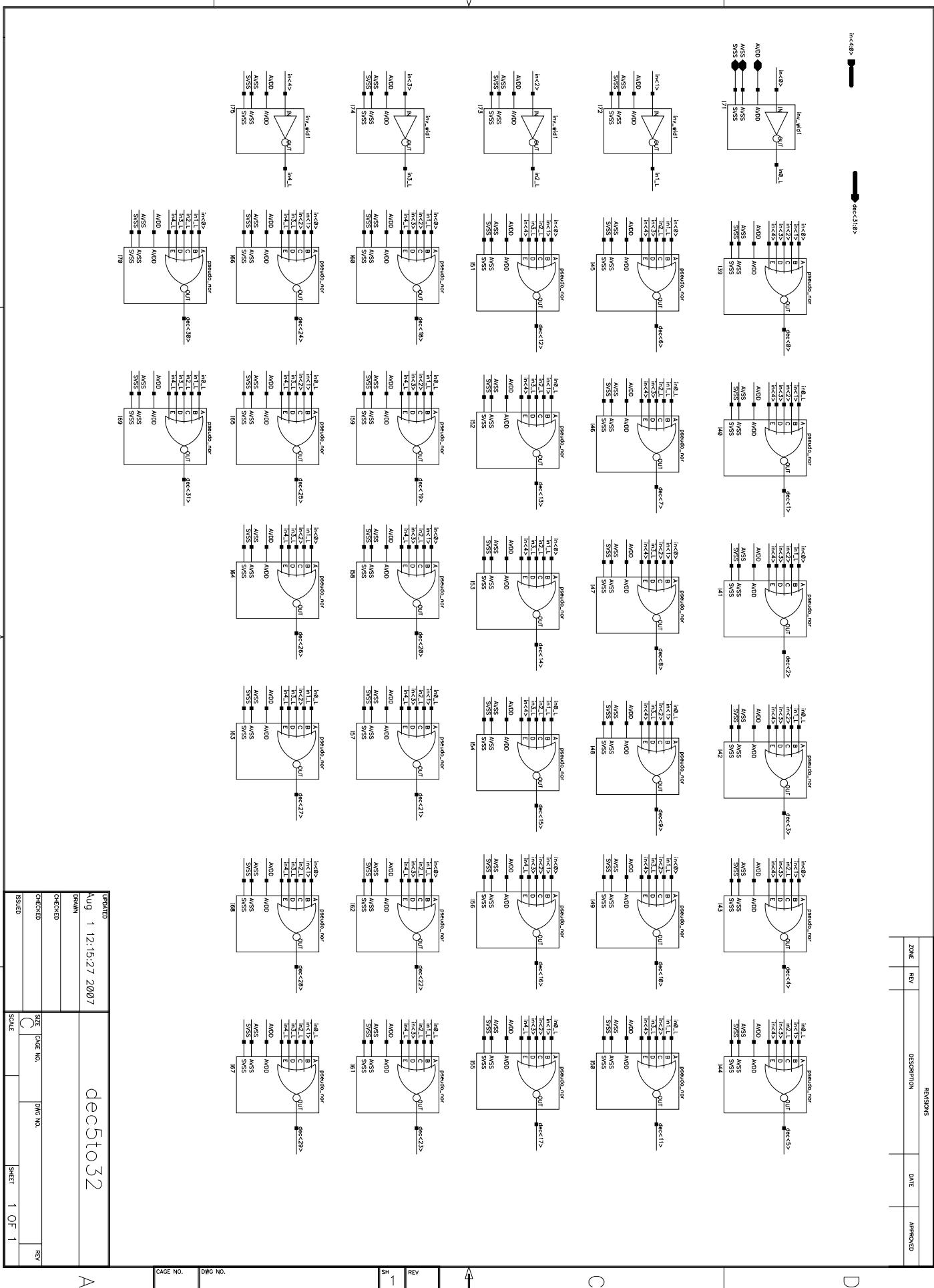
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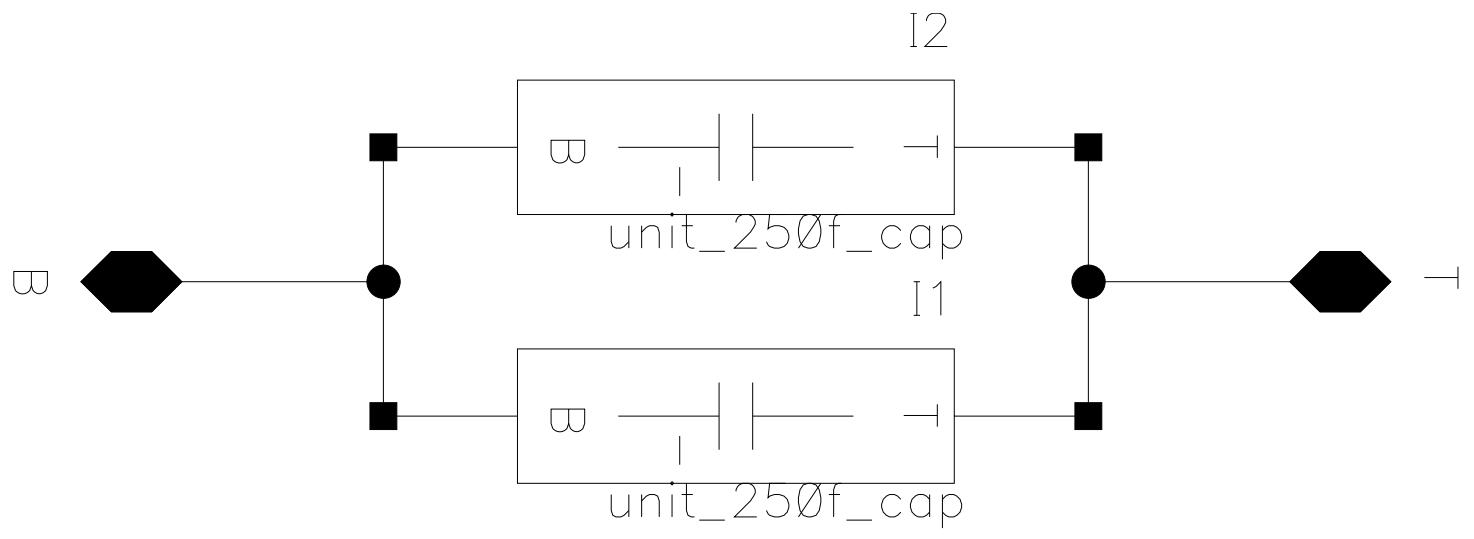


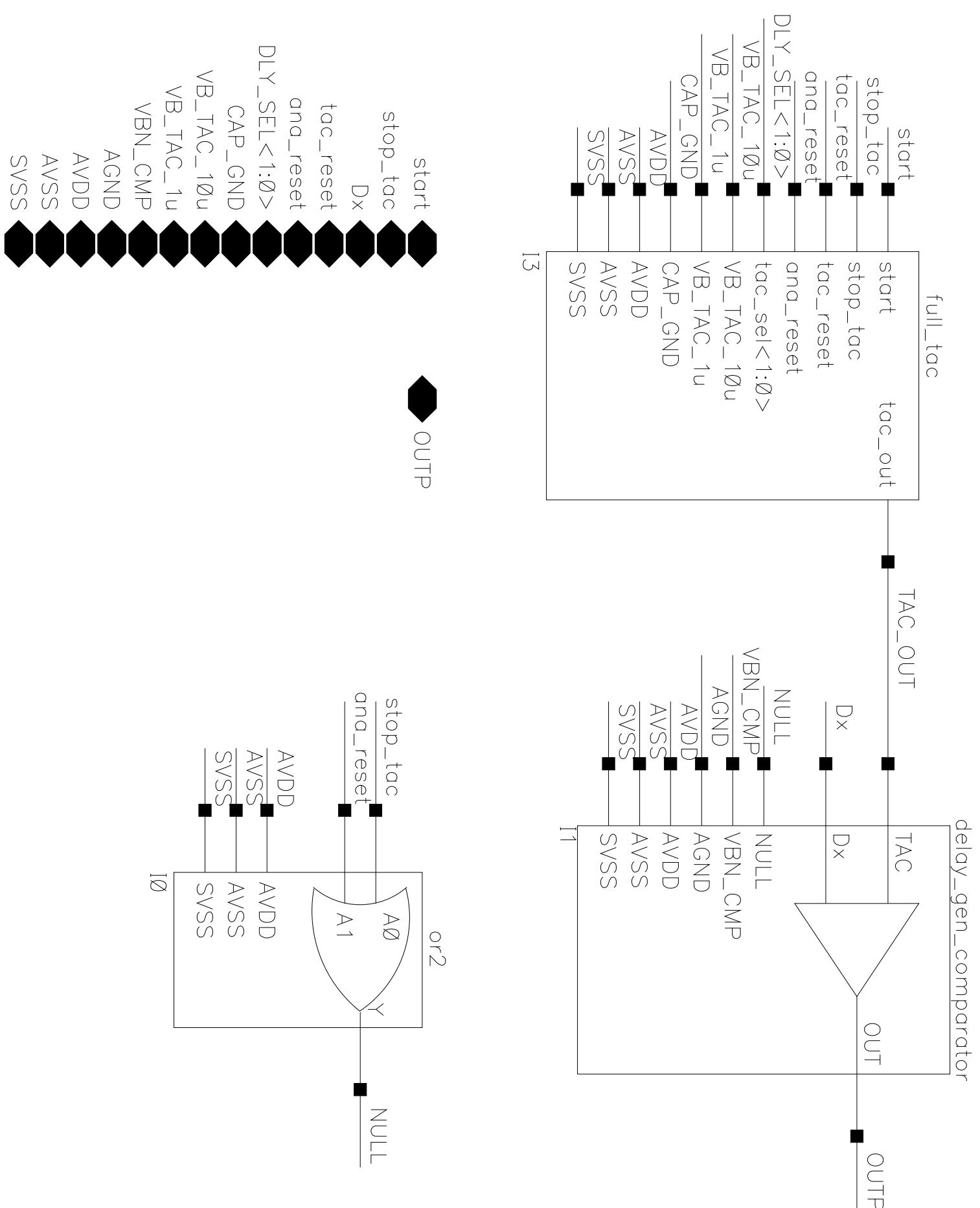
REVISIONS			
ZONE	REV	DESCRIPTION	DATE
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ISSUED			
SIZE	CAGE NO.		DWG NO.
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SCALE			SHEET 1 OF 1
		REV A	



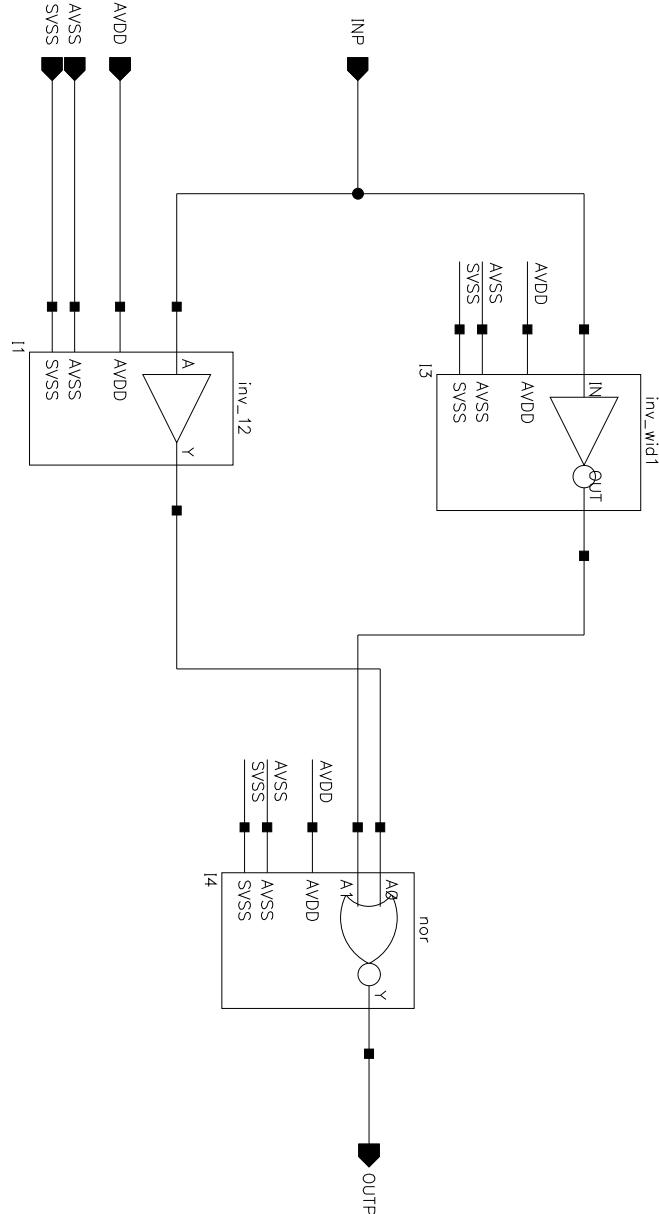




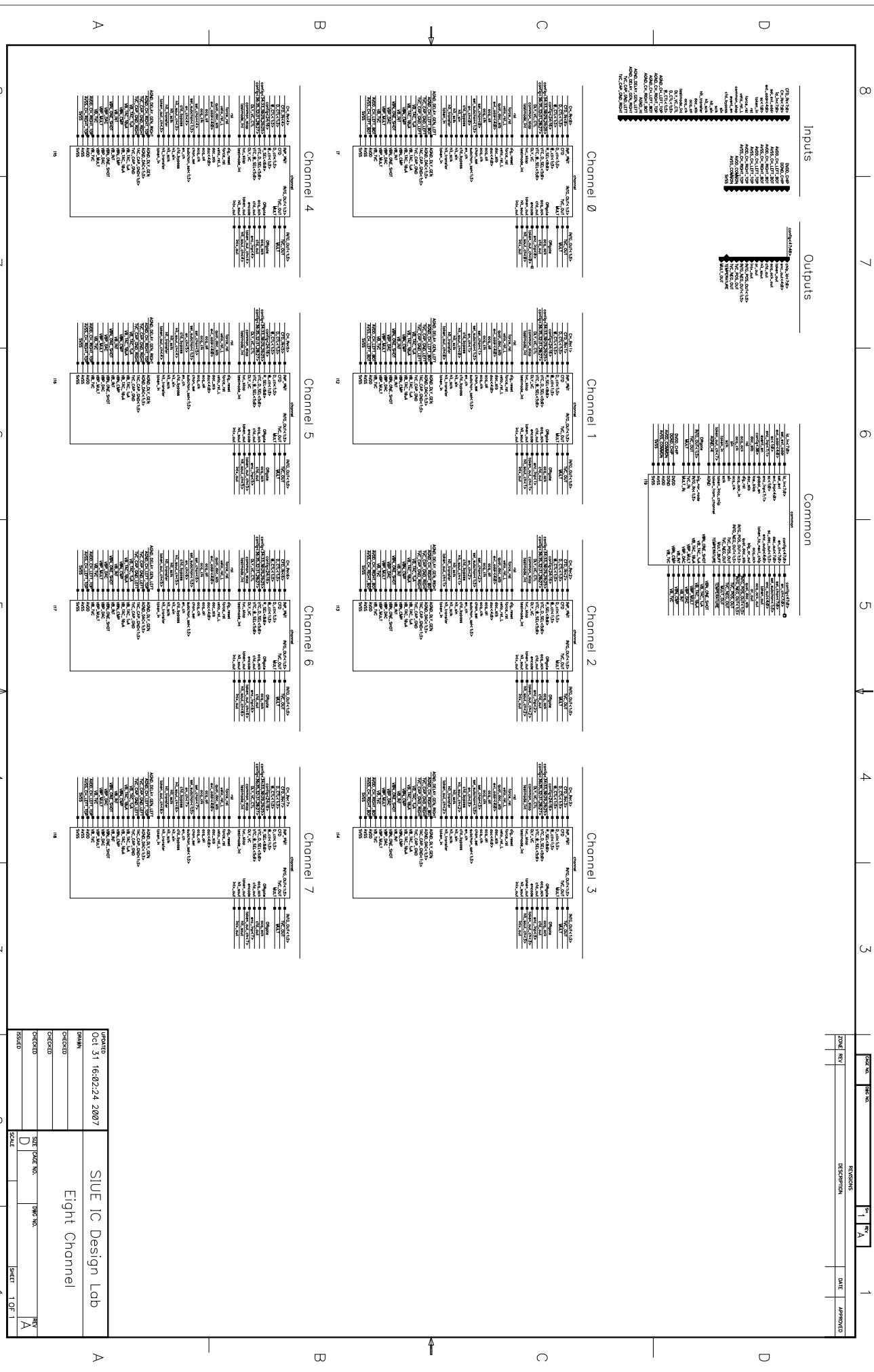


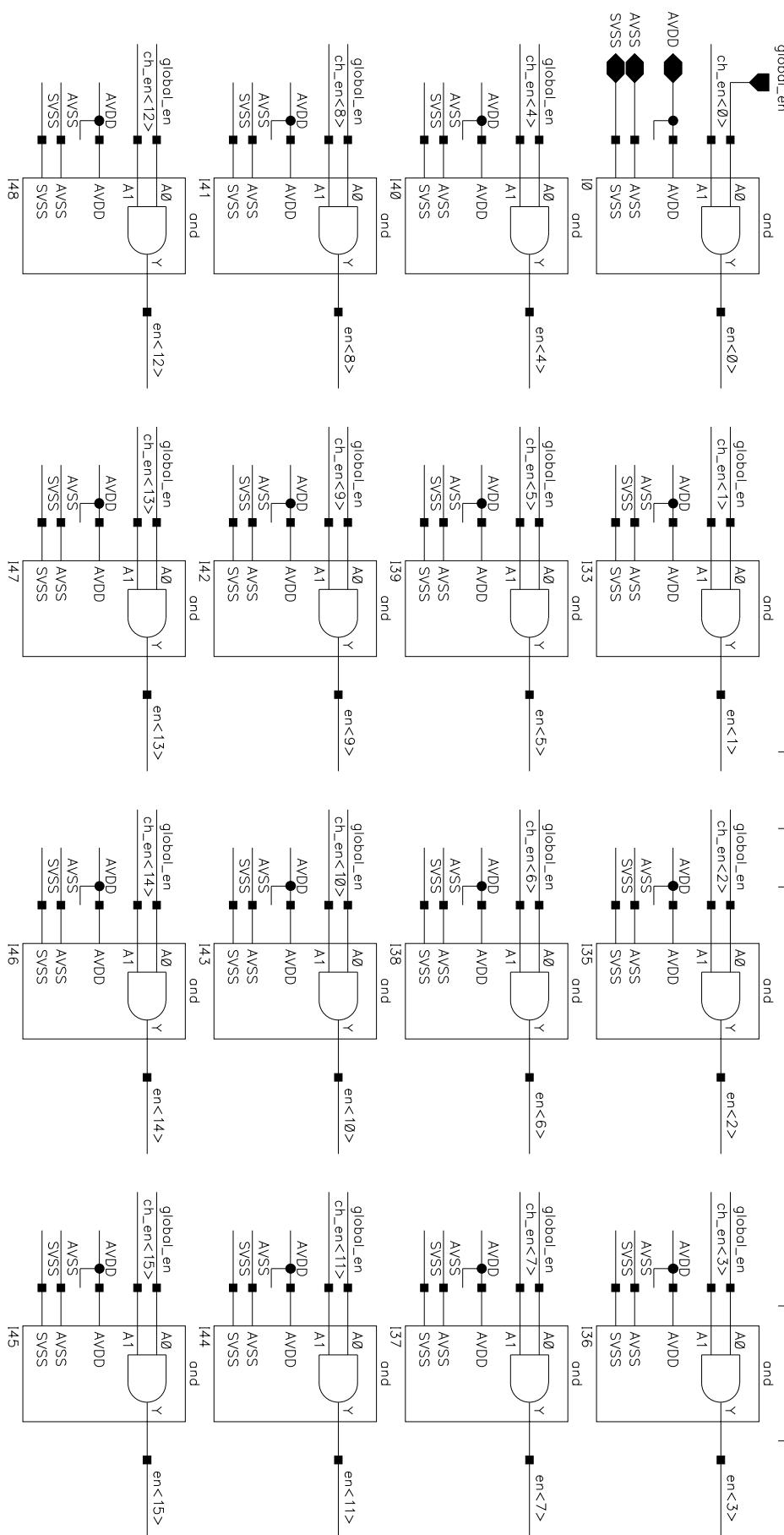


CAGE NO.		DWG NO.	REV
ZONE	REV	DESCRIPTION	
		DATE	APPROVED



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Jun 13 14:00:49 2007			
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	SIZE	CAGE NO.	DWG NO.
	SCALE		SHEET 1 OF 1
			REV





REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV A

# SU EIC Design Lab

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## Enable Logic

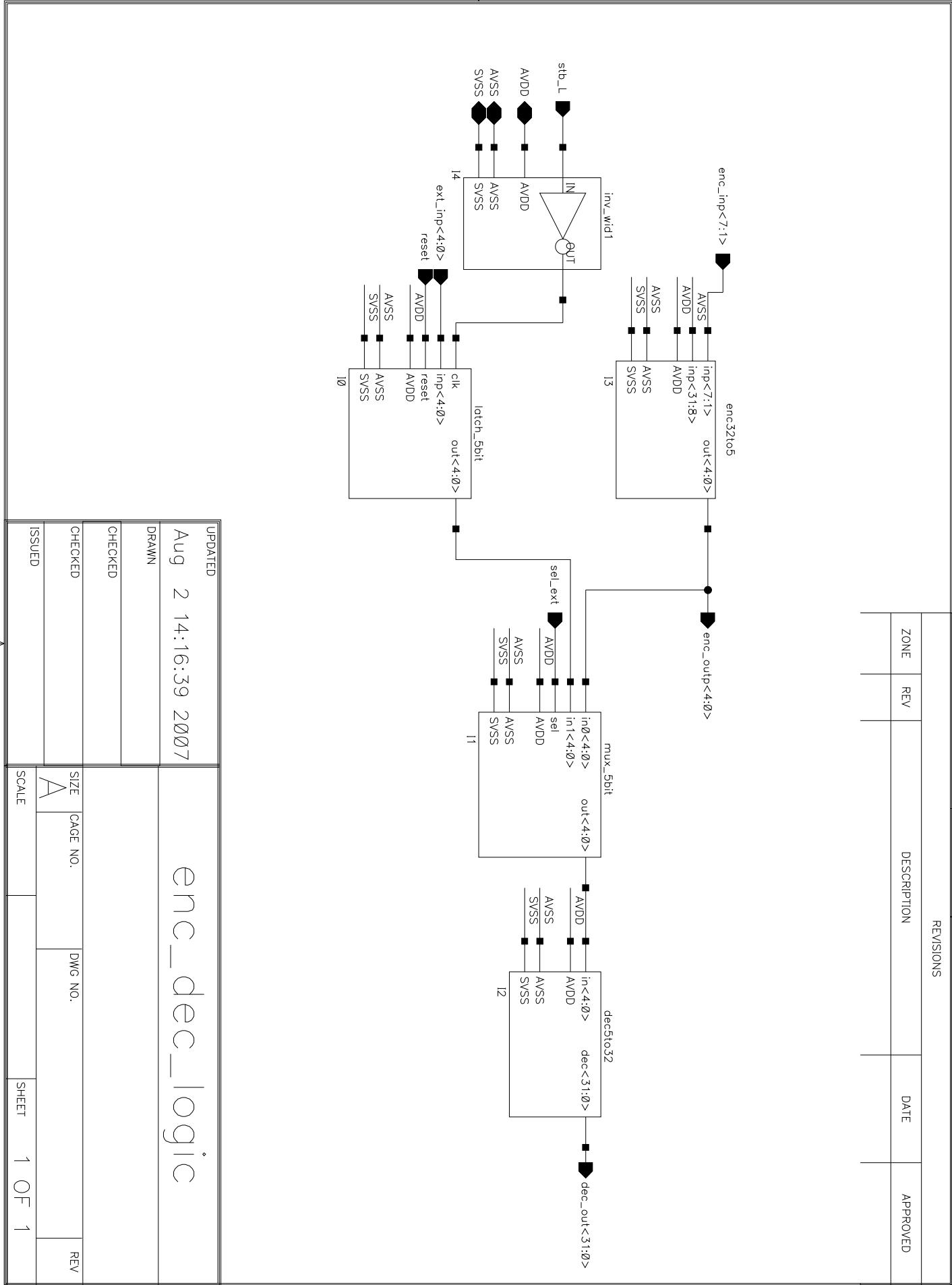
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	SIZE A	CAGE NO.	DWG NO.
	SCALE		
			1 OF 1
		REV A	

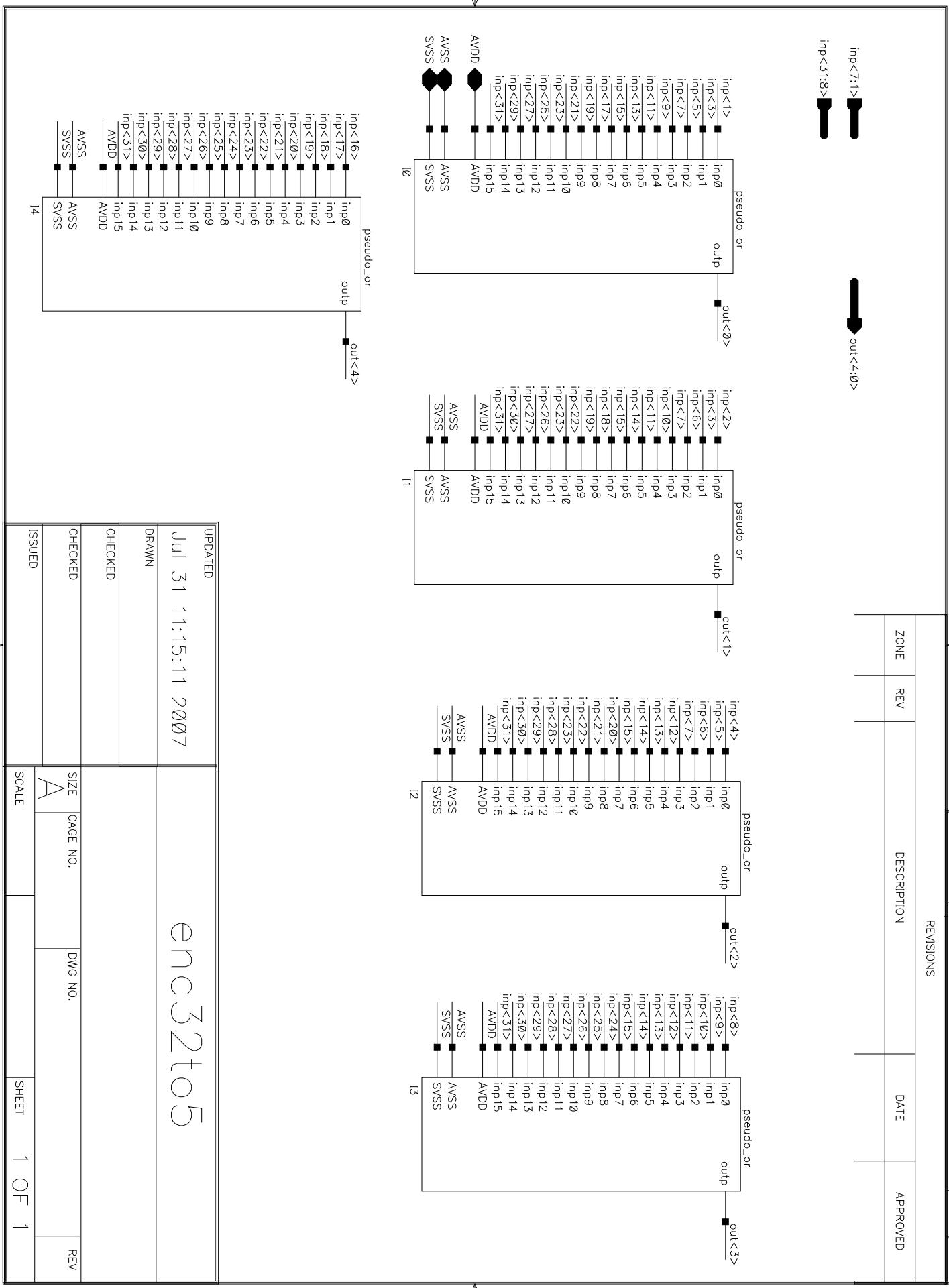
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CAGE NO. DWG NO. SH 1 REV

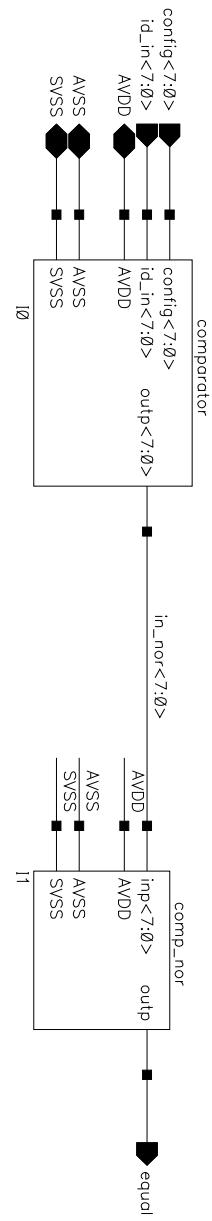
REVISIONS



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	SCALE			REV



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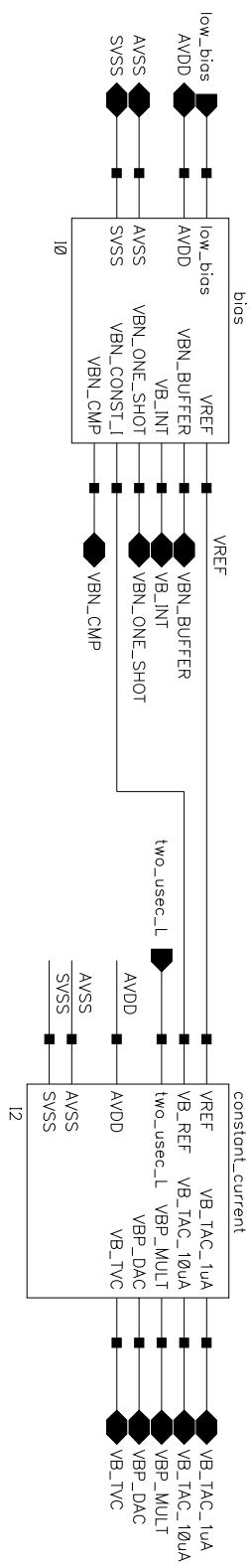


REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

equal logic.

UPDATED	equa _log c			
JUL 9 14:10:40 2007				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1

CAGE NO.	DWG NO.	REV		
		SH 1		
ZONE	REV	DESCRIPTION	DATE	APPROVED



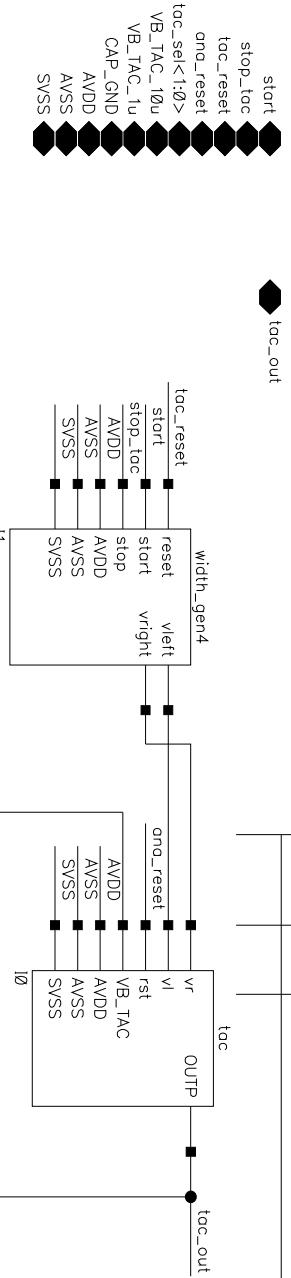
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Oct 30 14:17:59 2007			
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CHECKED			
CHECKED			
ISSUED			
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	SCALE		
		SHEET	1 OF 1
		REV	

CAGE NO.	DWG NO.	REV		
ZONE	REV	DESCRIPTION	DATE	APPROVED
			SH 1	REV



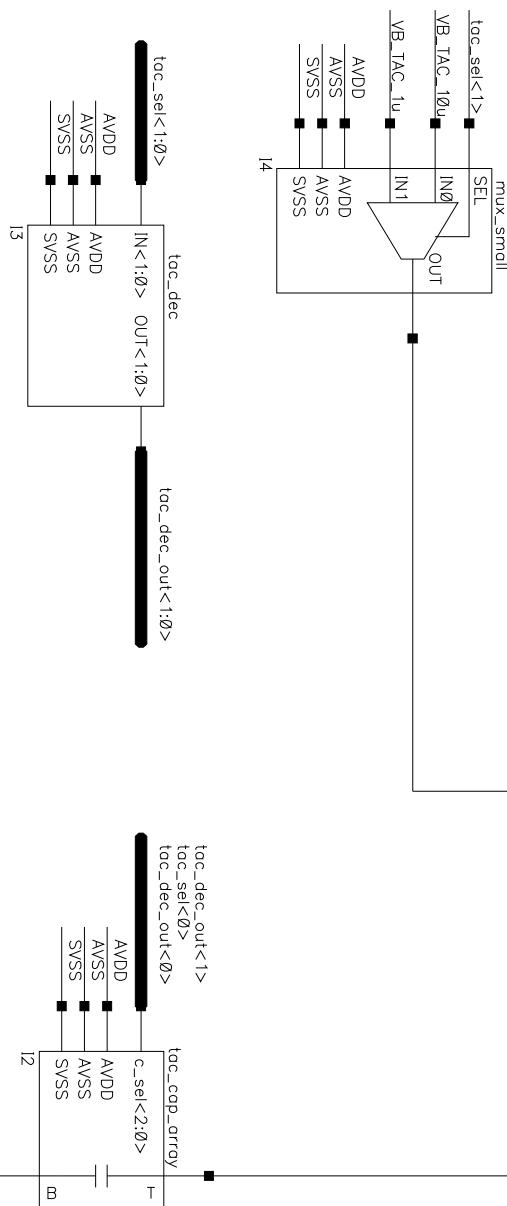
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REVISIONS



11

10



13

14

12

UPDATED

Oct 31 16:02:09 2007

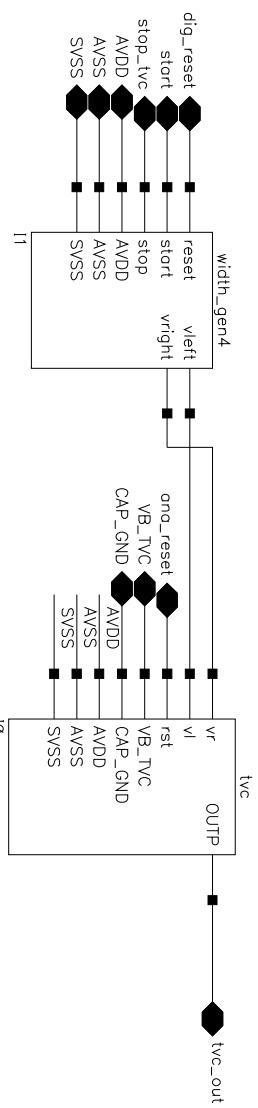
fULL\_tAC

DRAWN

tac_sel	l (uA)	C (pF)	T max (ns)	T min (ns)
00	10	0.2	50	5
01	10	1.0	250	25
10	1	0.6	1500	150
11	1	4.0	10000	1000

Note: Assume Vmax = 2.5 and Vmin = 0.25

ISSUED	SIZE	CAGE NO.	DWG NO.	SHEET	1 OF 1
CHECKED	SCALE				



ZONE	REV	DESCRIPTION		DATE	APPROVED
UPDATED					
JUL 9 11:21:55 2007					
DRAWN					
CHECKED					
CHECKED					
ISSUED					
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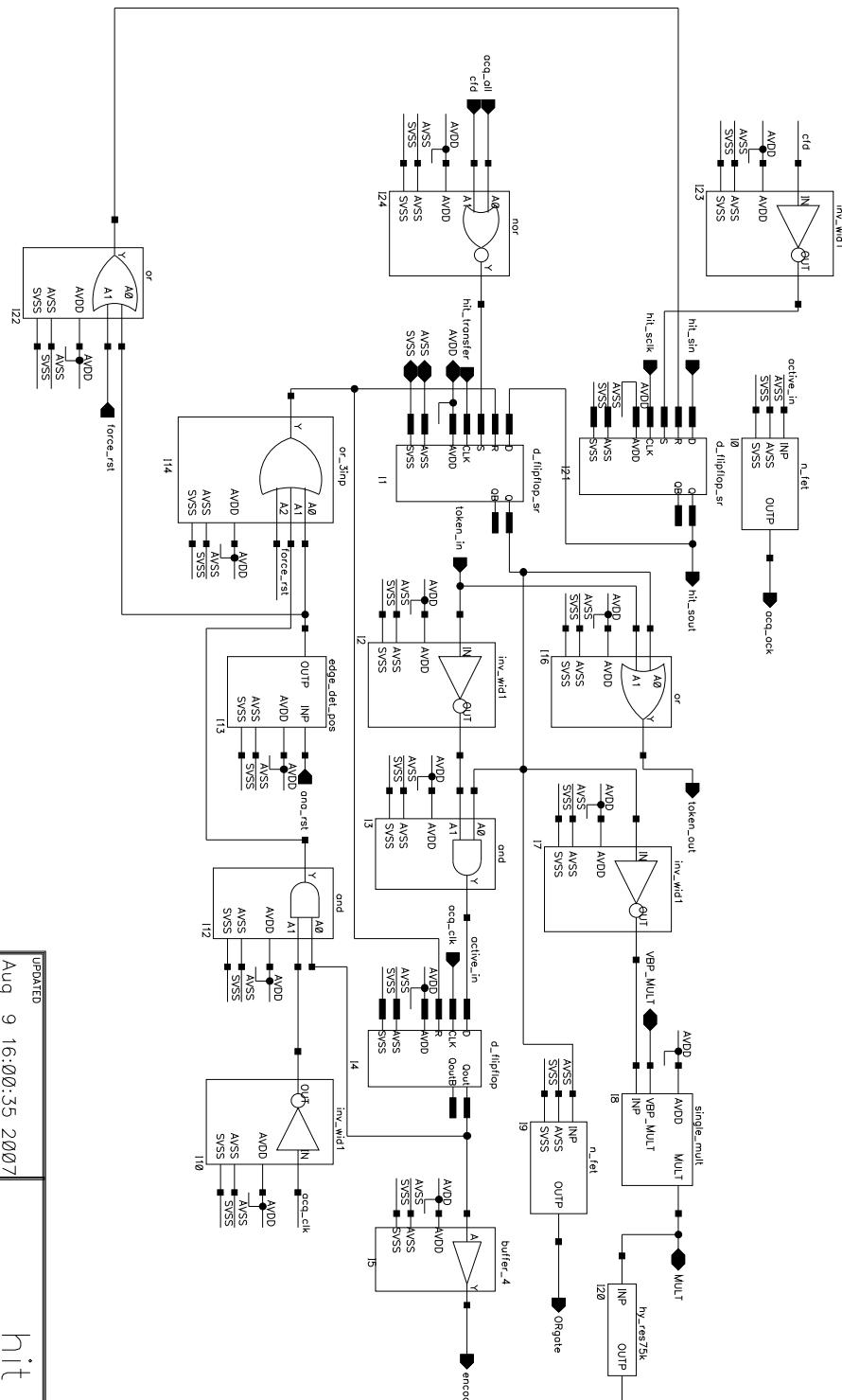
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ZONE REV

REVISIONS

DATE APPROVED

SH 1 REV



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CHECKED	
CHECKED	
ISSUED	

REV

SCALE

SIZE

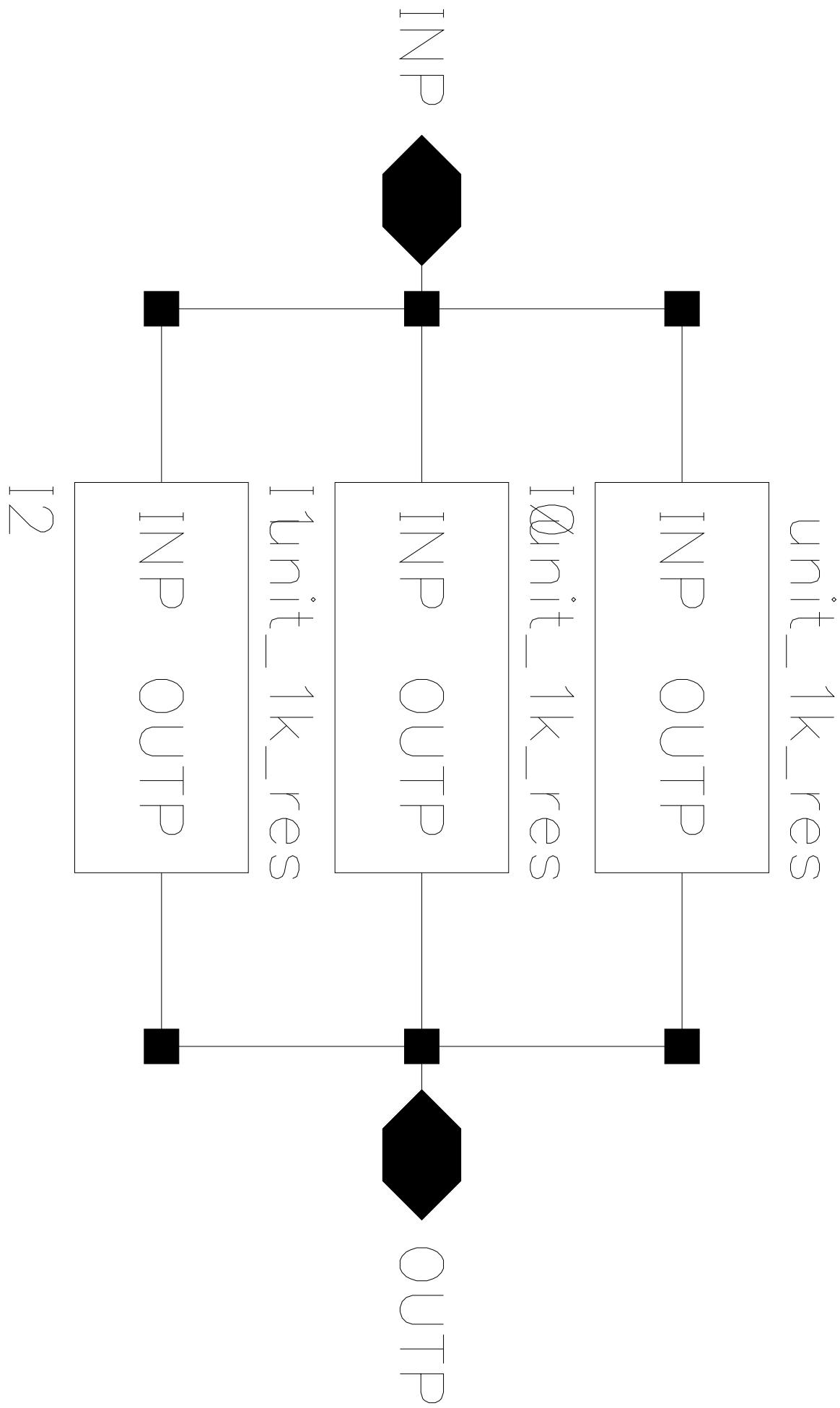
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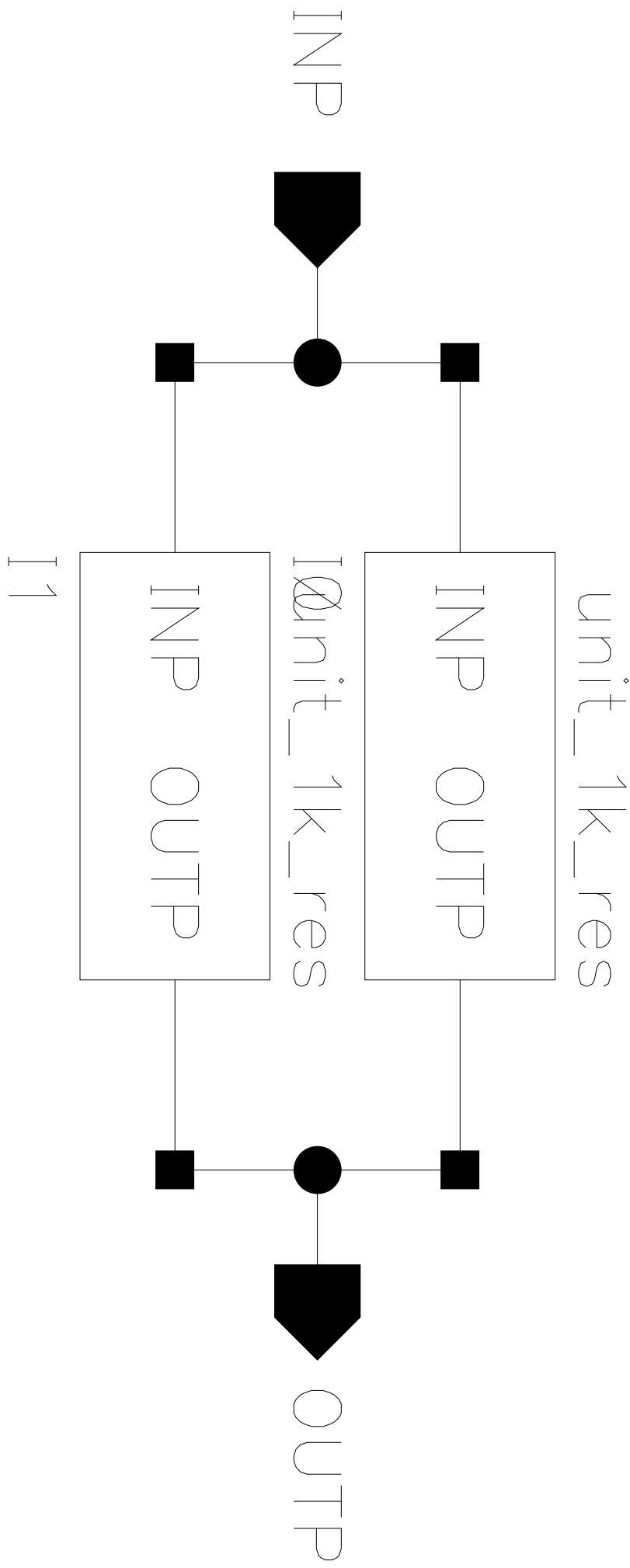
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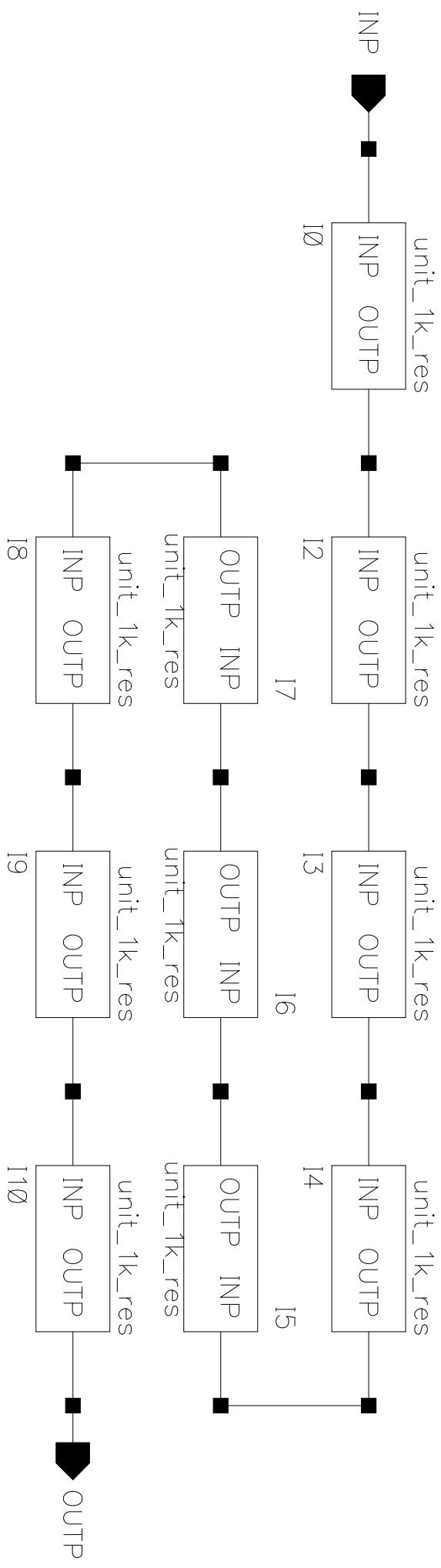
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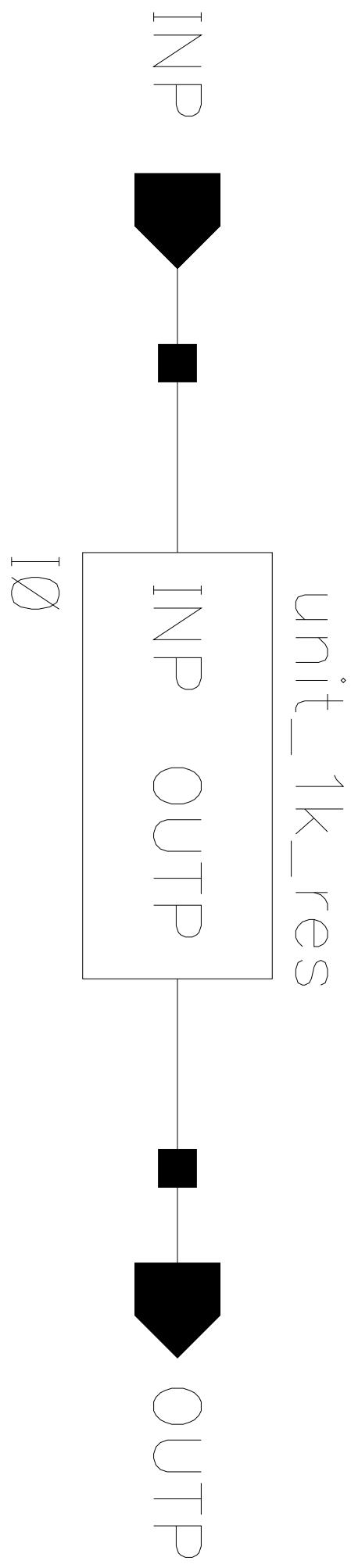
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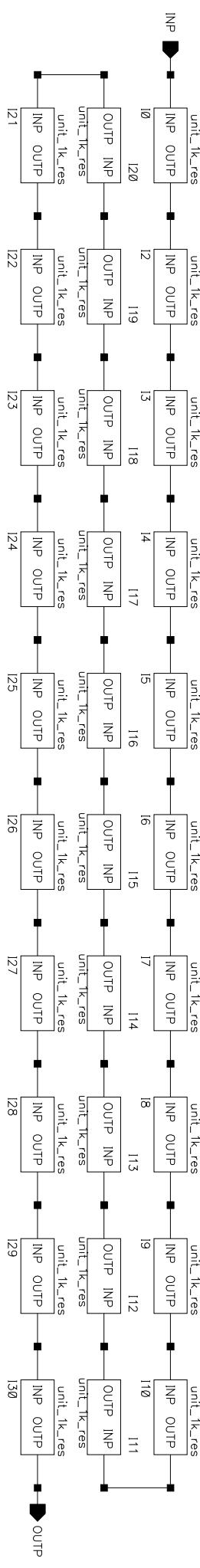
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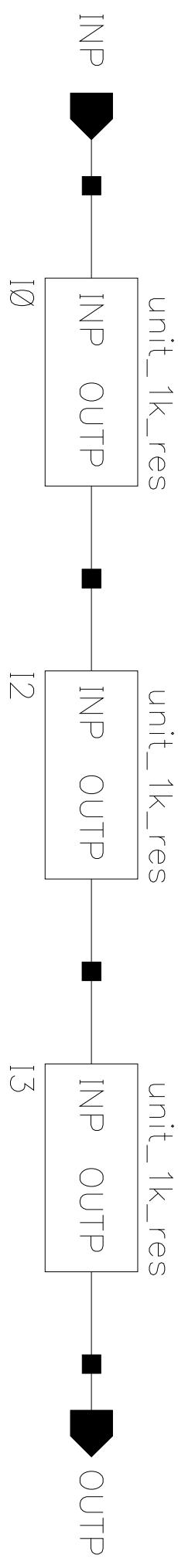


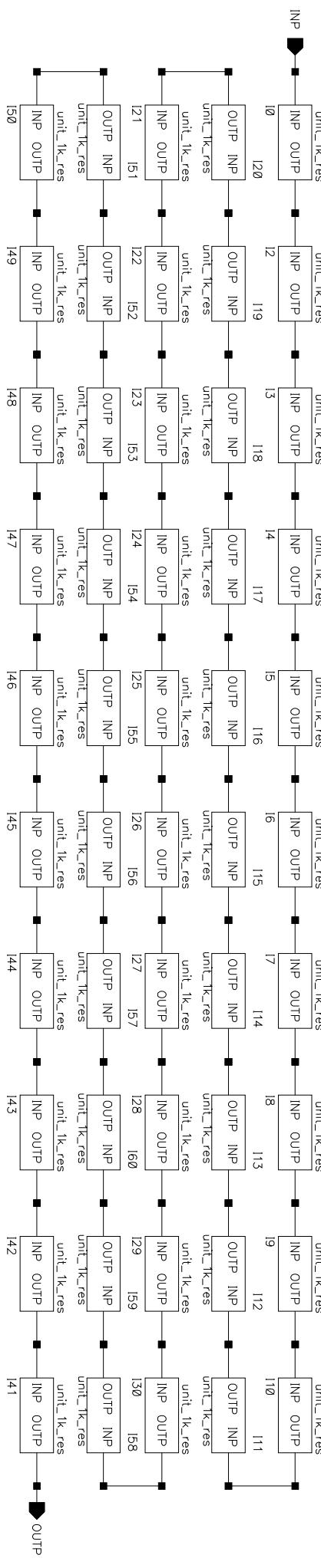


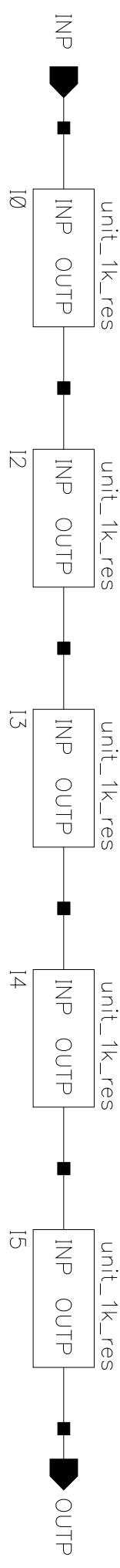


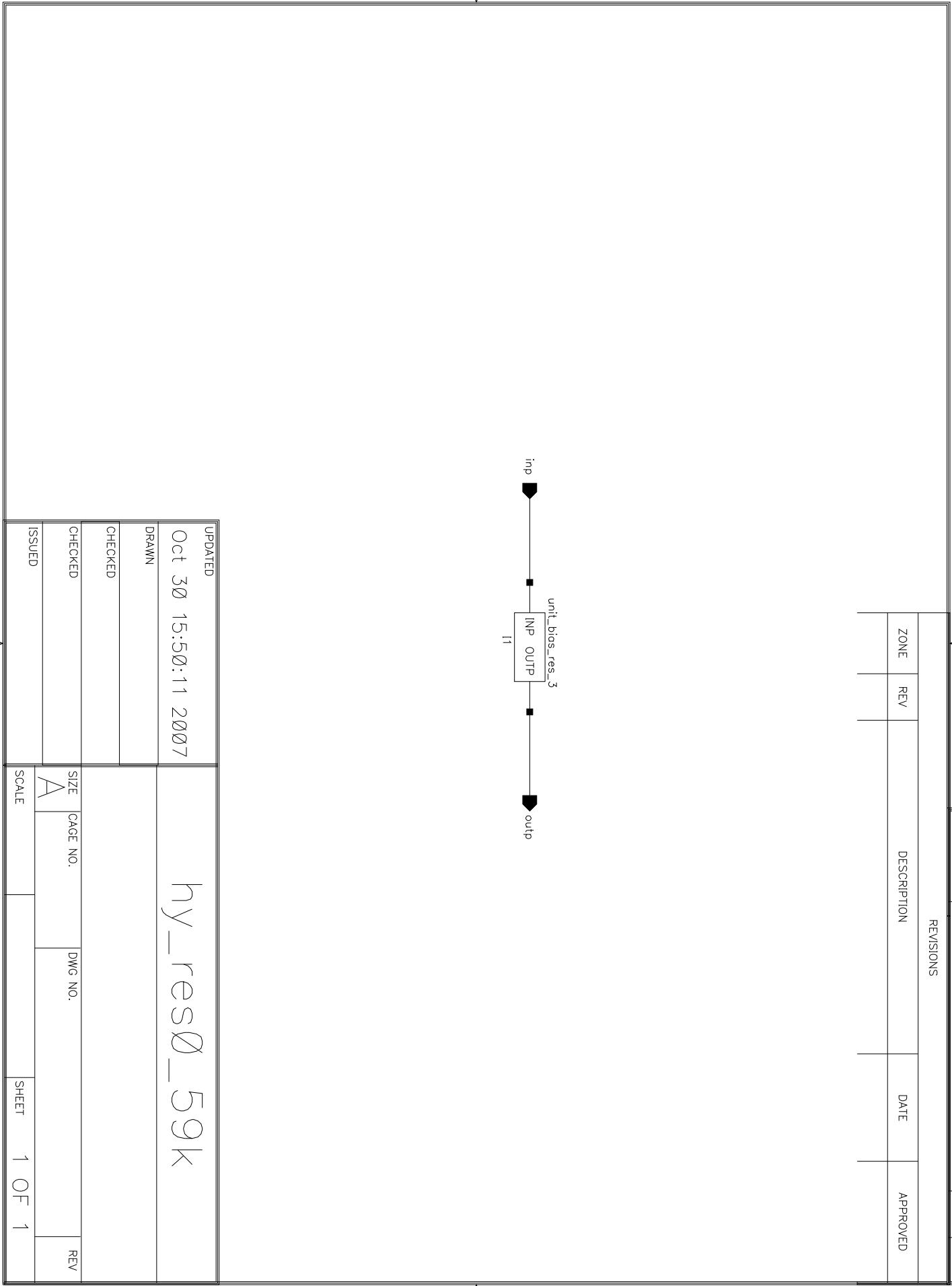


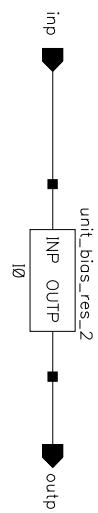






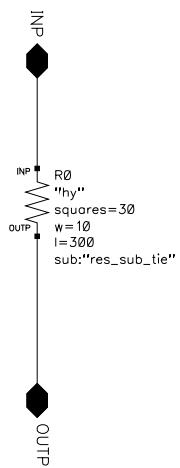






hy-res17k

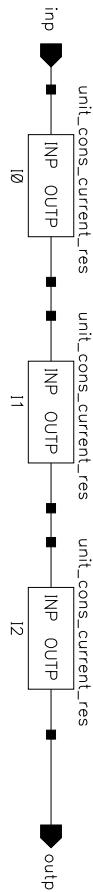
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DRAWN												
CHECKED												
CHECKED												
ISSUED	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20%; text-align: center;">SIZE</td> <td style="width: 40%; text-align: center;">CAGE NO.</td> <td style="width: 40%; text-align: center;">DWG NO.</td> </tr> <tr> <td style="text-align: center;">A</td> <td></td> <td></td> </tr> <tr> <td style="text-align: center;">SCALE</td> <td></td> <td></td> </tr> </table>			SIZE	CAGE NO.	DWG NO.	A			SCALE		
SIZE	CAGE NO.	DWG NO.										
A												
SCALE												
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%; text-align: center;">SHEET</td> <td style="width: 20%; text-align: center;">1</td> <td style="width: 40%; text-align: center;">OF 1</td> </tr> <tr> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> </tr> </table>			SHEET	1	OF 1						
SHEET	1	OF 1										
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%; text-align: center;">REV</td> <td style="width: 20%; text-align: center;"></td> <td style="width: 40%; text-align: center;"></td> </tr> <tr> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> </tr> </table>			REV								
REV												



UPDATED	hy_res30k		
Aug 16 14:34:22 2007			
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CHECKED	SIZE A	CAGE NO.	DWG NO.
ISSUED	SCALE		SHEET 1 OF 1
REV			

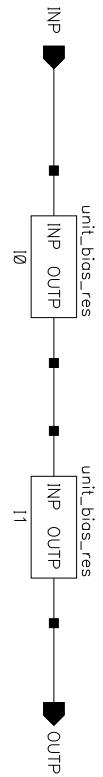
CAGE NO.	DWG NO.	SH 1	REV
ZONE	REV	DESCRIPTION	
		DATE	APPROVED

CAGE NO.		DWG NO.	SH 1	REV
ZONE	REV	DESCRIPTION		APPROVED
				DATE



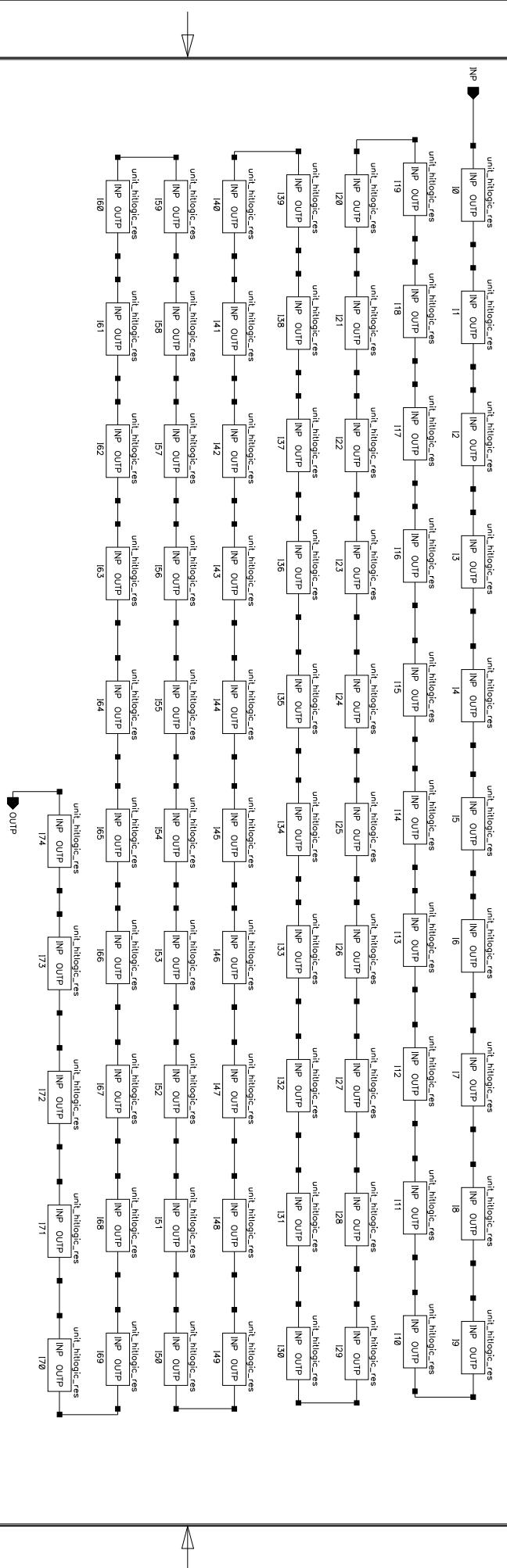
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Oct 30 15:34:02 2007			
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CHECKED			
CHECKED			
ISSUED			
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	A		
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		SHEET	1 OF 1
		REV	

CAGE NO.		DWG NO.	SH 1	REV	
ZONE	REV	DESCRIPTION		DATE	APPROVED



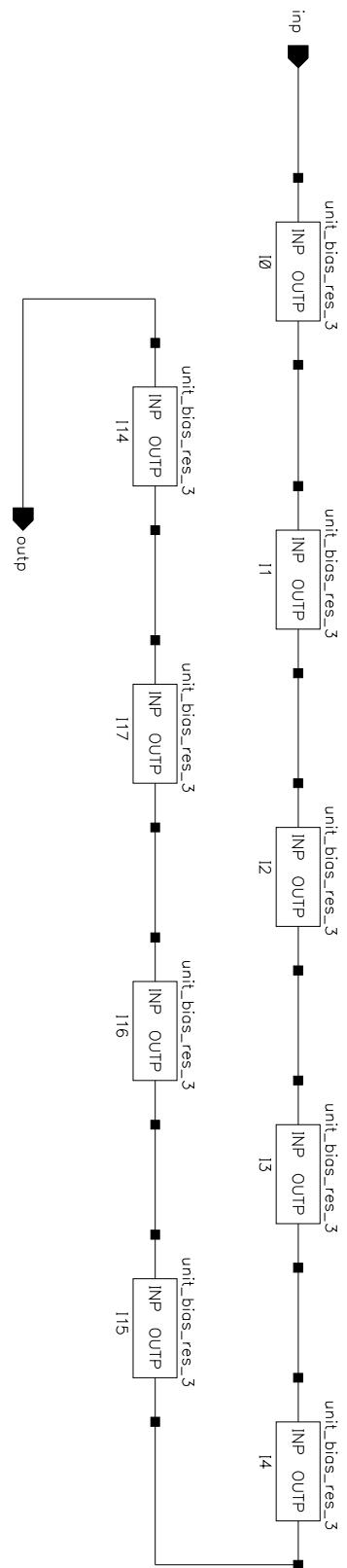
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ISSUED			
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SCALE			
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ZONE	REV	DESCRIPTION	DATE	APPROVED
			SH 1 REV	

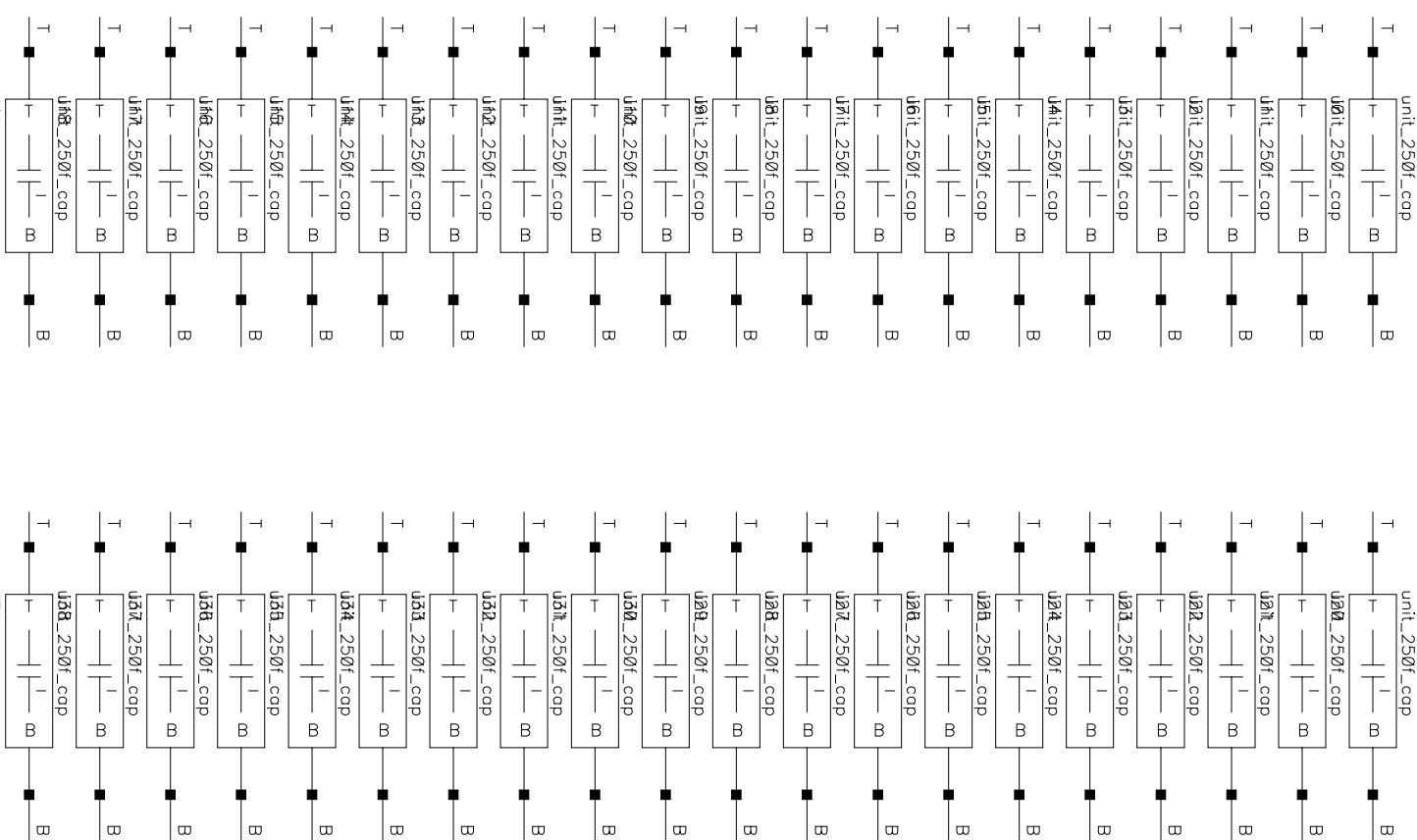


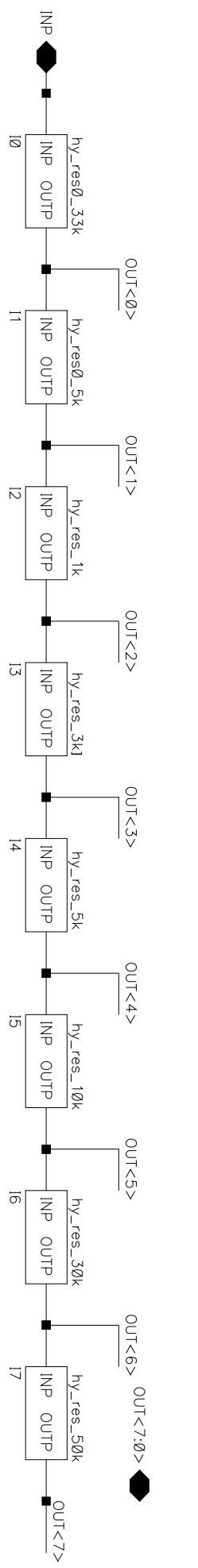
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CHECKED			
ISSUED	SCALE	SHEET	1 OF 1

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ZONE	REV	DESCRIPTION		DATE	APPROVED



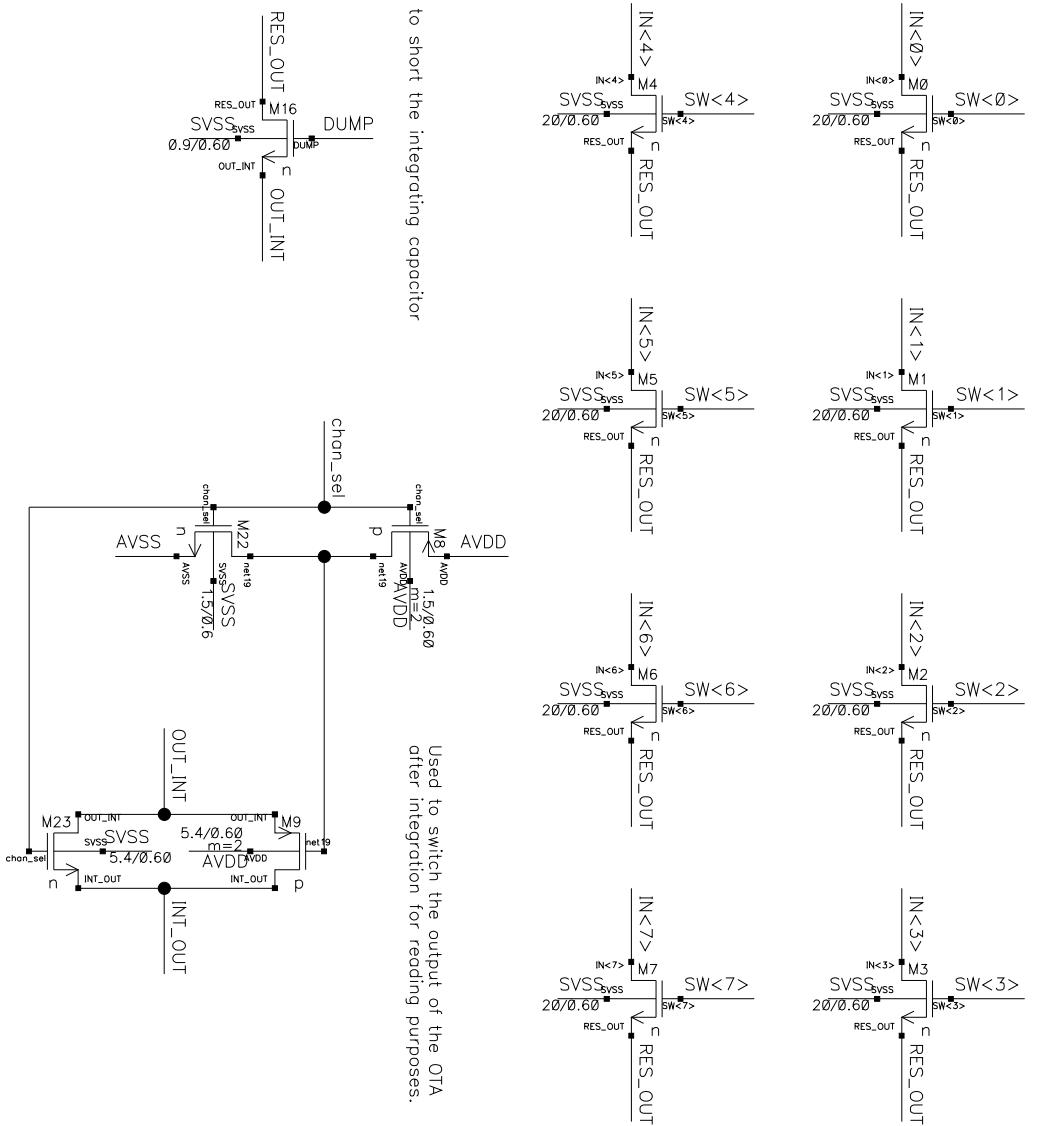
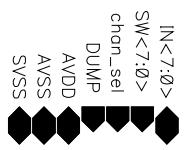
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Oct 30 15:37:15 2007			
DRAWN			
CHECKED			
ISSUED	SIZE A	CAGE NO.	DWG NO.
	SCALE		SHEET 1 OF 1
			REV





Output	Resistance
OUT<0>	0.5 K
OUT<1>	1 K
OUT<2>	2 K
OUT<3>	5 K
OUT<4>	10 K
OUT<5>	20 K
OUT<6>	50 K
OUT<7>	100 K

Resistances include the switch resistance following the resistor array.

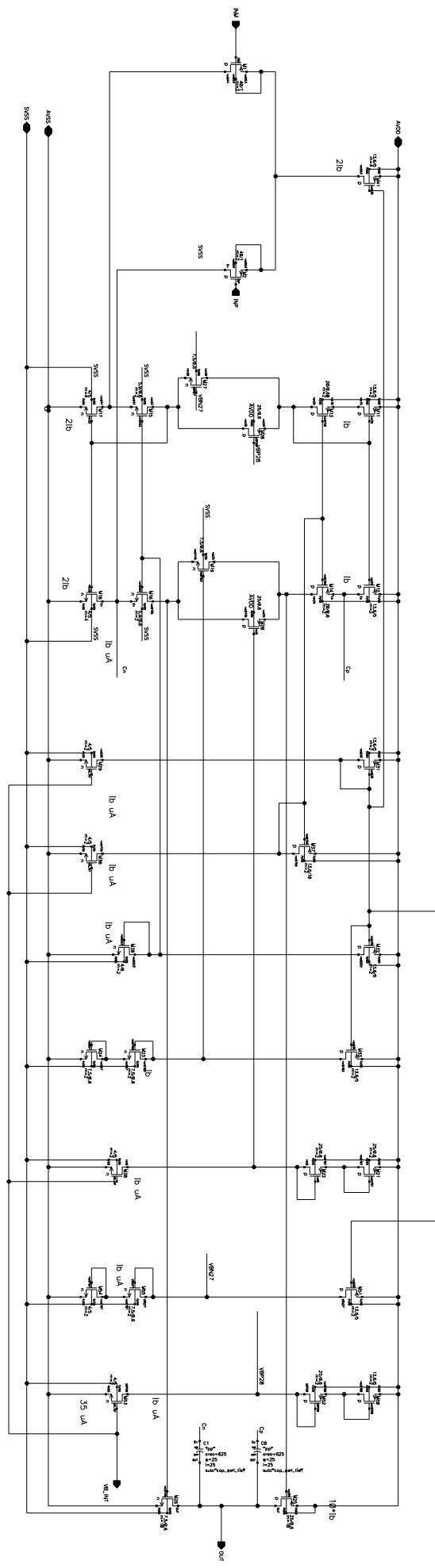


Resistances include the switch resistance and the resistor array preceding the switch.



Switch Resistance

Switch	Resistance
SW<0>	0.5 K
SW<1>	1 K
SW<2>	2 K
SW<3>	5 K
SW<4>	10 K
SW<5>	20 K
SW<6>	50 K
SW<7>	100 K

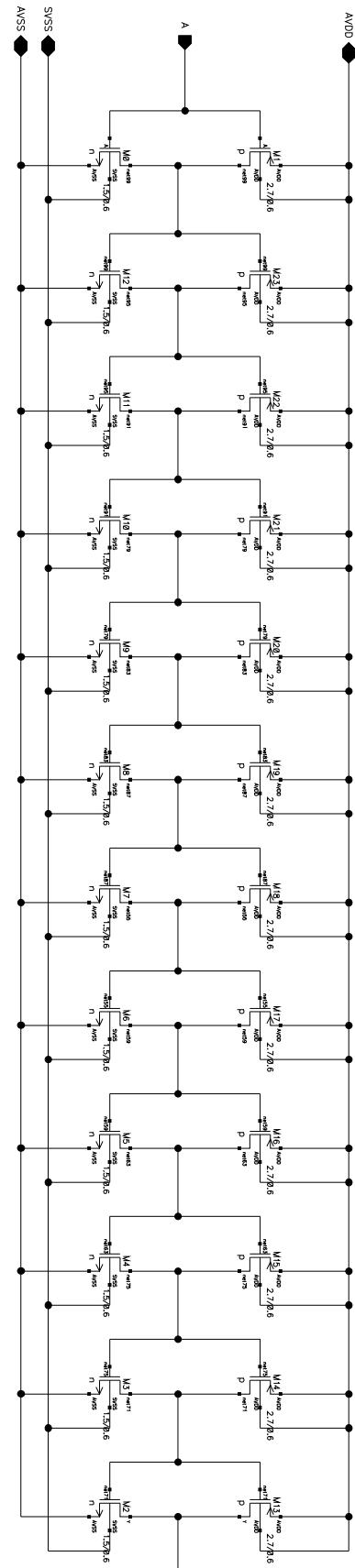


CAGE NO. DWG NO.

ZONE REV DESCRIPTION DATE APPROVED

REVISIONS

REV



UPDATED  
JUN 11 12:04:17 2007

INV\_12

DRAWN

CHECKED

CHECKED

ISSUED

SCALE

REV

SIZE

B

CAGE NO.

DWG NO.

REV

SHEET

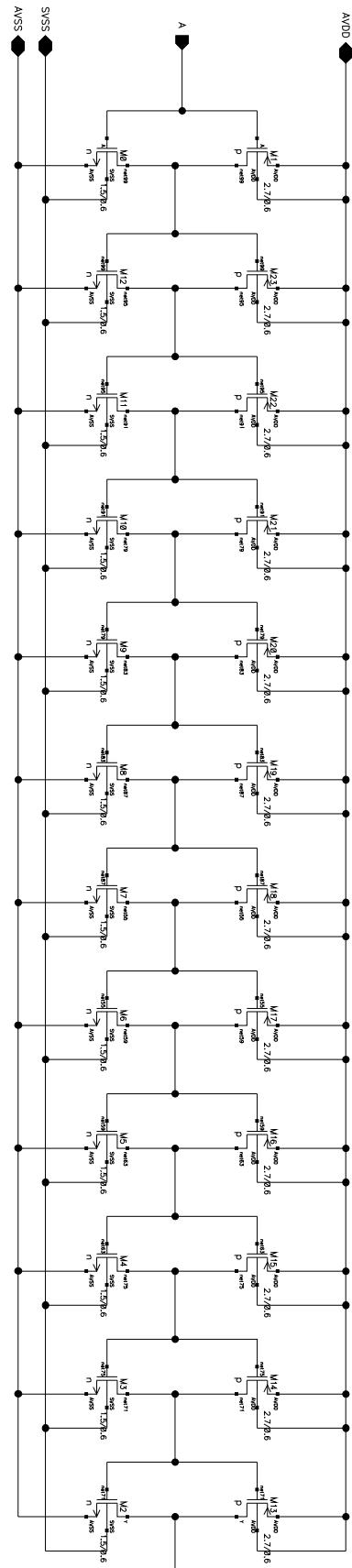
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CAGE NO. DWG NO.

ZONE REV DESCRIPTION DATE APPROVED

REVISIONS

REV

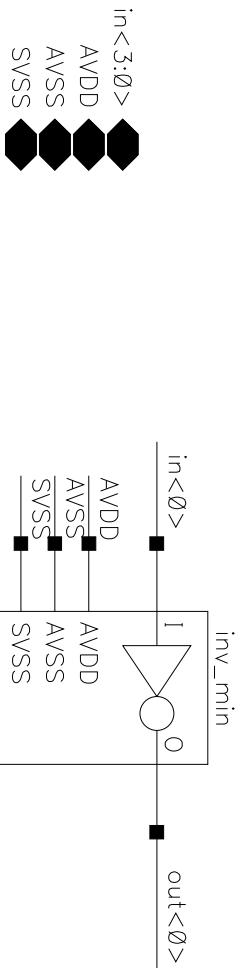


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JUN 11 12:04:17 2007

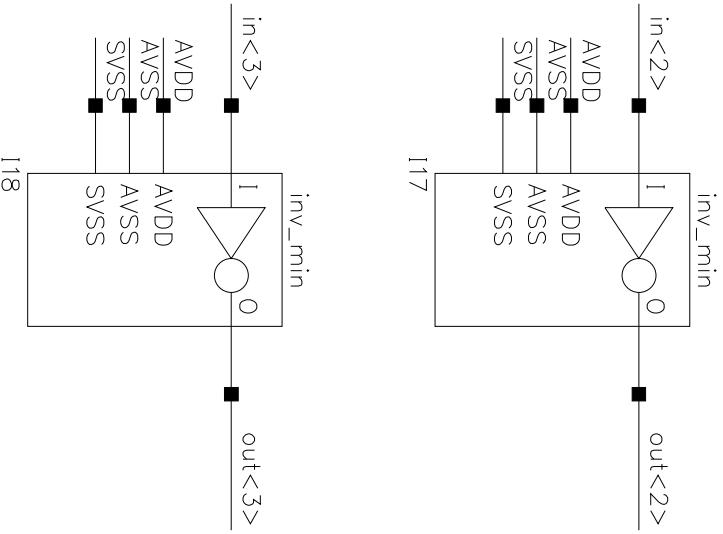
INV\_12

DRAWN  
CHECKED  
CHECKED  
ISSUED

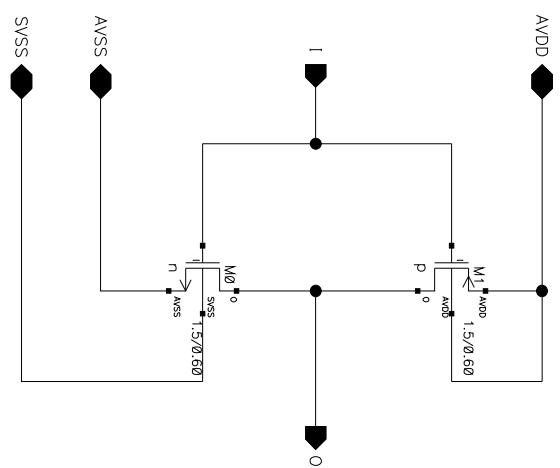
SIZE	CAGE NO.	DWG NO.	SCALE	SHEET
B				1 OF 1
REV				



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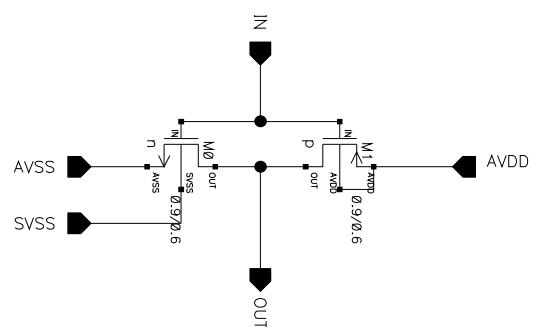


I18



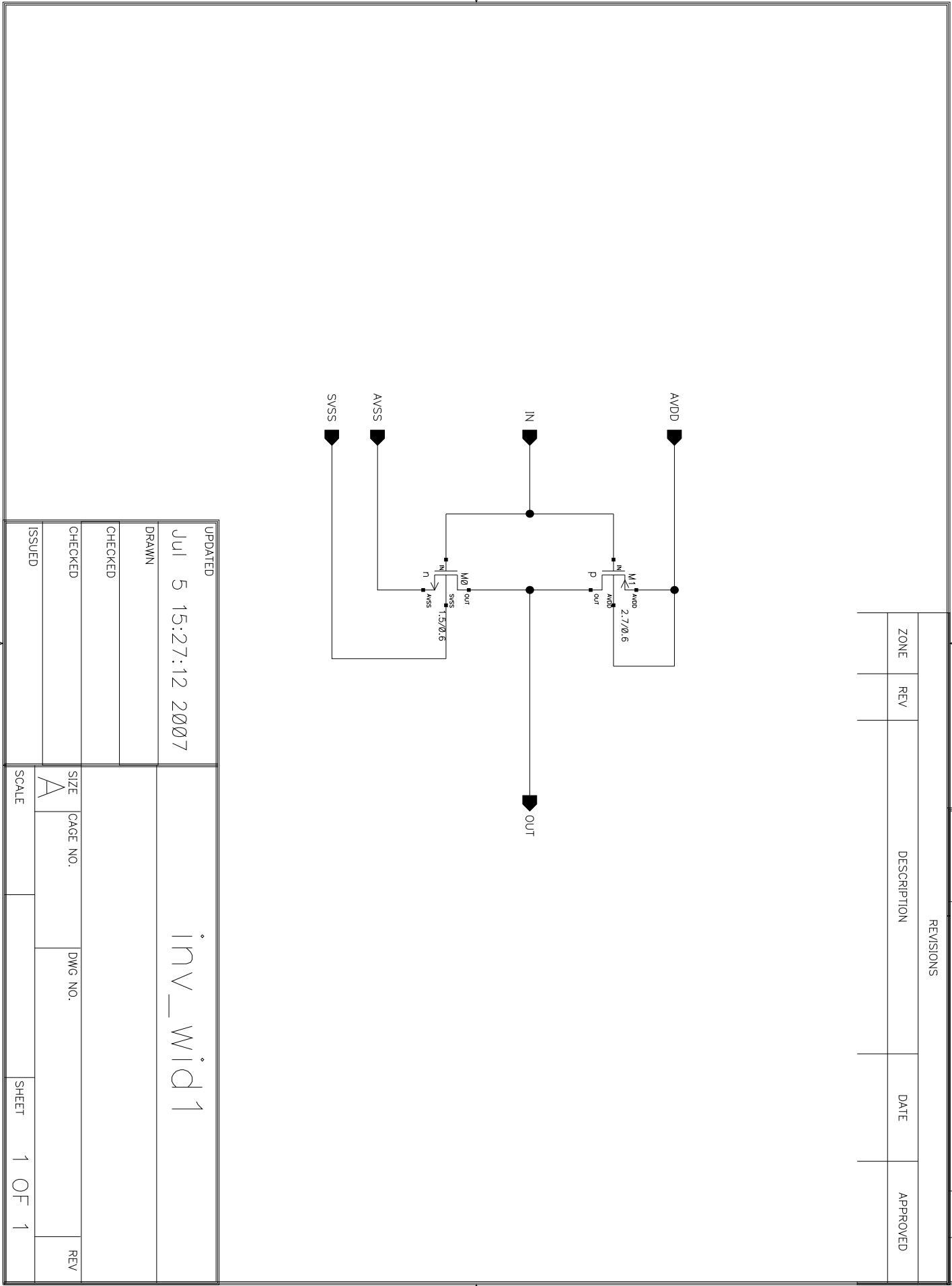
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SCALE			
REV			
		SHEET 1 OF 1	

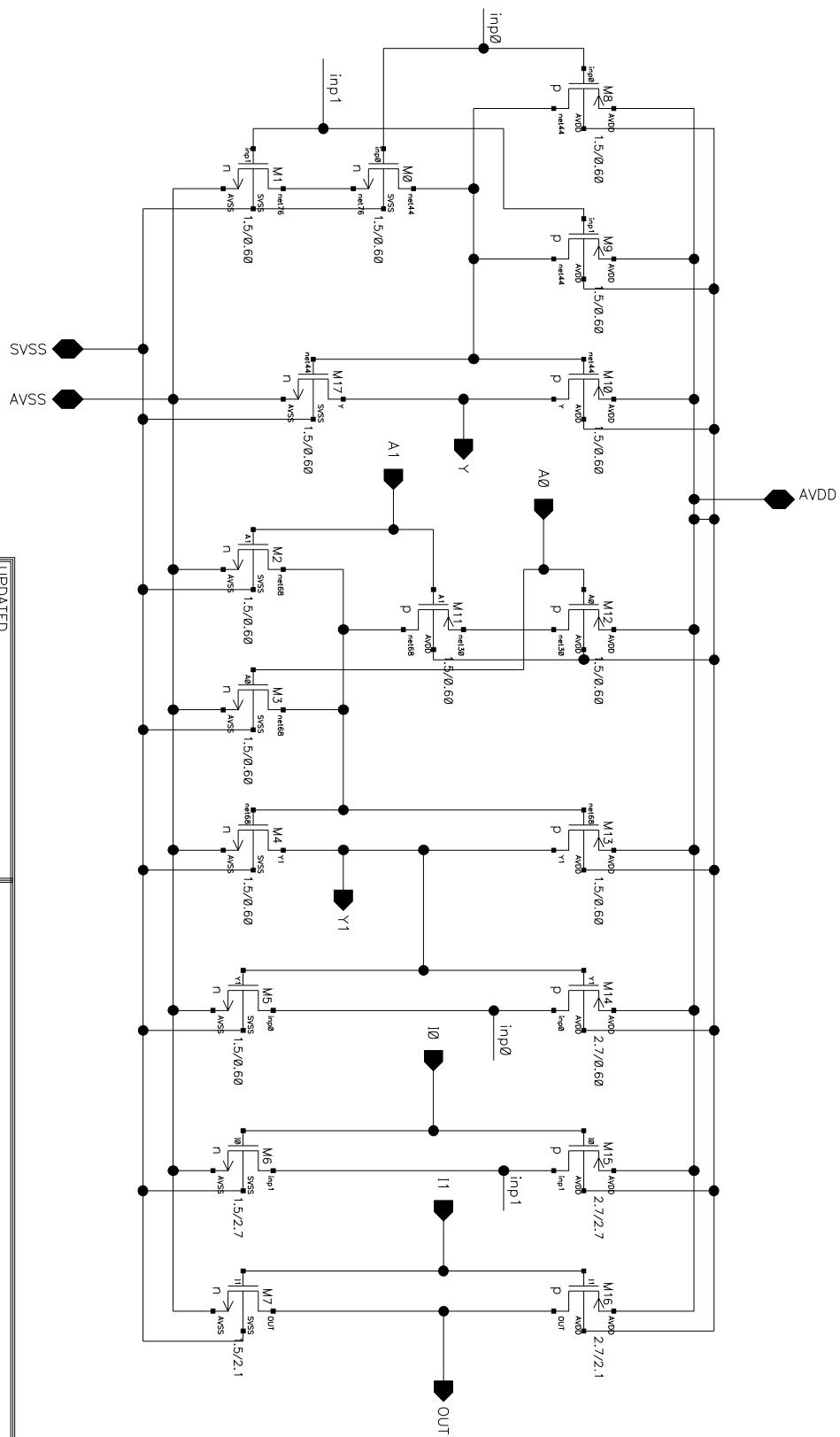
CAGE NO.	DWG NO.	REVISIONS	DATE	APPROVED



## inverter

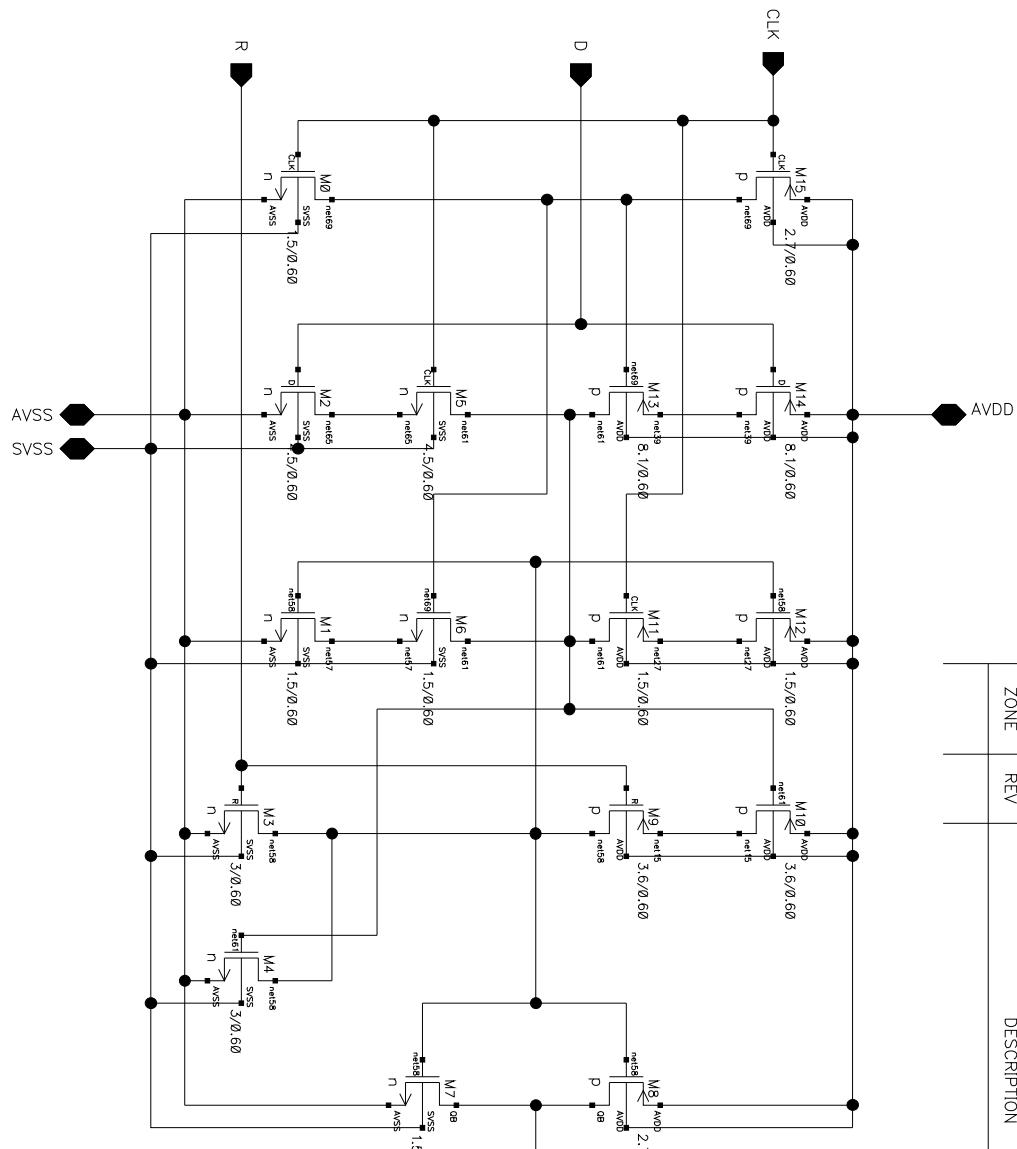
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CHECKED			
CHECKED			
ISSUED			
	SIZE A	CAGE NO.	DWG NO.
	SCALE		
			SHEET 1 OF 1 REV





REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

UPDATED			
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CHECKED	SIZE A	CAGE NO.	DWG NO.
ISSUED	SCALE		REV
		SHEET 1 OF 1	

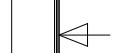


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ISSUED		
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		DWG NO.
		SHEET 1 OF 1
REV		

CAGE NO.	DWG NO.	REV	SH 1	REV
DESCRIPTION		DATE	REVISIONS	

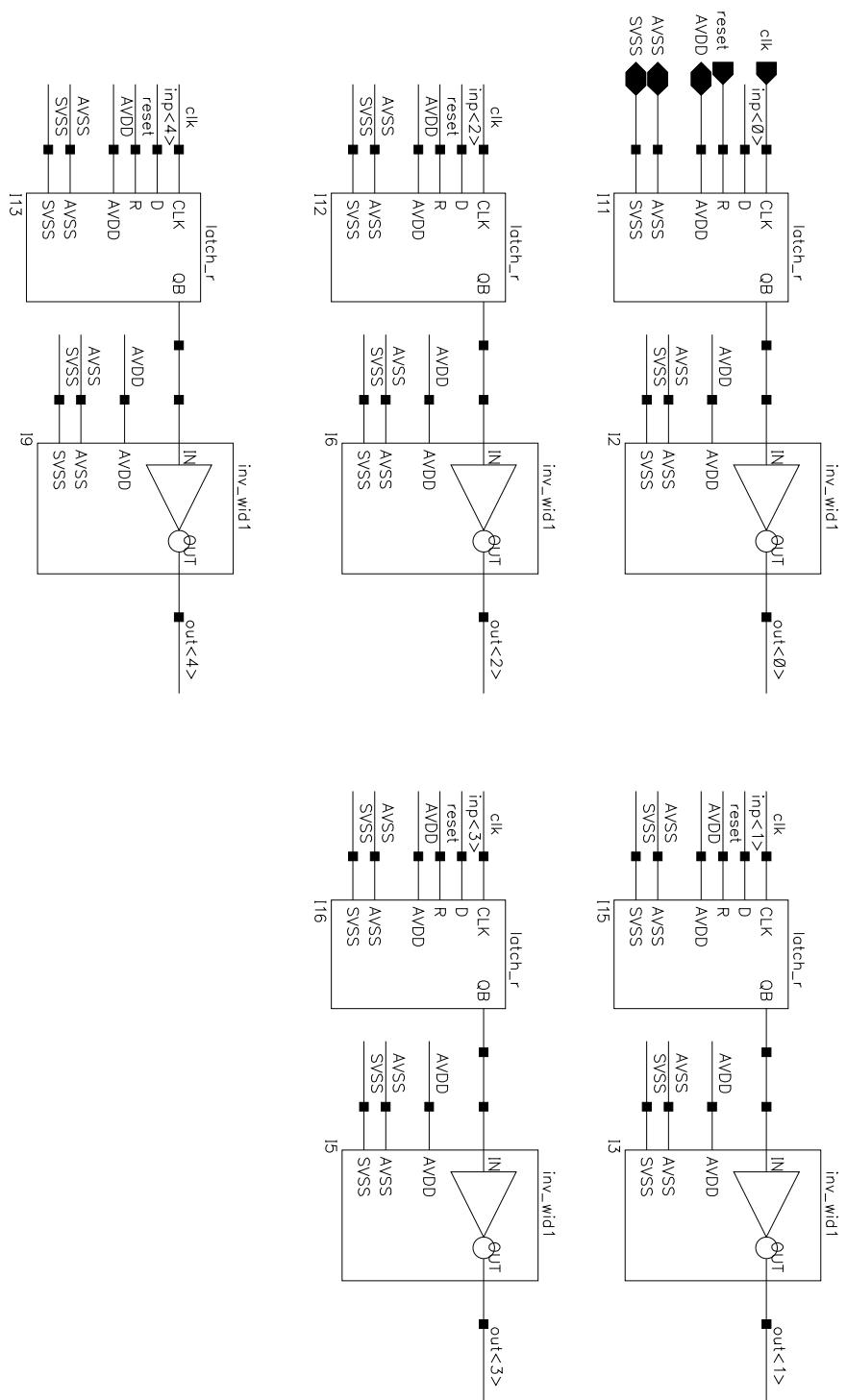
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out<4:0>



CAGE NO.	DWG NO.	SH 1	REV
ZONE	REV	DESCRIPTION	
		DATE	
			APPROVED

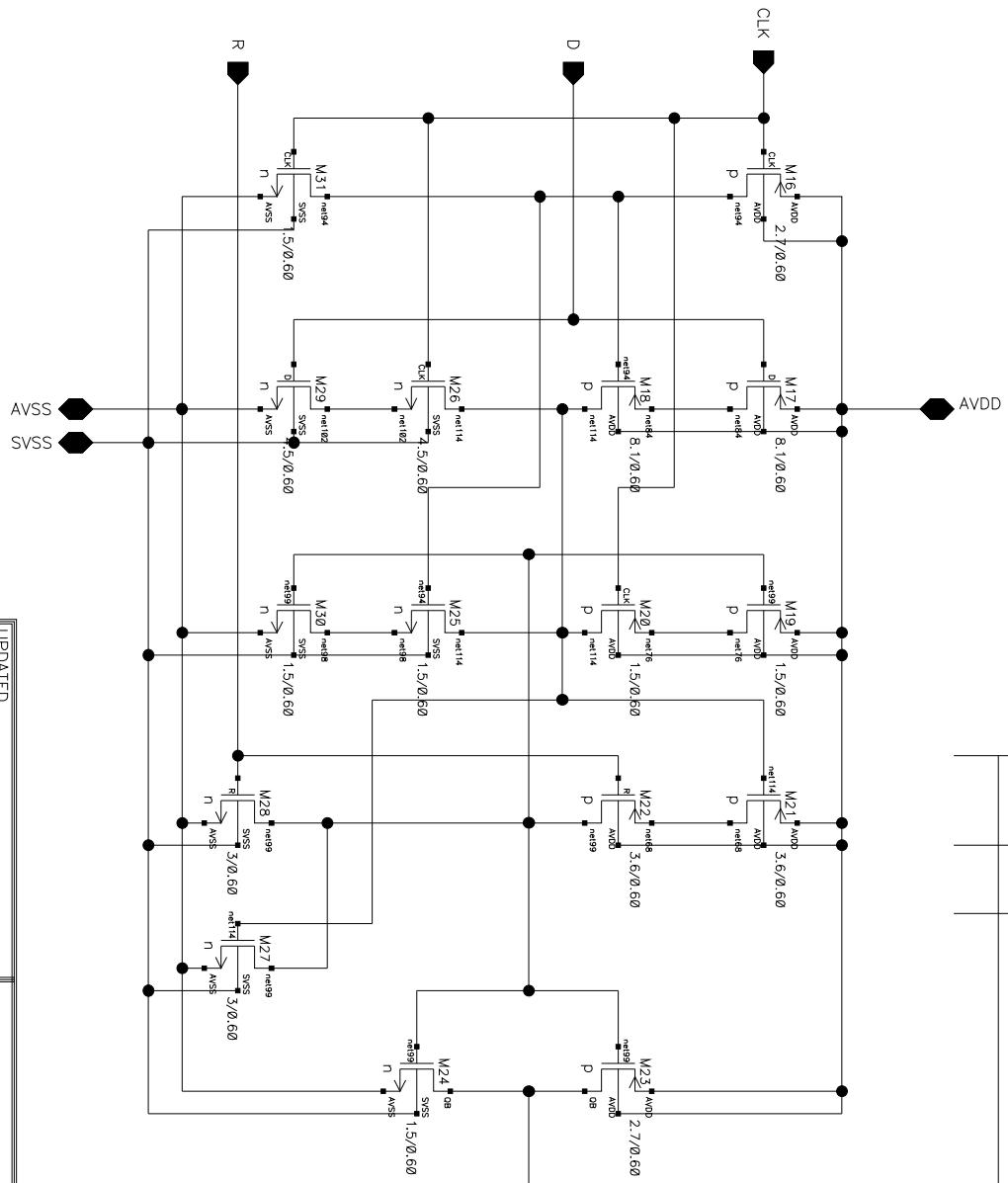
REVISIONS



UPDATED  
JUL 11 14:10:04 2007

## latch\_5bit

DRAWN	SIZE	CAGE NO.	DWG NO.
CHECKED	SCALE		
ISSUED			SHEET 1 OF 1
			REV



UPDATED

JUL 11 12:19:31 2007

latch\_r

DRAWN

CHECKED

CHECKED  
ISSUED

SCALE

SIZE

CAGE NO.

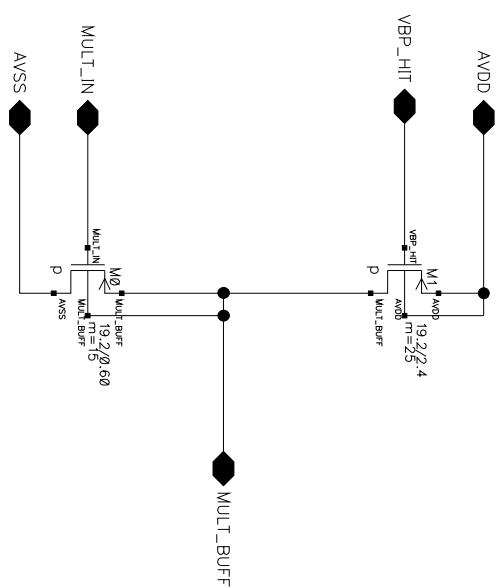
DWG NO.

SHEET

1 OF 1

REV

ZONE	REV	DESCRIPTION	DATE	APPROVED
			SH 1	REV



REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

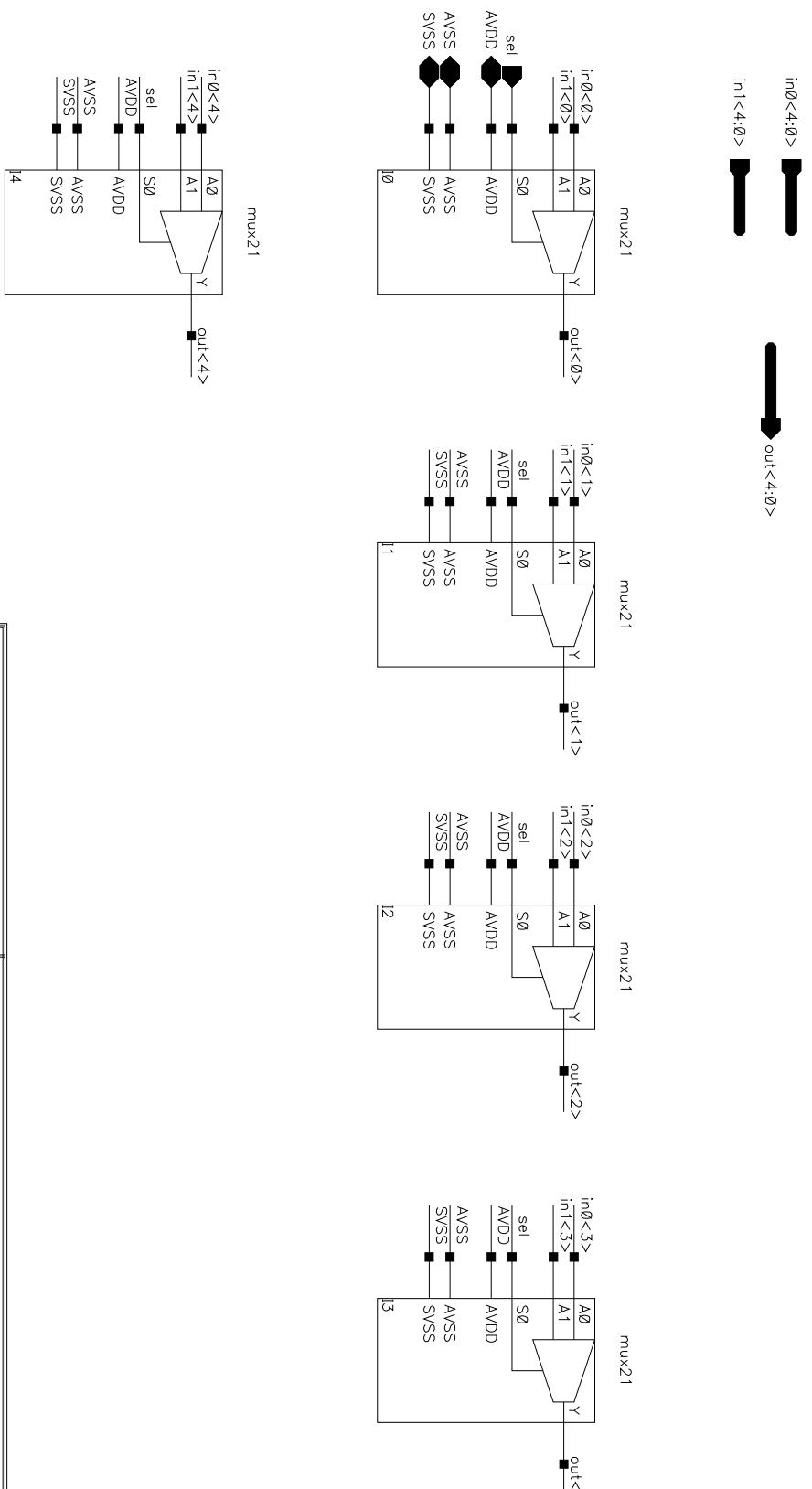
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CHECKED				
CHECKED				
ISSUED				
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	A			
	SCALE			
			SHEET 1 OF 1	

ZONE	REV	DESCRIPTION	DATE	APPROVED

CAGE NO. DWG NO. SH 1 REV

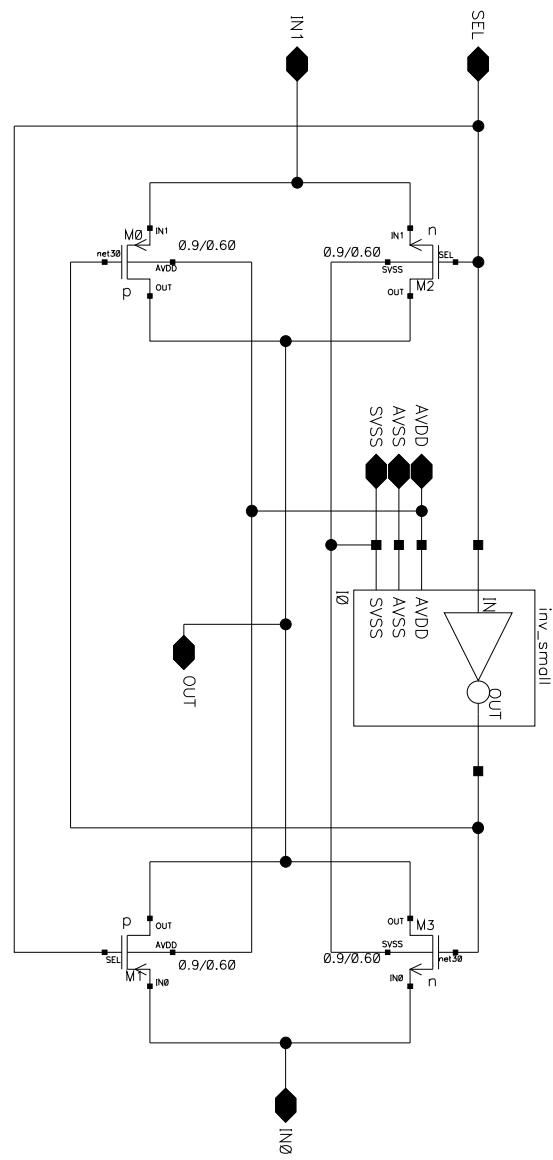
REVISIONS



UPDATED  
JUL 11 12:02:37 2007

MUX\_5bit

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ISSUED						

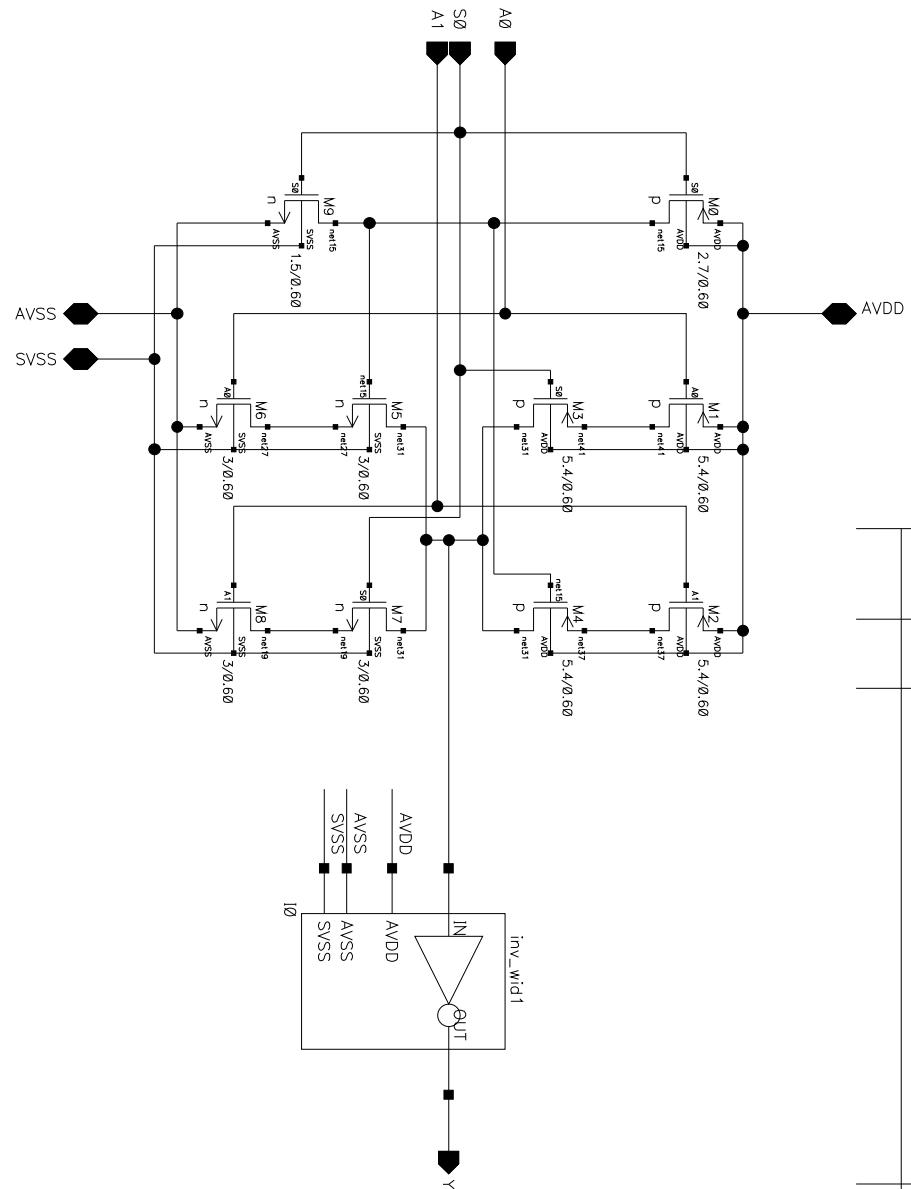


REVISIONS				SH 1	REV
ZONE	REV	DESCRIPTION	DATE	APPROVED	

$\mu_x - \min$

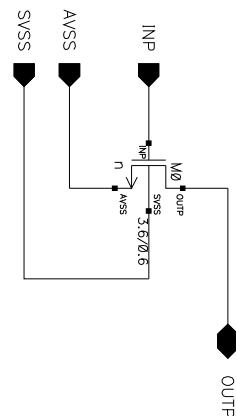
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ISSUED	

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ZONE	REV	DESCRIPTION		DATE	APPROVED



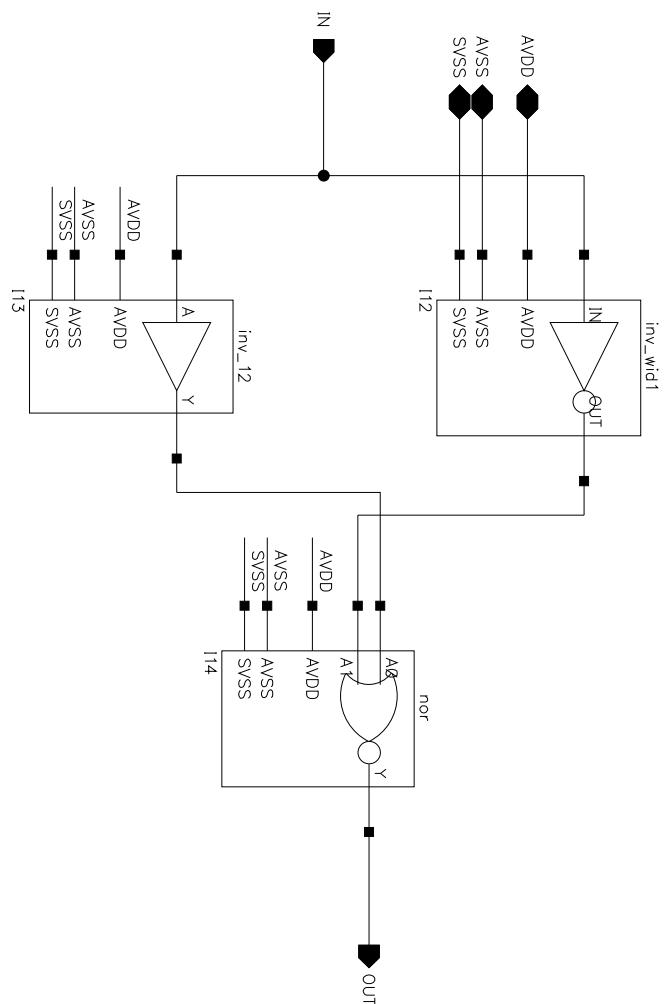
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CHECKED			
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SCALE			REV
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CAGE NO.	DWG NO.	REV
ZONE	REV	DESCRIPTION
		DATE
		APPROVED



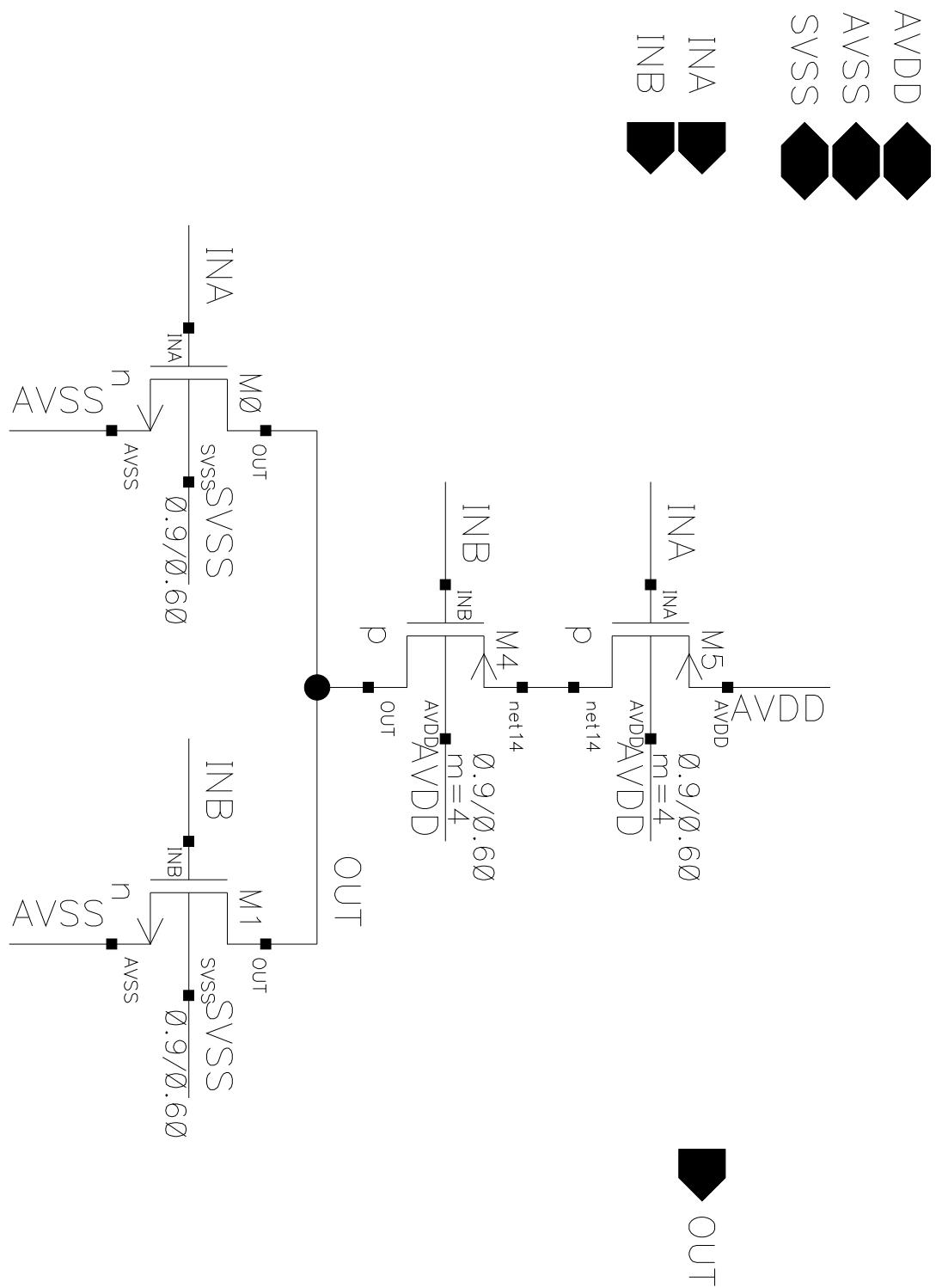
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CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO.
ISSUED	SCALE		SHEET 1 OF 1
			REV

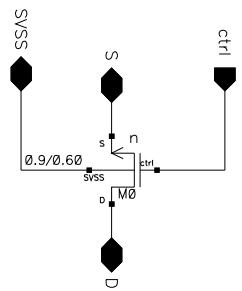
CAGE NO.		DWG NO.	REV	SH 1	REV A
ZONE	REV	DESCRIPTION		DATE	APPROVED



UPDATED	SIUE IC Design Lab		
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CHECKED			
ISSUED	SIZE A	CAGE NO.	DWG NO.
	SCALE		SHEET 1 OF 1

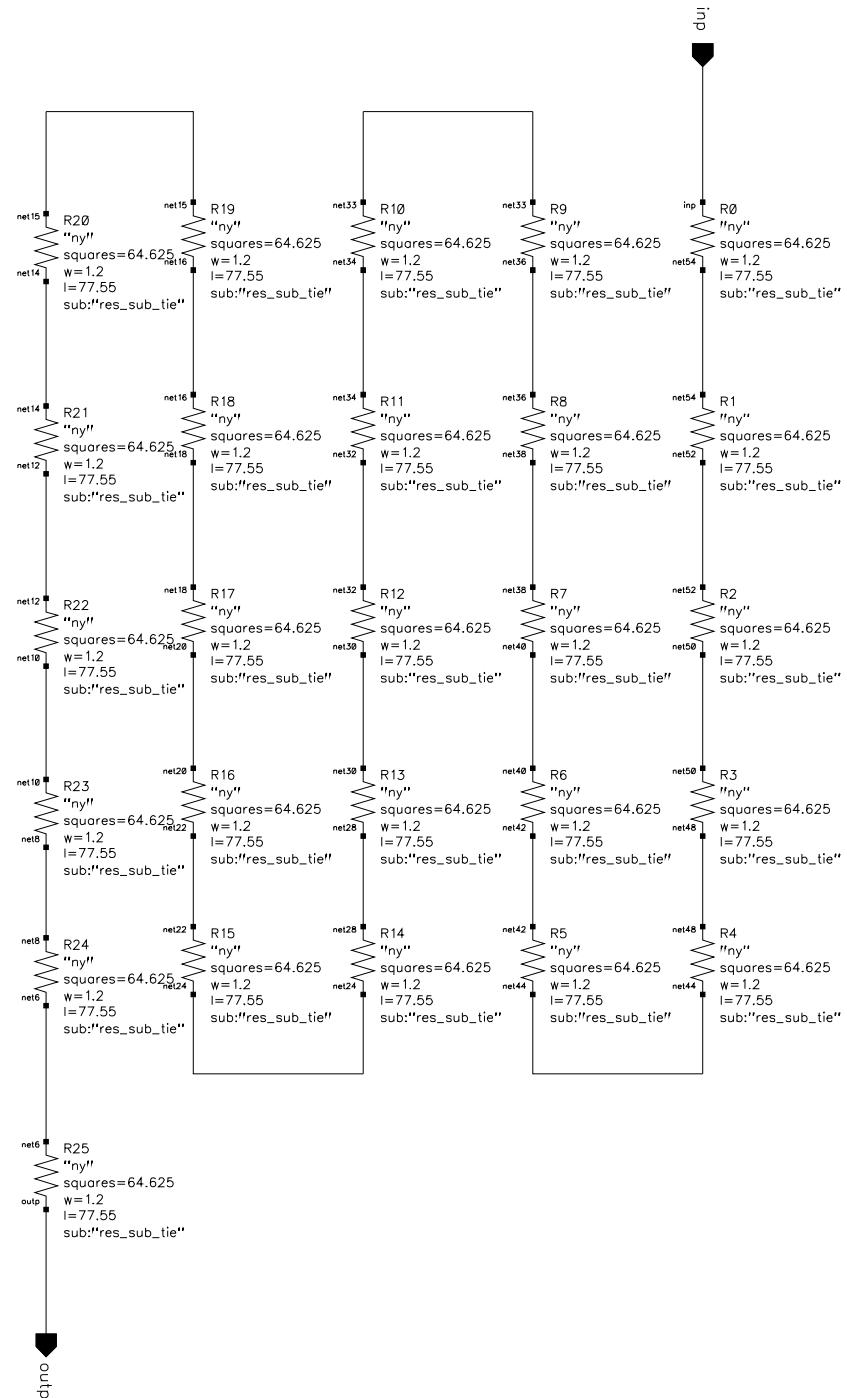






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CHECKED			
ISSUED	SIZE A	CAGE NO.	DWG NO.
	SCALE		SHEET 1 OF 1
			REV A

CAGE NO.	DWG NO.	REV		
		SH 1 A		
ZONE	REV	DESCRIPTION	DATE	APPROVED



ny\_res85k

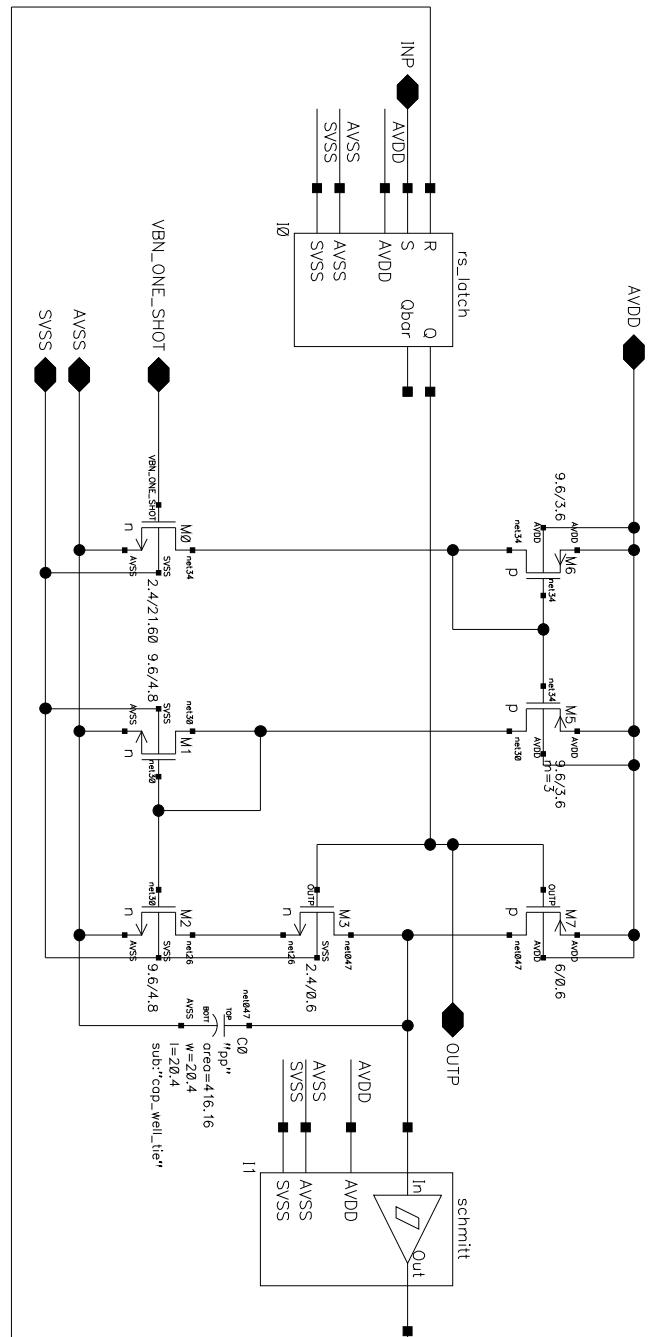
UPDATED

CHECKED

ISSUED

UPDATED	nY—res85k				
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CHECKED					
CHECKED					
ISSUED					
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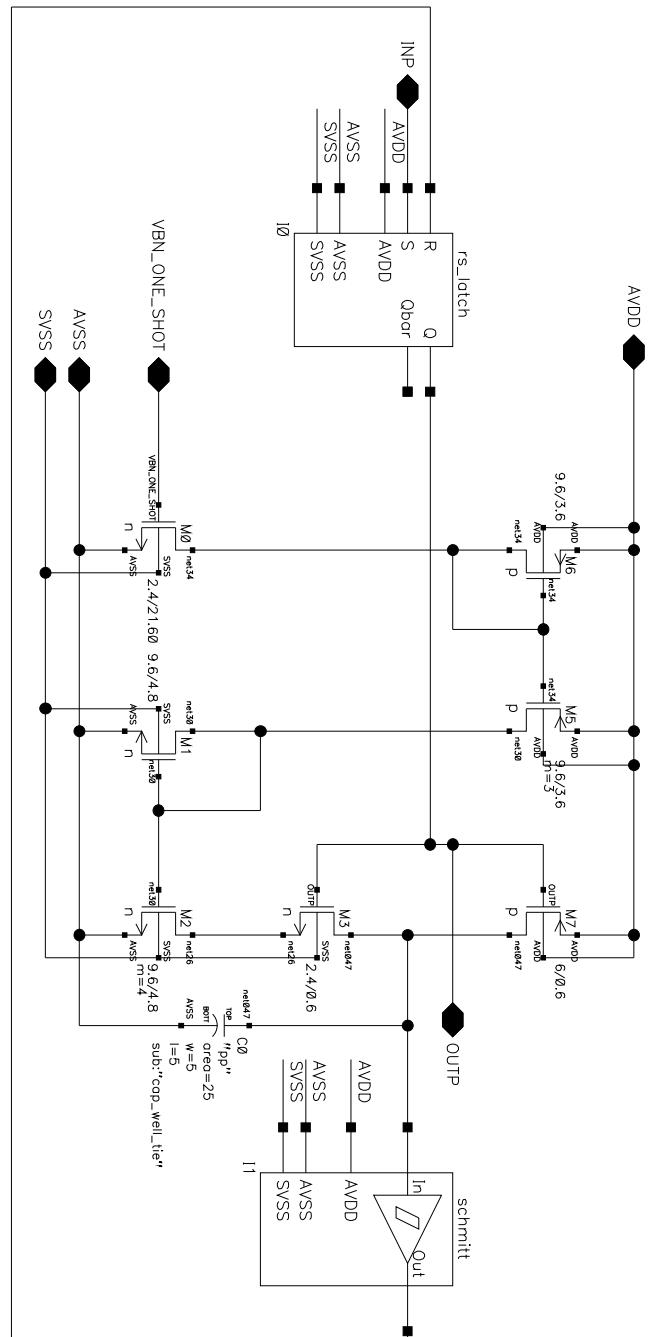
REVISIONS			
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			SH 1 REV



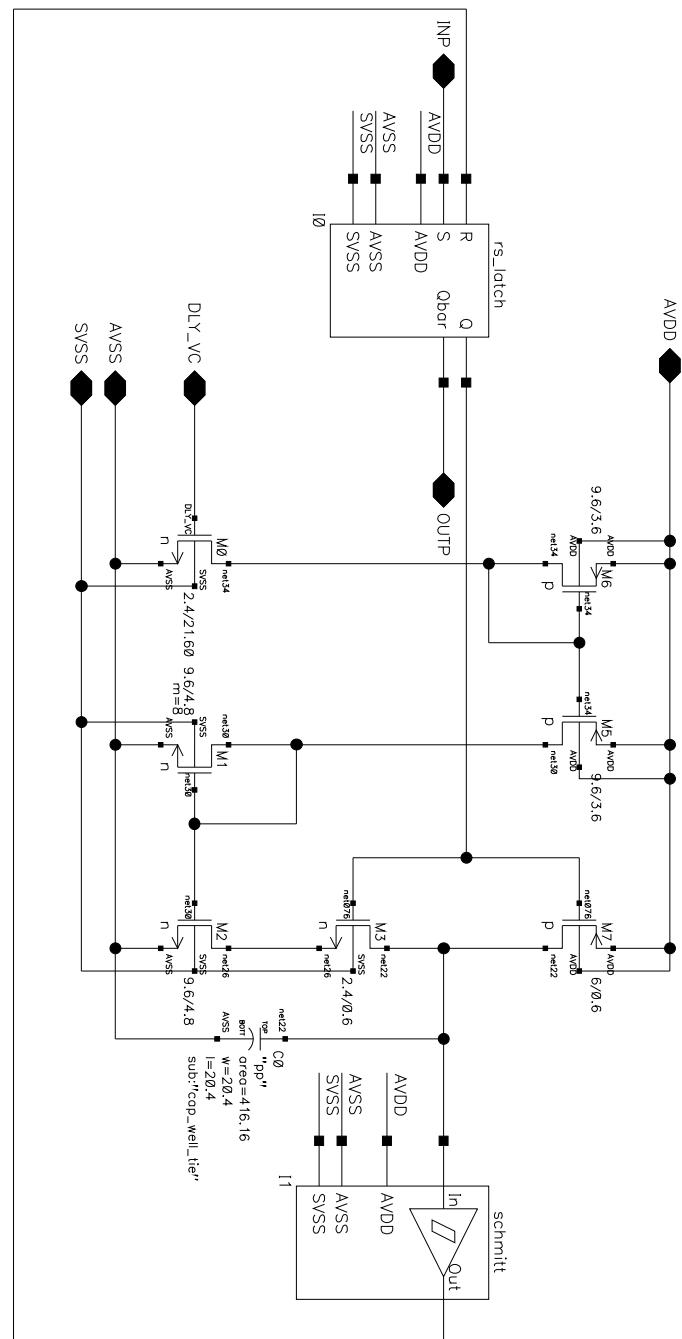
One\_Shot\_100ns

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ISSUED			
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	A		
	SCALE		
			SHEET 1 OF 1
			REV

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	One_Shot_100ns		
Aug 27 12:57:37 2007			
DRAWN			
CHECKED			
CHECKED	SIZE	CAGE NO.	DWG NO.
ISSUED	SCALE		SHEET 1 OF 1
	REV		



one-shot-vari.

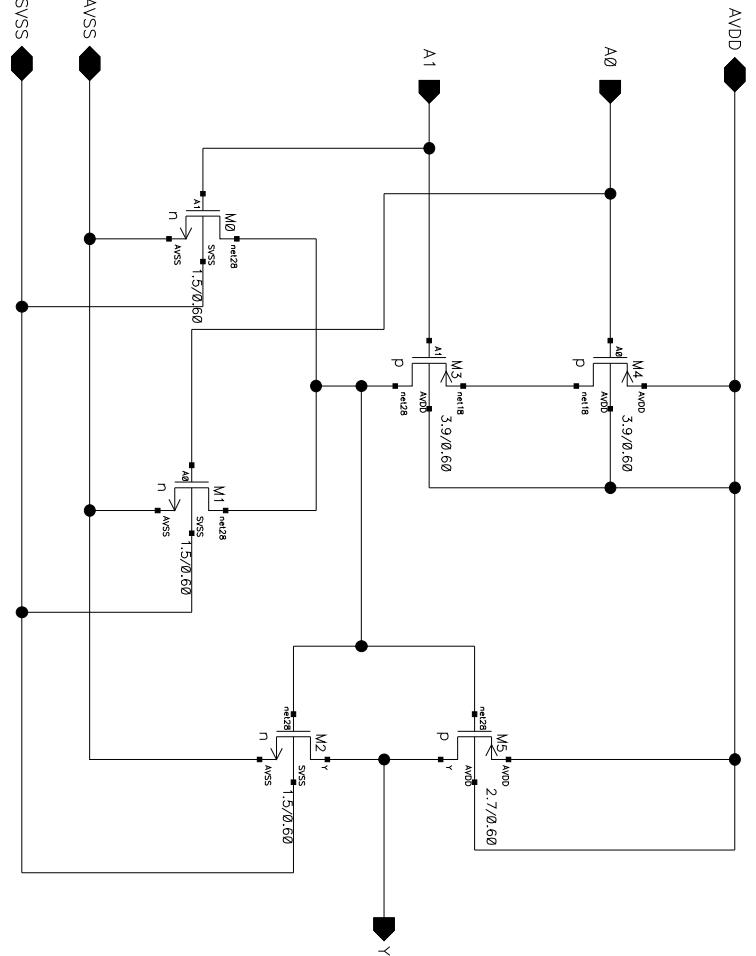
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UPDATED	Aug 14 10:41:49 2007
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CHECKED	
ISSUED	

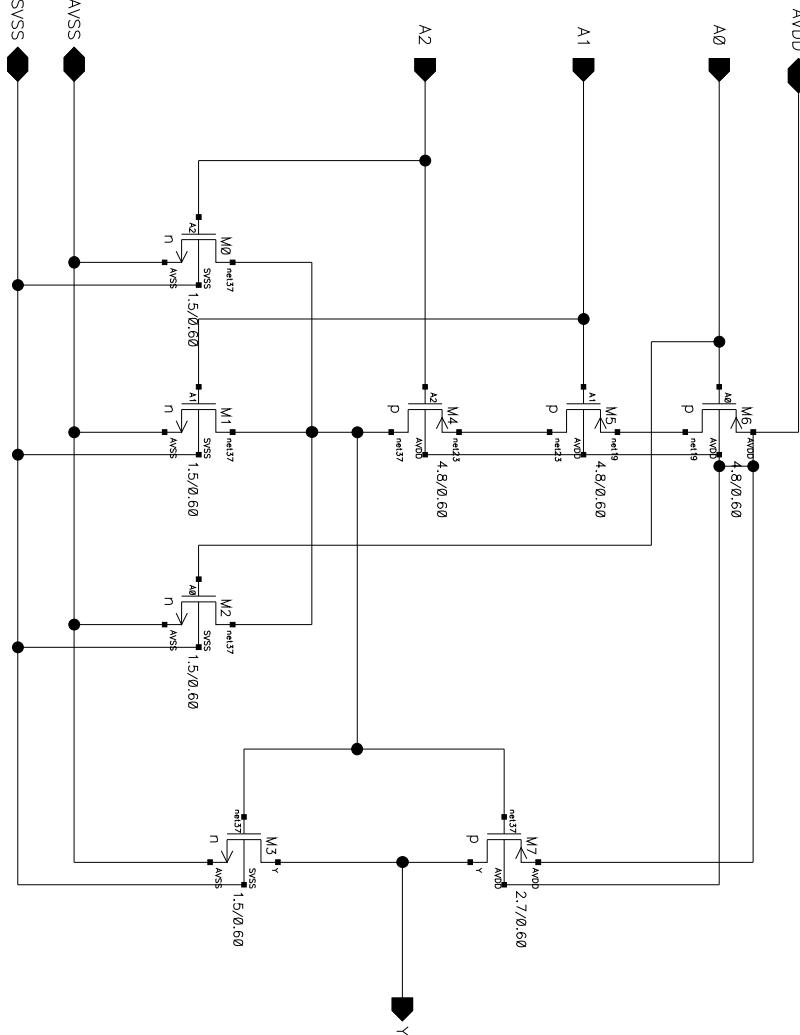
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REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

ZONE	REV	DESCRIPTION	DATE	APPROVED

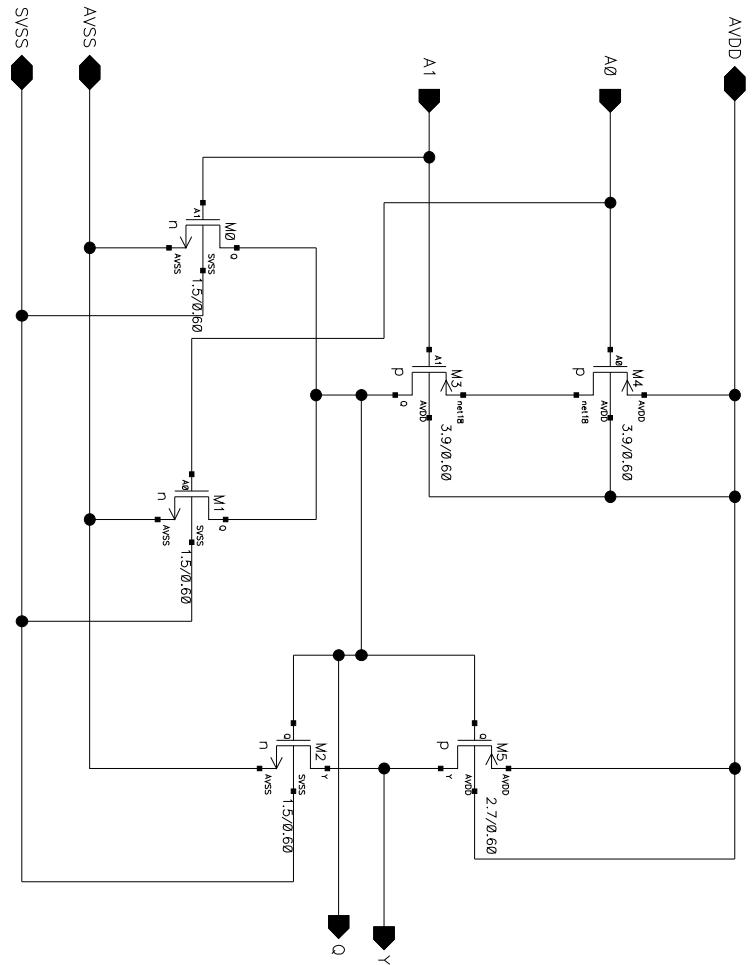


UPDATED	Jun 11 15:23:02 2007	○ ↵
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CHECKED		
ISSUED		
SIZE	CAGE NO.	DWG NO.
SCALE		
REV		
SHEET	1	OF 1



REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

UPDATED	Jun 11 15:46:50 2007		
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CHECKED			
ISSUED			
	SIZE A	CAGE NO.	DWG NO.
	SCALE		
			SHEET 1 OF 1 REV

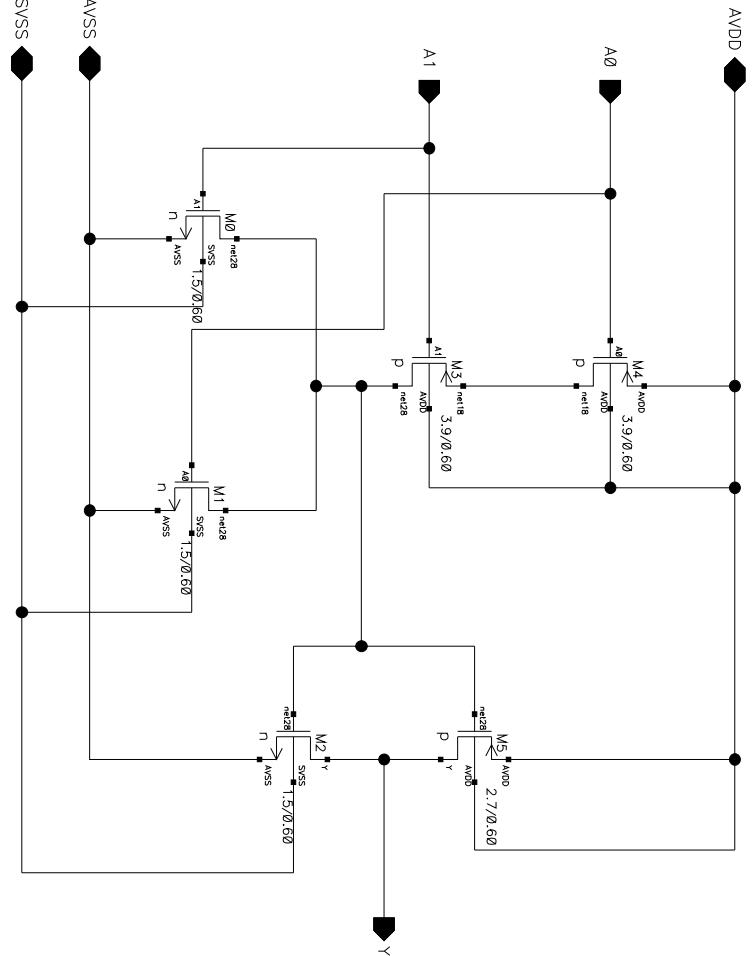


REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED

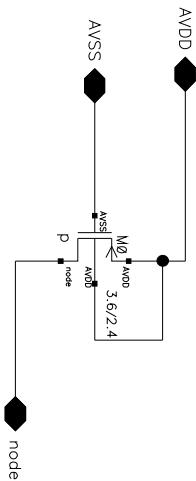
or-scratch

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ISSUED				
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ZONE	REV	DESCRIPTION	DATE	APPROVED



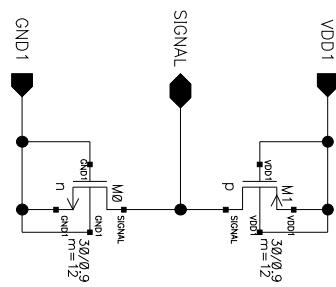
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CHECKED		
ISSUED		
SIZE	CAGE NO.	DWG NO.
SCALE		
REV		
	SHEET	1 OF 1



UPDATED	P_fet		
Aug 3 14:33:16 2007			
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CHECKED			
ISSUED	SIZE A	CAGE NO.	DWG NO.
	SCALE		SHEET 1 OF 1
			REV

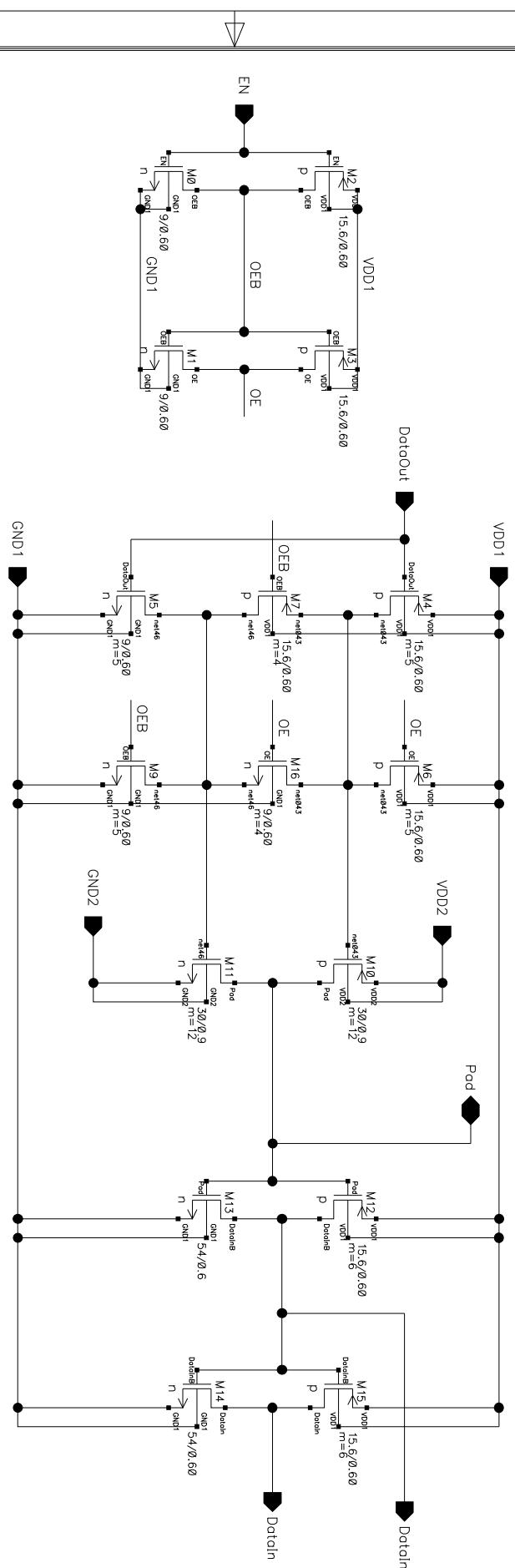
CAGE NO.	DWG NO.	SH 1	REV
ZONE	REV	DESCRIPTION	
		DATE	APPROVED

CAGE NO.		DWG NO.	REV	SH 1
ZONE	REV	DESCRIPTION		APPROVED
				DATE

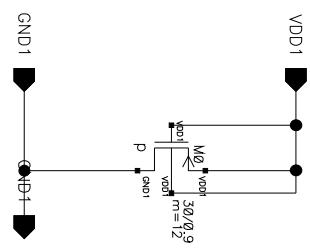


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	A		
	SCALE		
		SHEET	1 OF 1
		REV	

ZONE	REV	DESCRIPTION	DATE	APPROVED
			SH 1	REV



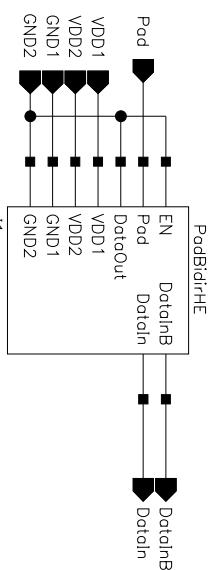
UPDATED	PadBiDirHE		
Jul 9 16:28:29 2003			
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ISSUED			
SIZE	CAGE NO.	DWG NO.	SHEET 1 OF 1
A			REV
SCALE			



REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

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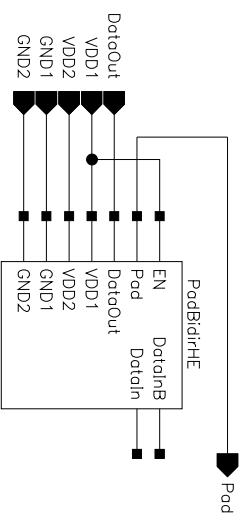
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CHECKED					
CHECKED					
ISSUED					
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	A				
	SCALE			SHEET	1 OF 1



11

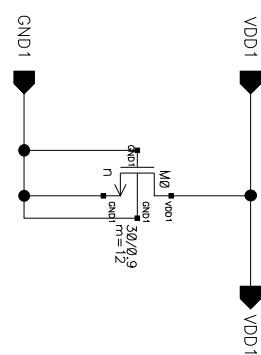
CAGE NO.		DWG NO.	REV	SH 1	REV
ZONE	REV	DESCRIPTION		DATE	APPROVED

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DRAWN					
CHECKED					
ISSUED					
	SIZE A	CAGE NO.	DWG NO.	SHEET 1 OF 1	REV
	SCALE				



UPDATED	PadOut		
JUL 9 16:11:11 2003			
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CHECKED			
CHECKED			
ISSUED			

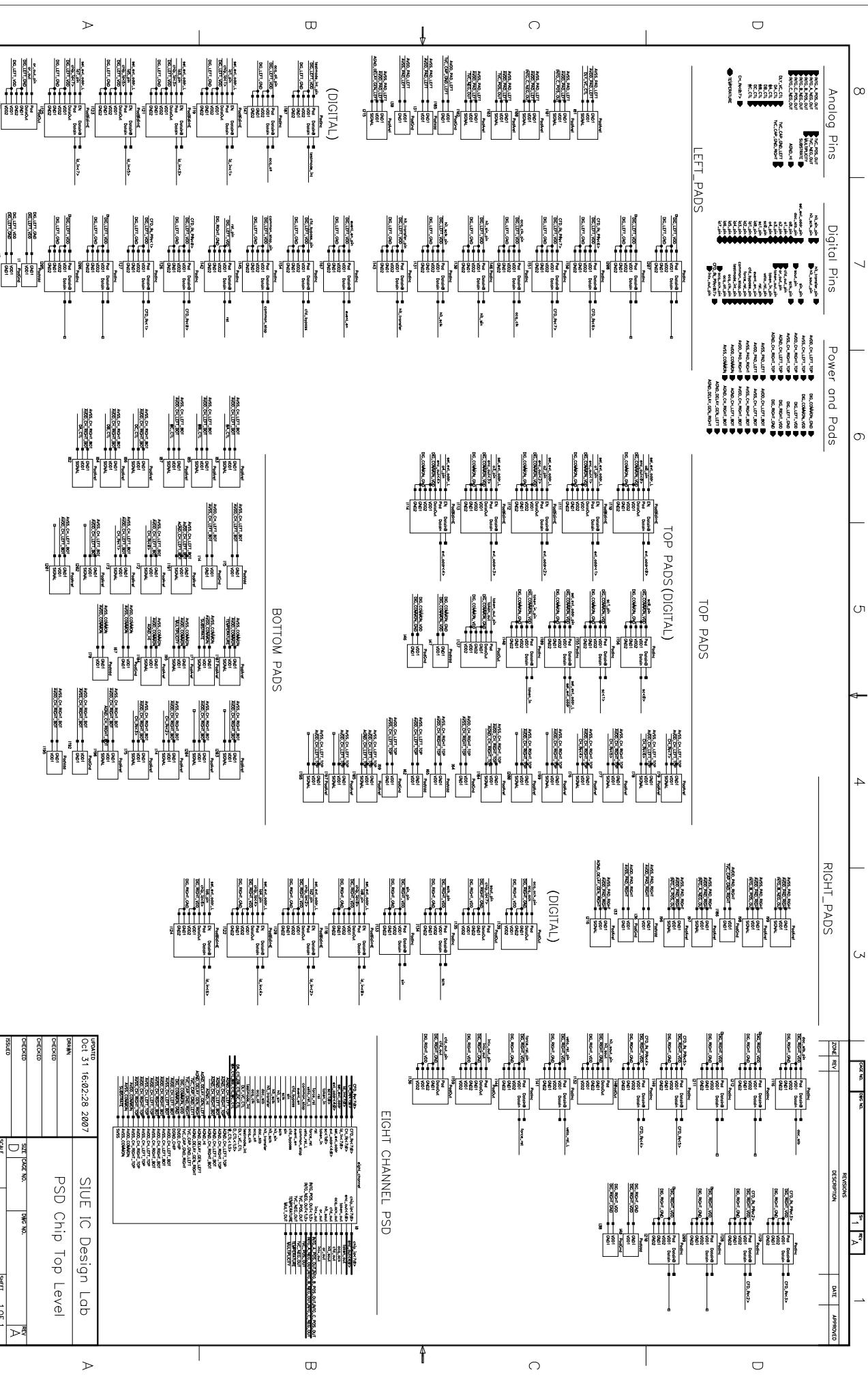
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ZONE	REV	DESCRIPTION	
		DATE	APPROVED

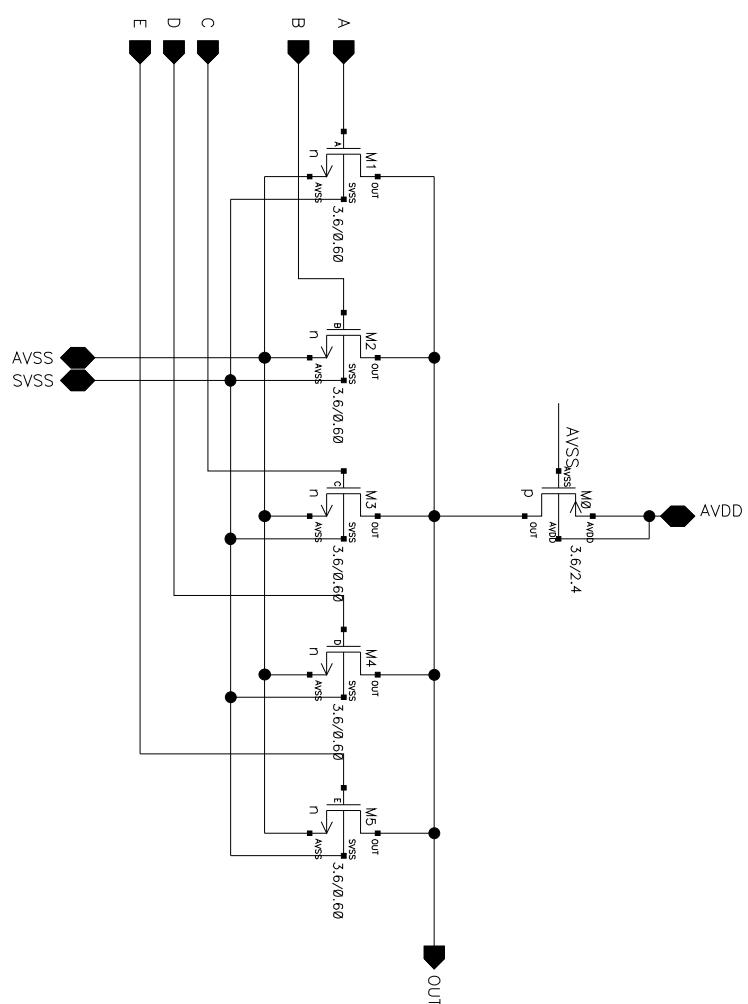


REVISIONS				SH 1	REV
ZONE	REV	DESCRIPTION	DATE	APPROVED	

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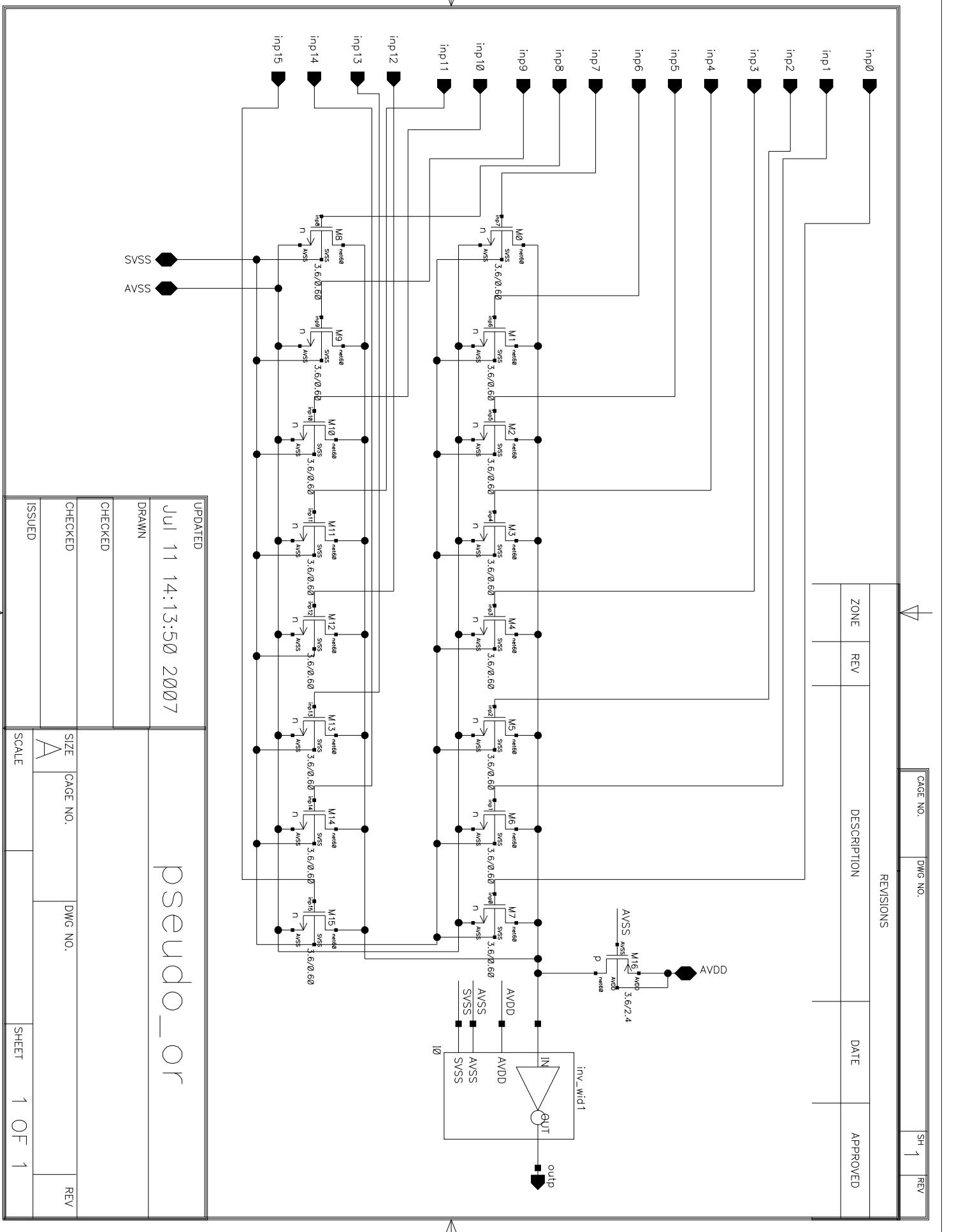
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CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED				
			SHEET 1 OF 1	

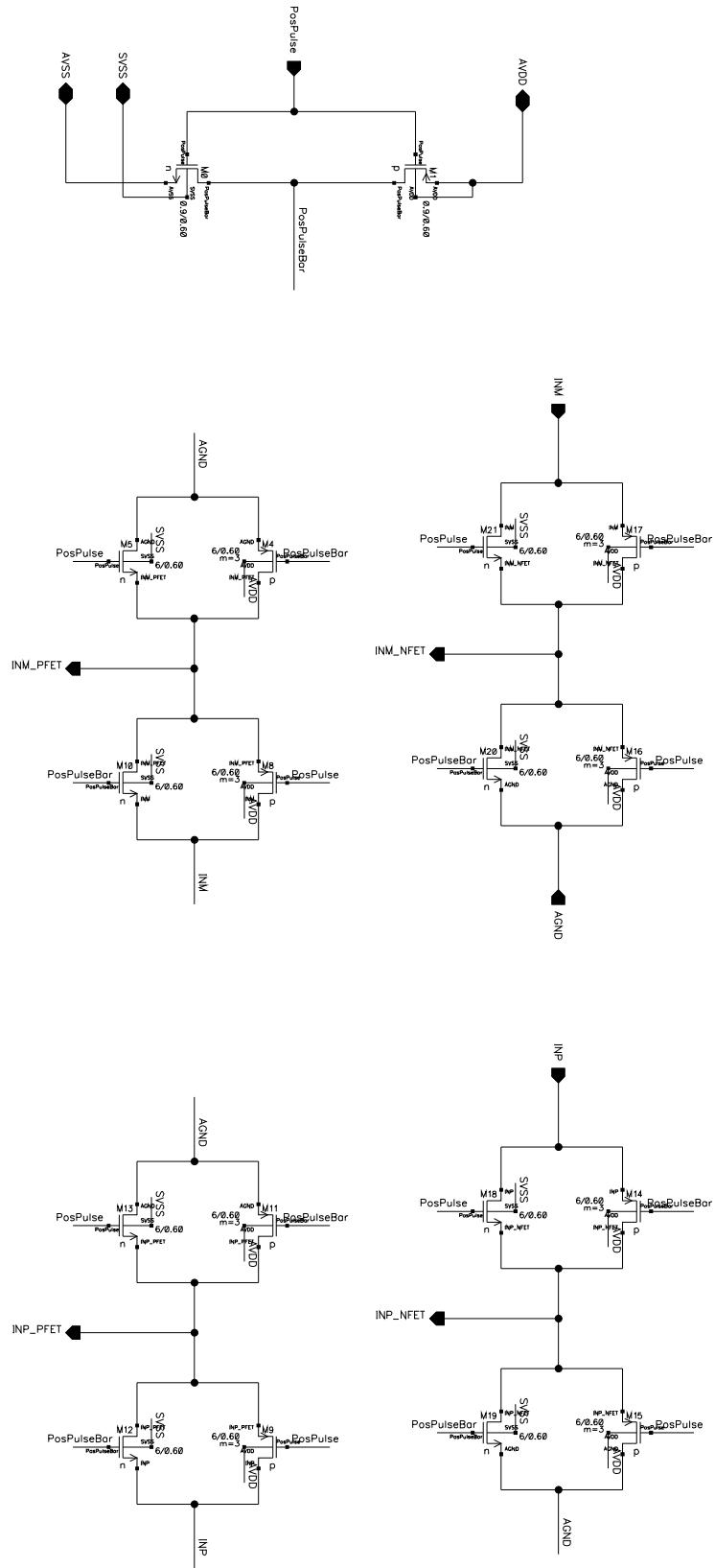




			
CAGE NO.	DWG NO.	SH 1	REV
ZONE	REV	DESCRIPTION	DATE
			APPROVED

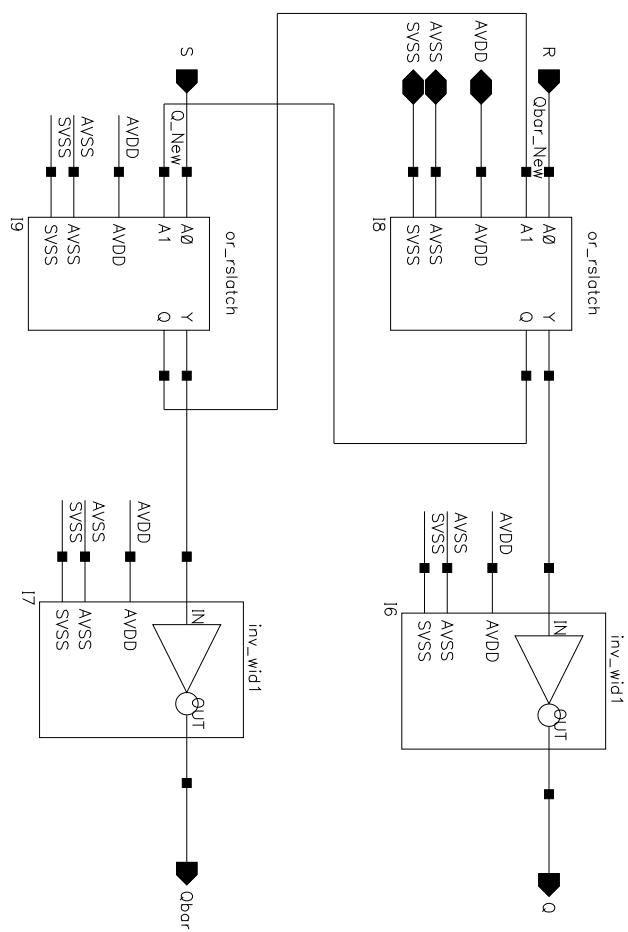
UPDATED	Jul 11 13:37:50 2007											
DRAWN												
CHECKED												
CHECKED												
ISSUED	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20%; text-align: center;">SIZE</td> <td style="width: 60%; text-align: center;">CAGE NO.</td> <td style="width: 20%; text-align: center;">DWG NO.</td> </tr> <tr> <td style="text-align: center;">A</td> <td></td> <td></td> </tr> <tr> <td style="text-align: center;">SCALE</td> <td></td> <td></td> </tr> </table>			SIZE	CAGE NO.	DWG NO.	A			SCALE		
SIZE	CAGE NO.	DWG NO.										
A												
SCALE												
		SHEET	1 OF 1									
		REV										





CAGE NO.		DWG NO.		REV	DESCRIPTION	DATE	APPROVED
ZONE	REV	SHEET	REV				
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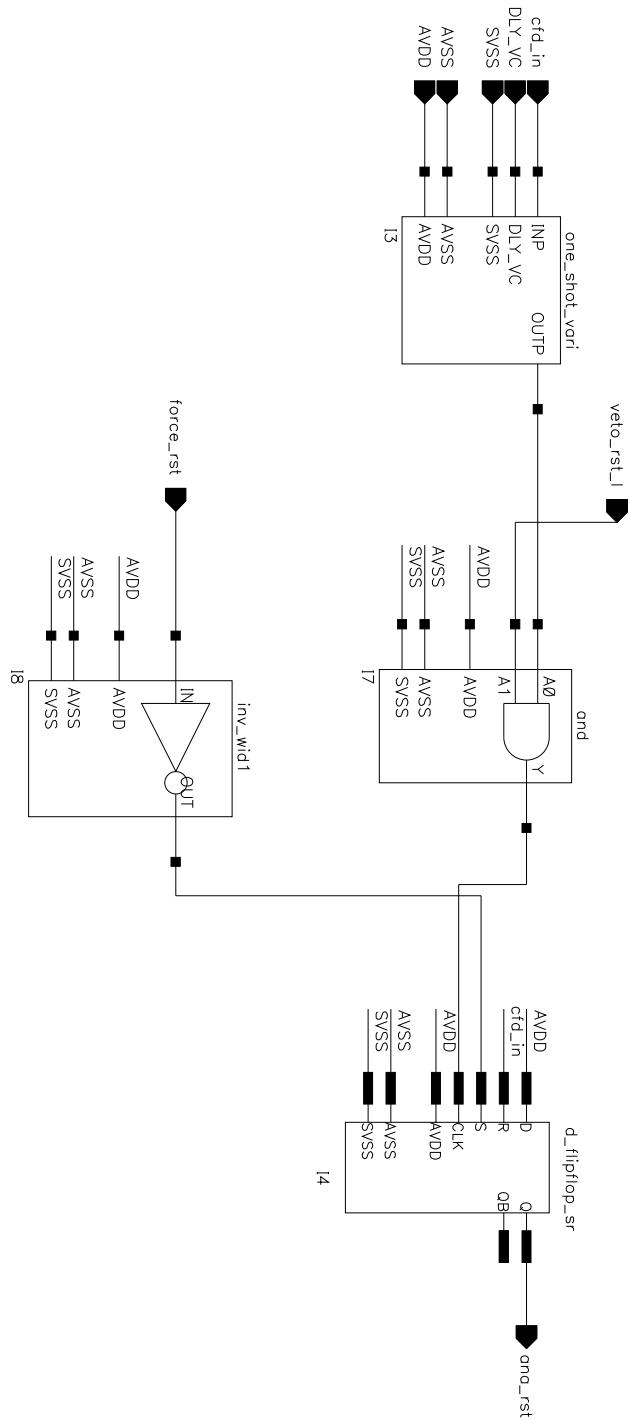
UPDATED	
Aug 7 16:55:04 2007	
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CHECKED	
ISSUED	
SCALE	
B	
SIZE	
CAGE NO.	
DWG NO.	
REV	
SHEET	
1 OF 1	



REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

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UPDATED	rsatch			
DRAWN				
CHECKED				
CHECKED				
ISSUED				
	SIZE A	CAGE NO.	DWG NO.	REV
	SCALE			SHEET 1 OF 1



REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV A

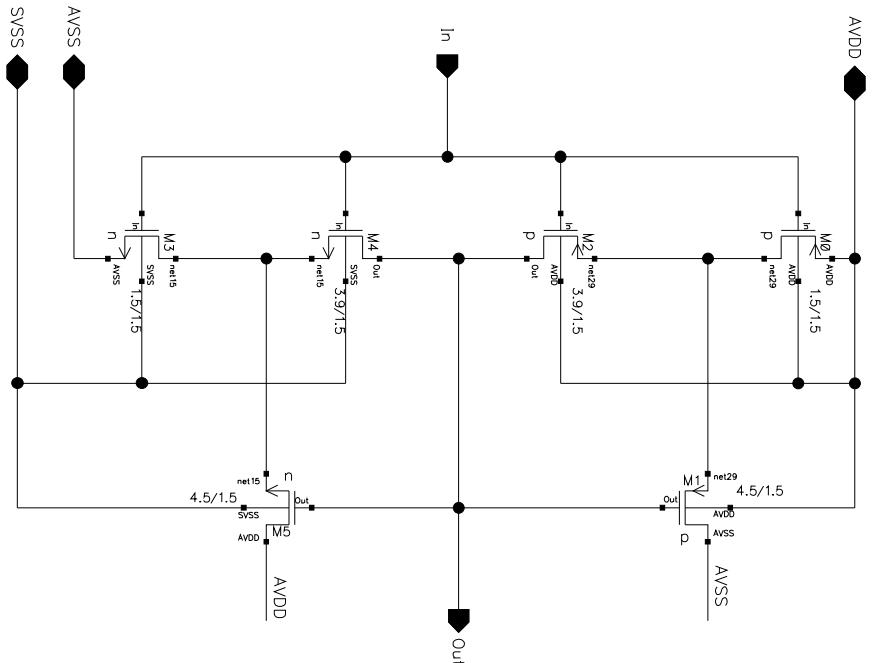
# SU EIC Design Lab

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## Reset Logic

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CHECKED	SIZE A SCALE	CASE NO.	DWG NO.
ISSUED			

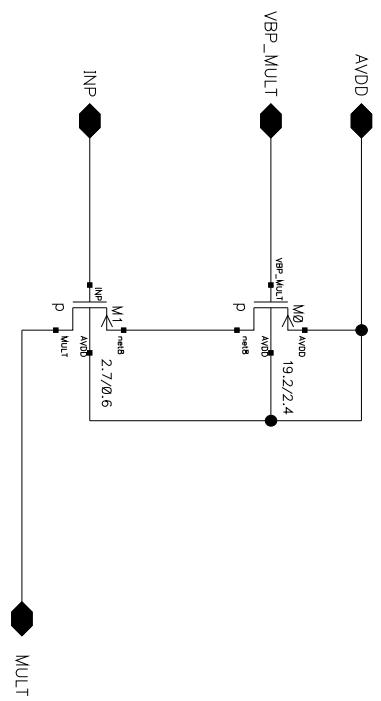
CAGE NO.	DWG NO.	REV	SH 1	REV
DESCRIPTION		DATE	APPROVED	



UPDATED  
Aug 13 11:29:31 2007

SCHMITT

DRAWN	SIZE	CAGE NO.	DWG NO.	REV
CHECKED				
ISSUED	SCALE			
			SHEET 1 OF 1	

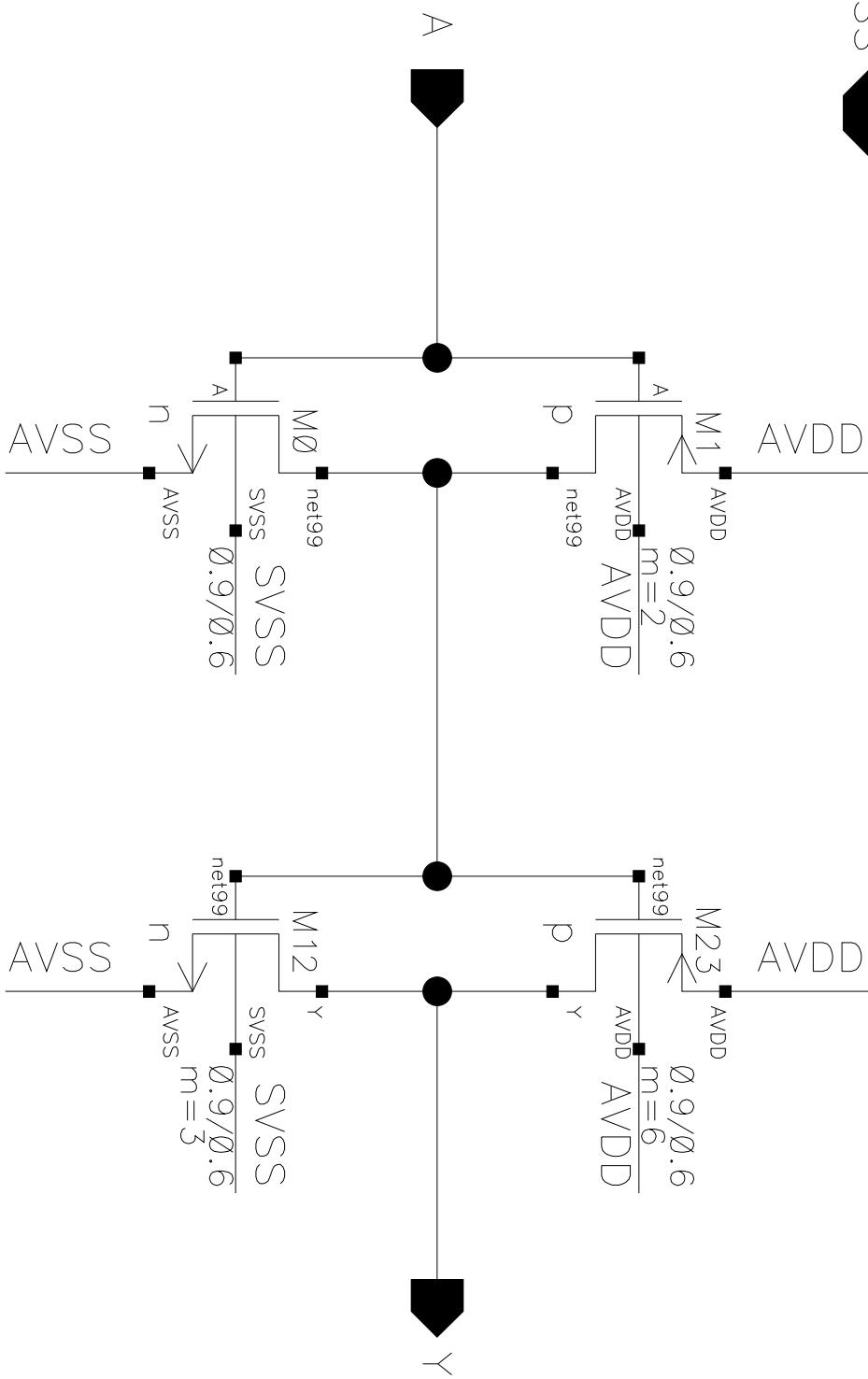
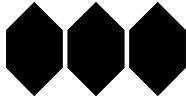


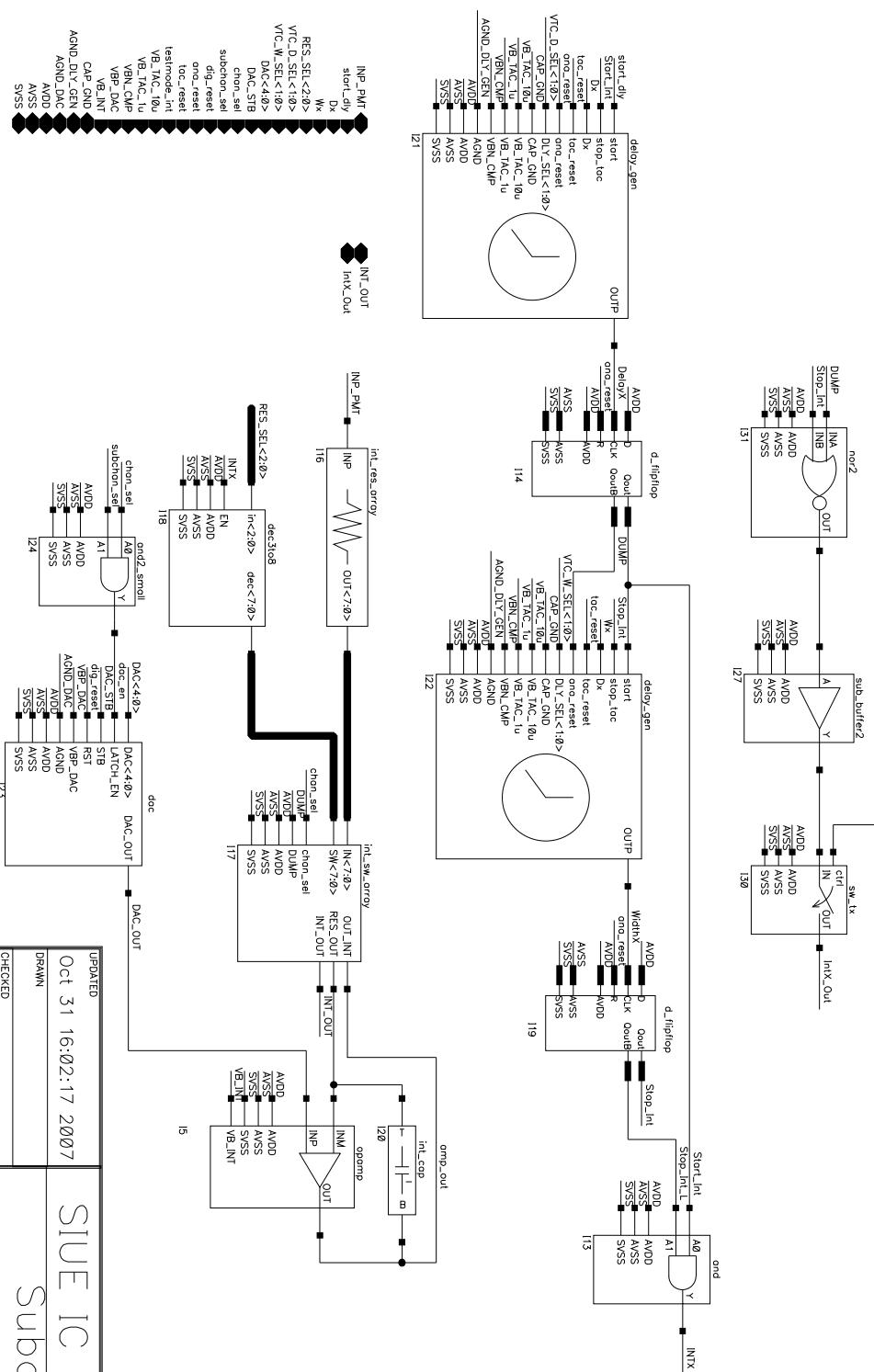
REVISIONS				REV
ZONE	REV	DESCRIPTION	DATE	APPROVED

## single\_mult

UPDATED	Jun 15 15:32:45 2007			
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CHECKED				
CHECKED				
ISSUED				
	SIZE A SCALE	CAGE NO.	DWG NO.	REV

AVDD  
AVSS  
SVSS

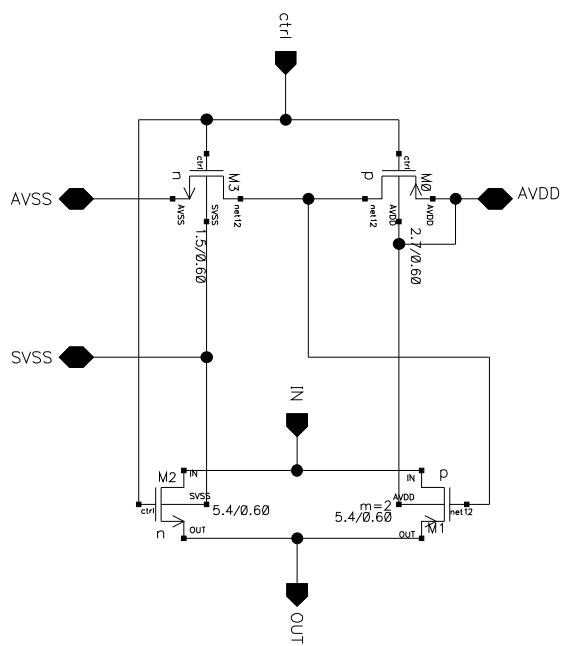




CASE NO.	DRG NO.	SH 1	REV A
ZONE	REV	DESCRIPTION	REVISIONS
			DATE

SIUE IC Design Lab  
Subchannel

Subchannel JE IC Design Lab

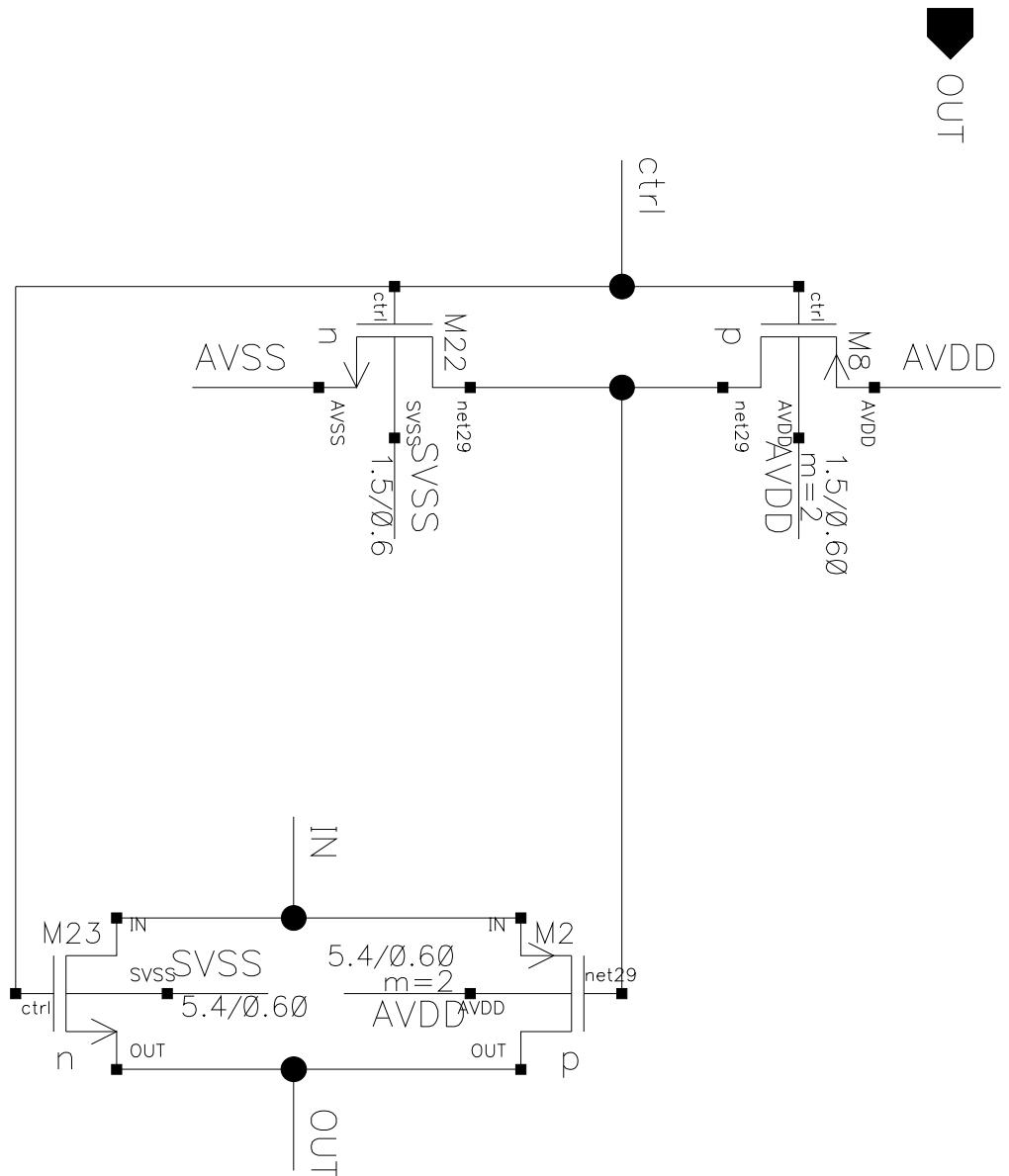
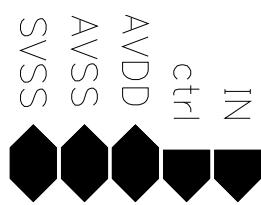


REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

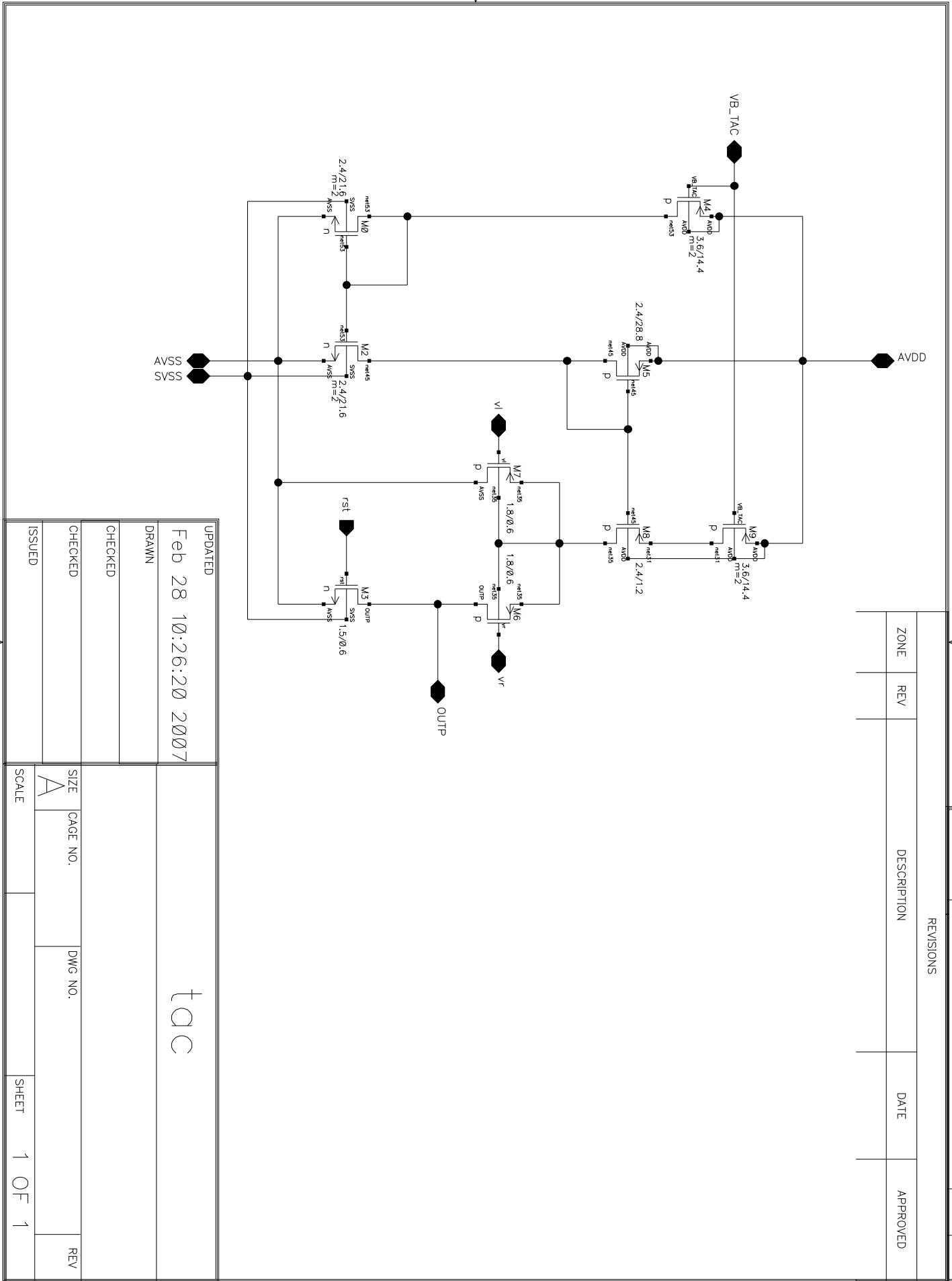
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Aug 13 15:55:31 2007

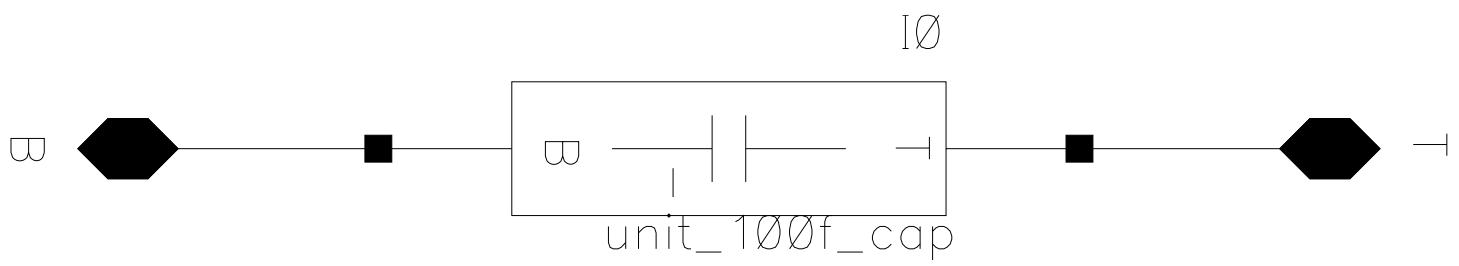
sw\_channel

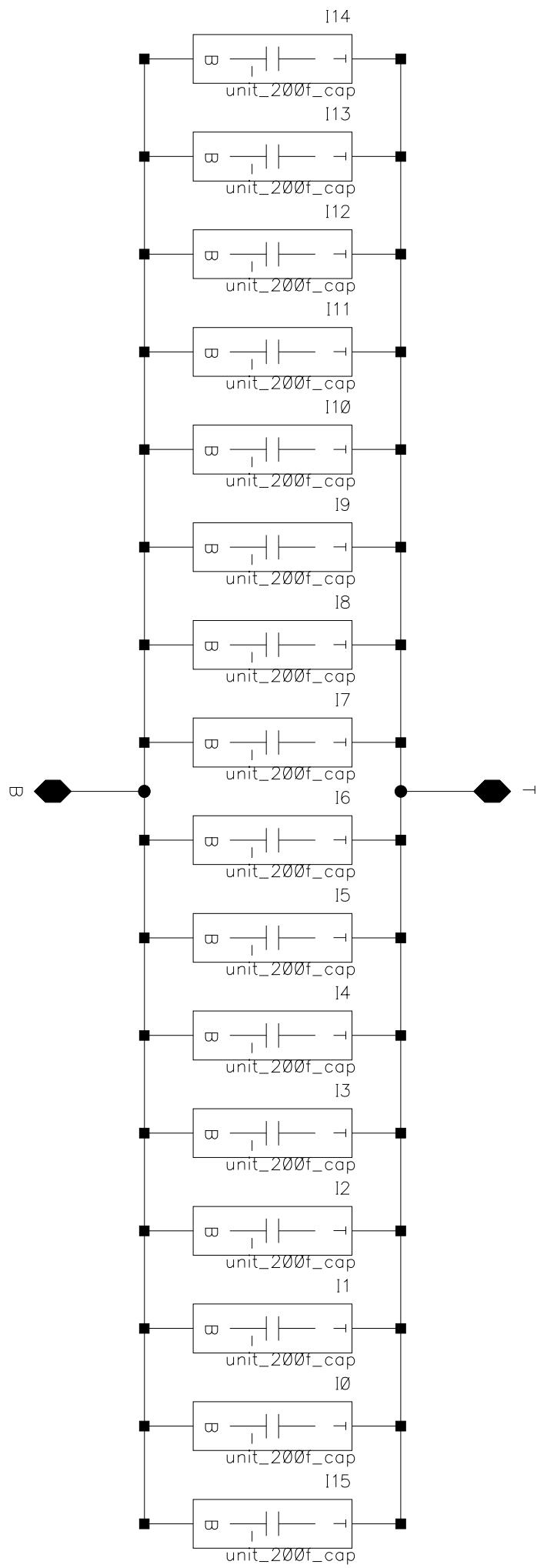
UPDATED	Aug 13 15:55:31 2007			
DRAWN				
CHECKED				
CHECKED				
ISSUED	SIZE A SCALE	CAGE NO.	DWG NO.	REV
				SHEET 1 OF 1

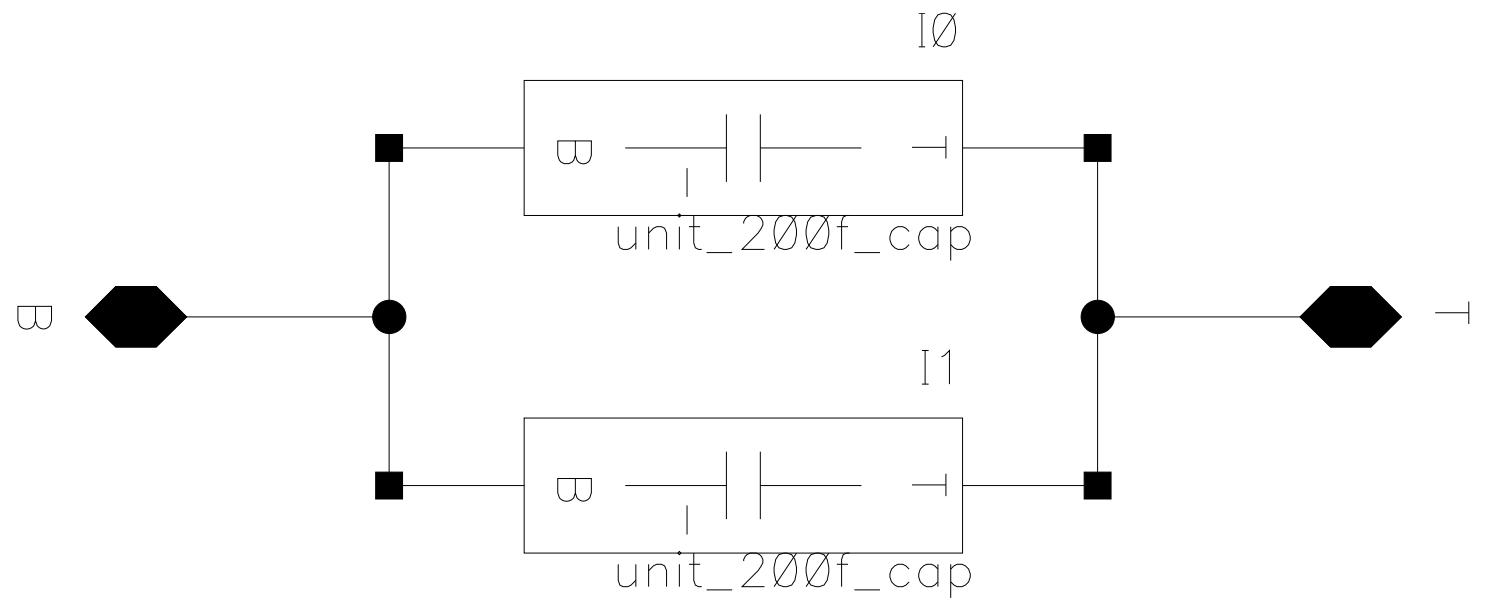


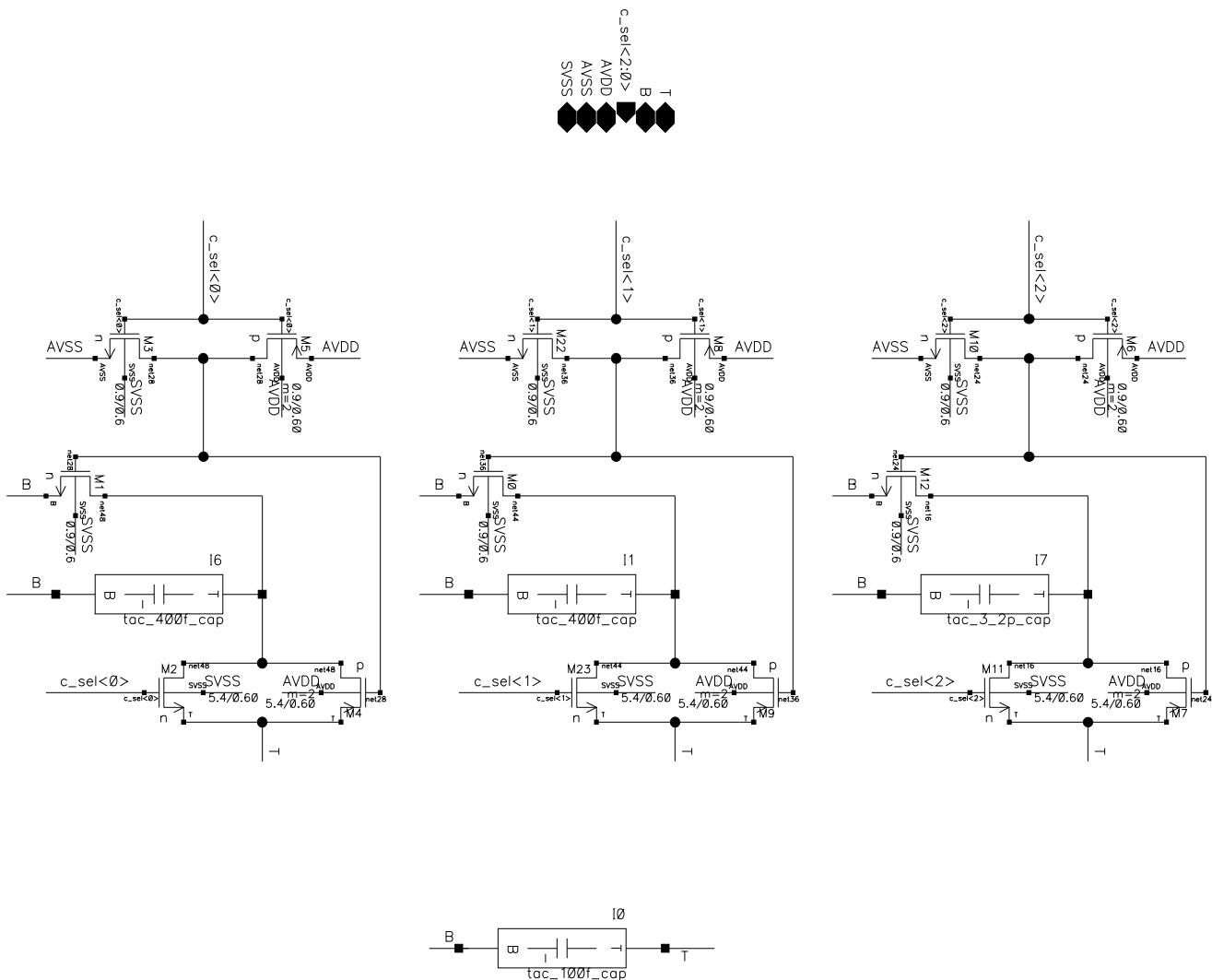
ZONE	REV	DESCRIPTION	DATE	APPROVED

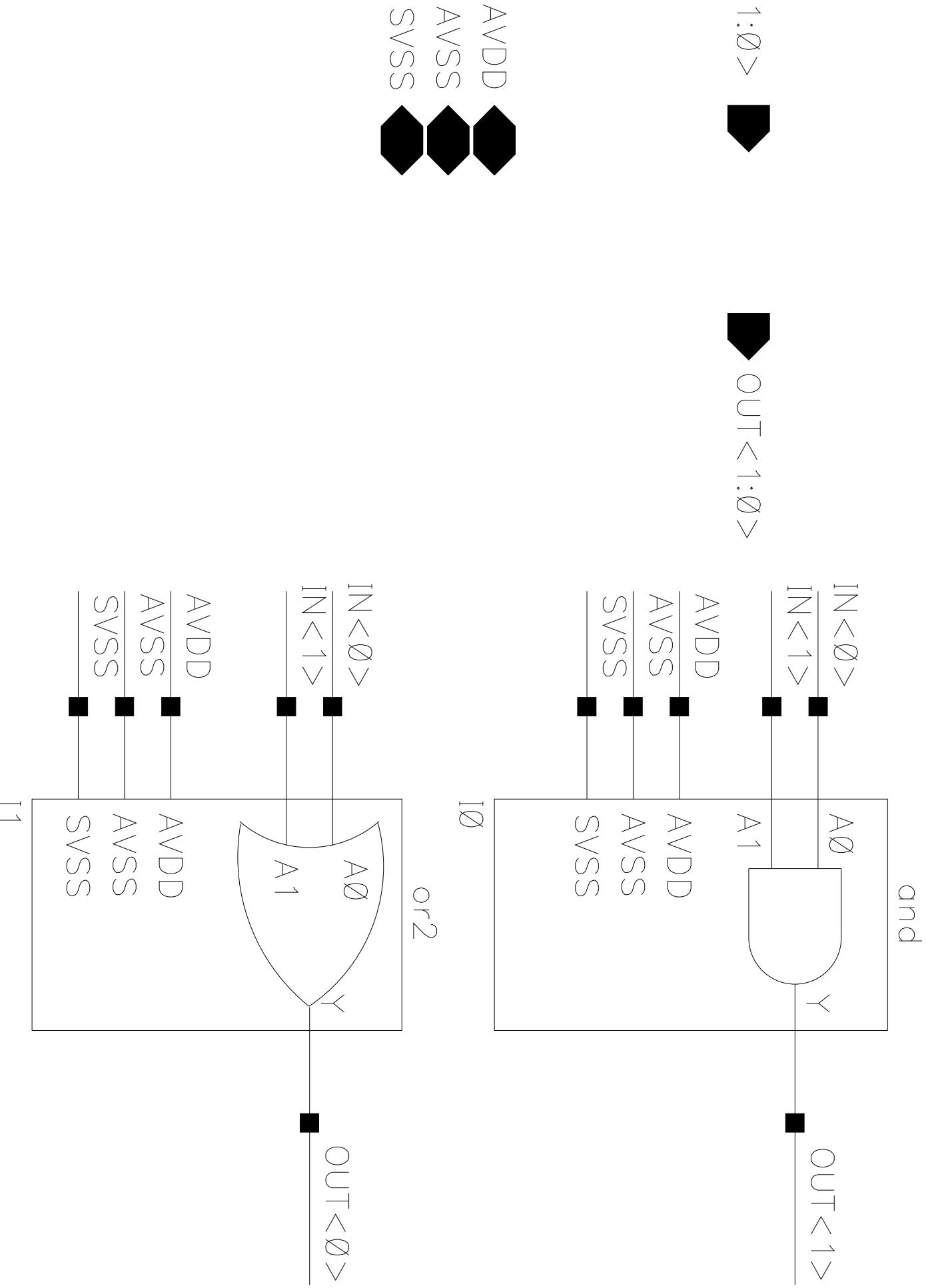


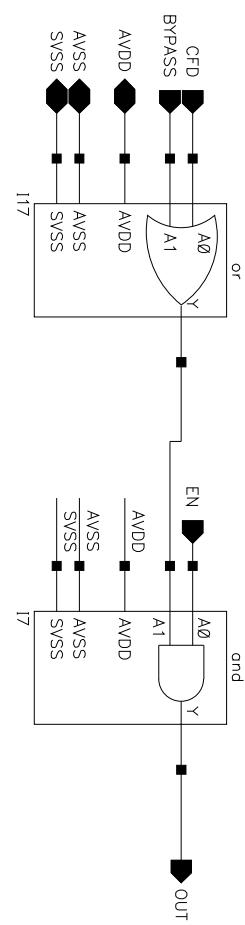








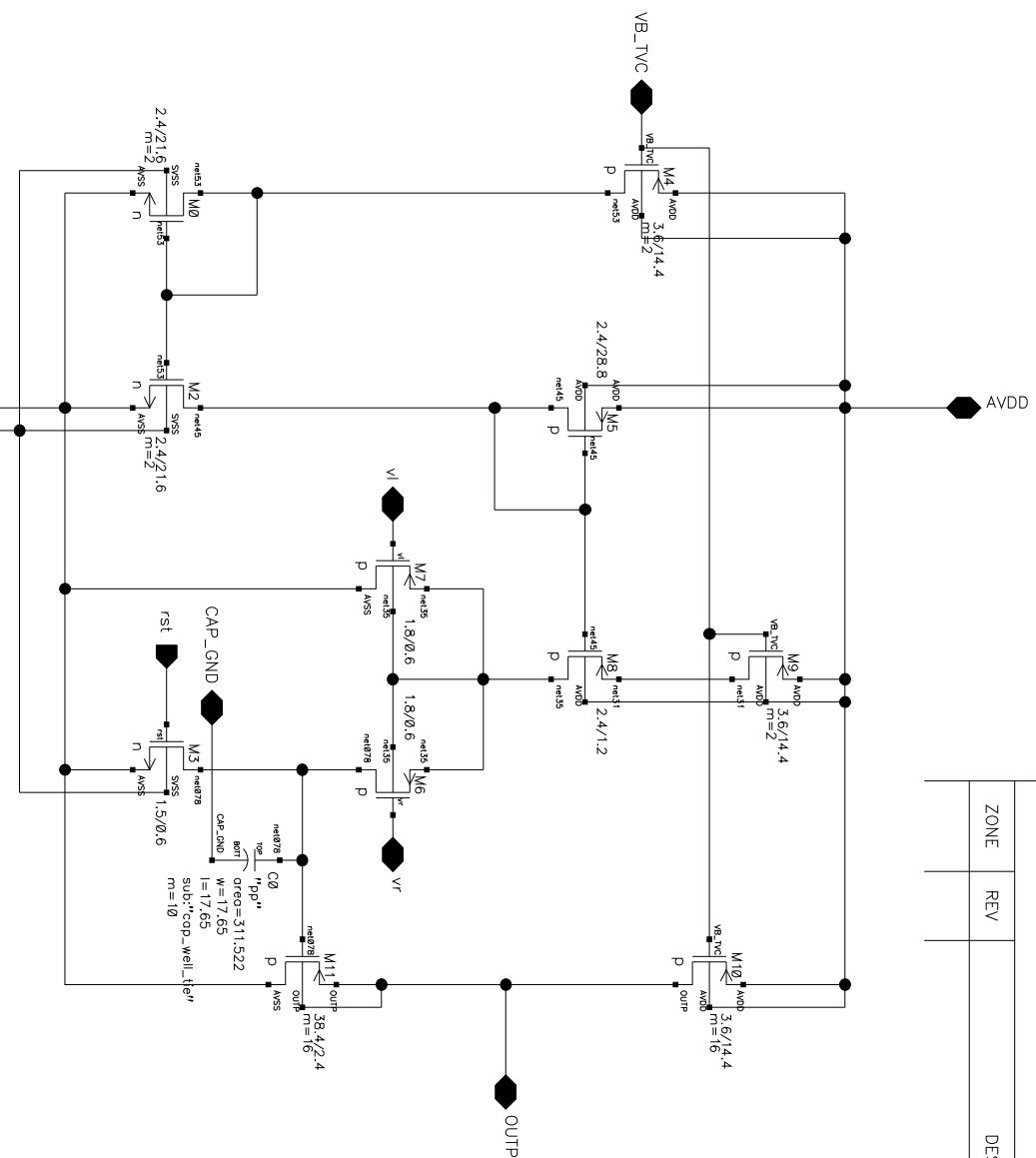




REV A			
CAGE NO.	DWG NO.	SH 1	REV A
ZONE	REV	DESCRIPTION	DATE

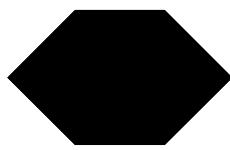
UPDATED	Aug 13 11:15:28 2007		
DRAWN	SIUE IC Design Lab		
CHECKED	Triggering Logic		
CHECKED			
ISSUED	SIZE A	CAGE NO.	DWG NO.
	SCALE		SHEET 1 OF 1
			REV A

ZONE	REV	DESCRIPTION		DATE	APPROVED
		CAGE NO.	DWG NO.		
REV 1					



UPDATED	JUL 5 15:59:25 2007	
DRAWN		
CHECKED		
ISSUED		
	SIZE SCAL	CAGE NO. DWG NO.
		SHEET 1 OF 1
	REV	

B



B

BOTT

TOP

CQ

T



T

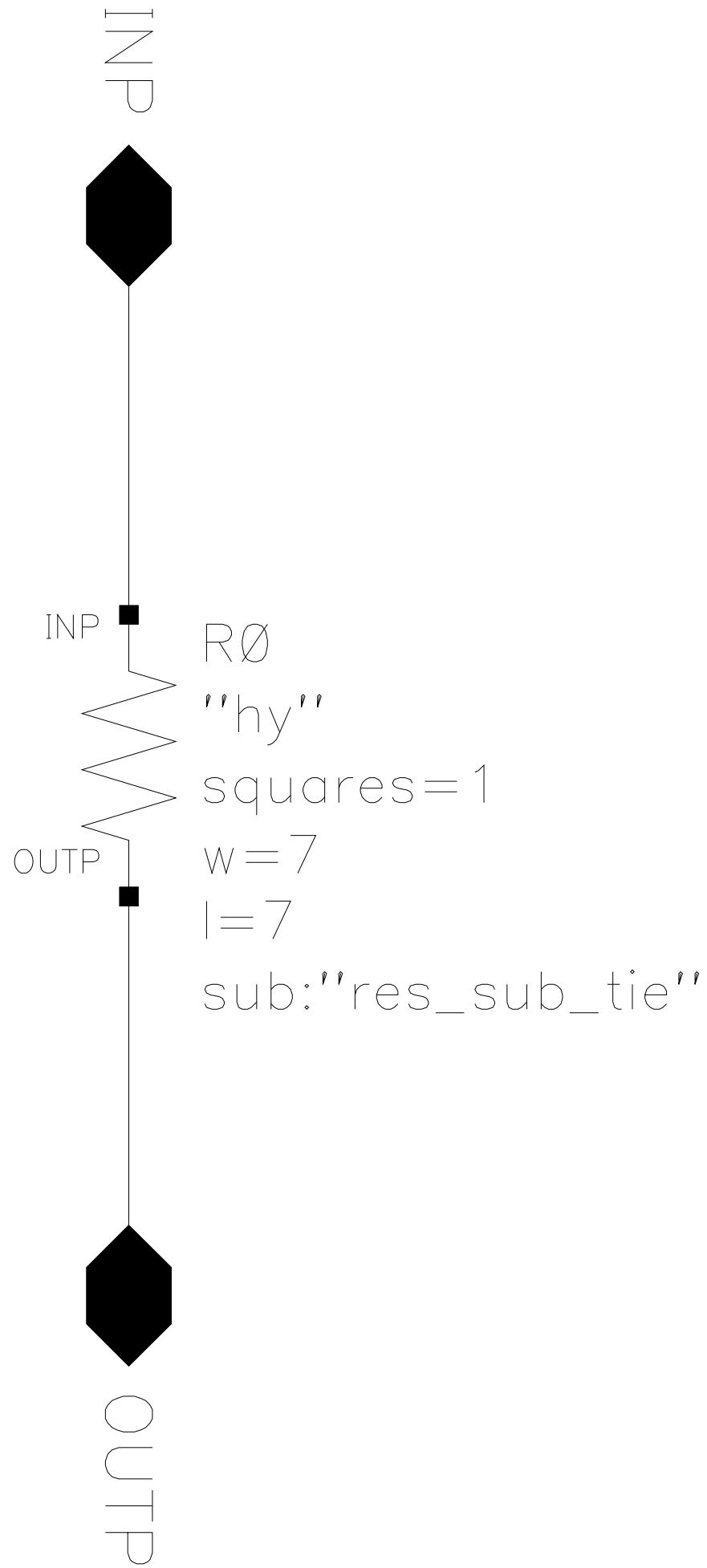
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$A_{\text{reg}} = 108.16$

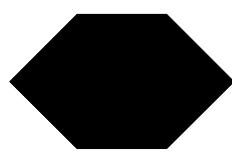
$W = 10.4$

$| = 10.4$

Sub: "cap\_well\_tie"



B



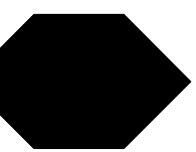
B

BOTT  
TOP

pp pp

CQ

T



T

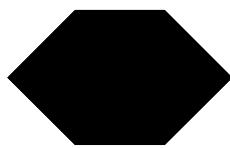
$A_{\text{req}} = 219.04$

$W = 14.8$

$| = 14.8$

sub: "cap\_well\_tie"

B



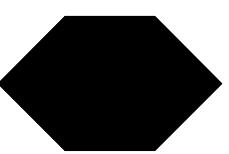
B

BOTT

TOP

CQ

T



T

pp

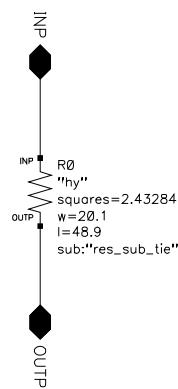
area = 275.228

W = 16.59

= 16.59

sub: "cap\_well\_tie"

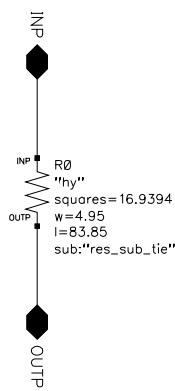
Resistor has  $l=48.9\mu$  and  $w=20.1\mu$



UPDATED	Jun 20 16:17:28 2005		
DRAWN	Unit_bias_res		
CHECKED			
ISSUED			
SIZE	CAGE NO.	DWG NO.	SH 1 REV
SCALE			
REV		SHEET 1 OF 1	

CAGE NO.	DWG NO.	REV
ZONE	REV	DESCRIPTION
		DATE
		APPROVED

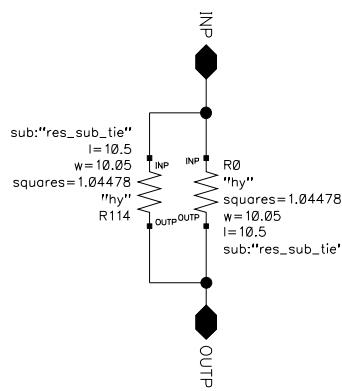
Resistor has  $l=83.85\mu$  and  $w=4.95\mu$



UPDATED	Jun 20 16:20:31 2005		
DRAWN	Unit_bias_res_2		
CHECKED			
ISSUED			
SIZE	CAGE NO. DWG NO.		
SCALE			
REV	SHEET 1 OF 1		

CAGE NO.	DWG NO.	SH 1	REV
ZONE	REV	DESCRIPTION	
		DATE	APPROVED

Resistor has  $l=10.5\mu$  and  $w=10.05\mu$   $m=2$



UPDATED  
Aug 14 14:19:17 2007

Unit\_bias\_res\_3

DRAWN

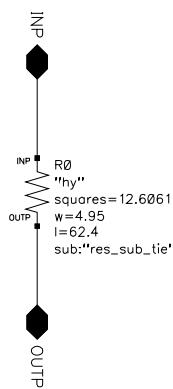
CHECKED

CHECKED  
ISSUED

SIZE	CAGE NO.	DWG NO.	REV
A			

CAGE NO.	DWG NO.	SH 1	REV
ZONE	REV	DESCRIPTION	
		DATE	APPROVED

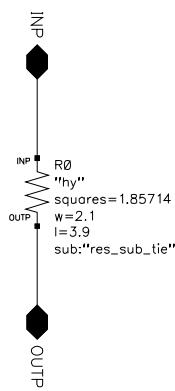
Resistor has  $l=62.4\mu$  and  $w=4.95\mu$



UPDATED	Jun 20 16:13:09 2005		
DRAWN	Unit_cons_Current_res		
CHECKED			
ISSUED			
SIZE	CAGE NO.	DWG NO.	SH 1 REV
A			
SCALE			
REV			
	SHEET	1 OF 1	

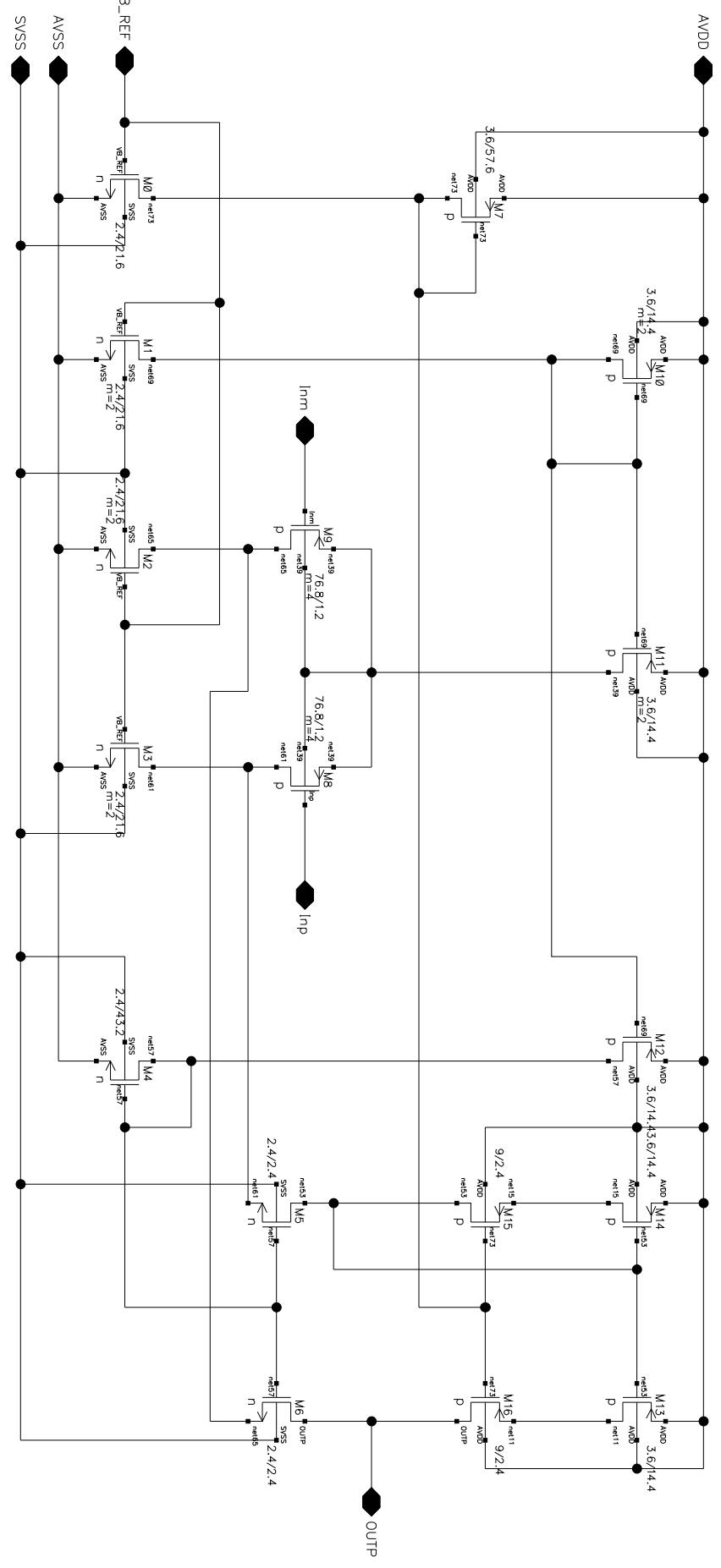
ZONE	REV	DESCRIPTION	DATE	APPROVED

Resistor has  $l=3.9\mu$  and  $w=2.1\mu$



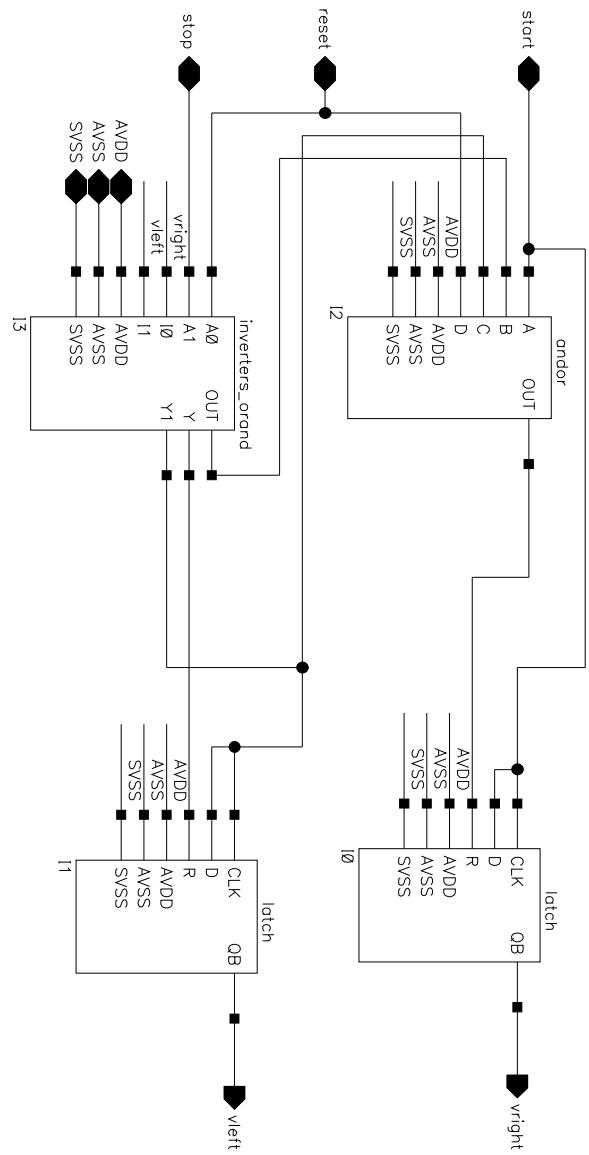
UPDATED	Jun 30 15:19:07 2005		
DRAWN			
CHECKED			
ISSUED			
SIZE	CAGE NO.	DWG NO.	SH 1 REV
SCALE			
REV		SHEET 1 OF 1	

CAGE NO.	DWG NO.	REV
ZONE	REV	DESCRIPTION
		DATE
		APPROVED



REVISIONS			
ZONE	REV	CAGE NO.	DWG NO.
		DATE	APPROVED

UPDATED	vref_buffer			
JUL 16 13:51:14 2007				
DRAWN				
CHECKED				
ISSUED				
CHECKED				
ISSUED				
	SIZE	CAGE NO.	DWG NO.	REV
	A			
SCALE				SHEET 1 OF 1

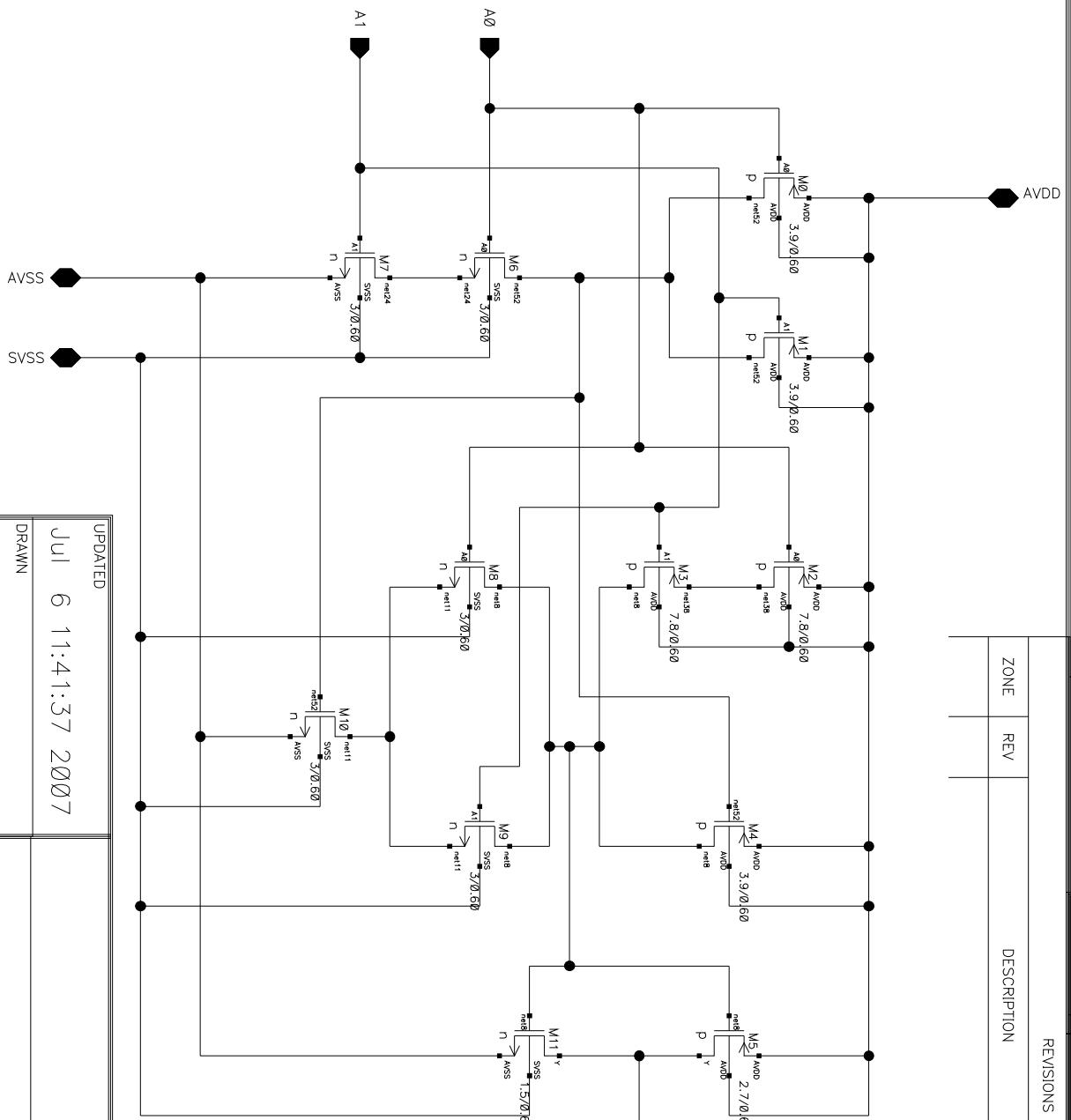


REVISIONS			
ZONE	REV	DESCRIPTION	DATE
			APPROVED
			SH 1 REV

width-gen

UPDATED	Jul 9 11:21:29 2007									
DRAWN										
CHECKED										
CHECKED										
ISSUED										
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SIZE	CAGE NO.					DWG NO.	REV			
		A								
SCALE			SHEET- 1 OF 1							

ZONE	REV	DESCRIPTION	DATE	APPROVED
			SH 1	REV



UPDATED  
JUL 6 11:41:37 2007

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ISSUED	SIZE	CAGE NO.	DWG NO.	SCALE	SHEET	1 OF 1
CHECKED				REV		

CAGE NO.

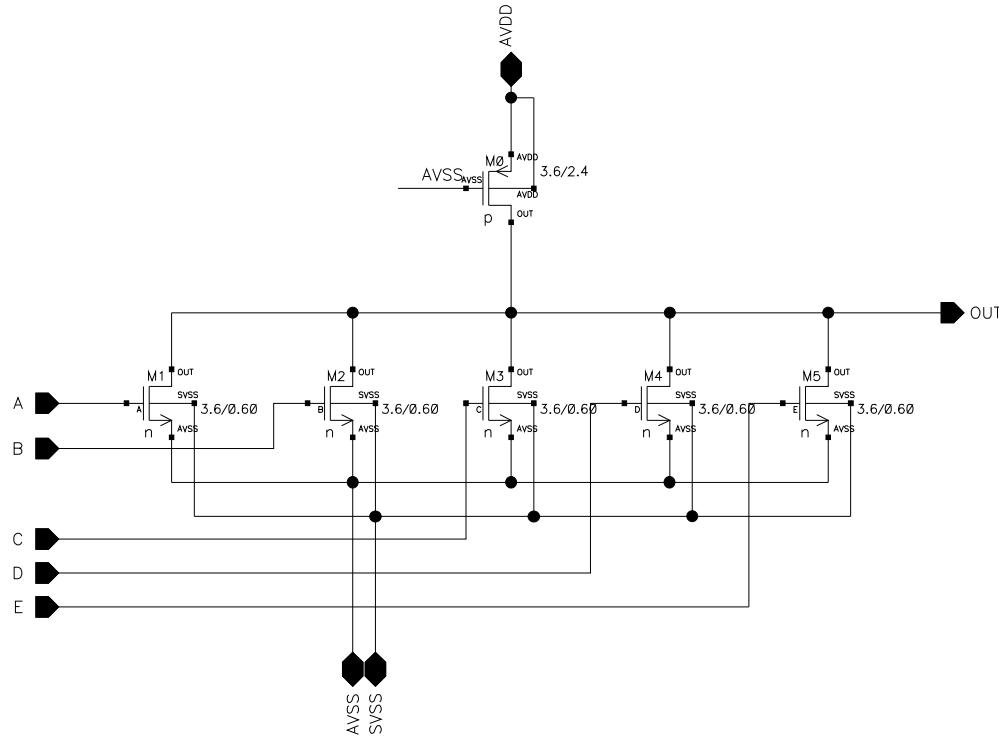
DWG NO.

SH 1

REV

## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED

Jul 11 13:37:50 2007

pseudo\_nor

DRAWN

CHECKED

CHECKED

ISSUED

SIZE  
A

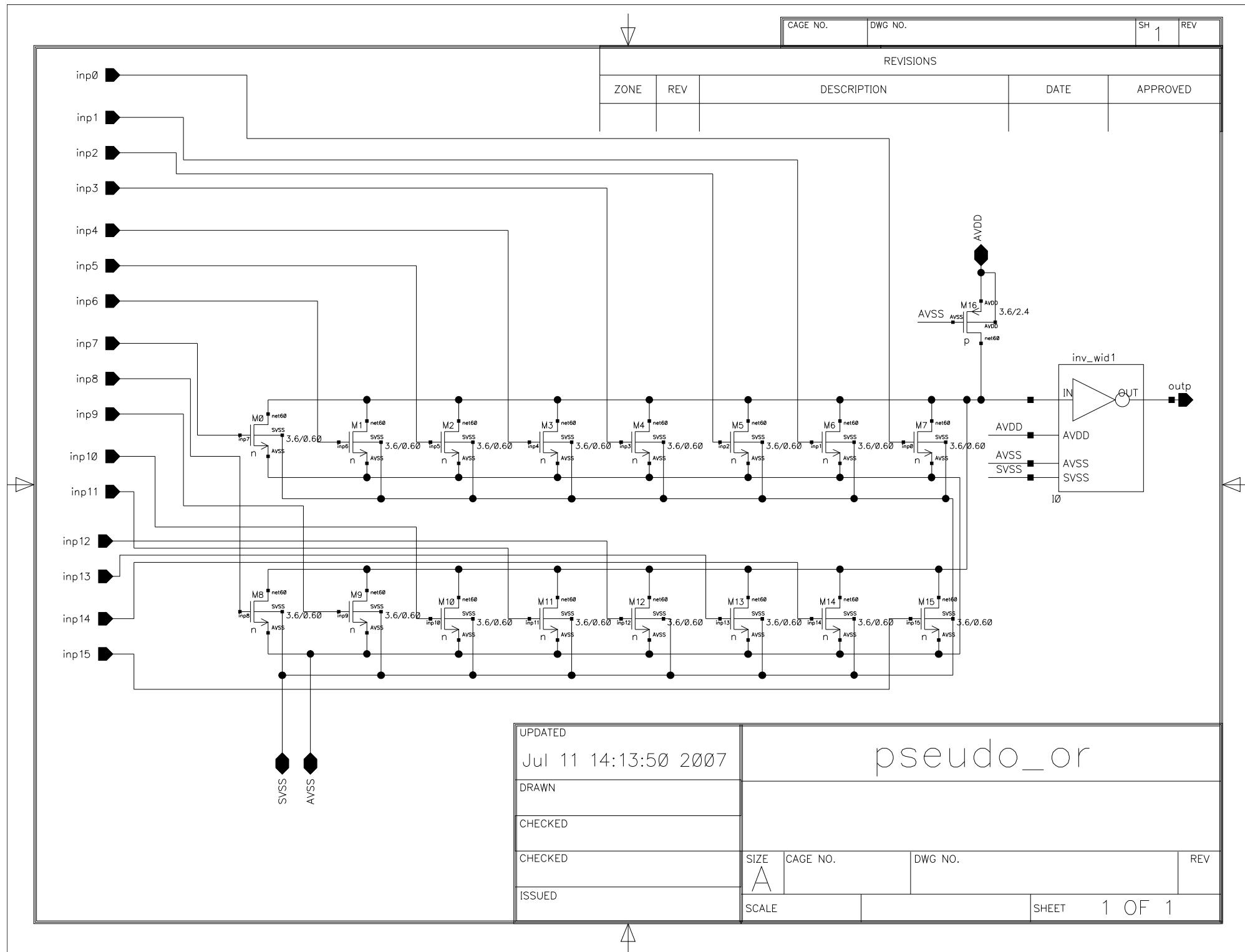
CAGE NO.

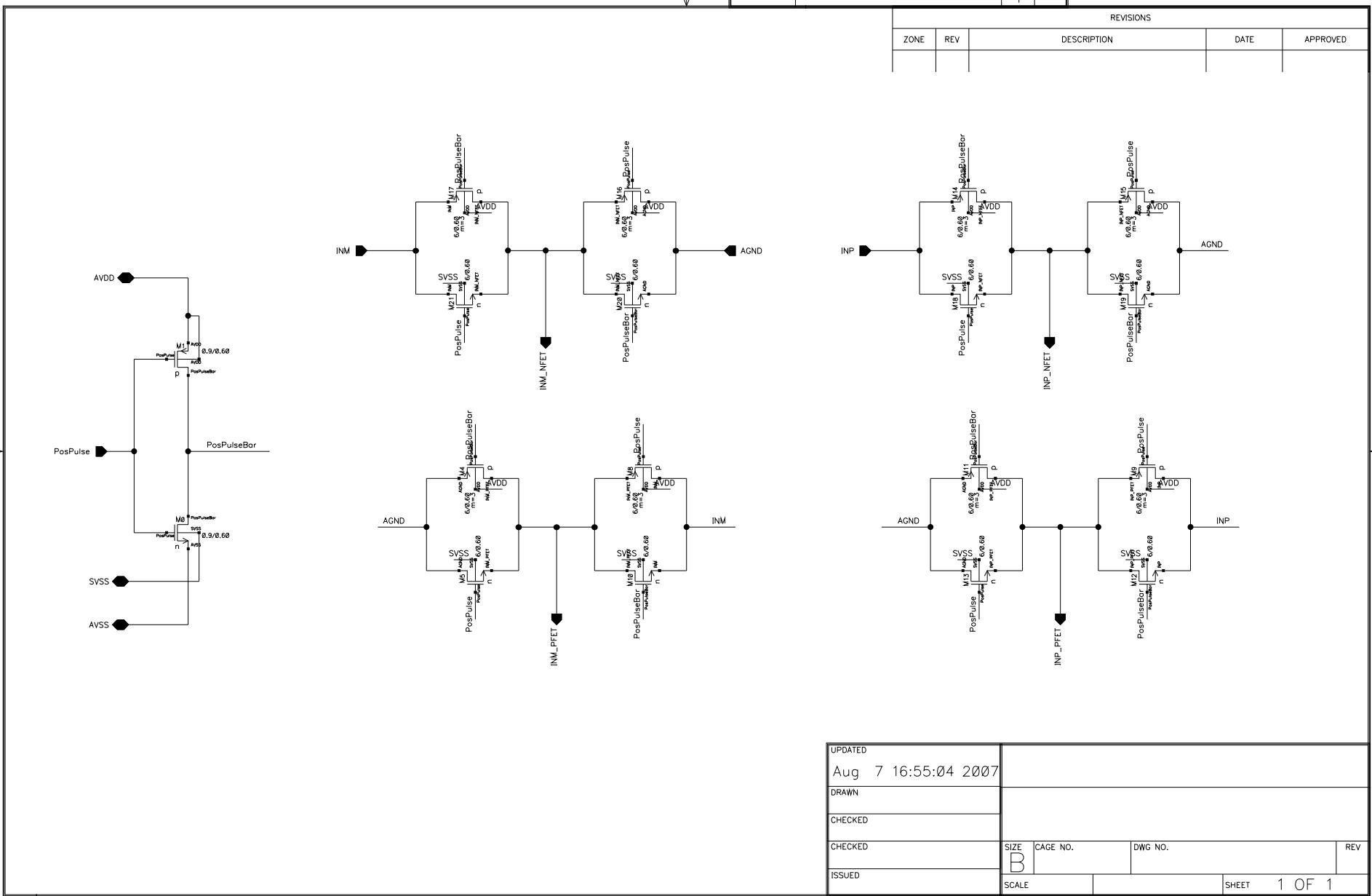
DWG NO.

REV

SCALE

SHEET 1 OF 1

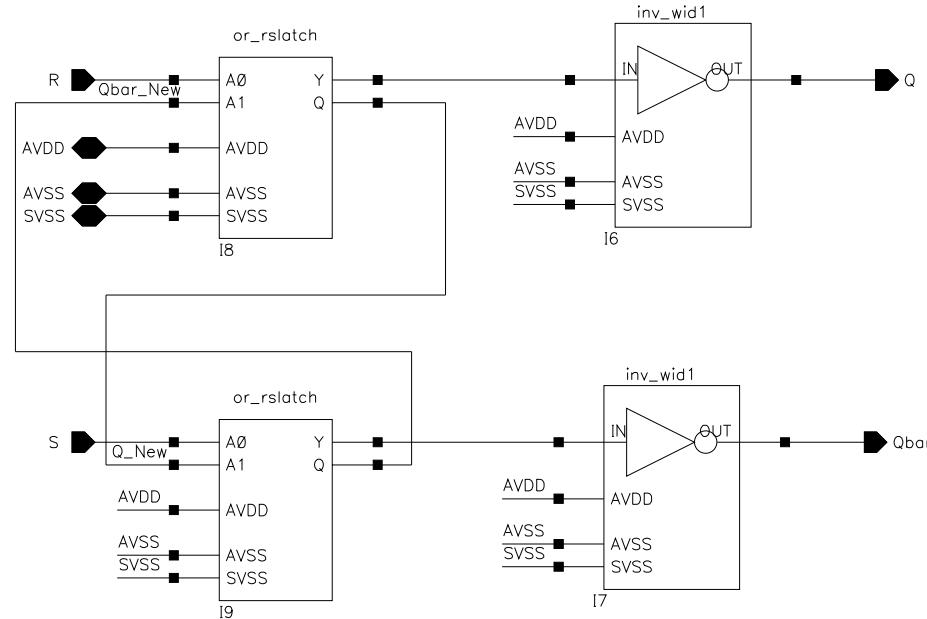




CAGE NO. DWG NO. SH 1 REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Aug 13 14:51:32 2007

rs\_latch

DRAWN

CHECKED

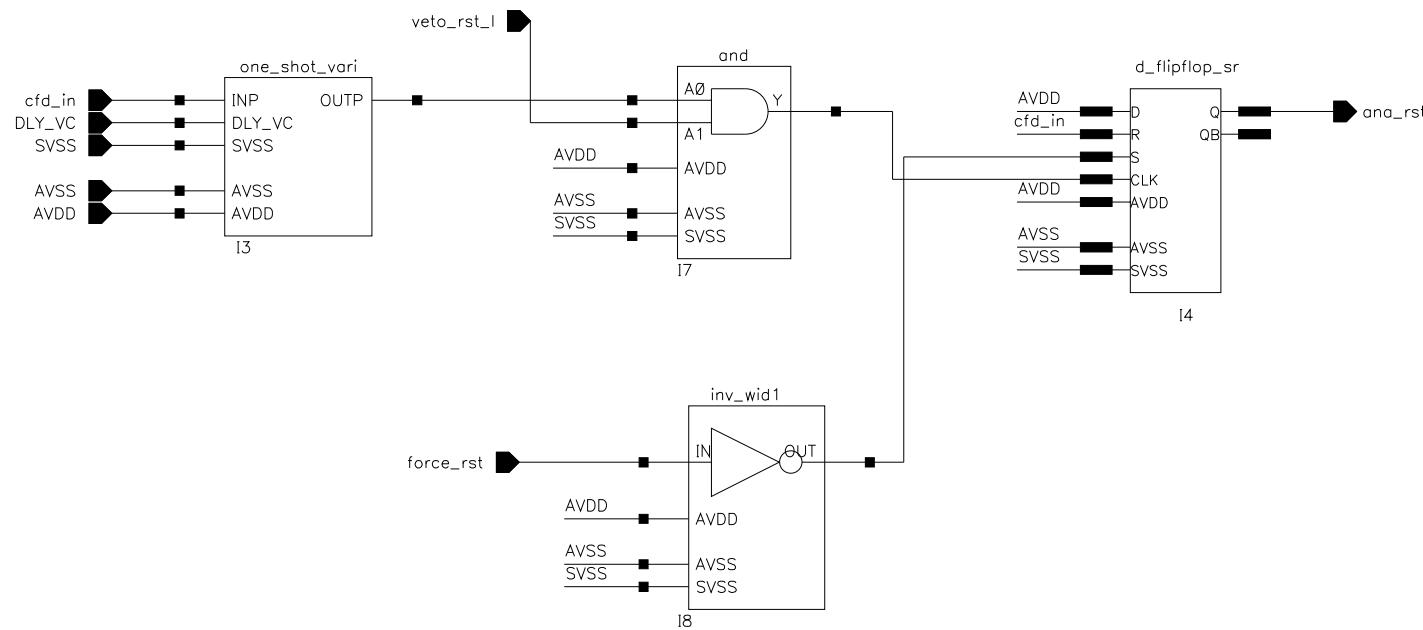
CHECKED

ISSUED

SIZE	CAGE NO.	DWG NO.	REV
A			
SCALE			
SHEET		1 OF 1	

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Aug 14 15:45:46 2007

DRAWN

CHECKED

CHECKED

ISSUED

SIUE IC Design Lab  
Reset Logic

SIZE A

CAGE NO.

DWG NO.

REV A

SCALE

SHEET 1 OF 1

CAGE NO.

DWG NO.

SH 1

REV

## REVISIONS

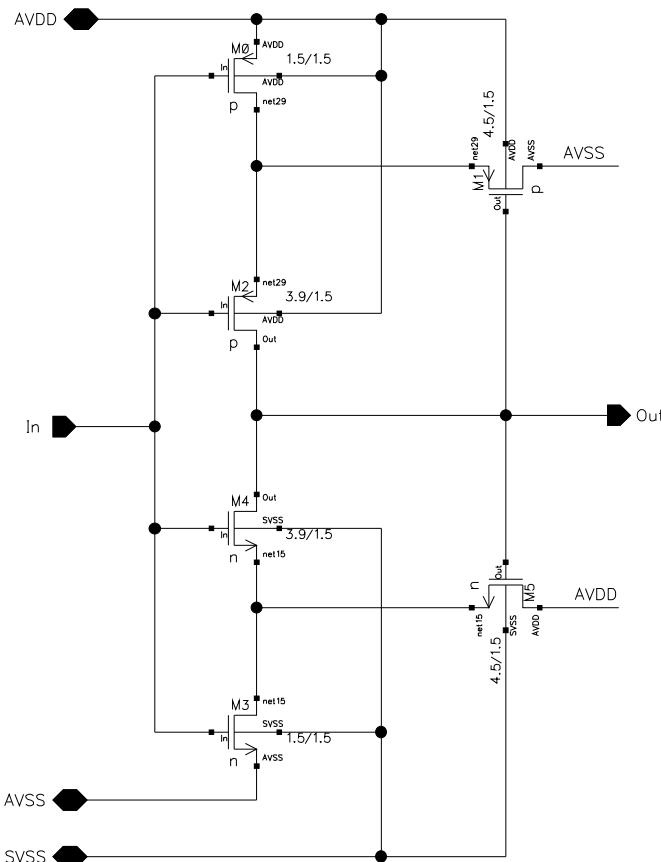
ZONE

REV

DESCRIPTION

DATE

APPROVED



UPDATED

Aug 13 11:29:31 2007

schmitt

DRAWN

CHECKED

CHECKED

ISSUED

SIZE  
A

CAGE NO.

DWG NO.

REV

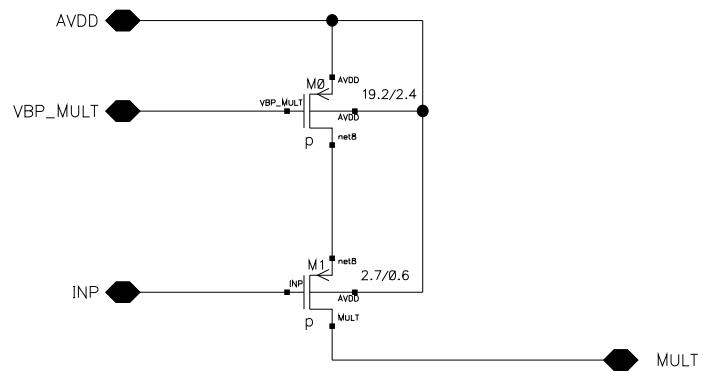
SCALE

SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Jun 15 15:32:45 2007

single\_mult

DRAWN

CHECKED

CHECKED

ISSUED

SIZE  
A  
SCALE

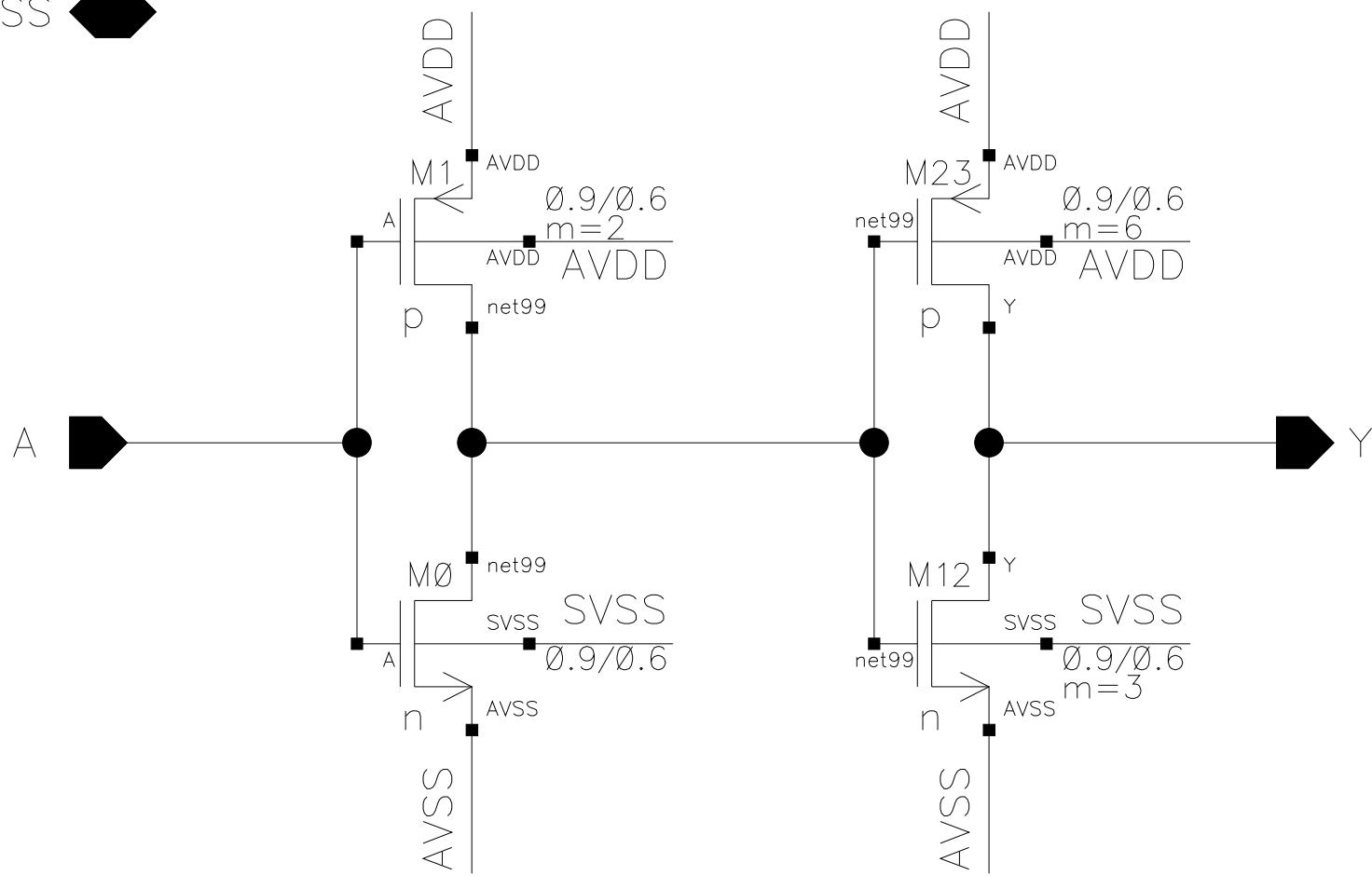
CAGE NO.

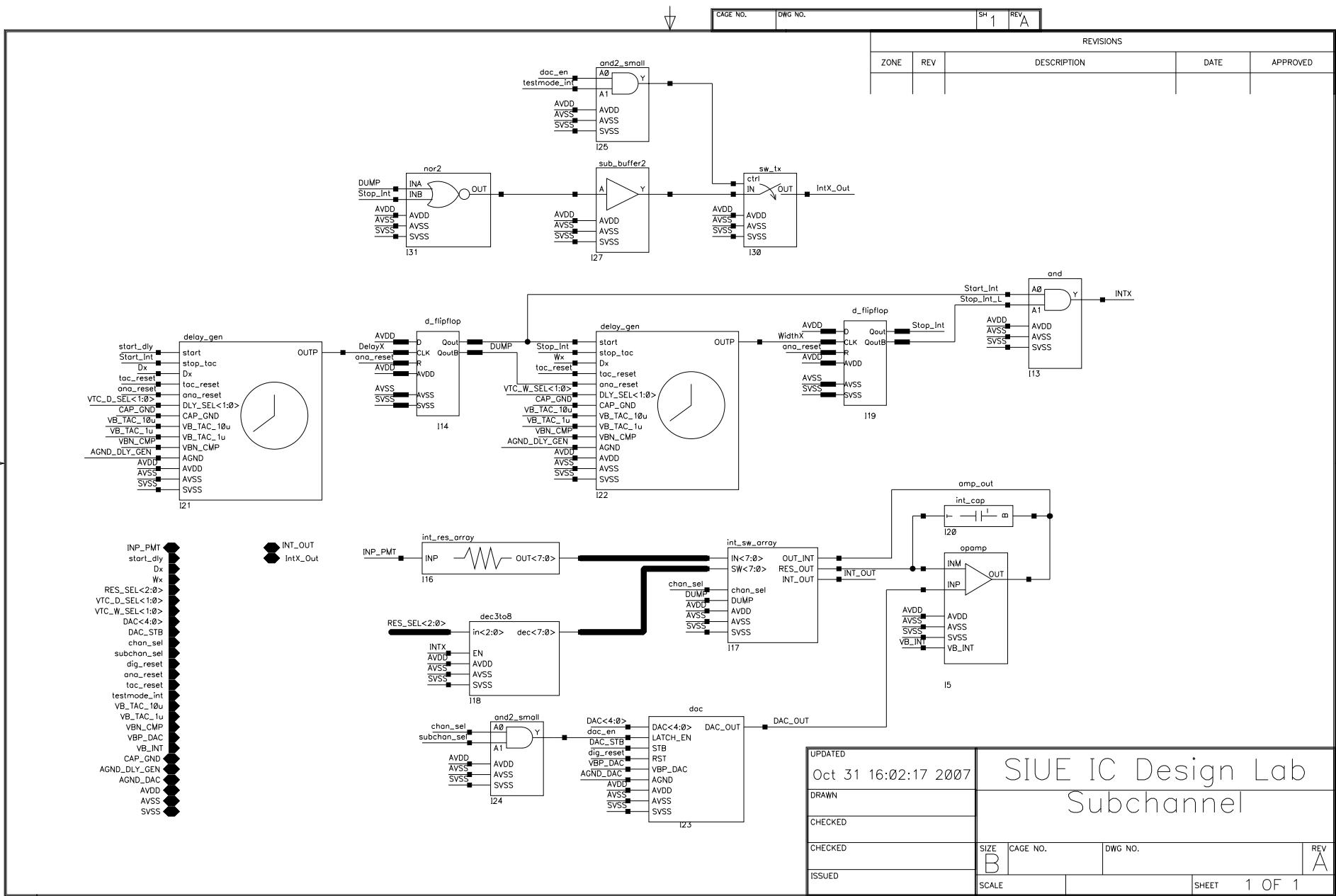
DWG NO.

REV

SHEET 1 OF 1

AVDD AVSS SVSS





CAGE NO.

DWG NO.

SH 1

REV

## REVISIONS

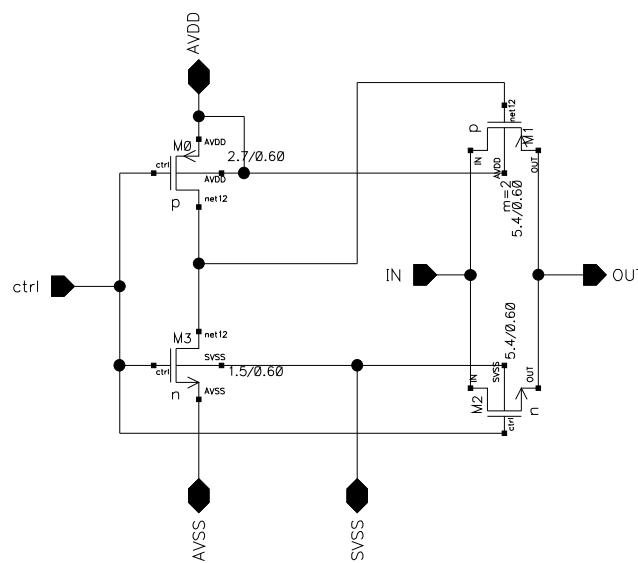
ZONE

REV

DESCRIPTION

DATE

APPROVED



UPDATED

Aug 13 15:55:31 2007

SW\_channel

DRAWN

CHECKED

CHECKED

ISSUED

SIZE

A

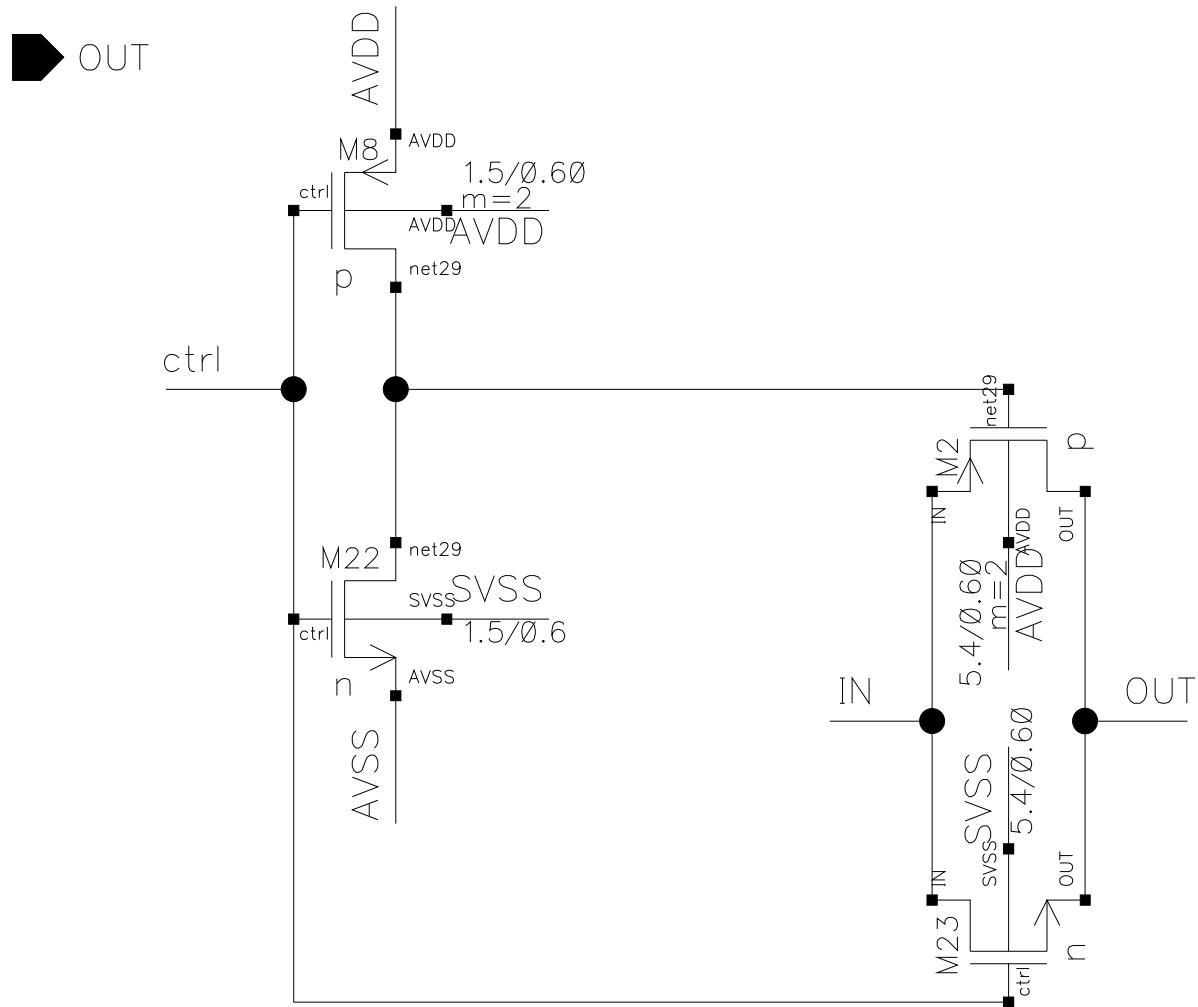
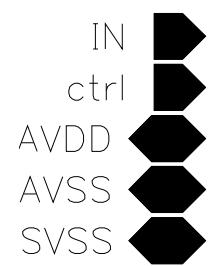
CAGE NO.

DWG NO.

REV

SCALE

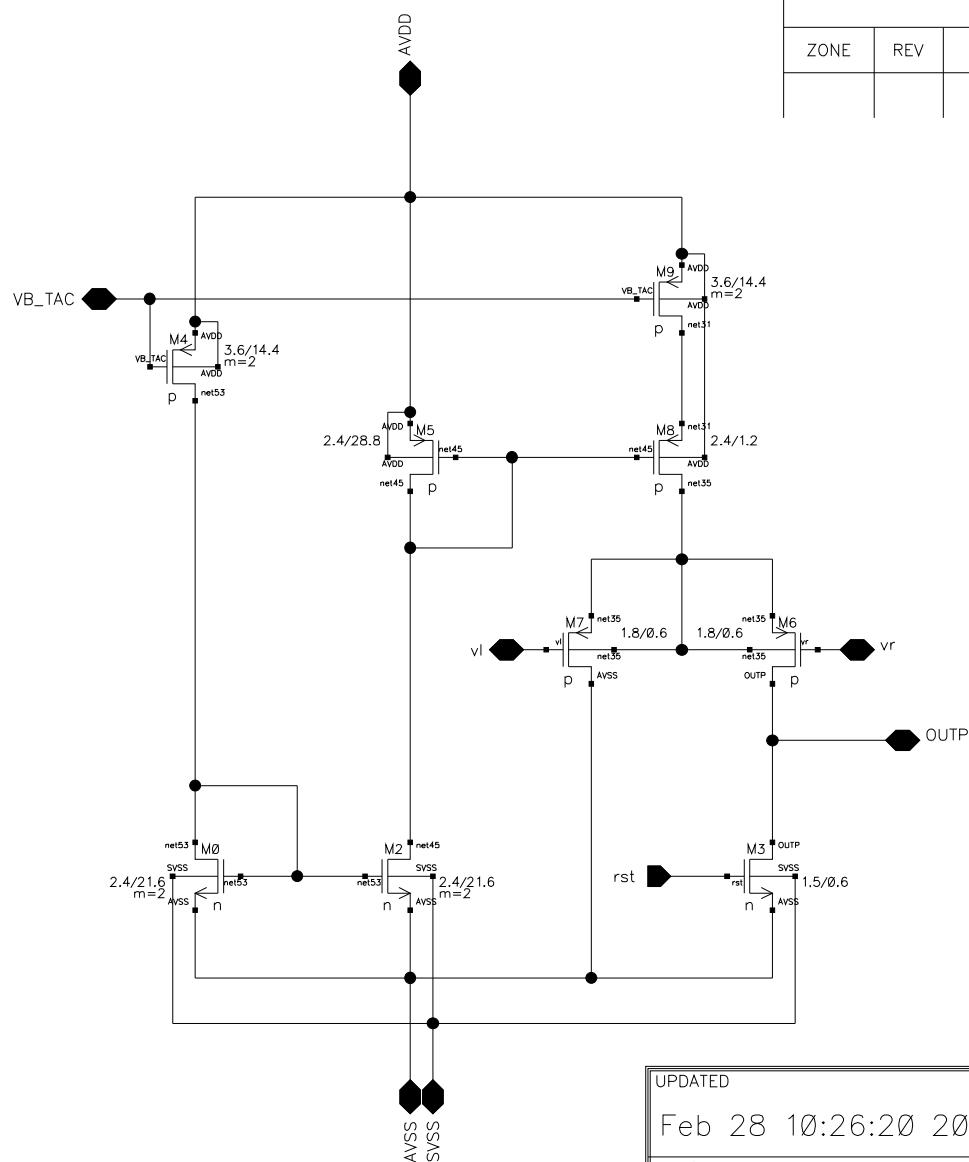
SHEET 1 OF 1



CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Feb 28 10:26:20 2007

tac

DRAWN

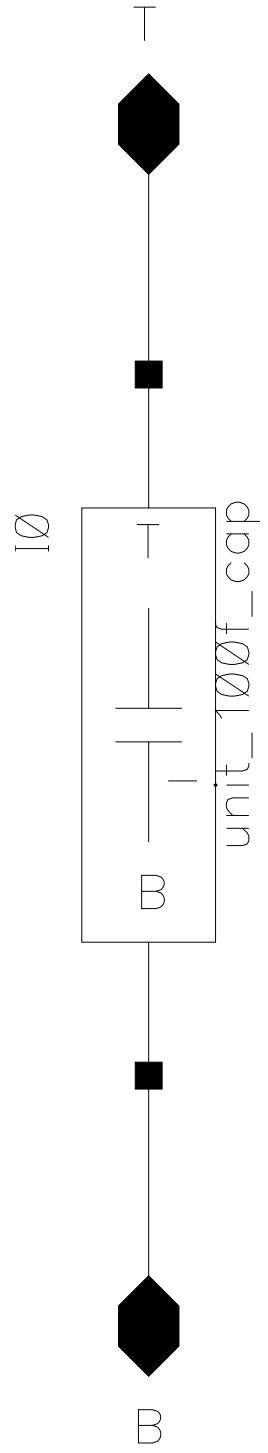
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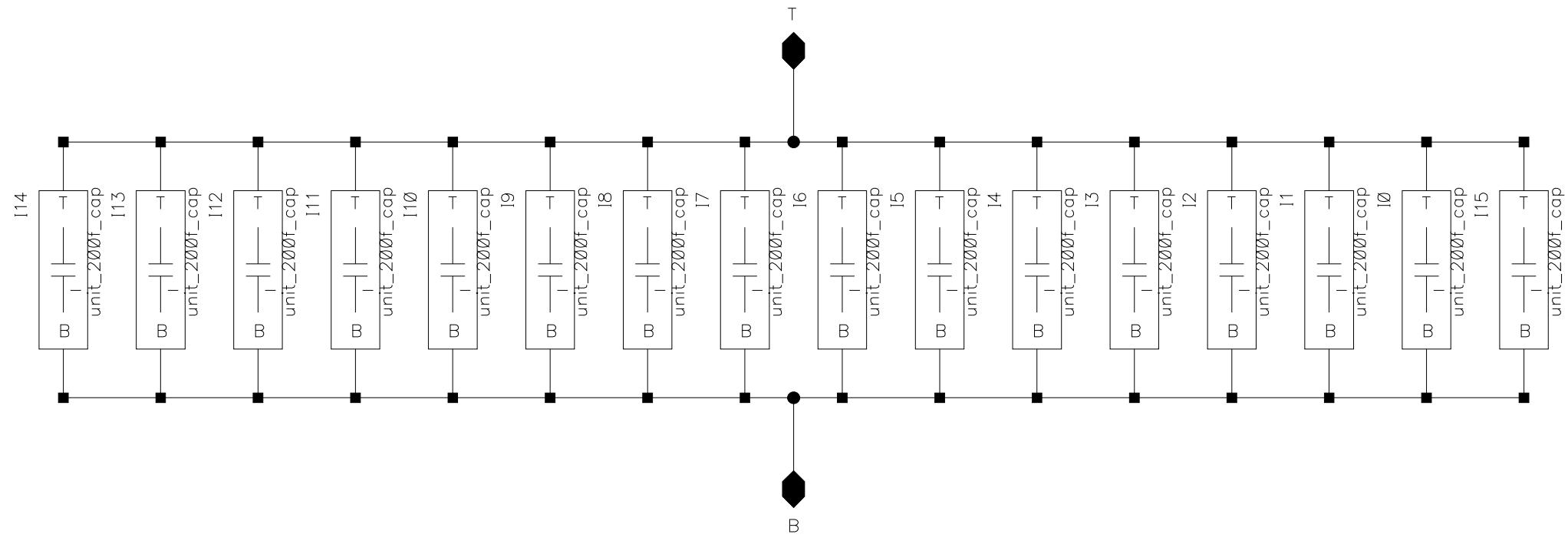
CHECKED

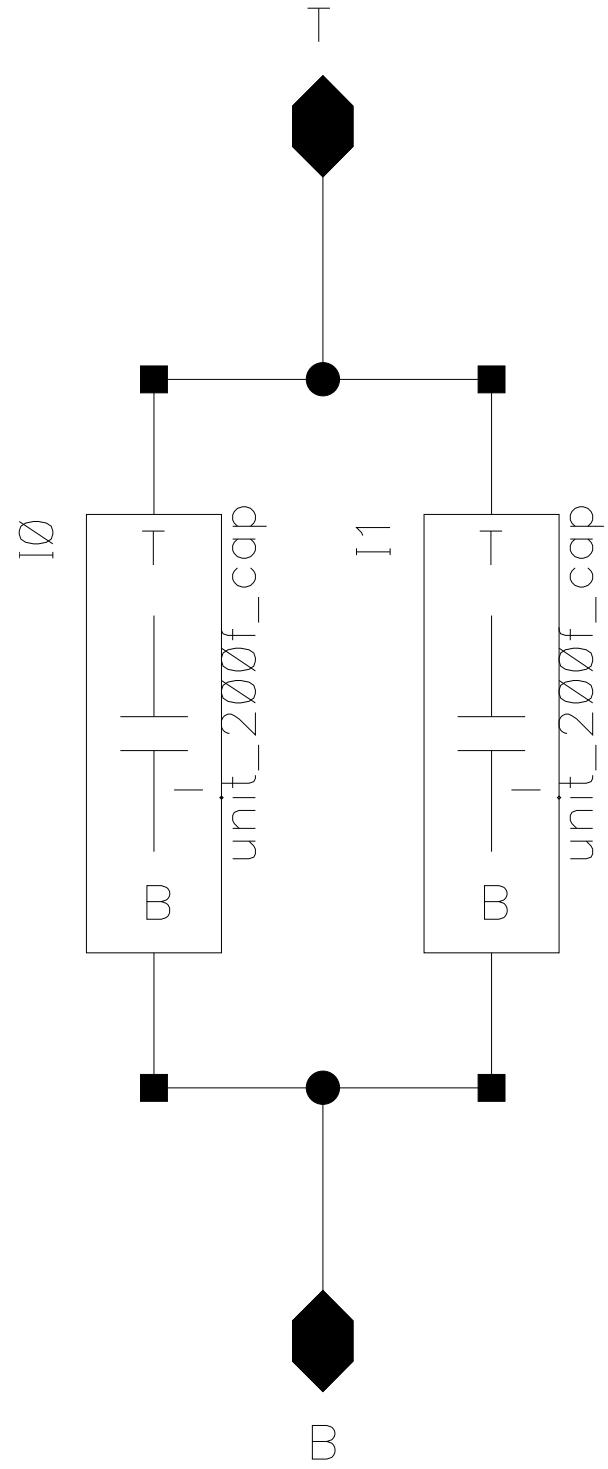
ISSUED

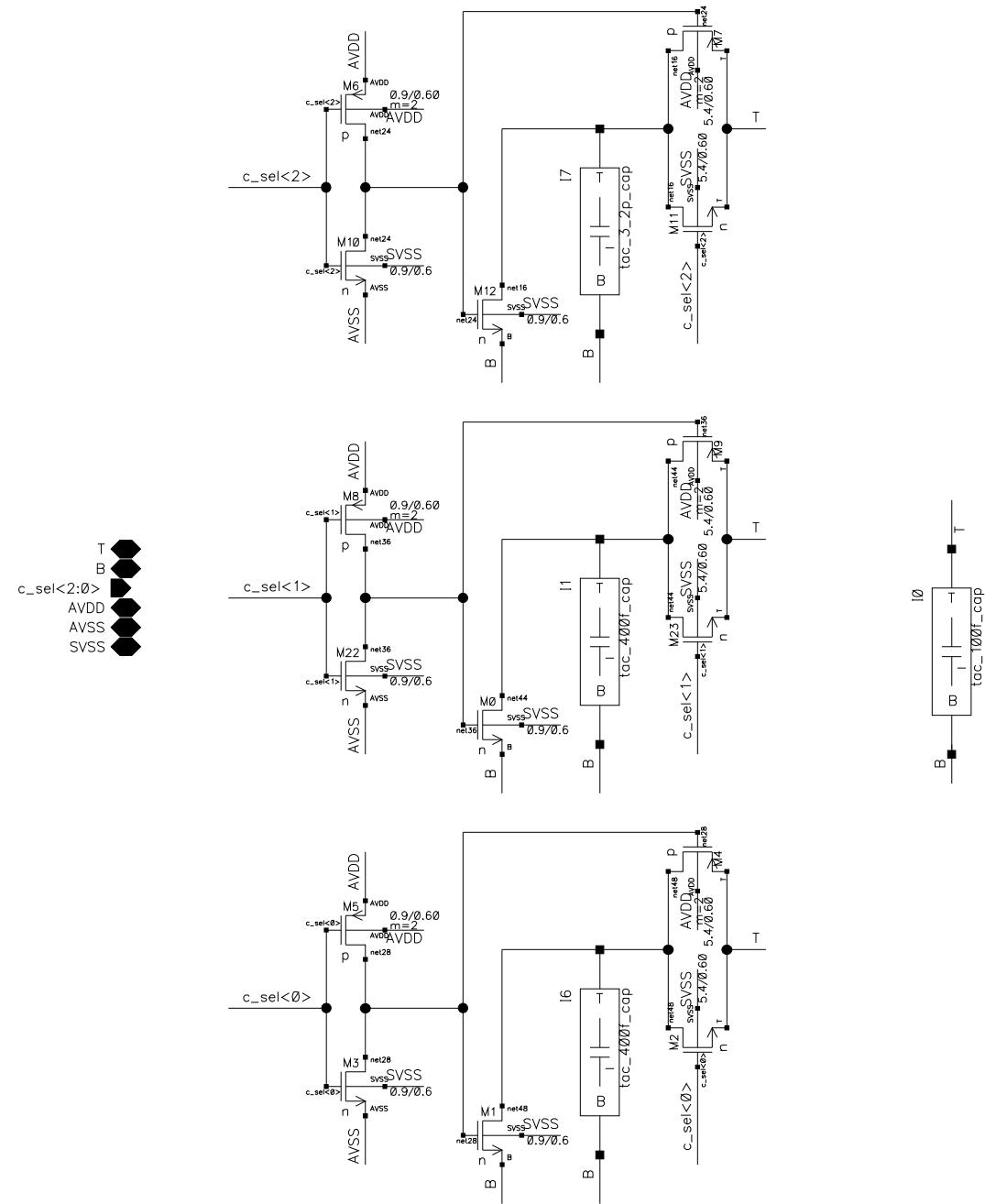
SIZE	CAGE NO.	DWG NO.	REV
A			

SCALE			SHEET 1 OF 1
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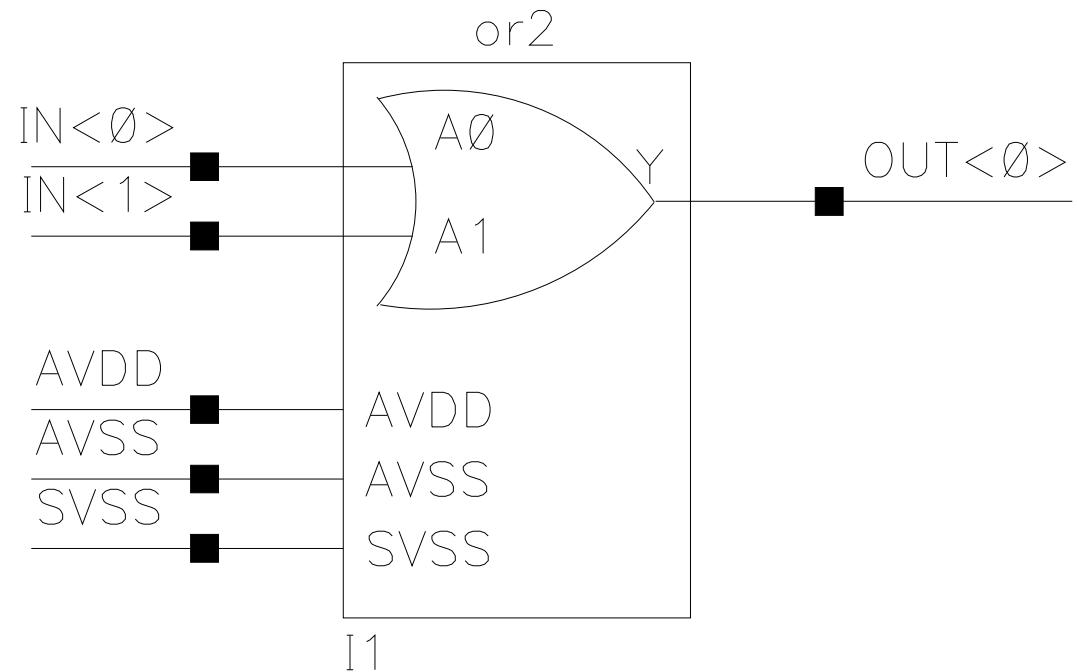
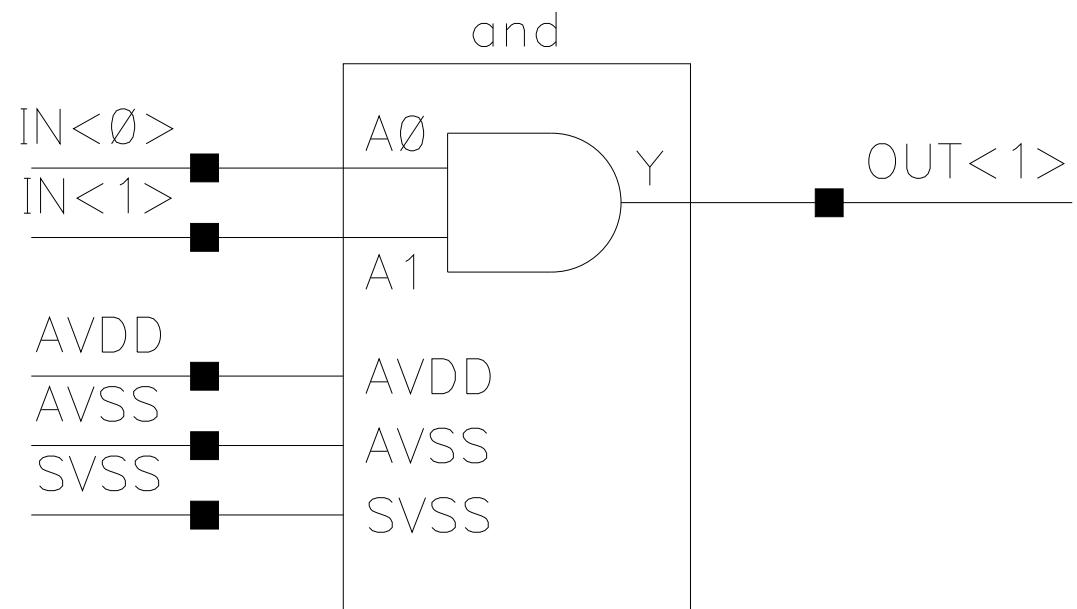




IN<1:0> 

 OUT<1:0>

AVDD   
AVSS   
SVSS 



CAGE NO.

DWG NO.

SH

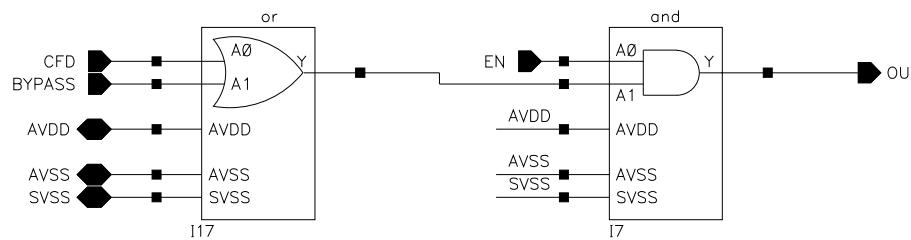
1

REV

A

## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Aug 13 11:15:28 2007

DRAWN

CHECKED

CHECKED

ISSUED

SIUE IC Design Lab  
Triggering Logic

SIZE  
A

CAGE NO.

DWG NO.

REV  
A

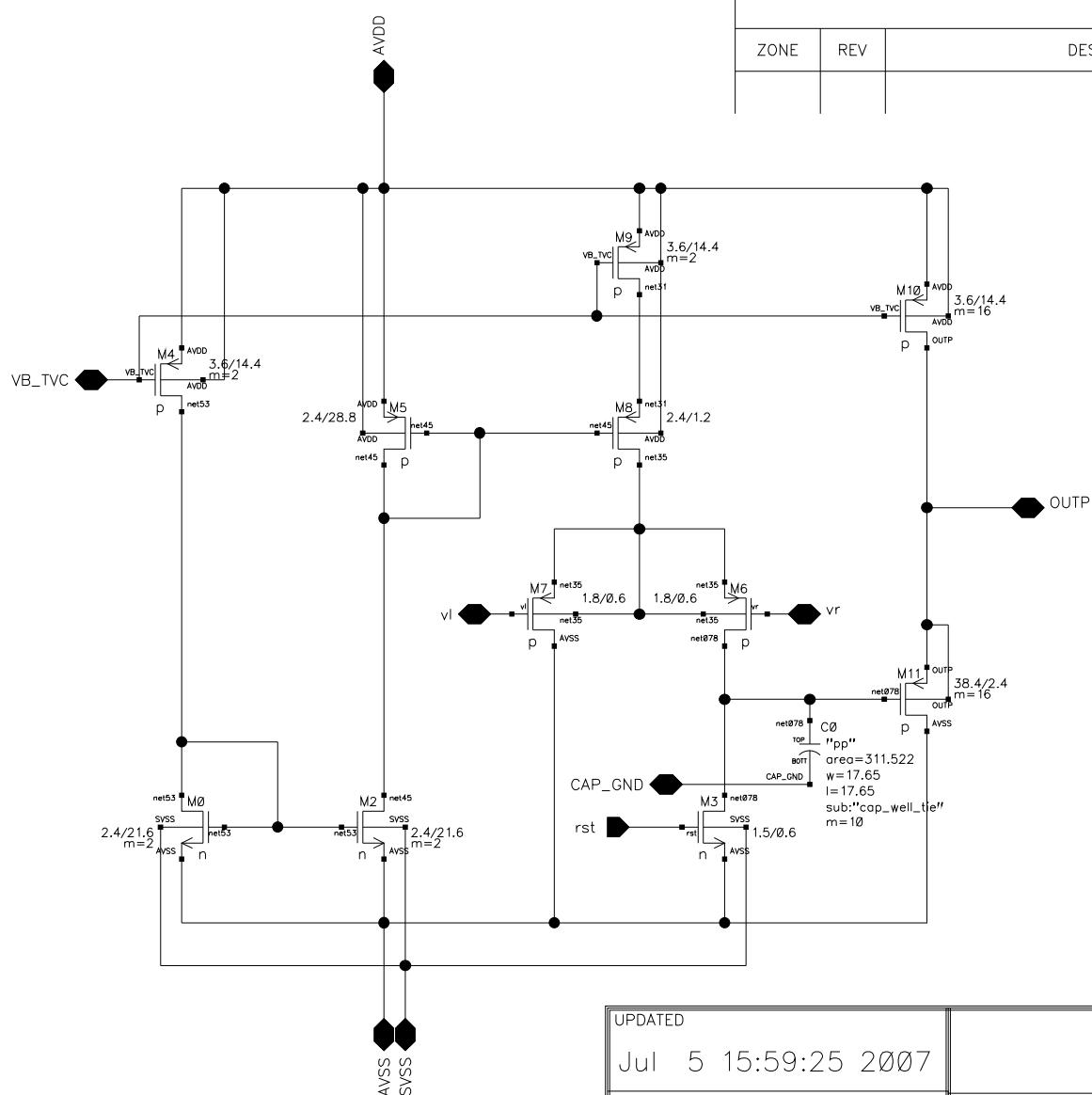
SCALE

SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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### REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Jul 5 15:59:25 2007

tvc

DRAWN

CHECKED

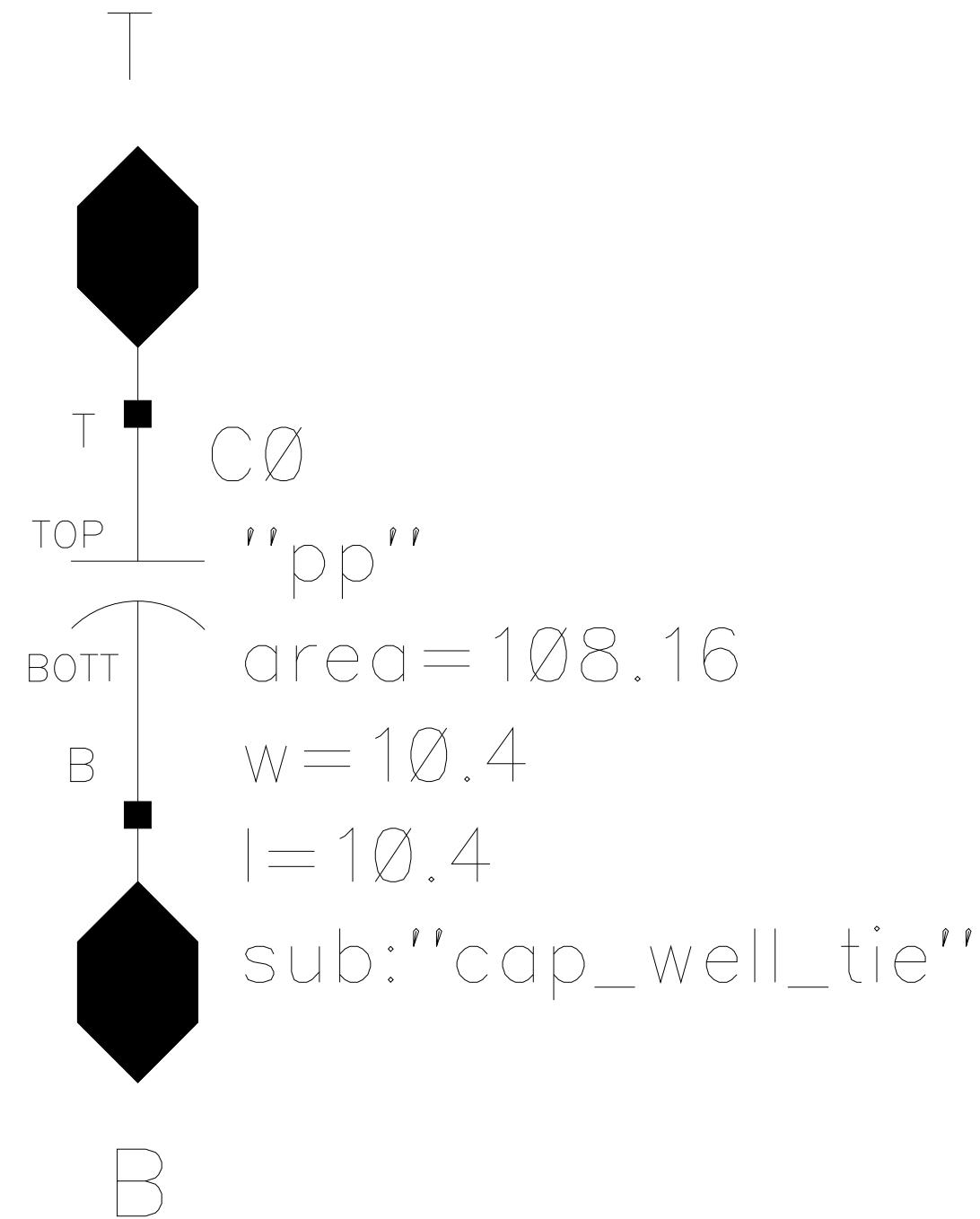
CHECKED

ISSUED

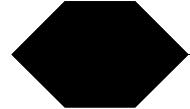
SIZE	CAGE NO.	DWG NO.	REV
A			

SCALE		
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SHEET 1 OF 1



INP



INP

RQ

“hy”

squares=1

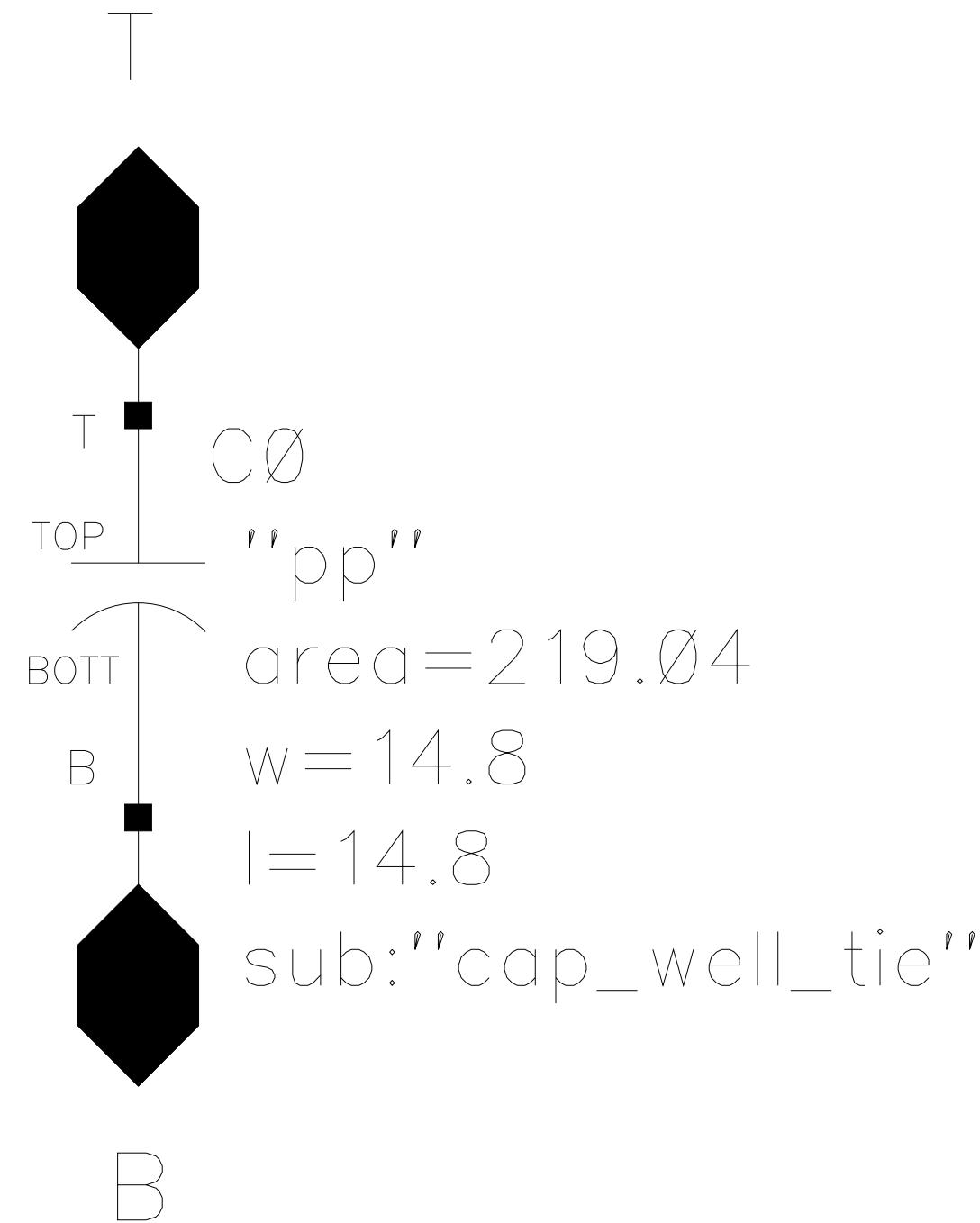
W=7

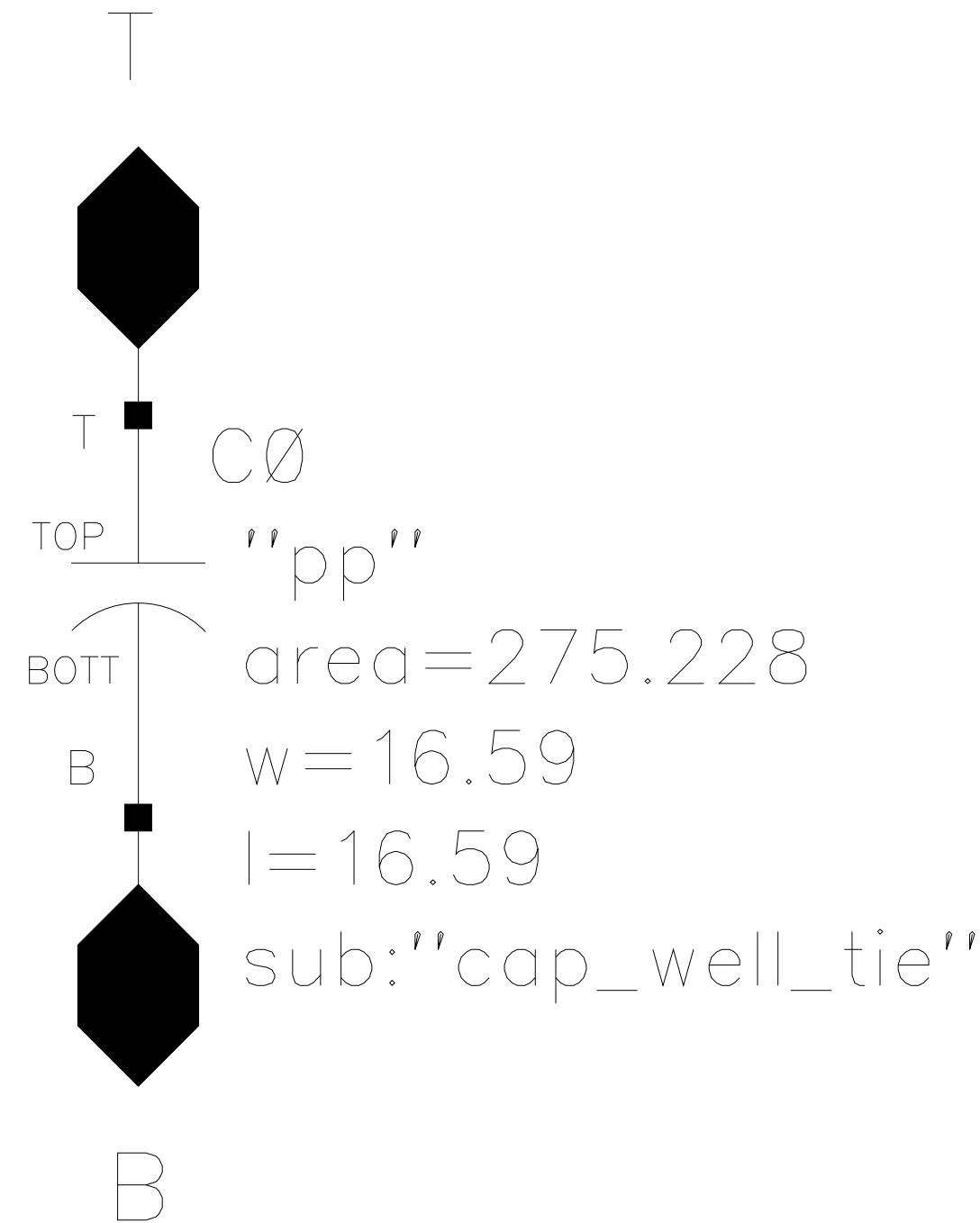
|=7

sub:’res\_sub\_tie’

OUTP

OUTP





CAGE NO.

DWG NO.

SH

1

REV

## REVISIONS

ZONE

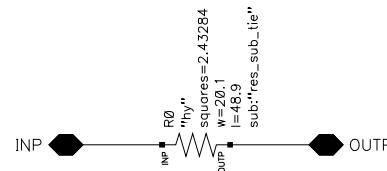
REV

DESCRIPTION

DATE

APPROVED

Resistor has  $l=48.9\mu$  and  $w=20.1\mu$



UPDATED

Jun 20 16:17:28 2005

DRAWN

CHECKED

CHECKED

ISSUED

SIZE  
A

CAGE NO.

DWG NO.

REV

SCALE

SHEET 1 OF 1

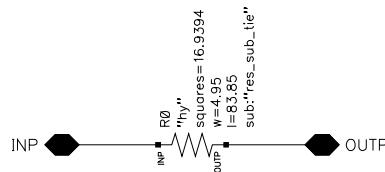
unit\_bias\_res

CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

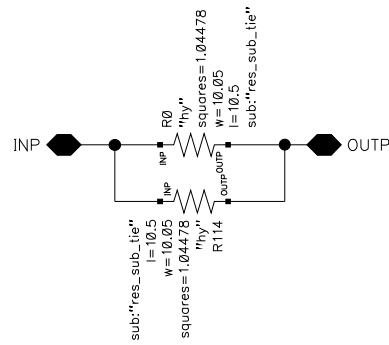
Resistor has  $l=83.85\mu$  and  $w=4.95\mu$



UPDATED Jun 20 16:20:31 2005	unit_bias_res_2		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO.
ISSUED	SCALE		REV
			SHEET 1 OF 1

	CAGE NO.	DWG NO.	SH	REV
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

Resistor has  $l=10.5\mu$  and  $w=10.05\mu$   $m=2$



UPDATED Aug 14 14:19:17 2007	unit_bias_res_3			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE			SHEET 1 OF 1

CAGE NO.

DWG NO.

SH

1

REV

## REVISIONS

ZONE

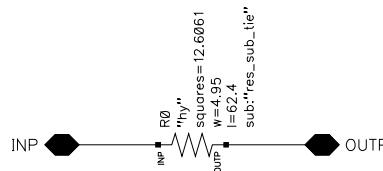
REV

DESCRIPTION

DATE

APPROVED

Resistor has  $l=62.4\mu$  and  $w=4.95\mu$



UPDATED

Jun 20 16:13:09 2005

DRAWN

CHECKED

CHECKED

ISSUED

unit\_cons\_current\_res

SIZE  
A

CAGE NO.

DWG NO.

REV

SCALE

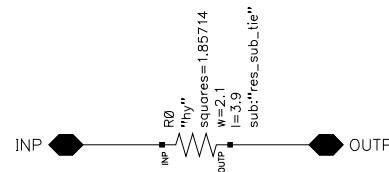
SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV
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REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

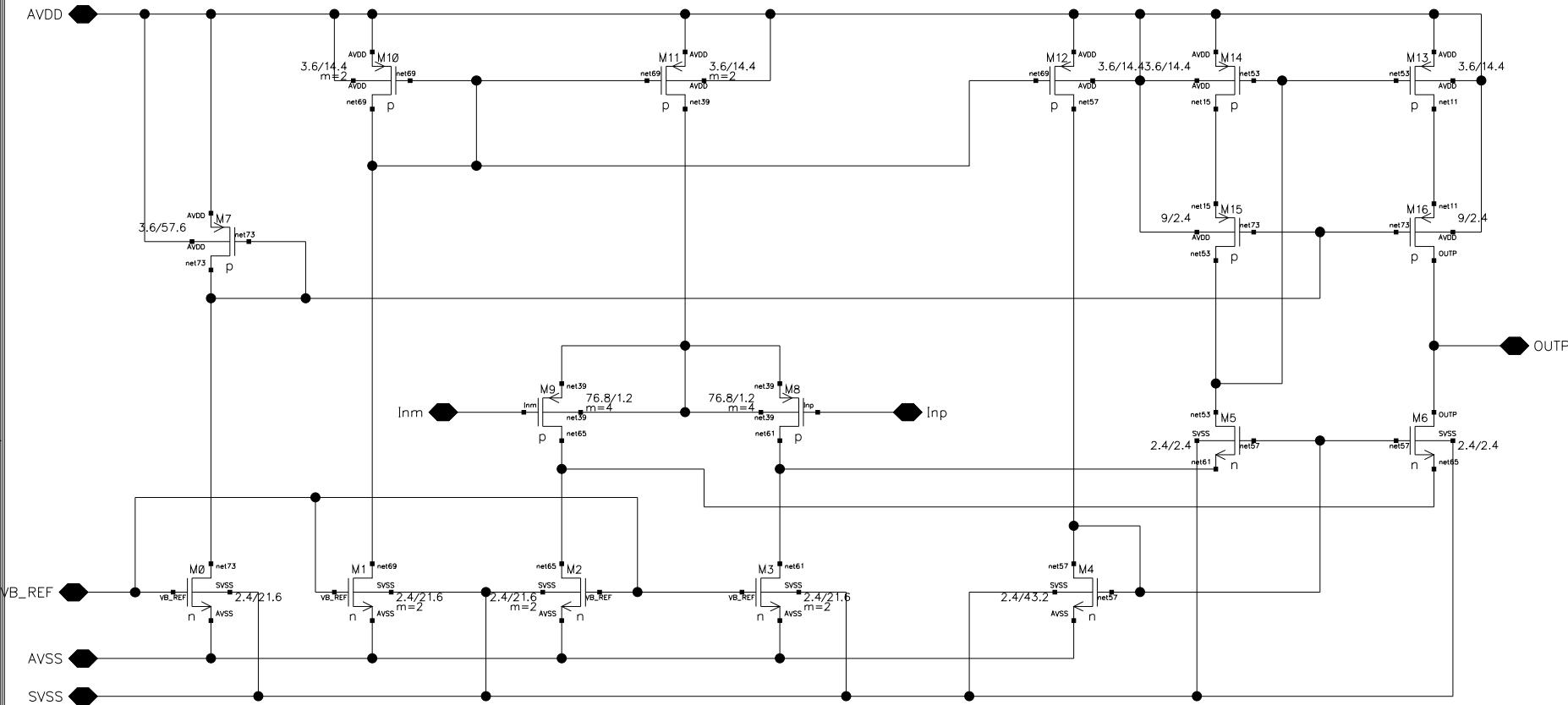
Resistor has  $l=3.9\mu$  and  $w=2.1\mu$



UPDATED Jun 30 15:19:07 2005	unit_hitlogic_res		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO.
ISSUED	SCALE		REV
			SHEET 1 OF 1

## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED

Jul 16 13:51:14 2007

vref\_buffer

DRAWN

CHECKED

CHECKED

ISSUED

SIZE  
A

CAGE NO.

DWG NO.

REV

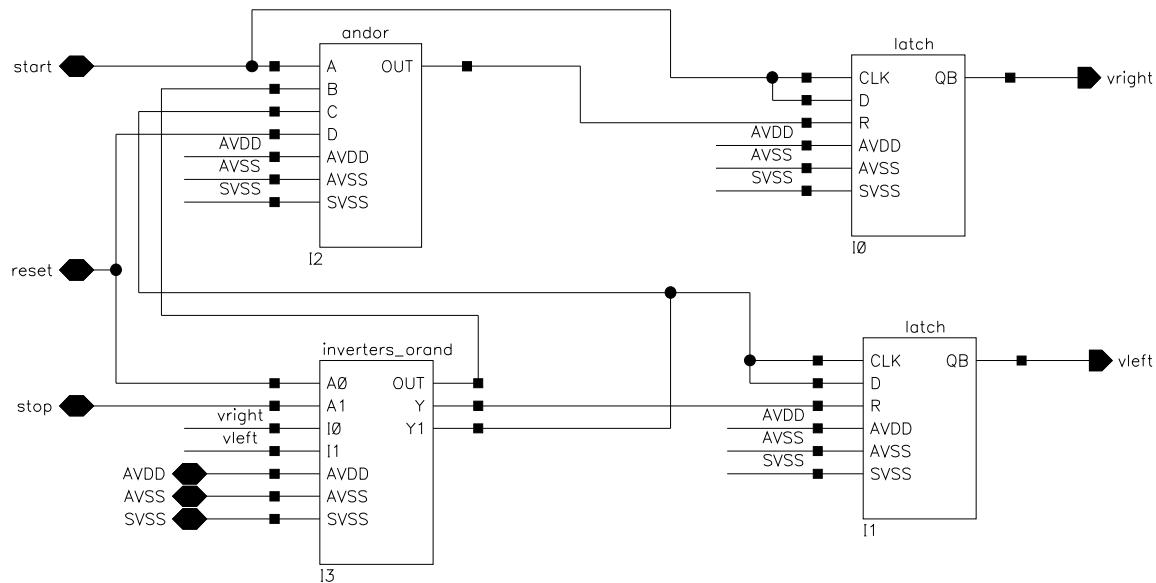
SCALE

SHEET

1 OF 1

## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED  
Jul 9 11:21:29 2007

width\_gen

DRAWN

CHECKED

CHECKED

ISSUED

SIZE	CAGE NO.	DWG NO.	REV
A			
SCALE			
SHEET		1 OF 1	

CAGE NO.

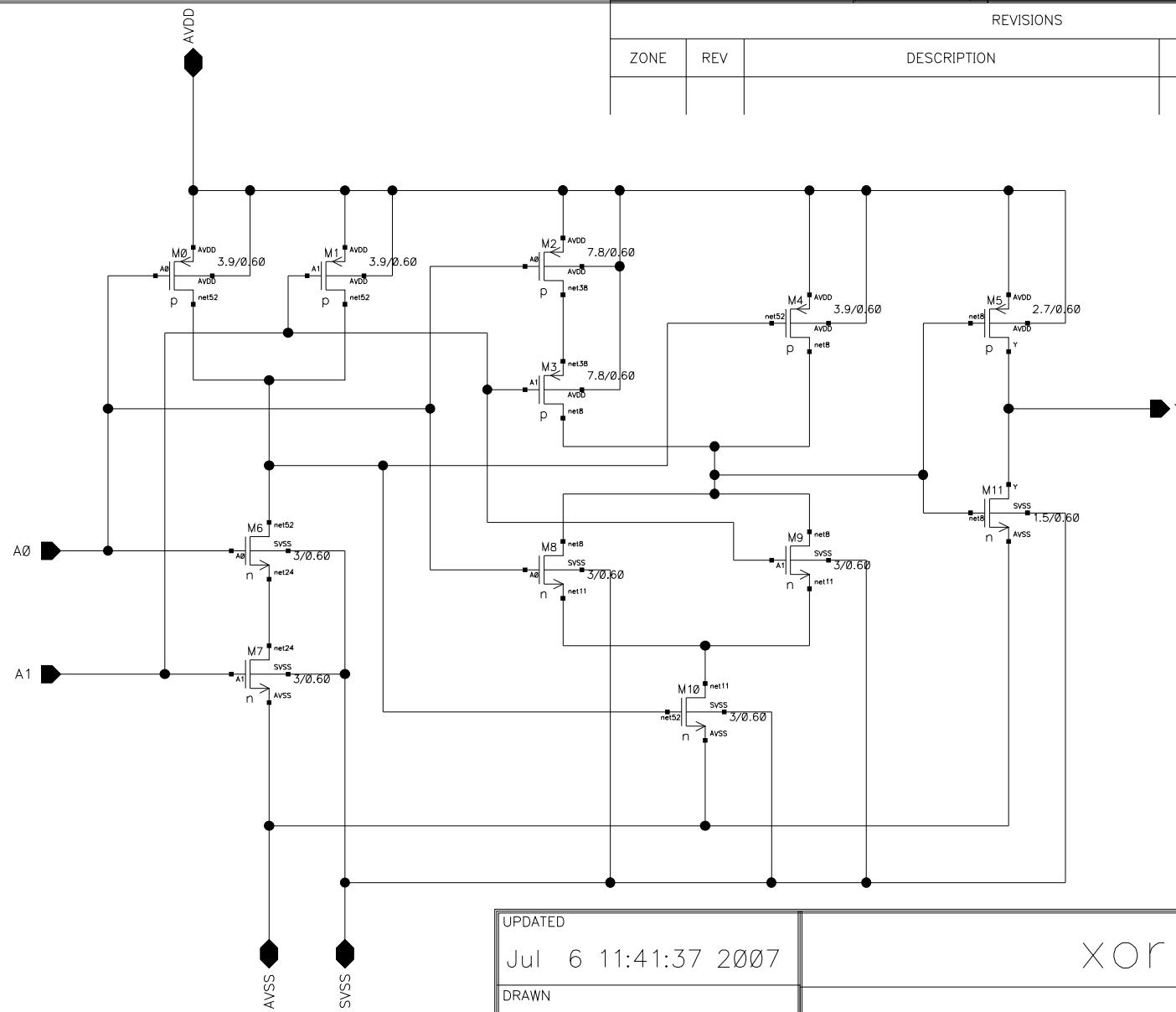
DWG NC

2

1

## REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED

Jul 6 11:41:37 2007

xor

DRAW

CHECKED

CHECKED

ISSUED

SIZ

E | CAGE NO

DWG NC

REV

SCA

SHEET 1 OF 1