

705-Carrier-Pinout-MASTER

Signal Name	Direction	Pin	b2b conn	carrier conn	\$\$\$\$\$\$\$\$
dummy_reset	Input	D9	dummy_reset	\$\$\$	
Led[0]	Output	A8	Led[0]	\$\$\$	
Led[1]	Output	L15	Led[1]	\$\$\$	
sys_clk	Input	P17	sys_clk	\$\$\$	
uart_rx	Input	R11	uart_rx	\$\$\$	
uart_tx	Output	L16	uart_tx	\$\$\$	
TSTAMP_CLK	Input	R10	JB1-86	J11-05	
TSTAMP_RST	Input	N17	JB1-91	J11-07	
COMMON_STOP	Input	L18	JB1-94	J11-08	
GLOB_ENA	Input	R12	JB1-92	J11-09	
EVENT_ENA	Input	M13	JB1-96	J11-10	
FORCE_RESET	Input	R13	JB1-88	J11-11	
TAKE_EVENT	Input	M18	JB1-98	J11-12	
SDO_B_0	Input	B12	JB1-99	J11-05	
SDO_C_0	Input	A18	JB1-44	J11-06	
SDO_T_0	Input	C14	JB1-87	J11-07	
SDO_A_1	Input	C16	JB1-81	J11-08	
SDO_B_1	Input	G17	JB1-71	J11-09	
SDO_C_1	Input	H17	JB1-69	J11-10	
SDO_T_1	Input	J13	JB1-57	J11-11	
ADC_SCLK_0	Output	K13	JB1-55	J11-12	
ADC_SCLK_1	Output	F18	JB1-47	J11-13	
CONV_0	Output	G18	JB1-45	J11-14	
CONV_1	Output	D18	JB1-37	J11-15	
DAC_LD	Output	E18	JB1-35	J11-16	
DAC_SCLK	Output	B17	JB1-46	J11-17	
DAC_DIN	Output	B18	JB1-42	J11-18	
cf_d_stb	Output	V12	JB2-14	J11-19	
cf_d_write	Output	N14	JB2-16	J11-20	
cf_d_neg_pol	Output	T11	JB2-32	J11-21	
cf_d_or	Input	T10	JB2-36	J11-22	
cf_d_reset	Output	H4	JB2-48	J11-23	
cf_d_global_ena	Output	E2	JB2-52	J11-24	
psd_sin	Output	G2	JB2-64	J11-25	
psd_sclk	Output	G6	JB2-66	J11-26	
psd_sout	Input	H2	JB2-62	J11-27	
psd_acq_ack_0	Input	D7	JB2-74	J11-28	
psd_acq_clk_0	Output	J4	JB2-46	J11-29	
psd_cf_d_out_0	Input	D2	JB2-54	J11-30	
psd_chan_addr_0[0]	BiDir	J5	JB2-99	J11-31	

705-Carrier-Pinout-MASTER

psd_chan_addr_0[1]	BiDir	B6	JB2-95	J11-32
psd_chan_addr_0[2]	BiDir	A4	JB2-87	J11-33
psd_chan_addr_0[3]	BiDir	A3	JB2-85	J11-34
psd_chan_addr_0[4]	BiDir	B2	JB2-81	J11-35
psd_dac_stb_0	Output	A1	JB2-77	J11-36
psd_intx_out_0	Input	E1	JB2-67	J11-37
psd_or_out_0	Input	C1	JB2-71	J11-38
psd_sc0_0	Output	H1	JB2-61	J11-39
psd_sc1_0	Output	G1	JB2-63	J11-40
psd_sel_ext_addr_0	Output	B14	JB1-93	J13-05
psd_test_mode_int_0	Output	B13	JB1-95	J13-06
psd_token_in_0	Output	A14	JB1-70	J13-07
psd_token_out_0	Input	C17	JB1-79	J13-08
psd_acq_ack_1	Input	D17	JB1-77	J13-09
psd_acq_clk_1	Output	E17	JB1-75	J13-10
psd_cfd_out_1	Input	J15	JB1-61	J13-11
psd_chan_addr_1[0]	BiDir	K15	JB1-59	J13-12
psd_chan_addr_1[1]	BiDir	H15	JB1-51	J13-13
psd_chan_addr_1[2]	BiDir	J14	JB1-49	J13-14
psd_chan_addr_1[3]	BiDir	J17	JB1-41	J13-15
psd_chan_addr_1[4]	BiDir	J18	JB1-39	J13-16
psd_dac_stb_1	Output	A15	JB1-58	J13-17
psd_intx_out_1	Input	A16	JB1-56	J13-18
psd_or_out_1	Input	D13	JB1-52	J13-19
psd_sc0_1	Output	D12	JB1-50	J13-20
psd_sc1_1	Output	B16	JB1-48	J13-21
psd_sel_ext_addr_1	Output	U12	JB2-12	J13-22
psd_test_mode_int_1	Output	P14	JB2-18	J13-23
psd_token_in_1	Output	H5	JB2-44	J13-24
psd_token_out_1	Input	F6	JB2-68	J13-25
psd_acq_all	Output	G4	JB2-56	J13-26
psd_cfd_bypass	Output	G3	JB2-58	J13-27
psd_force_rst	Output	E7	JB2-72	J13-28
psd_global_ena	Output	T9	JB2-38	J13-29
psd_reset	Output	H6	JB2-42	J13-30
psd_veto_reset	Output	K2	JB2-35	J13-31
TDC_SCLK	Output	B7	JB2-97	J13-32
TDC_DOUT	Input	U11	JB2-34	J13-33
TDC_DIN	Output	A5	JB2-91	J13-34
TDC_ENABLE	Output	B3	JB2-83	J13-35
TDC_CSB	Output	B1	JB2-75	J13-36
TDC_INTB	Input	C2	JB2-73	J13-37

705-Carrier-Pinout-MASTER

TDC_START	Output	F1	JB2-65	J13-38
TDC_STOP	Output	E3	JB2-55	J13-39
BUSY_OUT_L	Output	D3	JB2-57	J13-40
BOARD_ID[0]	Input	L4	JB1-3	J14-02
BOARD_ID[1]	Input	K5	JB1-5	J14-03
BOARD_ID[2]	Input	N6	JB1-9	J14-04
BOARD_ID[3]	Input	M6	JB1-11	J14-05
BOARD_ID[4]	Input	T8	JB1-15	J14-06
BOARD_ID[5]	Input	R8	JB1-17	J14-07
OR	Output	L6	JB1-21	J14-08
INTX_OUT	Output	L5	JB1-23	J14-09
DELAY_CLK	Output	P4	JB3-57	J2-05
DELAY_DATA	Output	P3	JB3-59	J2-06
DELAY_EN_L[0]	Output	N2	JB3-51	J2-07
DELAY_EN_L[1]	Output	N1	JB3-53	J2-08
DELAY_EN_L[2]	Output	M3	JB3-47	J2-09
DELAY_EN_L[3]	Output	M2	JB3-49	J2-10
DELAY_EN_L[4]	Output	T1	JB3-41	J2-11
DELAY_EN_L[5]	Output	R1	JB3-43	J2-12
I2C_SCL	BiDir	N16	JB2-23	J5-01
I2C_SDA	BiDir	M17	JB2-27	J5-02
CFD_OUT	Output	N15	JB2-21	J5-03
MUX_SEL[0]	Output	M16	JB2-25	J5-04
MUX_SEL[1]	Output	T14	JB2-22	J5-05
MUX_SEL[2]	Output	P15	JB2-26	J5-06
MUX_SEL[3]	Output	T15	JB2-24	J5-07
MUX_EN	Output	R15	JB2-28	J5-08
cfid_AD[7]	BiDir	F3	JB2-47	J6-01
cfid_AD[6]	BiDir	D5	JB2-51	J6-02
cfid_AD[5]	BiDir	F4	JB2-45	J6-03
cfid_AD[4]	BiDir	D4	JB2-53	J6-04
cfid_AD[3]	BiDir	J3	JB2-43	J6-05
cfid_AD[2]	BiDir	E5	JB2-33	J6-06
cfid_AD[1]	BiDir	J2	JB2-41	J6-07
cfid_AD[0]	BiDir	E6	JB2-31	J6-08

Cfg0

Signal Name	Direction	Pin	b2b_conn	carrier_conn	NO_USE
dummy_reset	Input	D9	dummy_reset	\$\$\$	
Led[0]	Output	A8	Led[0]	\$\$\$	
Led[1]	Output	L15	Led[1]	\$\$\$	
sys_clk	Input	P17	sys_clk	\$\$\$	
uart_rx	Input	R11	uart_rx	\$\$\$	
uart_tx	Output	L16	uart_tx	\$\$\$	
?	?	R10	JB1-86	J1-05	X
?	?	N17	JB1-91	J1-07	X
?	?	L18	JB1-94	J1-08	X
?	?	R12	JB1-92	J1-09	X
?	?	M13	JB1-96	J1-10	X
?	?	R13	JB1-88	J1-11	X
?	?	M18	JB1-98	J1-12	X
BOARD_ID[0]	Input	B12	JB1-99	J11-05	
BOARD_ID[1]	Input	A18	JB1-44	J11-06	
BOARD_ID[2]	Input	C14	JB1-87	J11-07	
BOARD_ID[3]	Input	C16	JB1-81	J11-08	
BOARD_ID[4]	Input	G17	JB1-71	J11-09	
BOARD_ID[5]	Input	H17	JB1-69	J11-10	
DELAY_CLK	Output	J13	JB1-57	J11-11	
DELAY_DATA	Output	K13	JB1-55	J11-12	
DELAY_EN_L[0]	Output	F18	JB1-47	J11-13	
DELAY_EN_L[1]	Output	G18	JB1-45	J11-14	
DELAY_EN_L[2]	Output	D18	JB1-37	J11-15	
DELAY_EN_L[3]	Output	E18	JB1-35	J11-16	
DELAY_EN_L[4]	Output	B17	JB1-46	J11-17	
DELAY_EN_L[5]	Output	B18	JB1-42	J11-18	
I2C_SCL	BiDir	V12	JB2-14	J11-19	
I2C_SDA	BiDir	N14	JB2-16	J11-20	
SDO_T_0	Input	T11	JB2-32	J11-21	
ADC_SCLK_0	Output	T10	JB2-36	J11-22	
CONV_0	Output	H4	JB2-48	J11-23	
psd_sin	Output	E2	JB2-52	J11-24	
psd_sclk	Output	G2	JB2-64	J11-25	
I2C_SCL	BiDir	G6	JB2-66	J11-26	
I2C_SDA	BiDir	H2	JB2-62	J11-27	
?	?	D7	JB2-74	J11-28	X
?	?	J4	JB2-46	J11-29	X

Cfg0

?	?	D2	JB2-54	J11-30	X
?	?	J5	JB2-99	J11-31	X
?	?	B6	JB2-95	J11-32	X
?	?	A4	JB2-87	J11-33	X
?	?	A3	JB2-85	J11-34	X
?	?	B2	JB2-81	J11-35	X
?	?	A1	JB2-77	J11-36	X
?	?	E1	JB2-67	J11-37	X
?	?	C1	JB2-71	J11-38	X
?	?	H1	JB2-61	J11-39	X
?	?	G1	JB2-63	J11-40	X
?	?	B14	JB1-93	J13-05	X
?	?	B13	JB1-95	J13-06	X
?	?	A14	JB1-70	J13-07	X
?	?	C17	JB1-79	J13-08	X
?	?	D17	JB1-77	J13-09	X
?	?	E17	JB1-75	J13-10	X
?	?	J15	JB1-61	J13-11	X
?	?	K15	JB1-59	J13-12	X
?	?	H15	JB1-51	J13-13	X
?	?	J14	JB1-49	J13-14	X
?	?	J17	JB1-41	J13-15	X
?	?	J18	JB1-39	J13-16	X
?	?	A15	JB1-58	J13-17	X
?	?	A16	JB1-56	J13-18	X
?	?	D13	JB1-52	J13-19	X
?	?	D12	JB1-50	J13-20	X
?	?	B16	JB1-48	J13-21	X
?	?	U12	JB2-12	J13-22	X
?	?	P14	JB2-18	J13-23	X
?	?	H5	JB2-44	J13-24	X
?	?	F6	JB2-68	J13-25	X
?	?	G4	JB2-56	J13-26	X
?	?	G3	JB2-58	J13-27	X
?	?	E7	JB2-72	J13-28	X
?	?	T9	JB2-38	J13-29	X
?	?	H6	JB2-42	J13-30	X
?	?	K2	JB2-35	J13-31	X
?	?	B7	JB2-97	J13-32	X
?	?	U11	JB2-34	J13-33	X
?	?	A5	JB2-91	J13-34	X

Cfg0

?	?	B3	JB2-83	J13-35	X
?	?	B1	JB2-75	J13-36	X
?	?	C2	JB2-73	J13-37	X
?	?	F1	JB2-65	J13-38	X
?	?	E3	JB2-55	J13-39	X
?	?	D3	JB2-57	J13-40	X

JCONN_PAIRS

R10	JB1-86	J1-05	TSTAMP_CLK
N17	JB1-91	J1-07	TSTAMP_RST
L18	JB1-94	J1-08	COMMON_STOP
R12	JB1-92	J1-09	GLOB_ENA
M13	JB1-96	J1-10	EVENT_ENA
R13	JB1-88	J1-11	FORCE_RESET
M18	JB1-98	J1-12	TAKE_EVENT
B12	JB1-99	J11-05	SDO_B_0
A18	JB1-44	J11-06	SDO_C_0
C14	JB1-87	J11-07	SDO_T_0
C16	JB1-81	J11-08	SDO_A_1
G17	JB1-71	J11-09	SDO_B_1
H17	JB1-69	J11-10	SDO_C_1
J13	JB1-57	J11-11	SDO_T_1
K13	JB1-55	J11-12	ADC_SCLK_0
F18	JB1-47	J11-13	ADC_SCLK_1
G18	JB1-45	J11-14	CONV_0
D18	JB1-37	J11-15	CONV_1
E18	JB1-35	J11-16	DAC_LD
B17	JB1-46	J11-17	DAC_SCLK
B18	JB1-42	J11-18	DAC_DIN
V12	JB2-14	J11-19	cfid_stb
N14	JB2-16	J11-20	cfid_write
T11	JB2-32	J11-21	cfid_neg_pol
T10	JB2-36	J11-22	cfid_or
H4	JB2-48	J11-23	cfid_reset
E2	JB2-52	J11-24	cfid_global_ena
G2	JB2-64	J11-25	psd_sin
G6	JB2-66	J11-26	psd_sclk
H2	JB2-62	J11-27	psd_sout
D7	JB2-74	J11-28	psd_acq_ack_0
J4	JB2-46	J11-29	psd_acq_clk_0
D2	JB2-54	J11-30	psd_cfid_out_0
J5	JB2-99	J11-31	psd_chan_addr_0[0]
B6	JB2-95	J11-32	psd_chan_addr_0[1]
A4	JB2-87	J11-33	psd_chan_addr_0[2]
A3	JB2-85	J11-34	psd_chan_addr_0[3]
B2	JB2-81	J11-35	psd_chan_addr_0[4]
A1	JB2-77	J11-36	psd_dac_stb_0
E1	JB2-67	J11-37	psd_intx_out_0
C1	JB2-71	J11-38	psd_or_out_0

JCONN_PAIRS

H1	JB2-61	J11-39	psd_sc0_0
G1	JB2-63	J11-40	psd_sc1_0
B14	JB1-93	J13-05	psd_sel_ext_addr_0
B13	JB1-95	J13-06	psd_test_mode_int_0
A14	JB1-70	J13-07	psd_token_in_0
C17	JB1-79	J13-08	psd_token_out_0
D17	JB1-77	J13-09	psd_acq_ack_1
E17	JB1-75	J13-10	psd_acq_clk_1
J15	JB1-61	J13-11	psd_cfd_out_1
K15	JB1-59	J13-12	psd_chan_addr_1[0]
H15	JB1-51	J13-13	psd_chan_addr_1[1]
J14	JB1-49	J13-14	psd_chan_addr_1[2]
J17	JB1-41	J13-15	psd_chan_addr_1[3]
J18	JB1-39	J13-16	psd_chan_addr_1[4]
A15	JB1-58	J13-17	psd_dac_stb_1
A16	JB1-56	J13-18	psd_intx_out_1
D13	JB1-52	J13-19	psd_or_out_1
D12	JB1-50	J13-20	psd_sc0_1
B16	JB1-48	J13-21	psd_sc1_1
U12	JB2-12	J13-22	psd_sel_ext_addr_1
P14	JB2-18	J13-23	psd_test_mode_int_1
H5	JB2-44	J13-24	psd_token_in_1
F6	JB2-68	J13-25	psd_token_out_1
G4	JB2-56	J13-26	psd_acq_all
G3	JB2-58	J13-27	psd_cfd_bypass
E7	JB2-72	J13-28	psd_force_rst
T9	JB2-38	J13-29	psd_global_ena
H6	JB2-42	J13-30	psd_reset
K2	JB2-35	J13-31	psd_veto_reset
B7	JB2-97	J13-32	TDC_SCLK
U11	JB2-34	J13-33	TDC_DOUT
A5	JB2-91	J13-34	TDC_DIN
B3	JB2-83	J13-35	TDC_ENABLE
B1	JB2-75	J13-36	TDC_CSB
C2	JB2-73	J13-37	TDC_INTB
F1	JB2-65	J13-38	TDC_START
E3	JB2-55	J13-39	TDC_STOP
D3	JB2-57	J13-40	BUSY_OUT_L
L4	JB1-3	J14-02	BOARD_ID[0]
K5	JB1-5	J14-03	BOARD_ID[1]
N6	JB1-9	J14-04	BOARD_ID[2]
M6	JB1-11	J14-05	BOARD_ID[3]

JCONN_PAIRS

T8	JB1-15	J14-06	BOARD_ID[4]
R8	JB1-17	J14-07	BOARD_ID[5]
L6	JB1-21	J14-08	OR
L5	JB1-23	J14-09	INTX_OUT
P4	JB3-57	J2-05	DELAY_CLK
P3	JB3-59	J2-06	DELAY_DATA
N2	JB3-51	J2-07	DELAY_EN_L[0]
N1	JB3-53	J2-08	DELAY_EN_L[1]
M3	JB3-47	J2-09	DELAY_EN_L[2]
M2	JB3-49	J2-10	DELAY_EN_L[3]
T1	JB3-41	J2-11	DELAY_EN_L[4]
R1	JB3-43	J2-12	DELAY_EN_L[5]
N16	JB2-23	J5-01	I2C_SCL
M17	JB2-27	J5-02	I2C_SDA
N15	JB2-21	J5-03	CFD_OUT
M16	JB2-25	J5-04	MUX_SEL[0]
T14	JB2-22	J5-05	MUX_SEL[1]
P15	JB2-26	J5-06	MUX_SEL[2]
T15	JB2-24	J5-07	MUX_SEL[3]
R15	JB2-28	J5-08	MUX_EN
F3	JB2-47	J6-01	cfid_AD[7]
D5	JB2-51	J6-02	cfid_AD[6]
F4	JB2-45	J6-03	cfid_AD[5]
D4	JB2-53	J6-04	cfid_AD[4]
J3	JB2-43	J6-05	cfid_AD[3]
E5	JB2-33	J6-06	cfid_AD[2]
J2	JB2-41	J6-07	cfid_AD[1]
E6	JB2-31	J6-08	cfid_AD[0]

Input
Input
Input
Input
Input
Input
Input
Input
Input
Input
Input
Input
Input
Input
Output
Output
Output
Output
Output
Output
Output
Output
Output
Output
Output
Input
Output
Output
Output
Output
Input
Input
Output
Input
BiDir
BiDir
BiDir
BiDir
BiDir
Output
Input
Input

JCONN_PAIRS

Output
Output
Output
Output
Output
Input
Input
Output
Input
BiDir
BiDir
BiDir
BiDir
BiDir
Output
Input
Input
Output
Output
Output
Output
Output
Output
Input
Output
Output
Output
Output
Output
Output
Output
Output
Output
Output
Input
Output
Output
Output
Input
Output
Output
Output
Input
Input
Input
Input
Input

JCONN_PAIRS

Input
Input
Output
Output
Output
Output
Output
Output
Output
Output
Output
Output
BiDir
BiDir
Output
Output
Output
Output
Output
Output
BiDir
BiDir
BiDir
BiDir
BiDir
BiDir
BiDir
BiDir