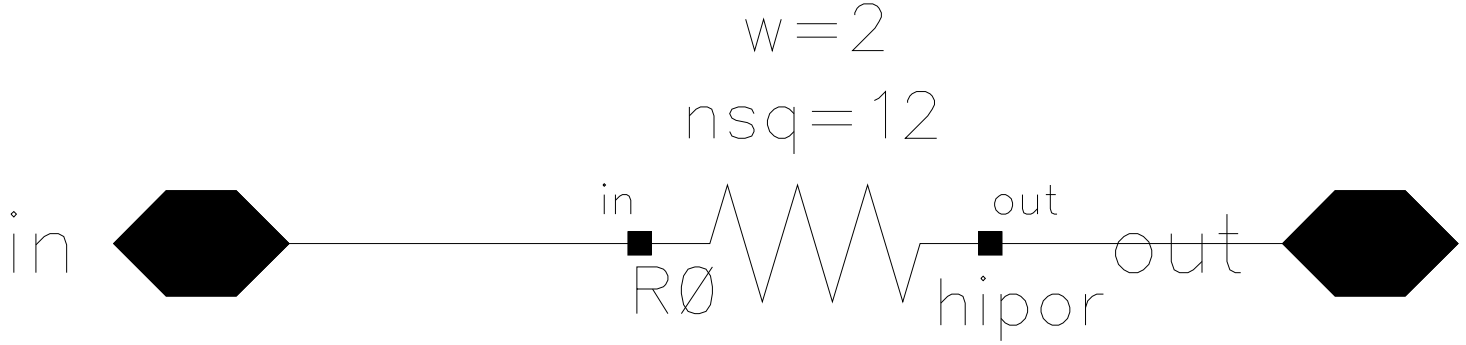
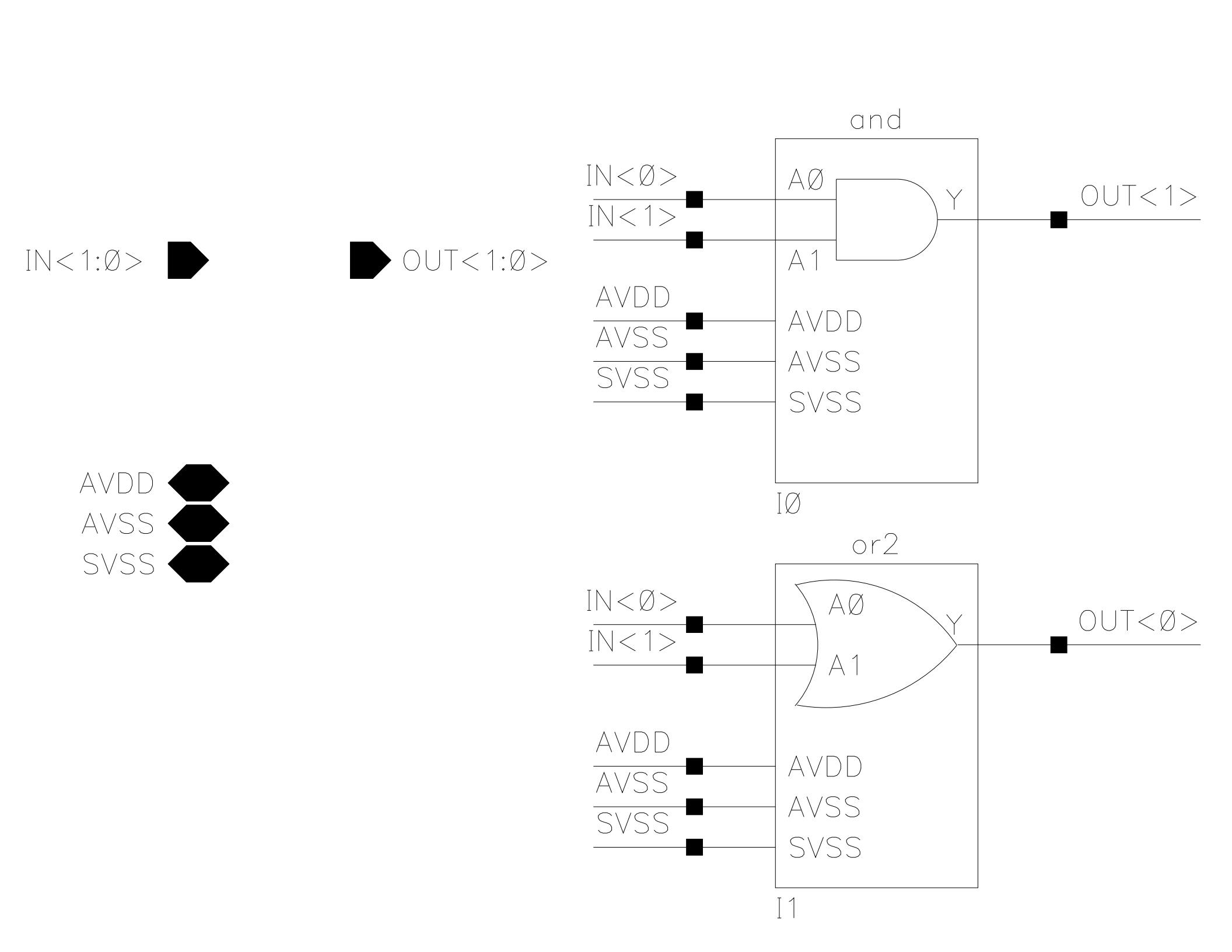
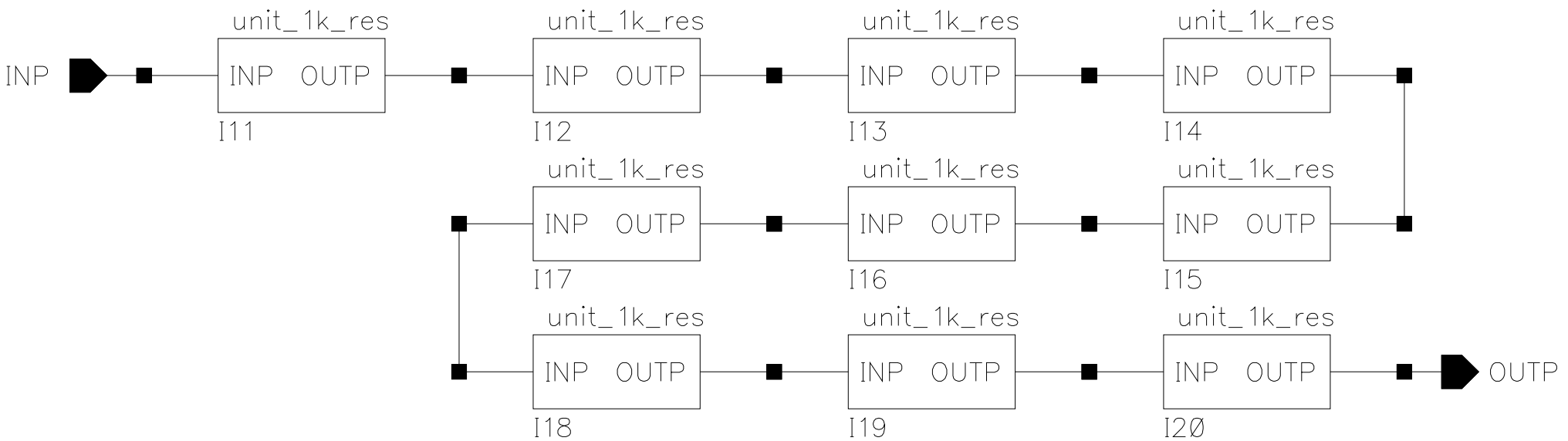

w=2
nsq=12
in
in
out
RØ
hipor
out

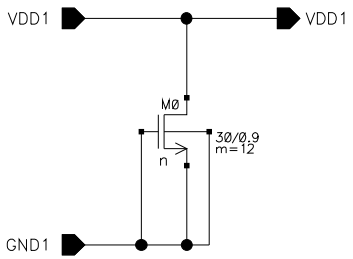

IN<1:0>
OUT<1:0>
AVDD
AVSS
SVSS
and
IN<0>
IN<1>
A0
A1
Y
OUT<1>
AVDD
AVSS
SVSS
AVDD
AVSS
SVSS
I0
or2
IN<0>
IN<1>
A0
A1
Y
OUT<0>
AVDD
AVSS
SVSS
AVDD
AVSS
SVSS
I1


INP
unit_1k_res
INP OUTP
I11
unit_1k_res
INP OUTP
I12
unit_1k_res
INP OUTP
I13
unit_1k_res
INP OUTP
I14
unit_1k_res
INP OUTP
I15
unit_1k_res
INP OUTP
I16
unit_1k_res
INP OUTP
I17
unit_1k_res
INP OUTP
I18
unit_1k_res
INP OUTP
I19
unit_1k_res
INP OUTP
I2Ø
OUTP

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

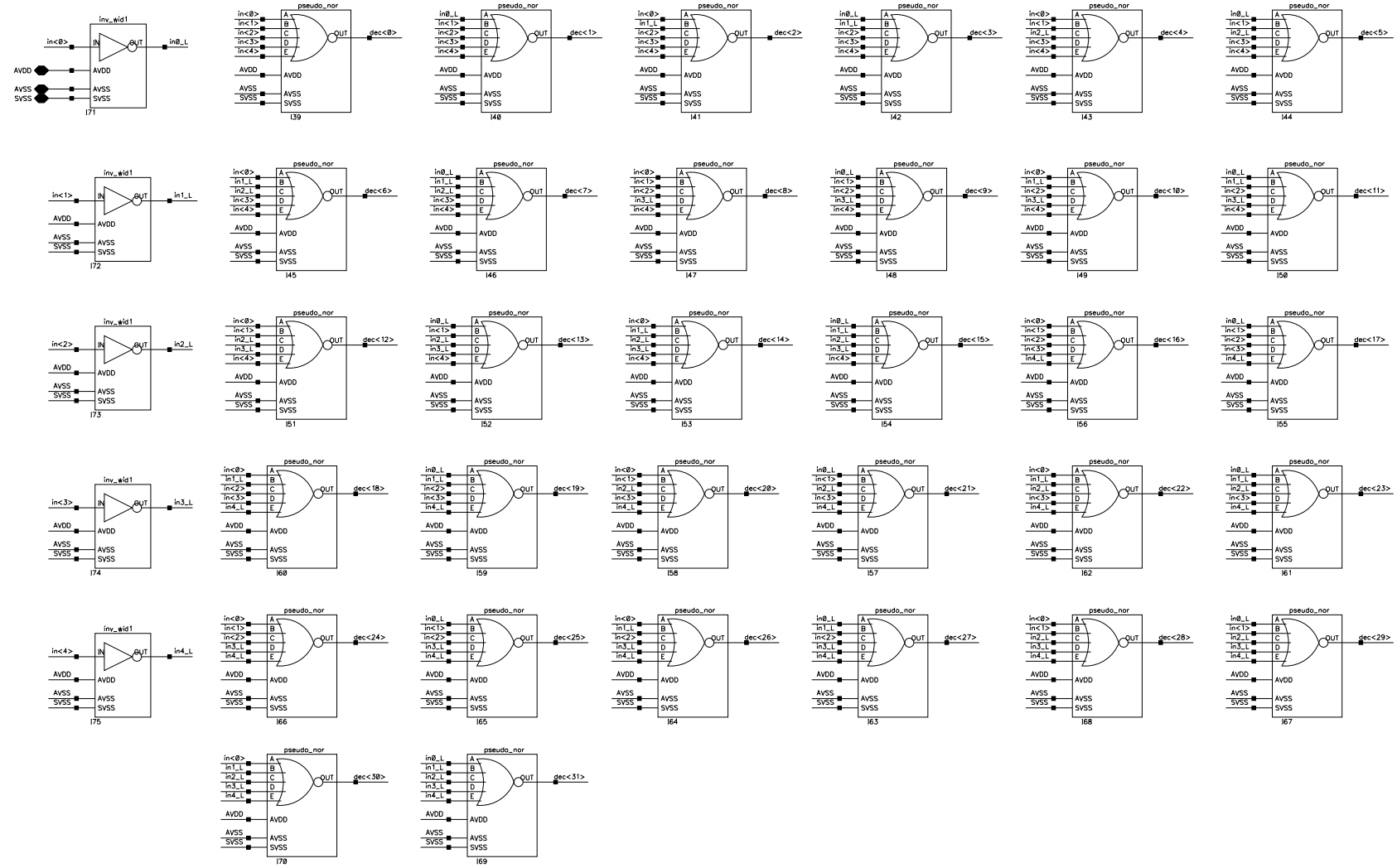


UPDATED Nov 11 15:36:54 2004	PadVdd			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

in<4:0>

dec<31:0>



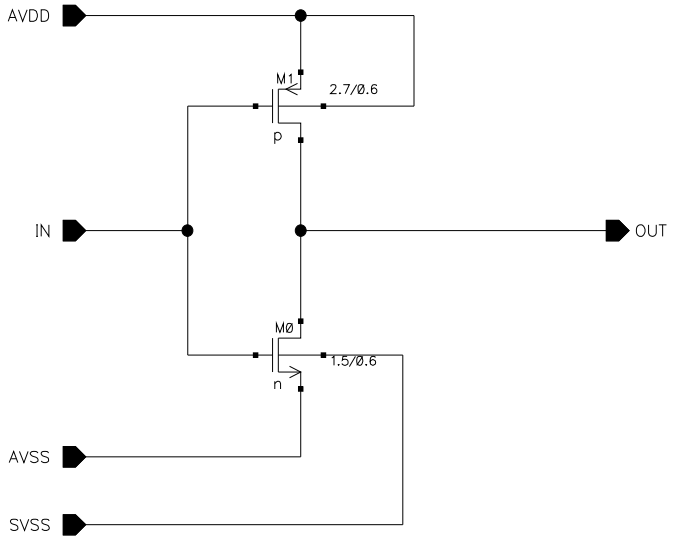
UPDATED	dec5to32
Jun 25 14:18:49 2010	
DRAWN	
CHECKED	
CHECKED	SIZE C · CAGE NO. · DWG NO. · REV
ISSUED	SCALE · SHEET 1 OF 1

REV · SH 1 · DWG NO. · CAGE NO.

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

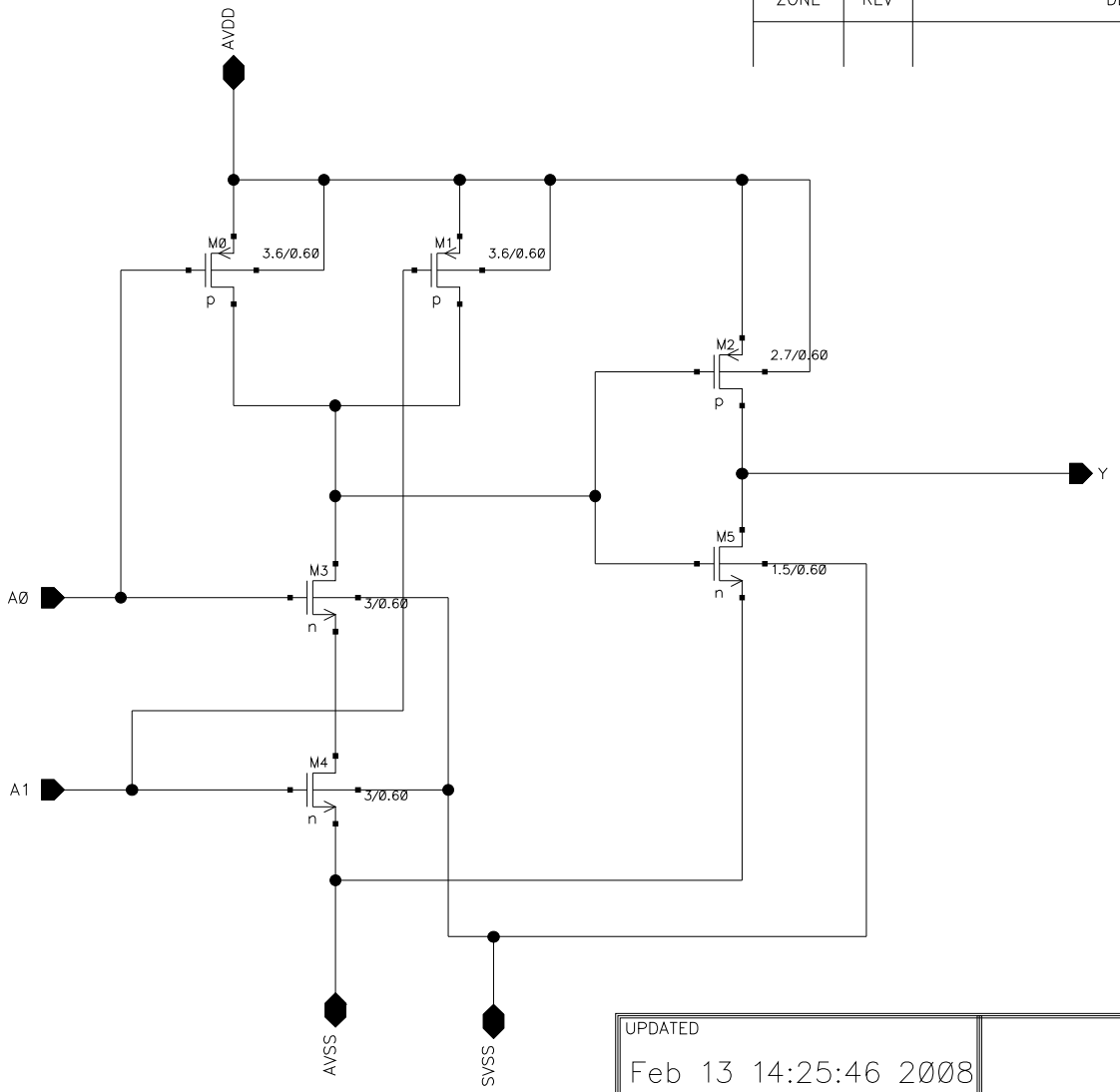


UPDATED Jul 5 15:27:12 2007	inv_wid1			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

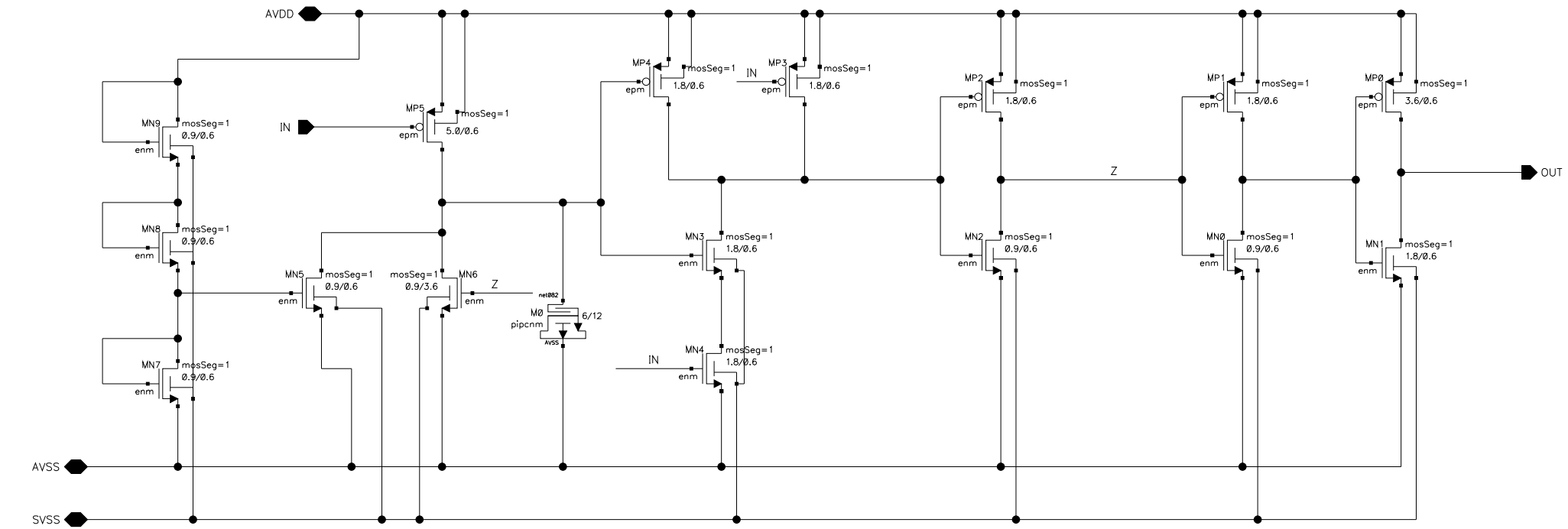
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



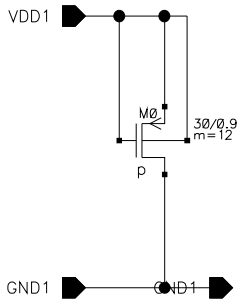
UPDATED Feb 13 14:25:46 2008	and			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


AVDD
IN
MP5
mosSeg=1
5.0/0.6
epm
MP4
1.8/0.6
MP3
MP2
MP1
MP0
3.6/0.6
MN9
0.9/0.6
MN8
MN7
MN5
MN6
0.9/3.6
MN3
1.8/0.6
MN4
MN2
MN0
MN1
enm
Z
M0
pipcnm
6/12
net082
AVSS
SVSS
OUT

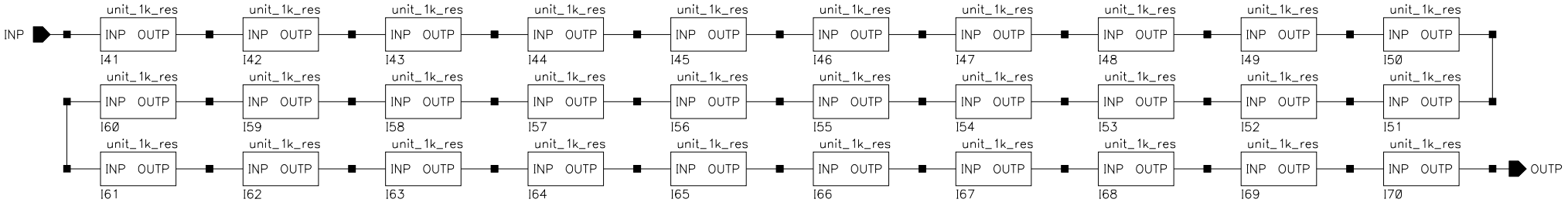
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



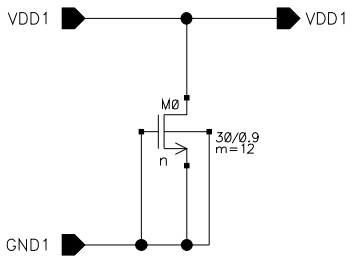
UPDATED Nov 11 15:38:19 2ØØ4	PadGnd			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


INP
unit_1k_res
INP OUTP
I41
I42
I43
I44
I45
I46
I47
I48
I49
I50
I60
I59
I58
I57
I56
I55
I54
I53
I52
I51
I61
I62
I63
I64
I65
I66
I67
I68
I69
I70
OUTP

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

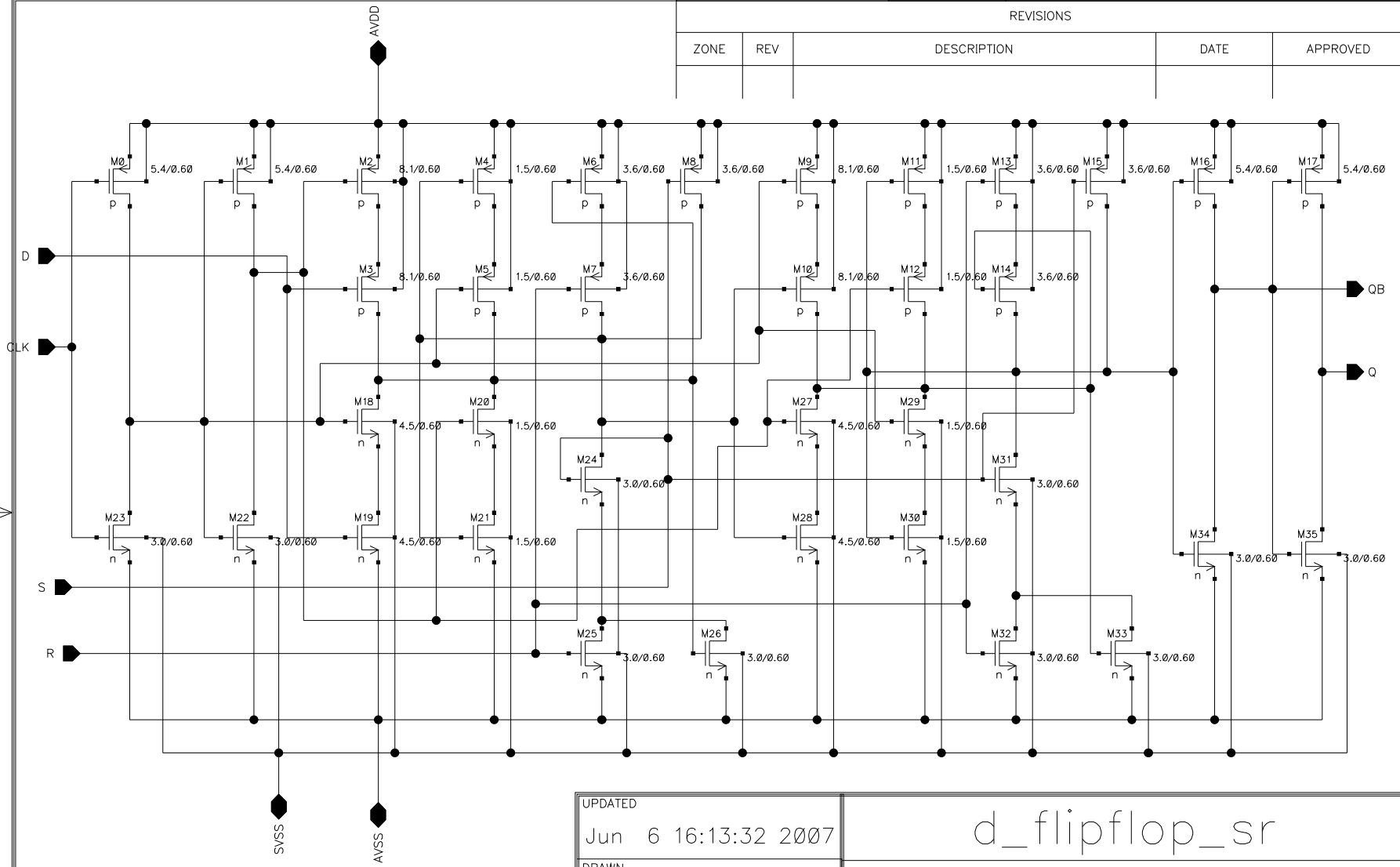


UPDATED Nov 11 15:36:54 2004	PadVdd			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	Jun 6 16:13:32 2007
DRAWN	
CHECKED	
CHECKED	
ISSUED	

d_flipflop_sr

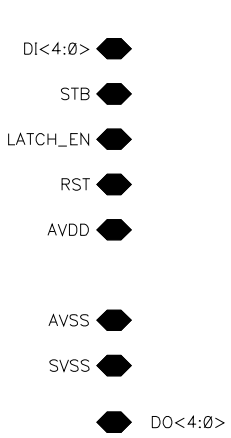
SIZE	CAGE NO.	DWG NO.	REV
A			

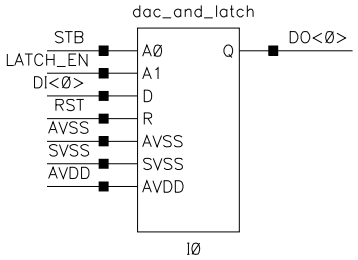
SCALE		SHEET 1 OF 1

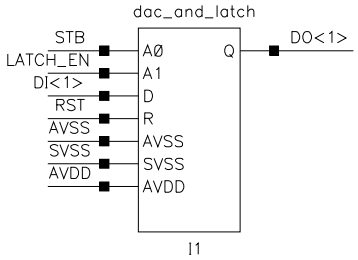
CAGE NO.	DWG NO.	SH 1	REV

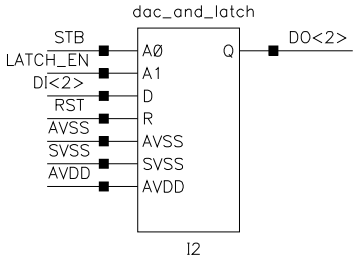
REVISIONS

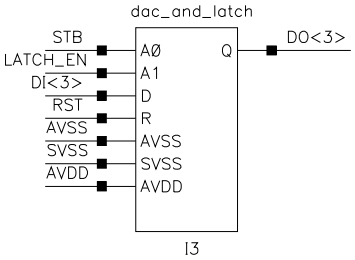
ZONE	REV	DESCRIPTION	DATE	APPROVED

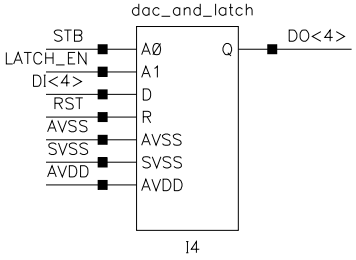










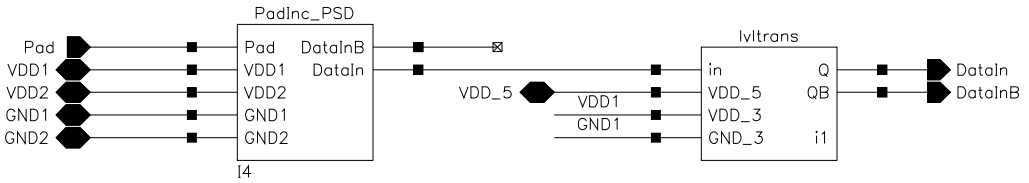


UPDATED Mar 16 13:32:09 2010	le_dac_reg		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

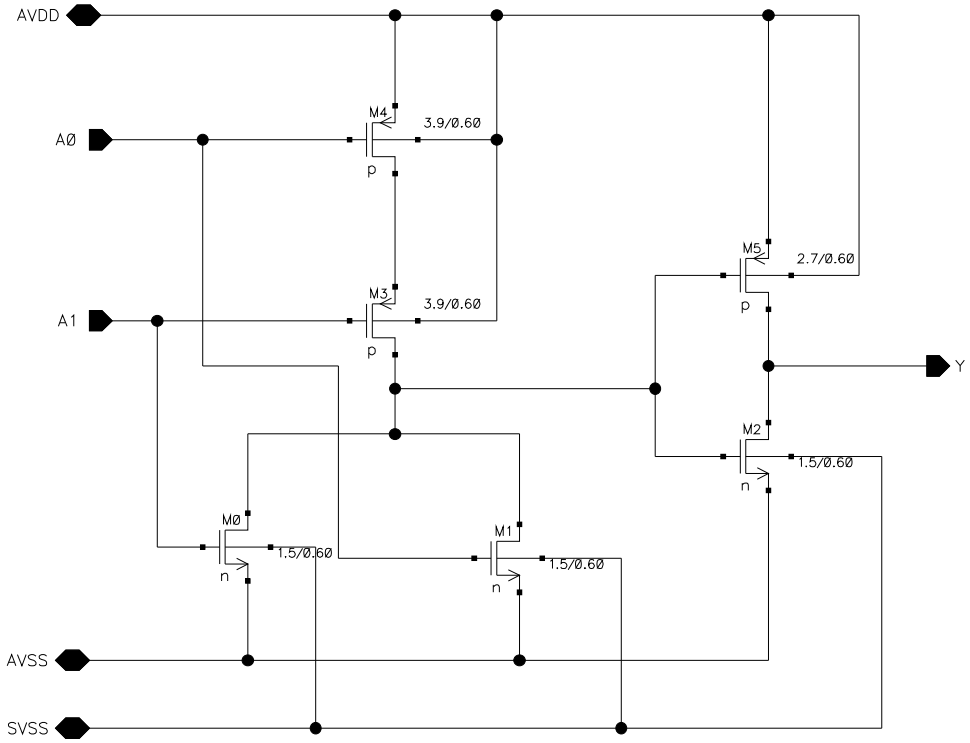


UPDATED Mar 2 14:45:17 2017	PadInc		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

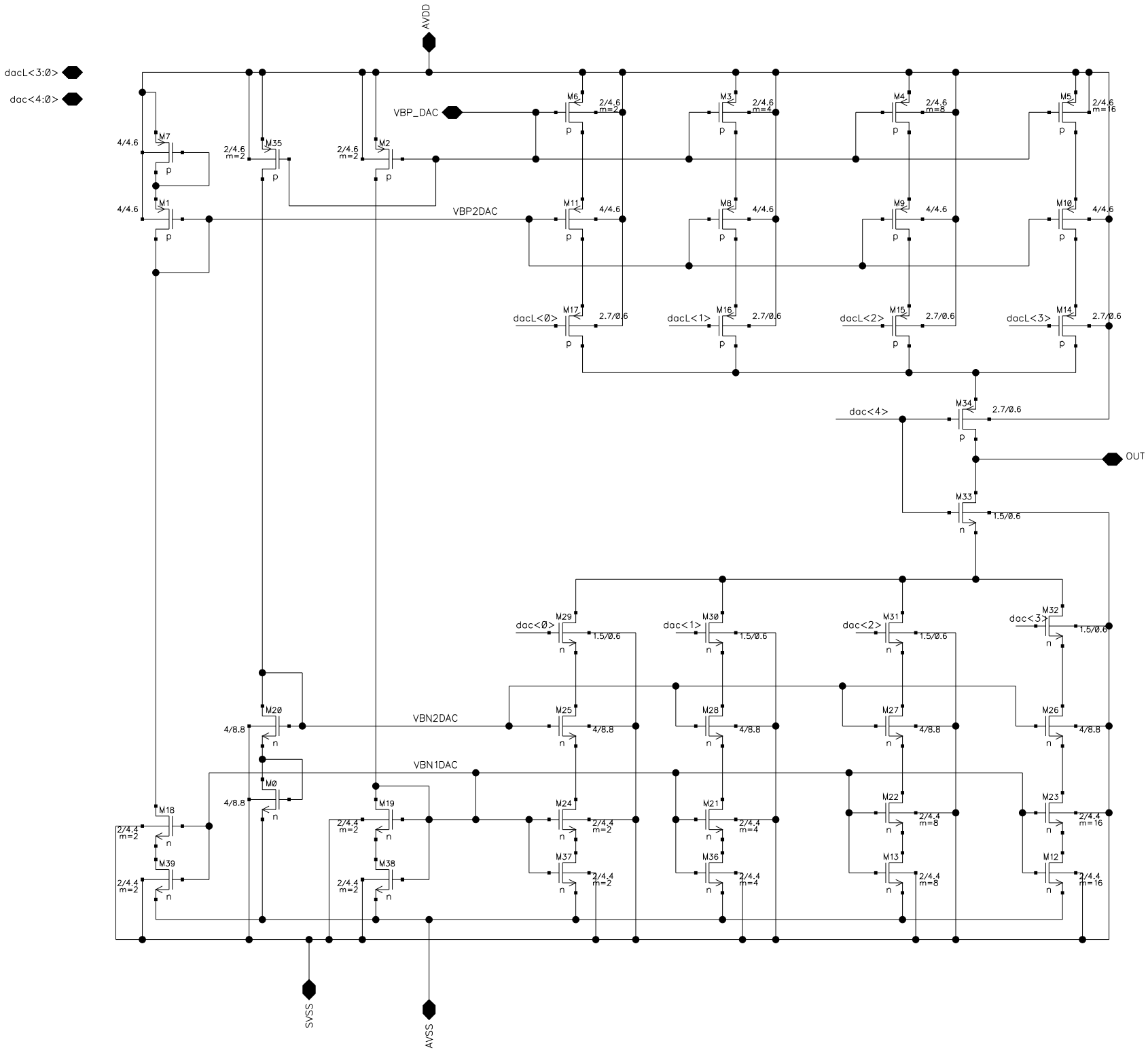
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

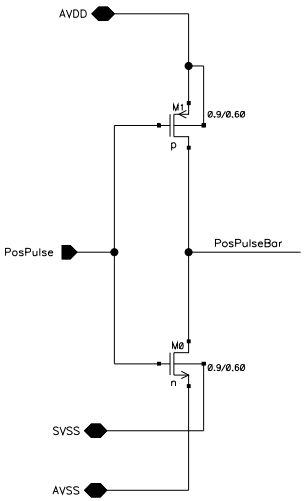


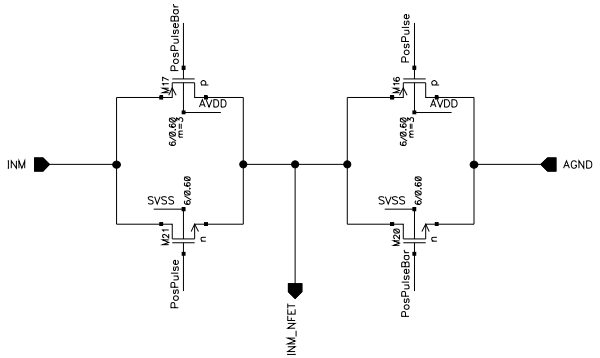
UPDATED Jun 11 15:23:02 2007	Or			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

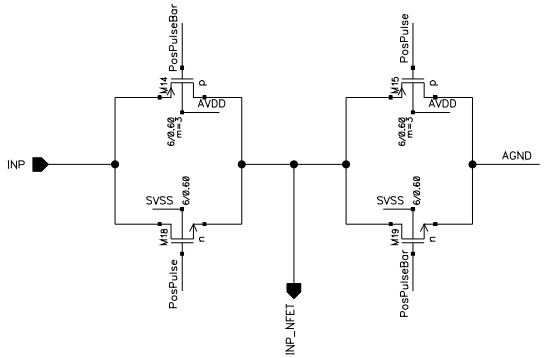

AVDD
dacL<3:0>
dac<4:0>
VBP_DAC
VBP2DAC
VBN2DAC
VBN1DAC
OUT
SVSS
AVSS
M6
M3
M4
M5
M7
M35
M2
M1
M11
M8
M9
M10
M17
M16
M15
M14
dacL<0>
dacL<1>
dacL<2>
dacL<3>
M34
dac<4>
M33
M29
M30
M31
M32
dac<0>
dac<1>
dac<2>
dac<3>
M20
M0
M25
M28
M27
M26
M18
M19
M24
M21
M22
M23
M39
M38
M37
M36
M13
M12
2/4.6
m=2
m=4
m=8
m=16
4/4.6
2.7/0.6
1.5/0.6
4/8.8
2/4.4
p
n

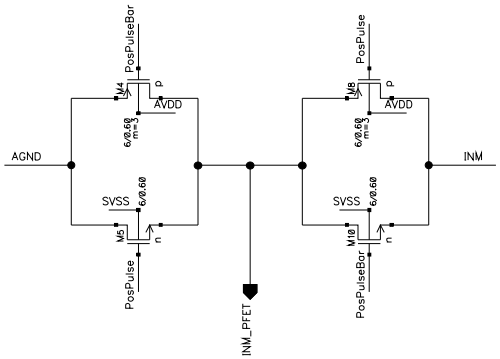
CAGE NO.	DWG NO.	SH	REV
		1	

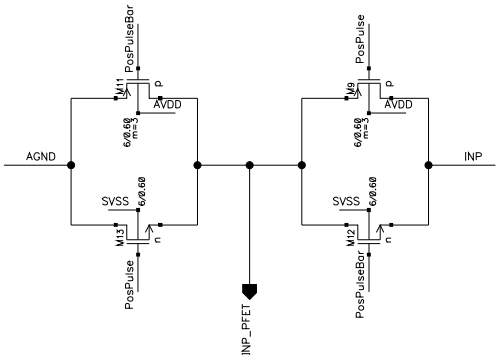
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



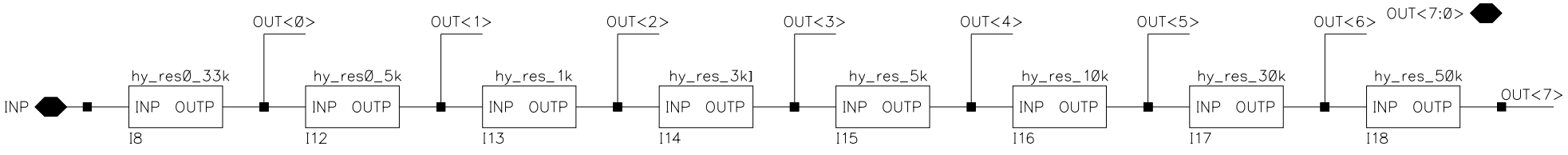






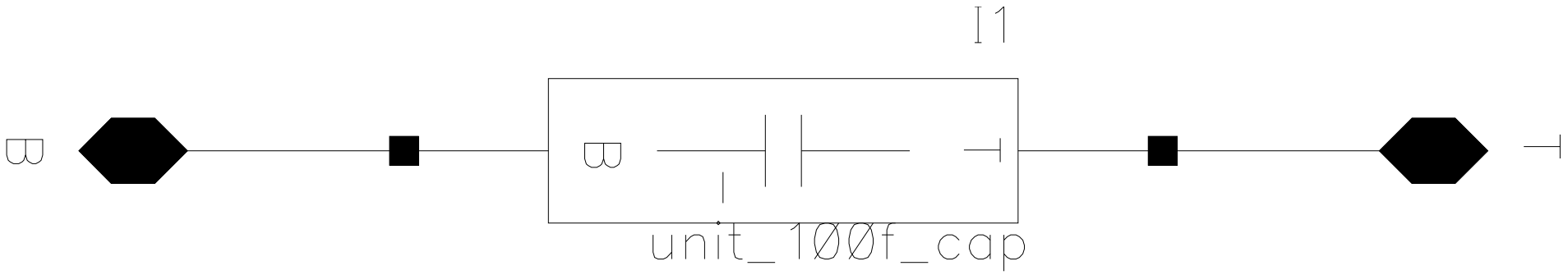


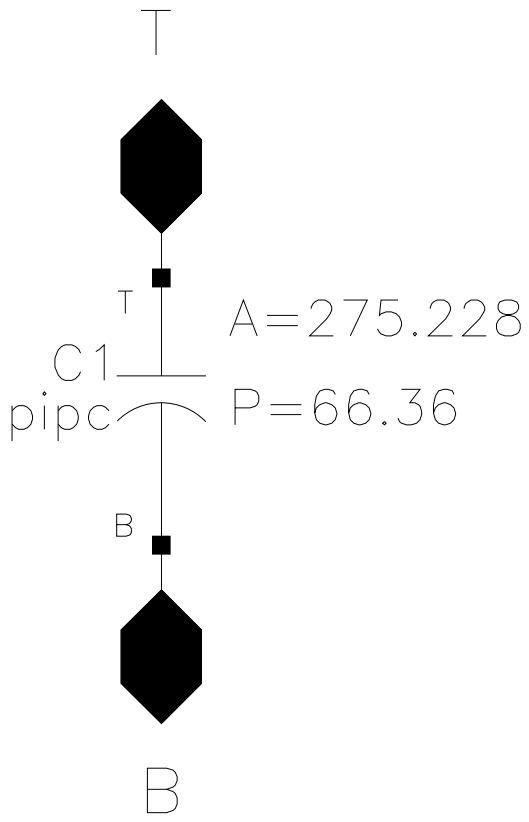
UPDATED			
Aug 7 16:55:04 2007			
DRAWN			
CHECKED			
CHECKED	SIZE B	CAGE NO.	DWG NO. REV
ISSUED	SCALE		SHEET 1 OF 1

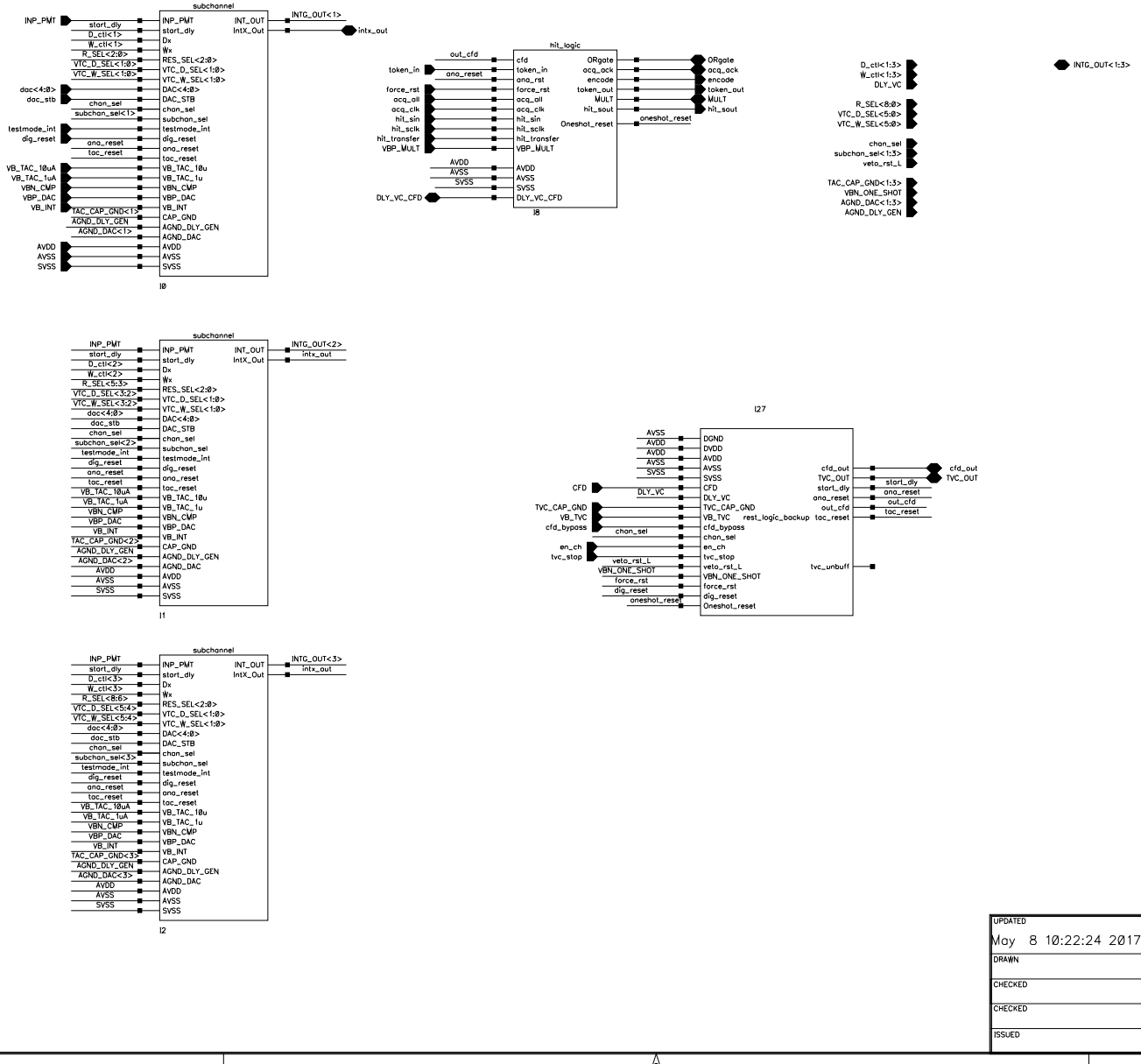


Output	Resistance
OUT<0>	0.5 K
OUT<1>	1 K
OUT<2>	2 K
OUT<3>	5 K
OUT<4>	10 K
OUT<5>	20 K
OUT<6>	50 K
OUT<7>	100 K

Resistances include the switch resistance following the resistor array.


I1
B
B
T
unit_100f_cap


T
T
A=275.228
C1
pipc
P=66.36
B
B



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

UPDATED	May 8 10:22:24 2017
DRAWN	
CHECKED	
CHECKED	
ISSUED	

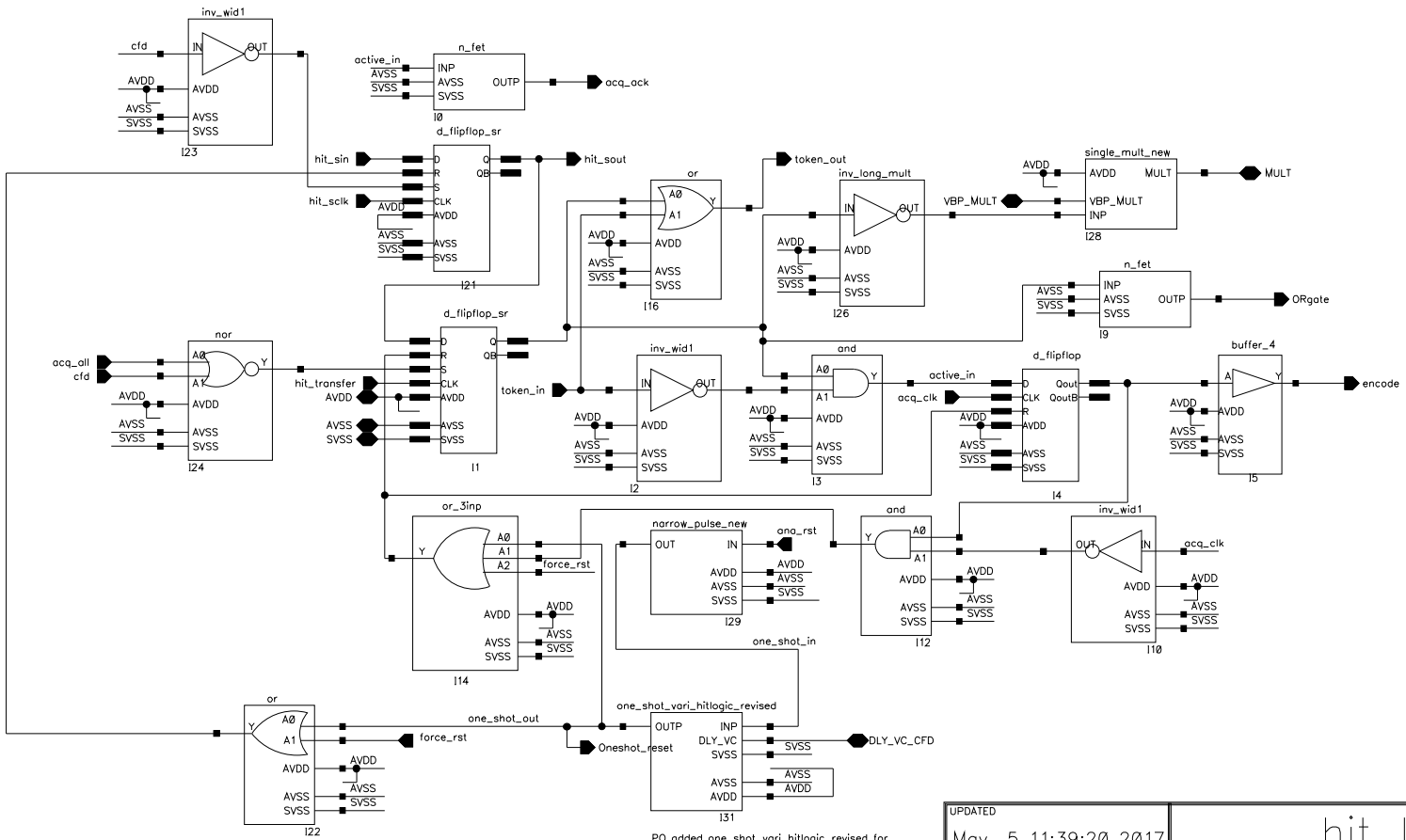
SIUE IC Design Lab
Channel

SIZE	CAGE NO.	DWG NO.	REV
C			A
SCALE		SHEET	1 OF 1

REV A
SH 1
DWG NO.
CAGE NO.

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



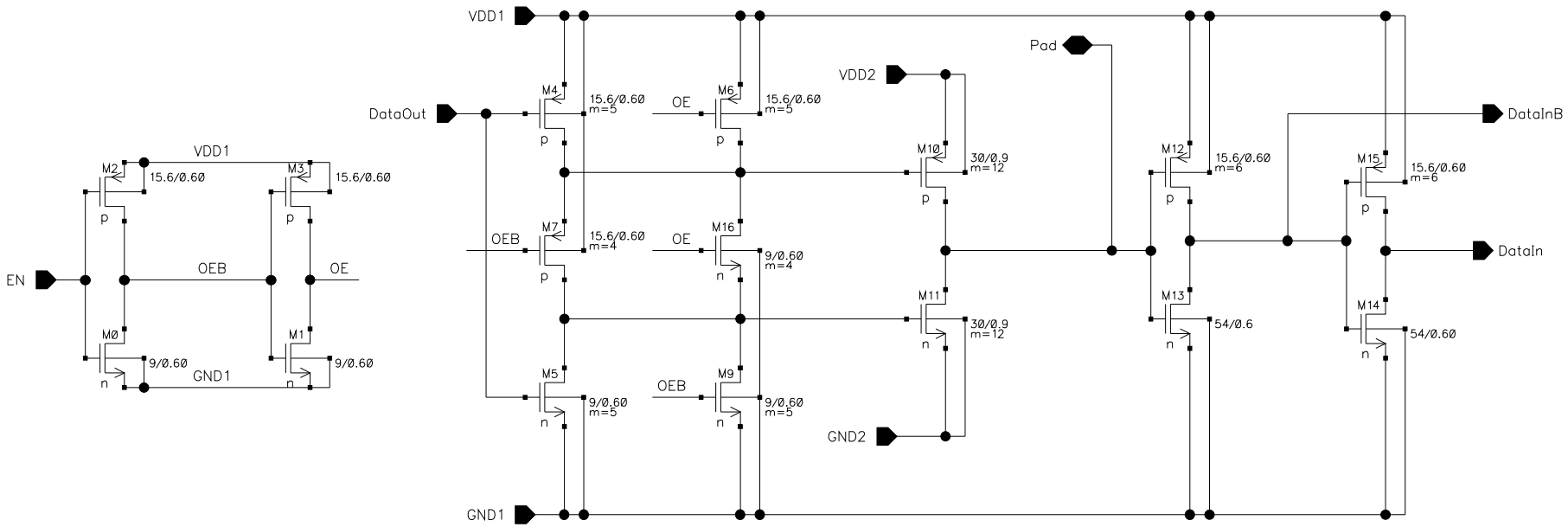
PO added one_shot_vari_hitlogic_revised for PSDchip_ver4 04/19/2017

UPDATED	hit_logic		
May 5 11:39:20 2017			
DRAWN			
CHECKED			
CHECKED	SIZE B	CAGE NO.	DWG NO. REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

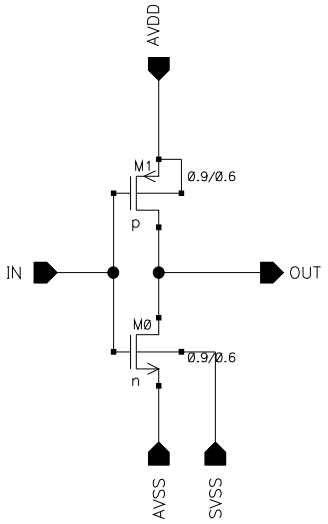


UPDATED Jul 9 16:28:29 2003	PadBidirHE		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

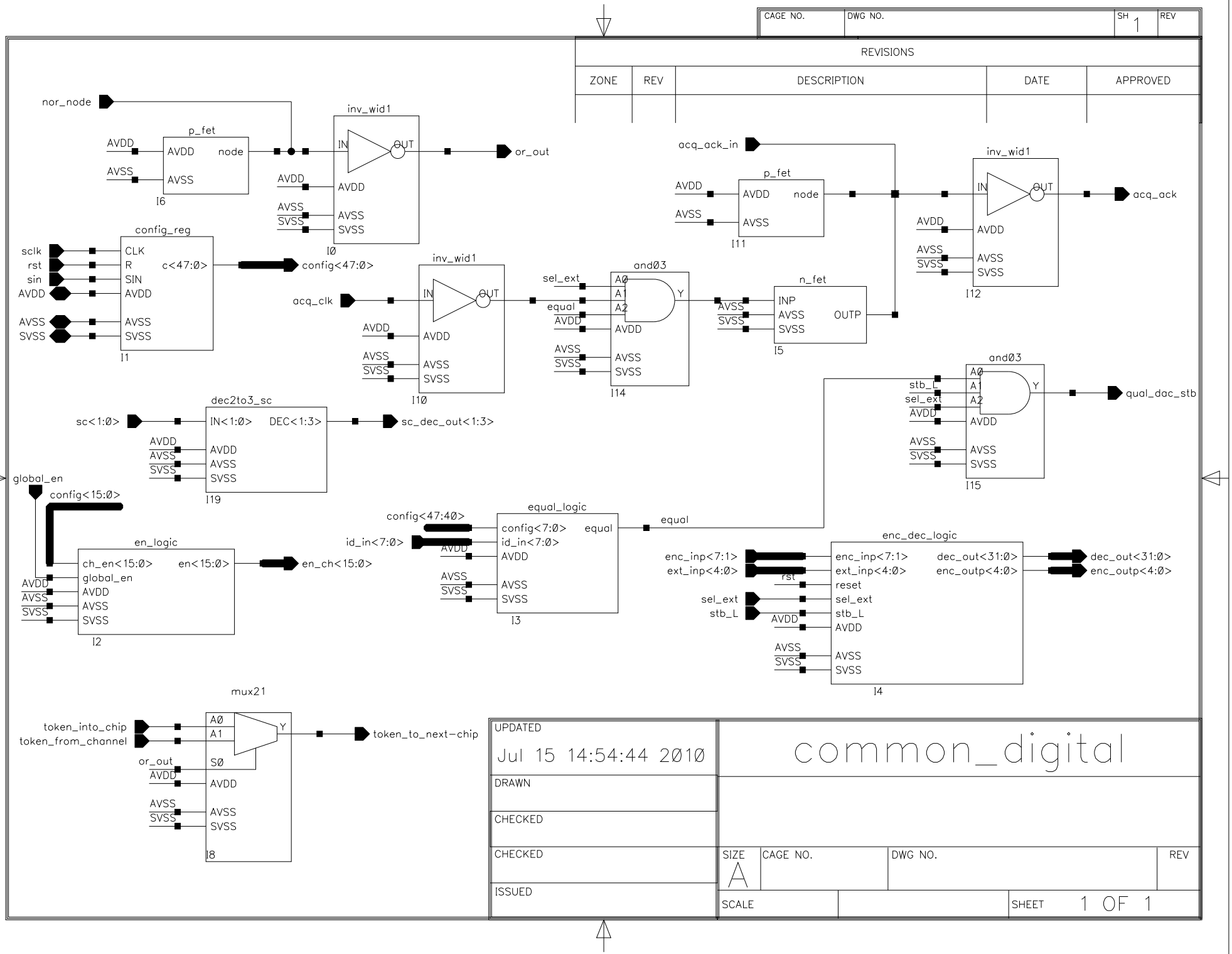
CAGE NO.	DWG NO.	SH 1	REV

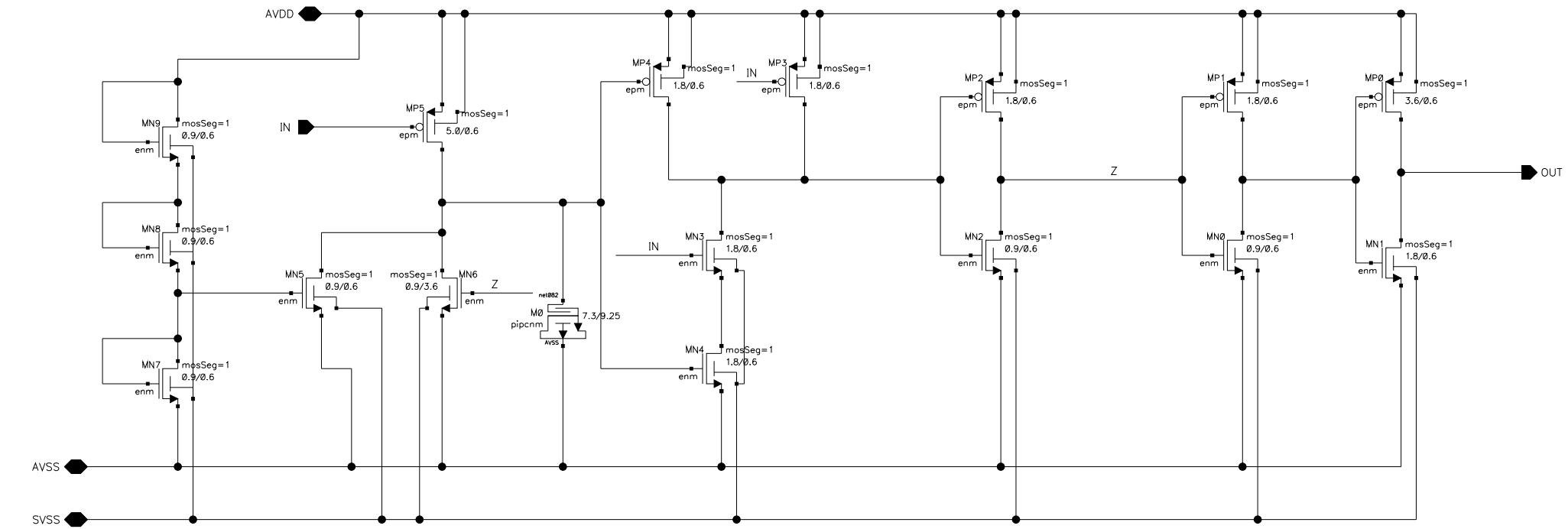
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Aug 15 11:38:53 2007	inverter			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

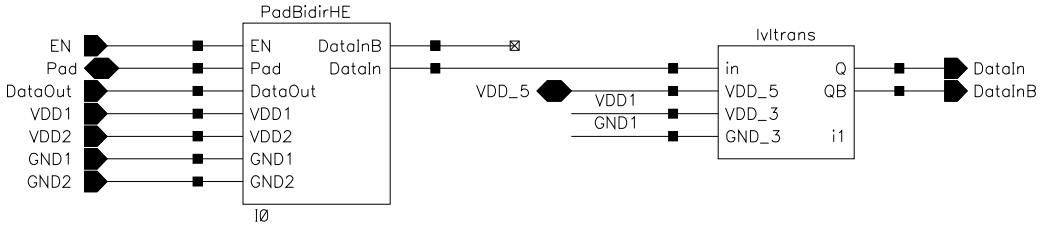

CAGE NO.
DWG NO.
SH 1
REV
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
nor_node
p_fet
AVDD
AVSS
AVDD
node
AVSS
I6
inv_wid1
IN
OUT
AVDD
AVSS
SVSS
or_out
I0
acq_ack_in
p_fet
I11
inv_wid1
acq_ack
I12
config_reg
sclk
rst
sin
AVDD
AVSS
SVSS
CLK
R
SIN
c<47:0>
config<47:0>
I1
inv_wid1
acq_clk
I10
and03
sel_ext
equal
A0
A1
A2
Y
I14
n_fet
INP
OUTP
I5
and03
stb_L
sel_ext
qual_dac_stb
I15
dec2to3_sc
sc<1:0>
IN<1:0>
DEC<1:3>
sc_dec_out<1:3>
I19
global_en
config<15:0>
en_logic
ch_en<15:0>
en<15:0>
en_ch<15:0>
I2
equal_logic
config<47:40>
id_in<7:0>
config<7:0>
equal
I3
enc_dec_logic
enc_inp<7:1>
ext_inp<4:0>
rst
sel_ext
stb_L
reset
dec_out<31:0>
enc_outp<4:0>
I4
mux21
token_into_chip
token_from_channel
or_out
S0
token_to_next-chip
I8
UPDATED
Jul 15 14:54:44 2010
DRAWN
CHECKED
CHECKED
ISSUED
common_digital
SIZE
A
CAGE NO.
DWG NO.
REV
SCALE
SHEET 1 OF 1


AVDD
IN
MP5
mosSeg=1
5.0/0.6
epm
MP4
1.8/0.6
MP3
MP2
MP1
MP0
3.6/0.6
MN9
0.9/0.6
enm
MN8
MN7
MN5
MN6
0.9/3.6
Z
net082
MØ
pipcnm
7.3/9.25
AVSS
MN3
1.8/0.6
MN4
MN2
MNØ
MN1
OUT
SVSS

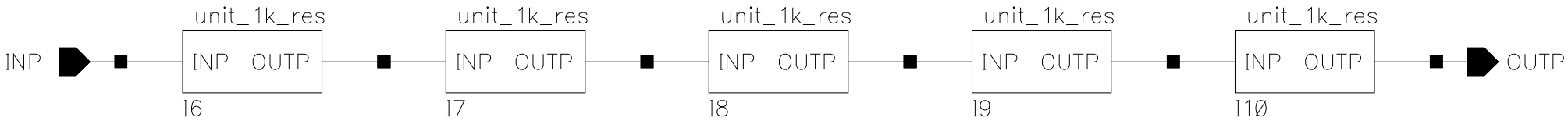
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



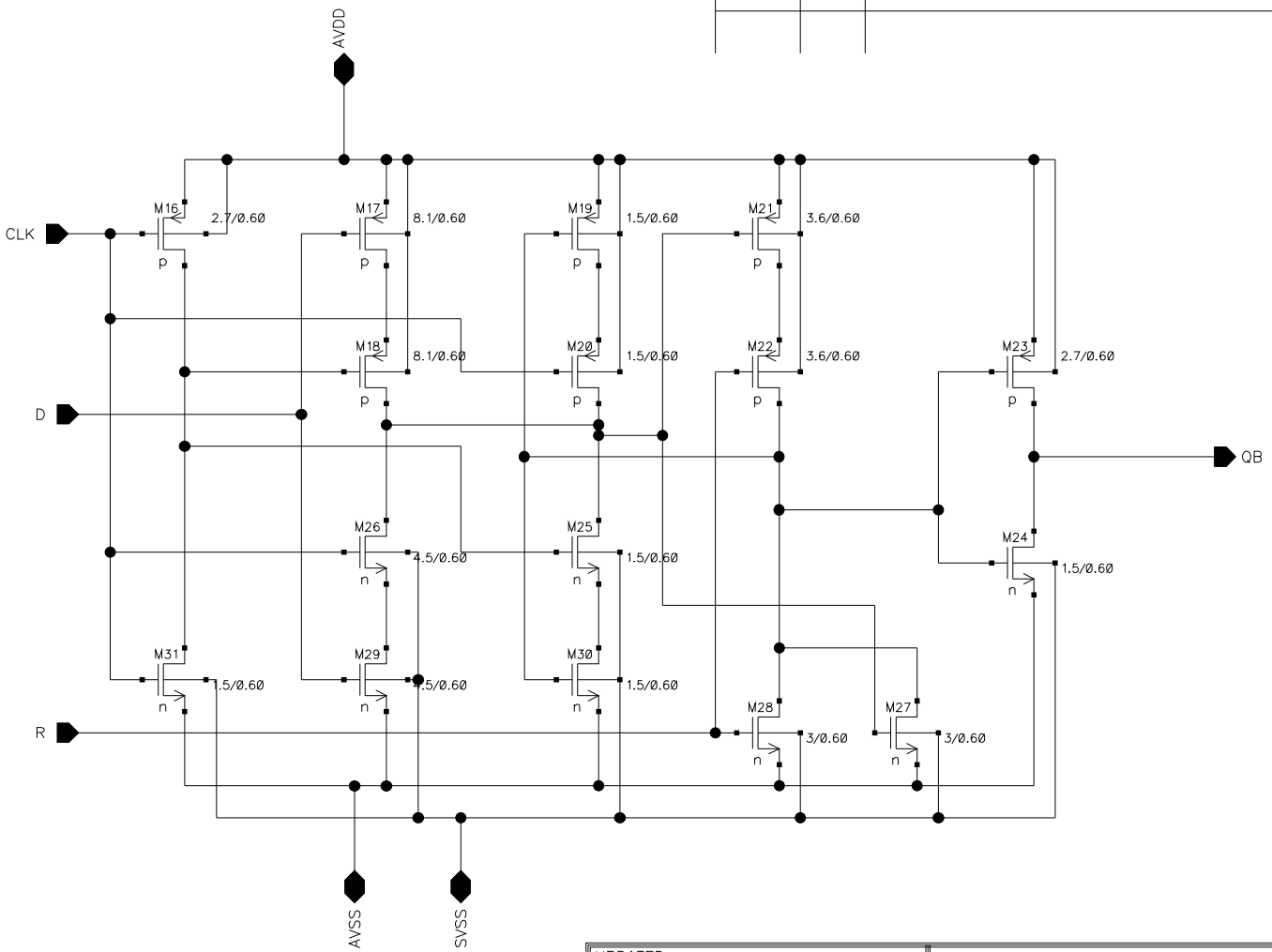
UPDATED	PadBidirHE			
May 2 09:02:12 2016				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


INP
unit_1k_res
INP OUTP
I6
unit_1k_res
INP OUTP
I7
unit_1k_res
INP OUTP
I8
unit_1k_res
INP OUTP
I9
unit_1k_res
INP OUTP
I1Ø
OUTP

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

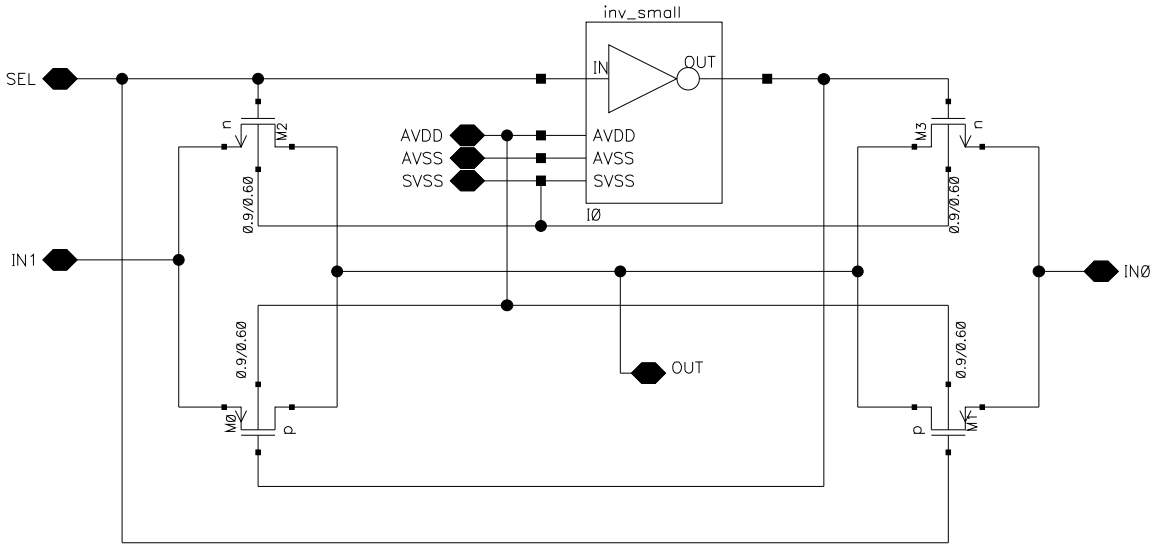


UPDATED Mar 16 13:47:13 2010	latch_r		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

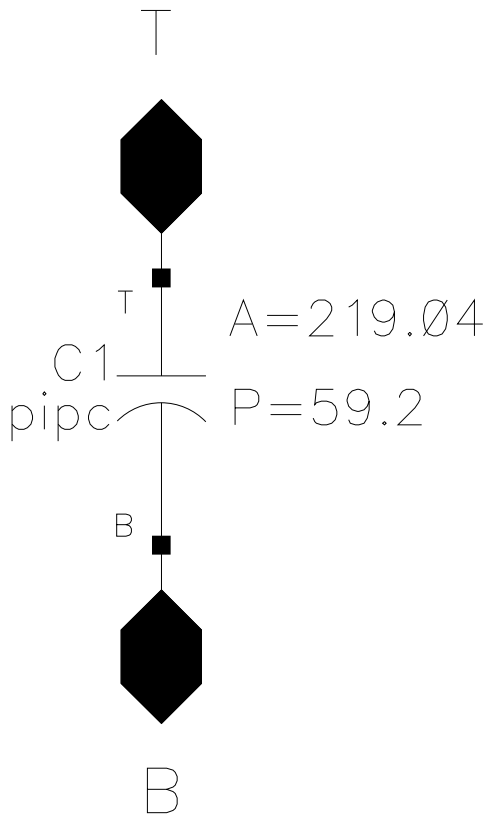
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



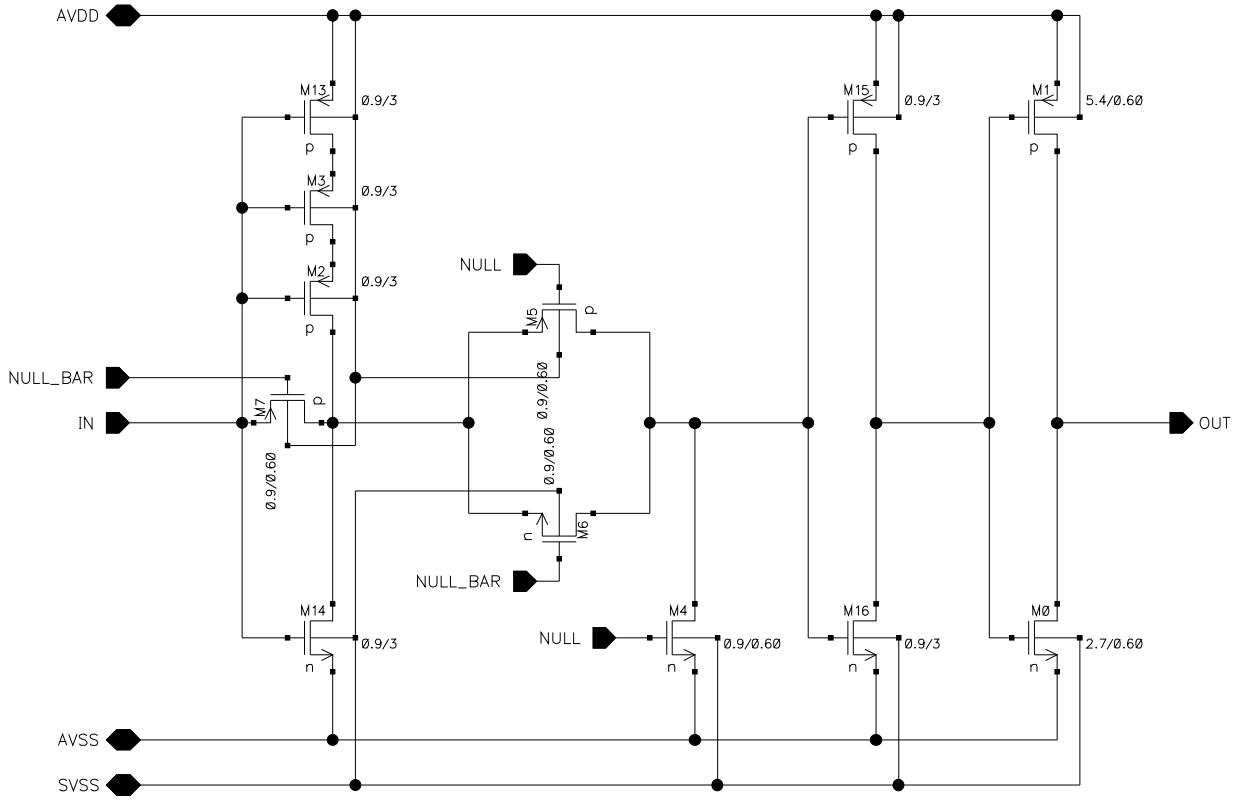
UPDATED	mux_min			
Jun 5 11:38:02 2007				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


T
T
A=219.Ø4
C1
pipc
P=59.2
B
B

CAGE NO.	DWG NO.	SH 1	REV A

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



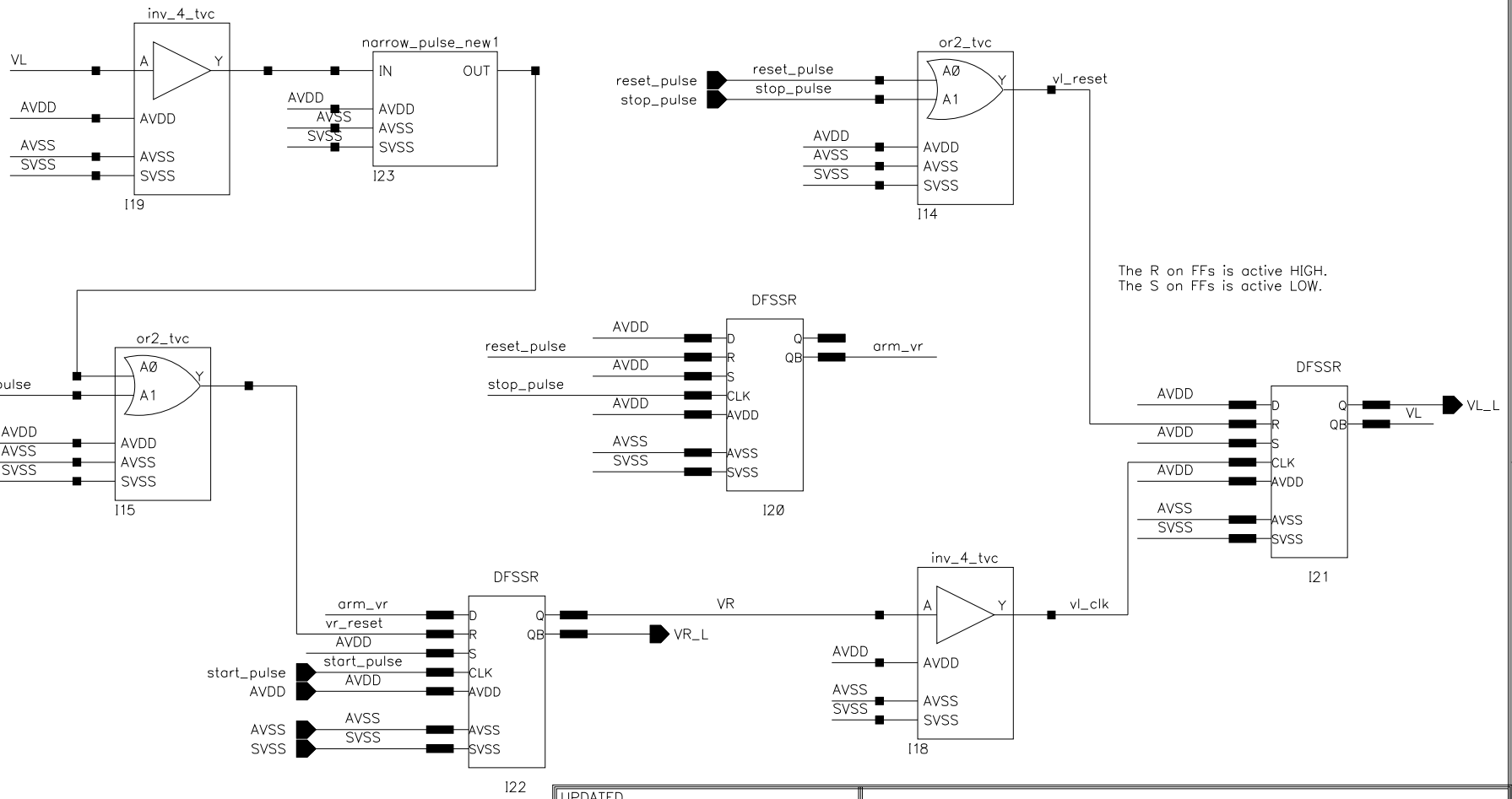
UPDATED	SIUE IC Design Lab
Jul 10 13:06:58 2007	Comparator
DRAWN	Buffer & Invert
CHECKED	
CHECKED	
ISSUED	

SIZE	CAGE NO.	DWG NO.	REV
A			A
SCALE		SHEET	1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

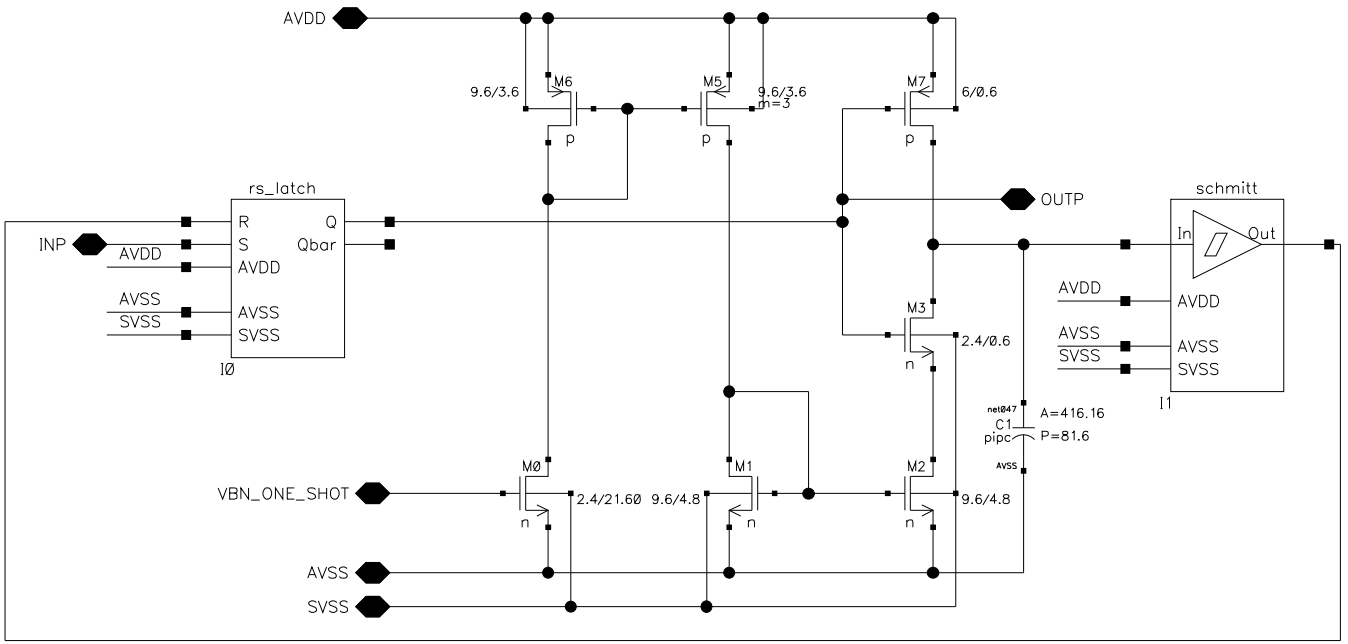


UPDATED			
Nov 15 15:08:07 2011			
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

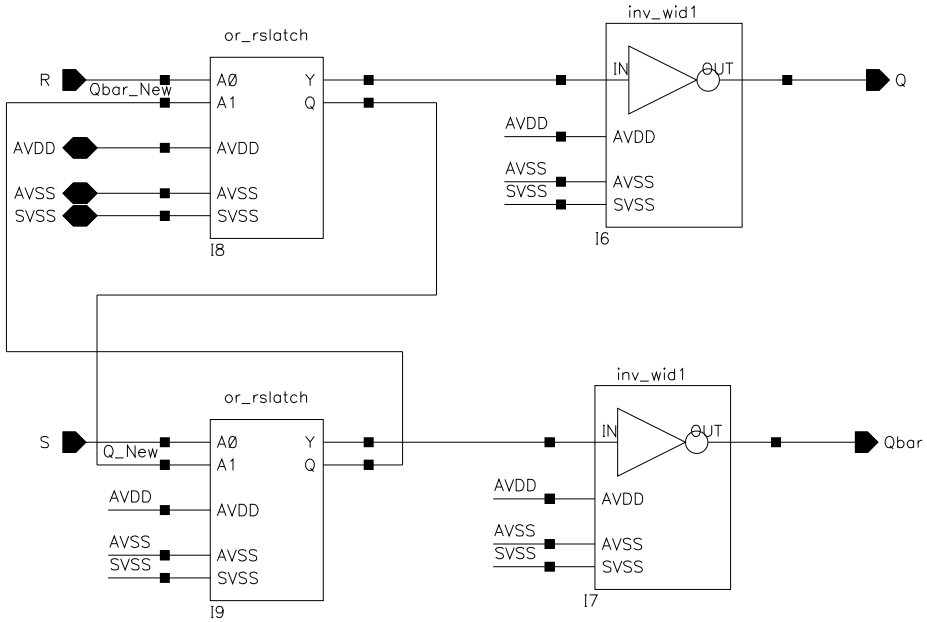


UPDATED	Jul 5 12:57:14 2011	one_shot_100ns	
DRAWN			
CHECKED			
CHECKED		SIZE A / CAGE NO. / DWG NO. / REV	
ISSUED		SCALE / SHEET 1 OF 1	

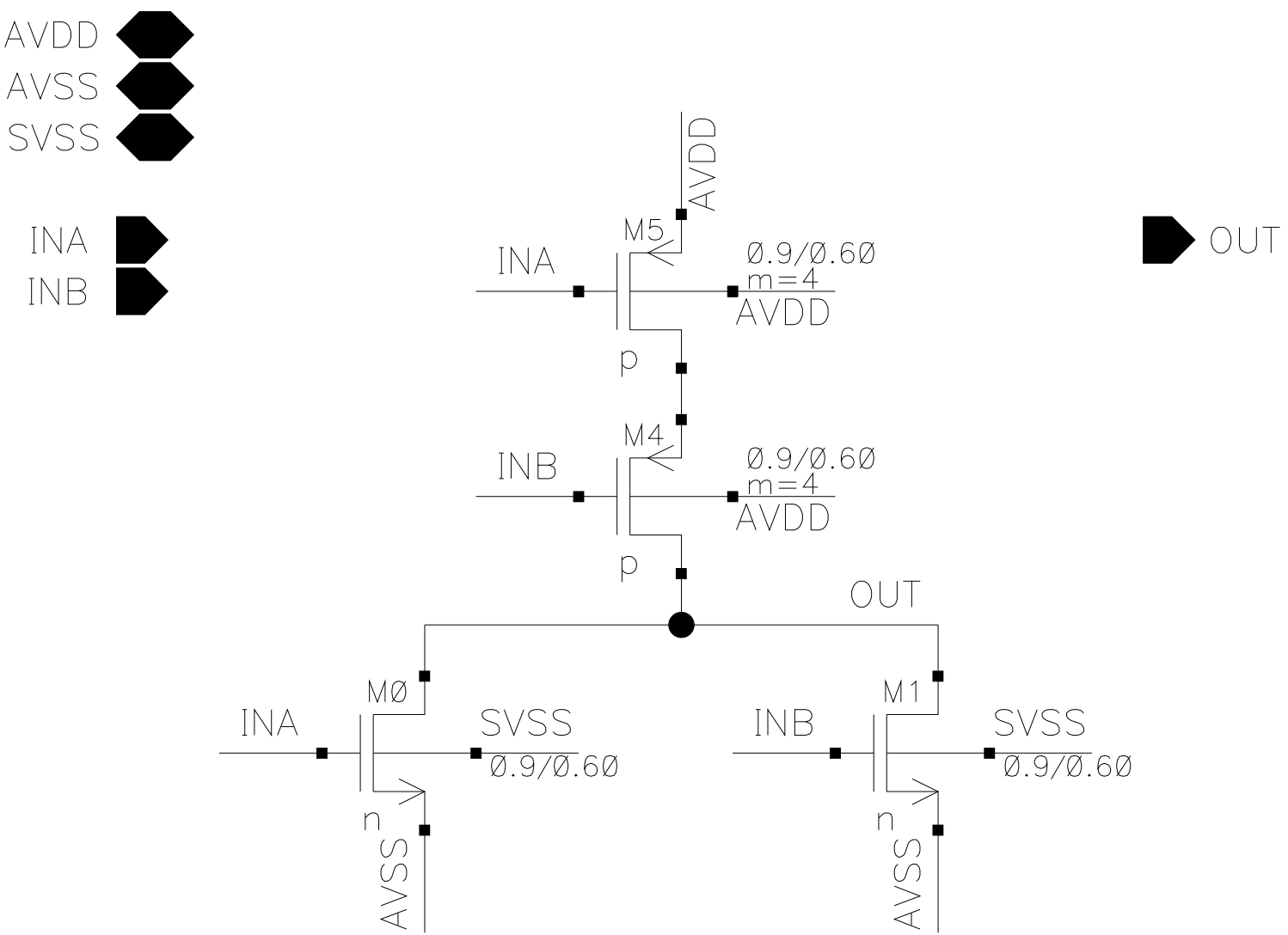
CAGE NO.	DWG NO.	SH 1	REV

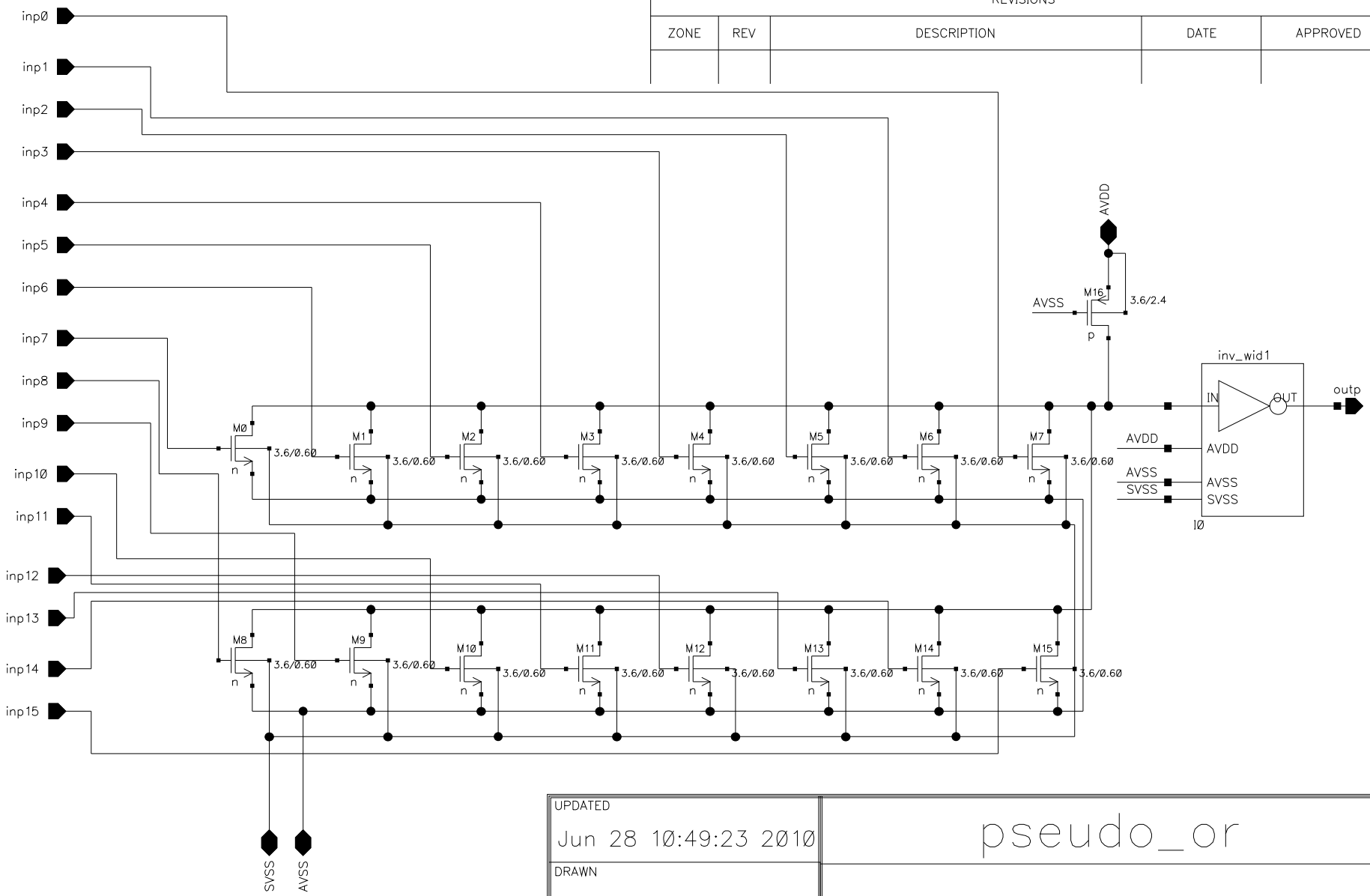
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	rs_latch			
Jun 22 14:23:13 2010				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


AVDD
AVSS
SVSS
INA
INB
OUT
AVDD
M5
INA
Ø.9/Ø.6Ø
m=4
AVDD
p
M4
INB
Ø.9/Ø.6Ø
m=4
AVDD
p
OUT
MØ
INA
SVSS
Ø.9/Ø.6Ø
n
AVSS
M1
INB
SVSS
Ø.9/Ø.6Ø
n
AVSS



CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

UPDATED	Jun 28 10:49:23 2010
DRAWN	
CHECKED	
CHECKED	
ISSUED	

pseudo_or

SIZE	CAGE NO.	DWG NO.	REV
A			

SCALE		SHEET 1 OF 1

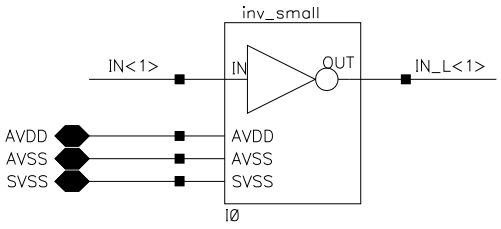
CAGE NO.	DWG NO.	SH 1	REV A

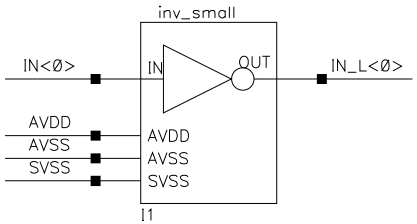
REVISIONS

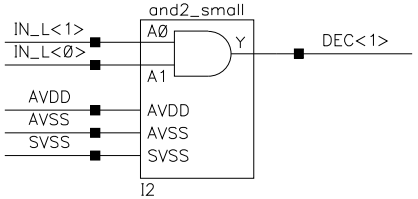
ZONE	REV	DESCRIPTION	DATE	APPROVED

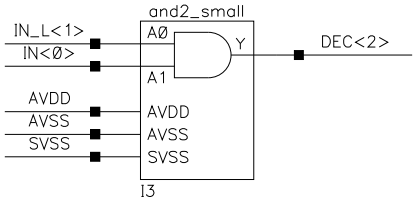
IN<1:0>

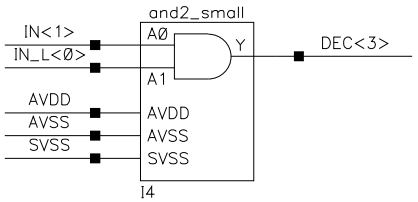
DEC<1:3>









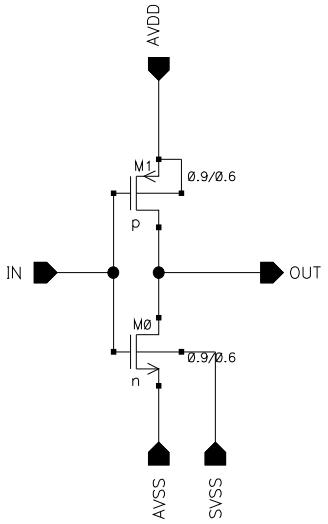


UPDATED Jun 25 13:38:46 2010	SIUE IC Design Lab Decoder 2 to 3 Subchannel Selects
DRAWN	
CHECKED	
CHECKED	SIZE A | CAGE NO. | DWG NO. | REV A
ISSUED	SCALE | SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

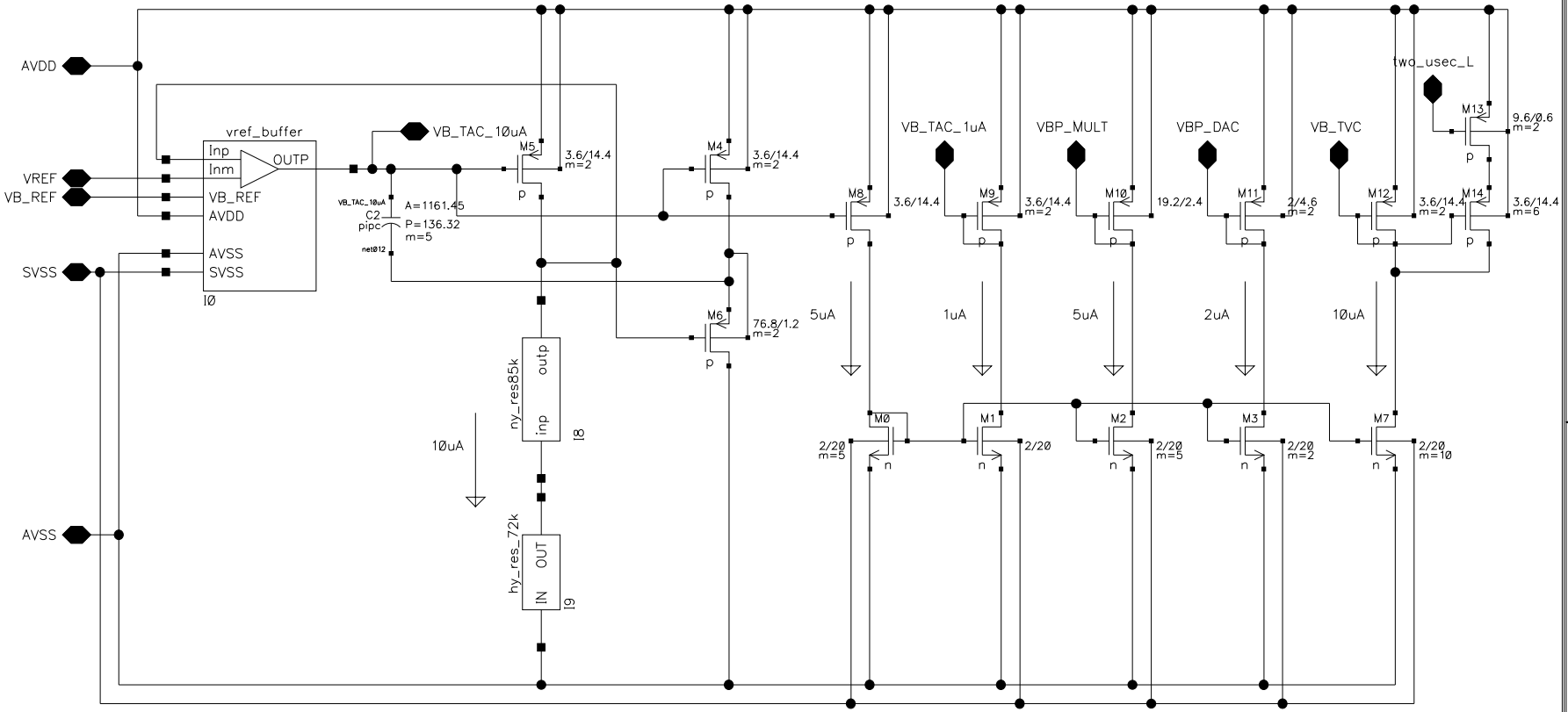


UPDATED	inverter			
Feb 15 18:52:17 2008				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH	REV
		1	A

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



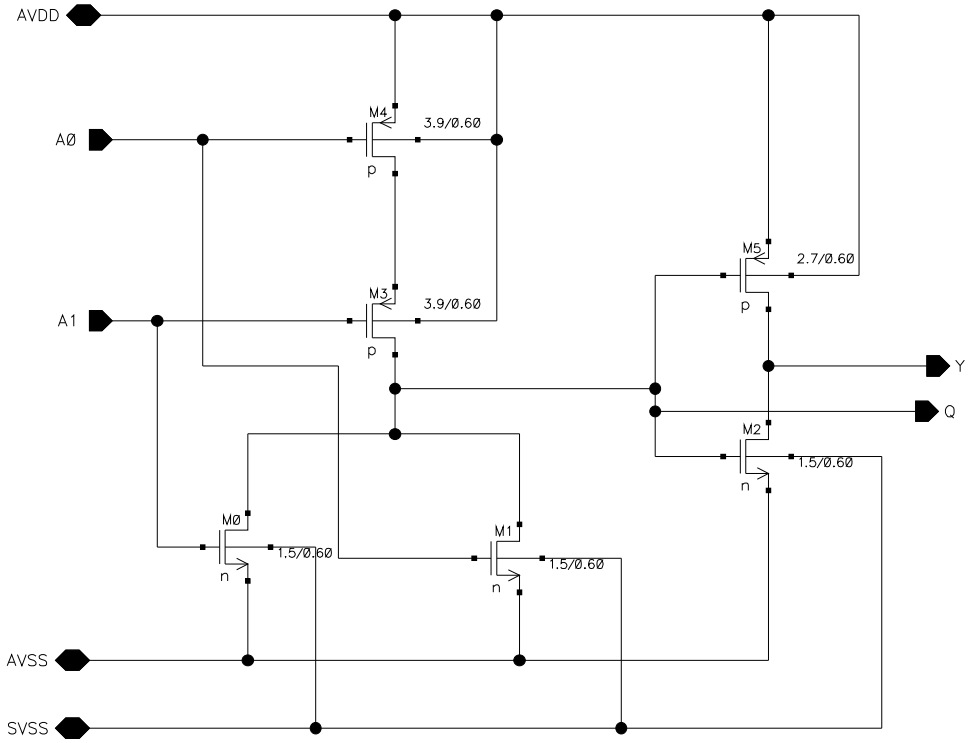
UPDATED	SIUE IC Design Lab
Oct 12 11:23:35 2011	Constant Current
DRAWN	
CHECKED	
CHECKED	
ISSUED	

SIZE	CAGE NO.	DWG NO.	REV
A			A
SCALE		SHEET	1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

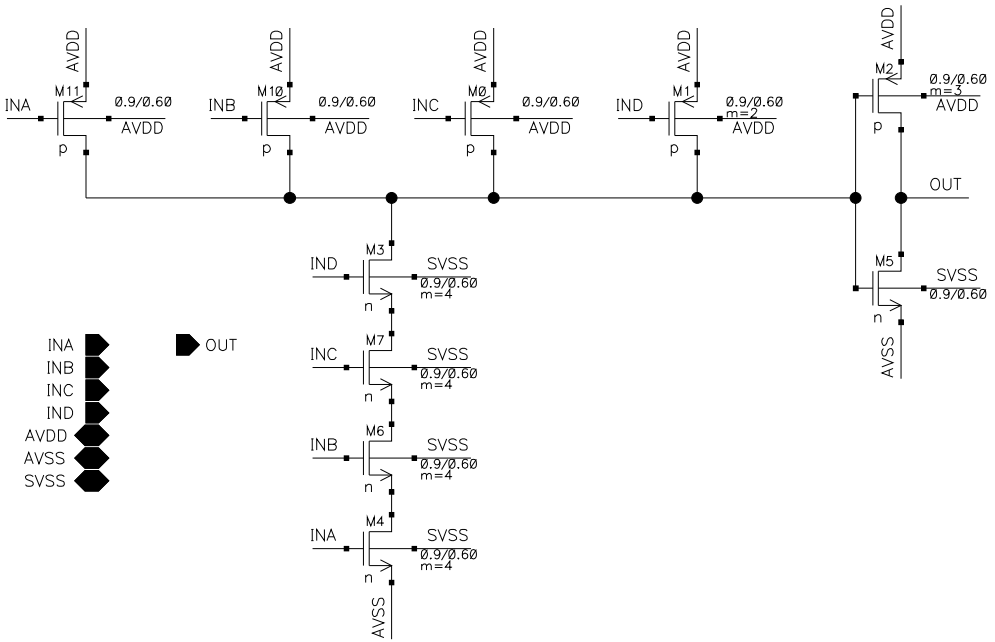


UPDATED Aug 13 14:15:03 2007	or_rslatch			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

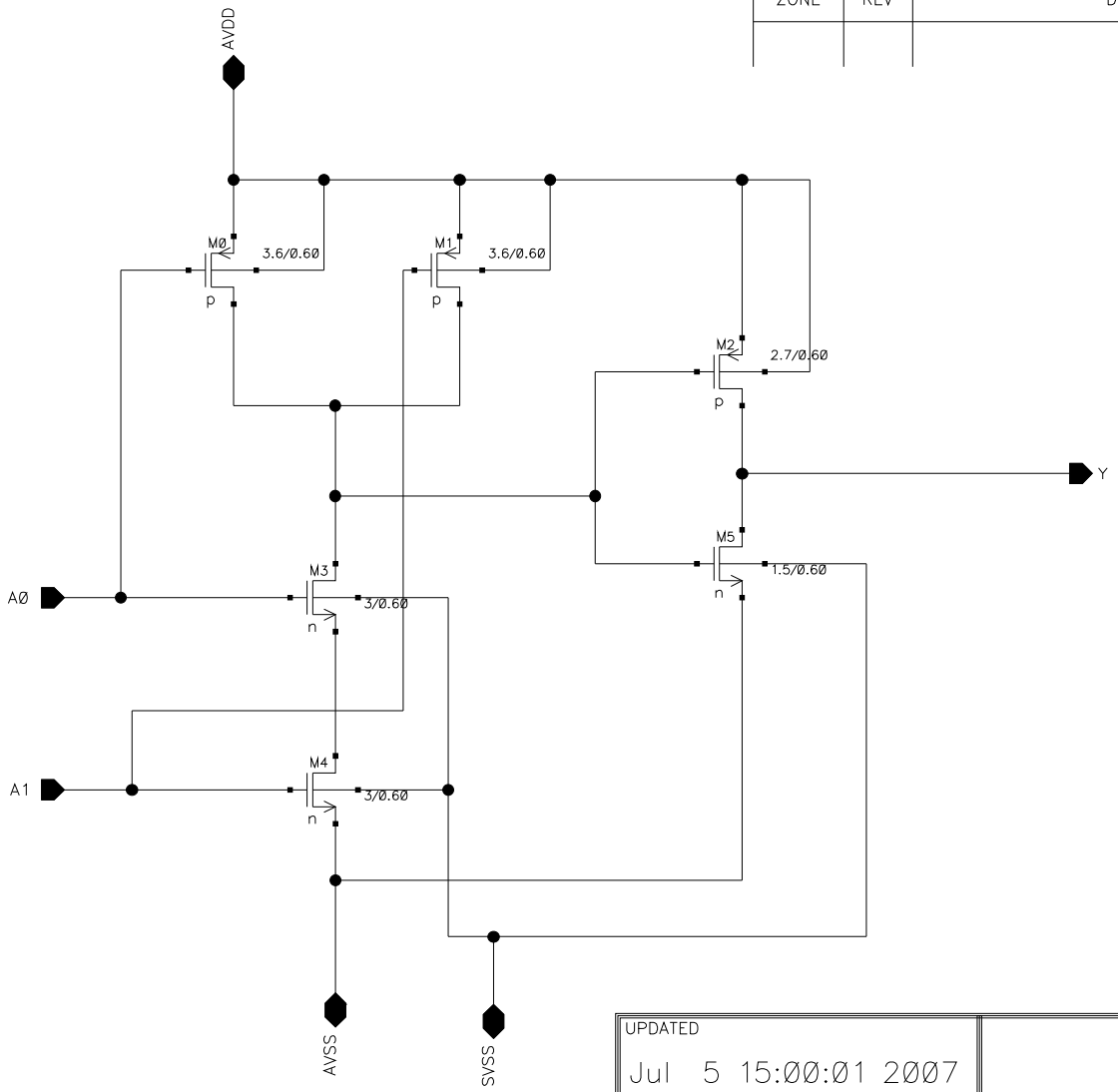


UPDATED Feb 20 16:35:34 2007	and			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

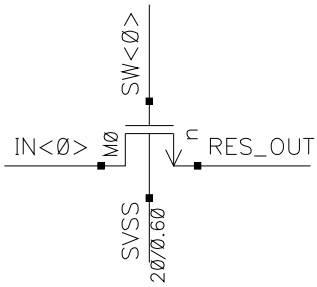
ZONE	REV	DESCRIPTION	DATE	APPROVED

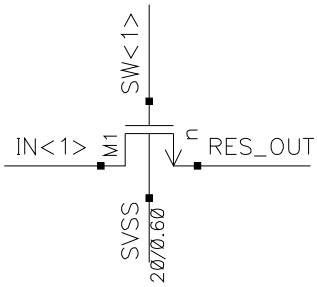


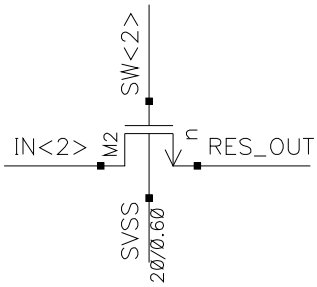
UPDATED Jul 5 15:00:01 2007	and			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

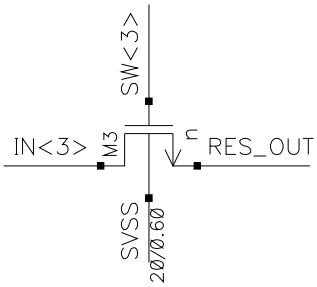
Switch	Resistance
SW<0>	0.5 K
SW<1>	1 K
SW<2>	2 K
SW<3>	5 K
SW<4>	10 K
SW<5>	20 K
SW<6>	50 K
SW<7>	100 K

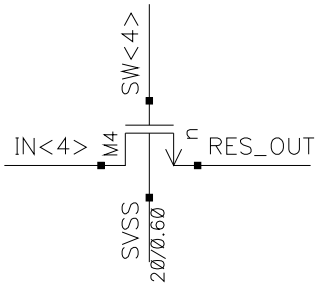
Resistances include the switch resistance and the resistor array preceding the switch.

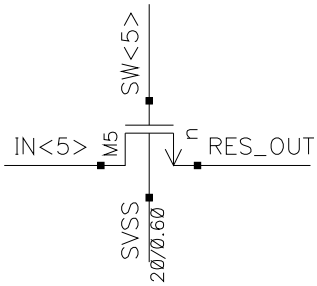


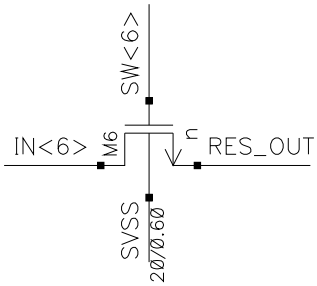


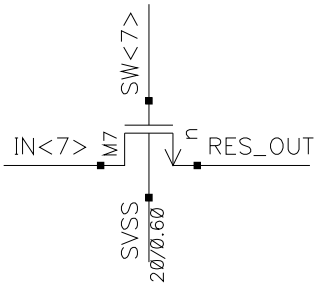




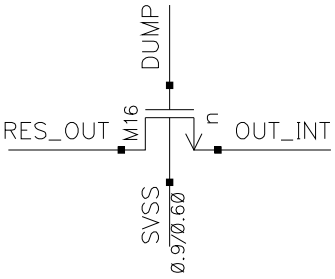


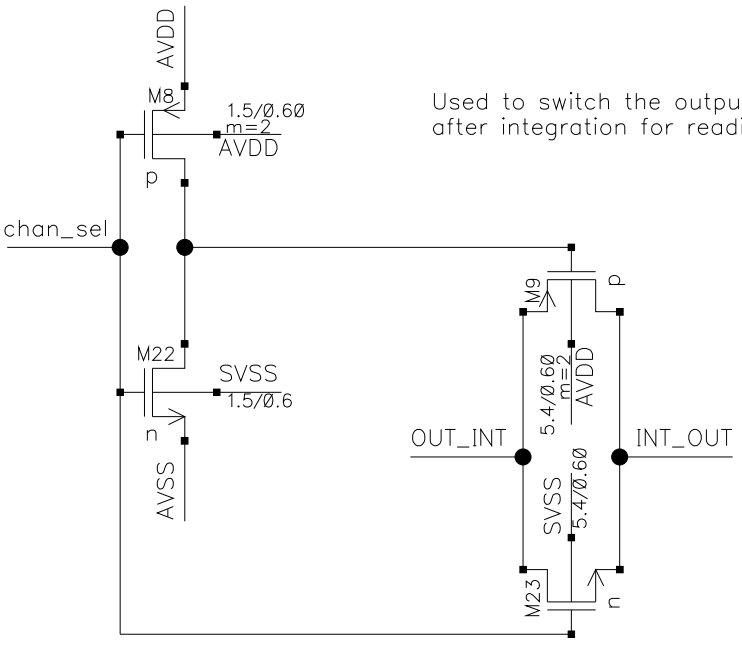






Used to short the integrating capacitor



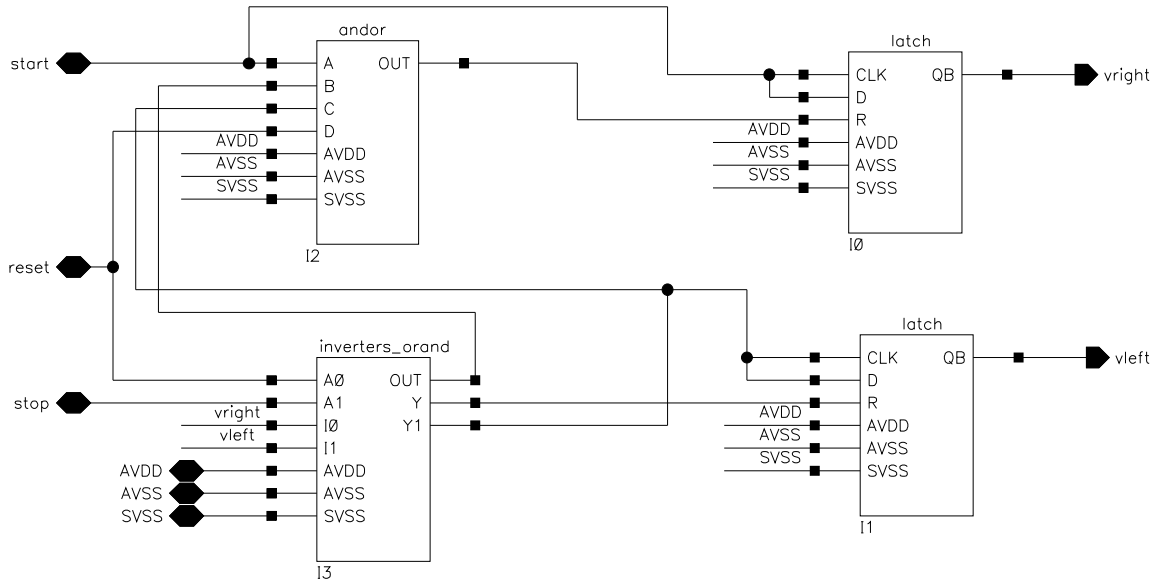


Used to switch the output of the OTA after integration for reading purposes.

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

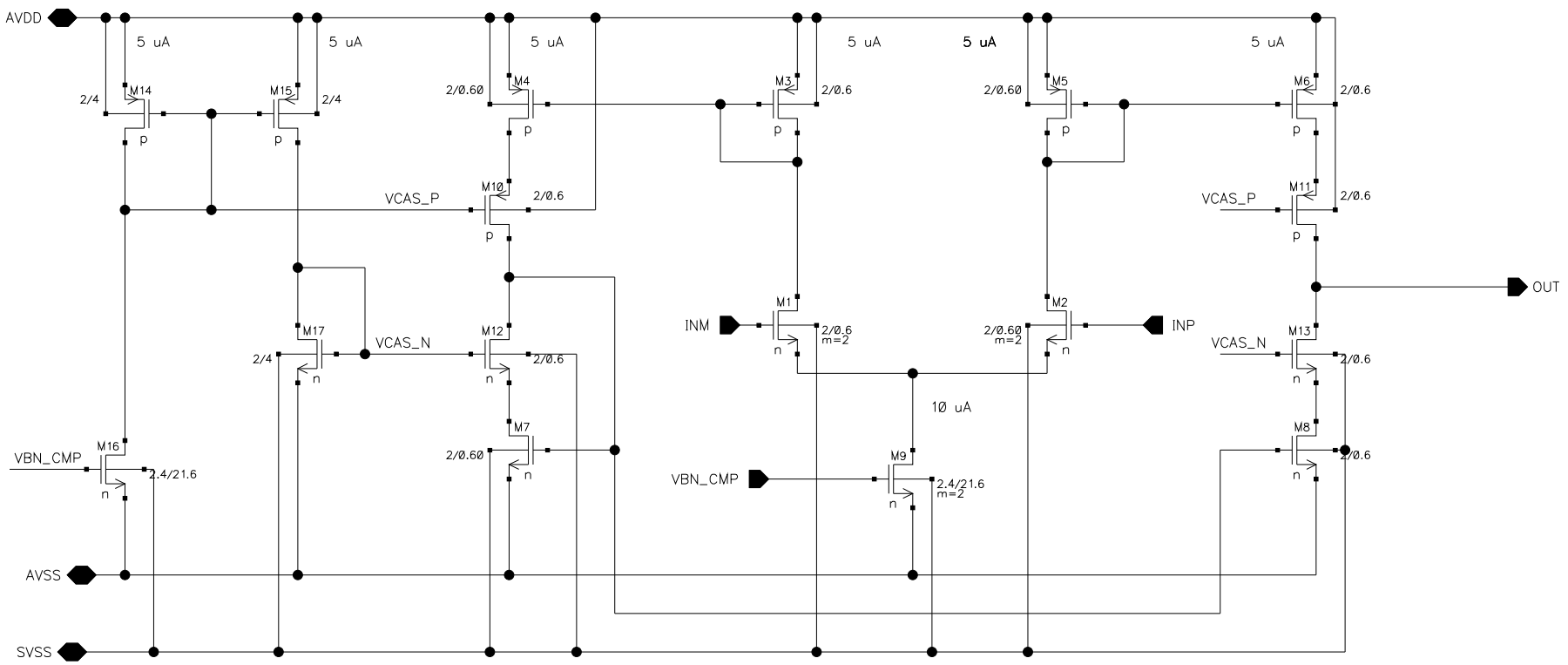


UPDATED	width_gen		
Jul 9 11:21:29 2007			
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



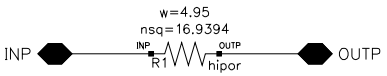
Supply current is 30 uA.
Power consumption is 150 uWatts.

UPDATED Jul 9 10:40:35 2007	SIUE IC Design Lab		
DRAWN	Comparator		
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

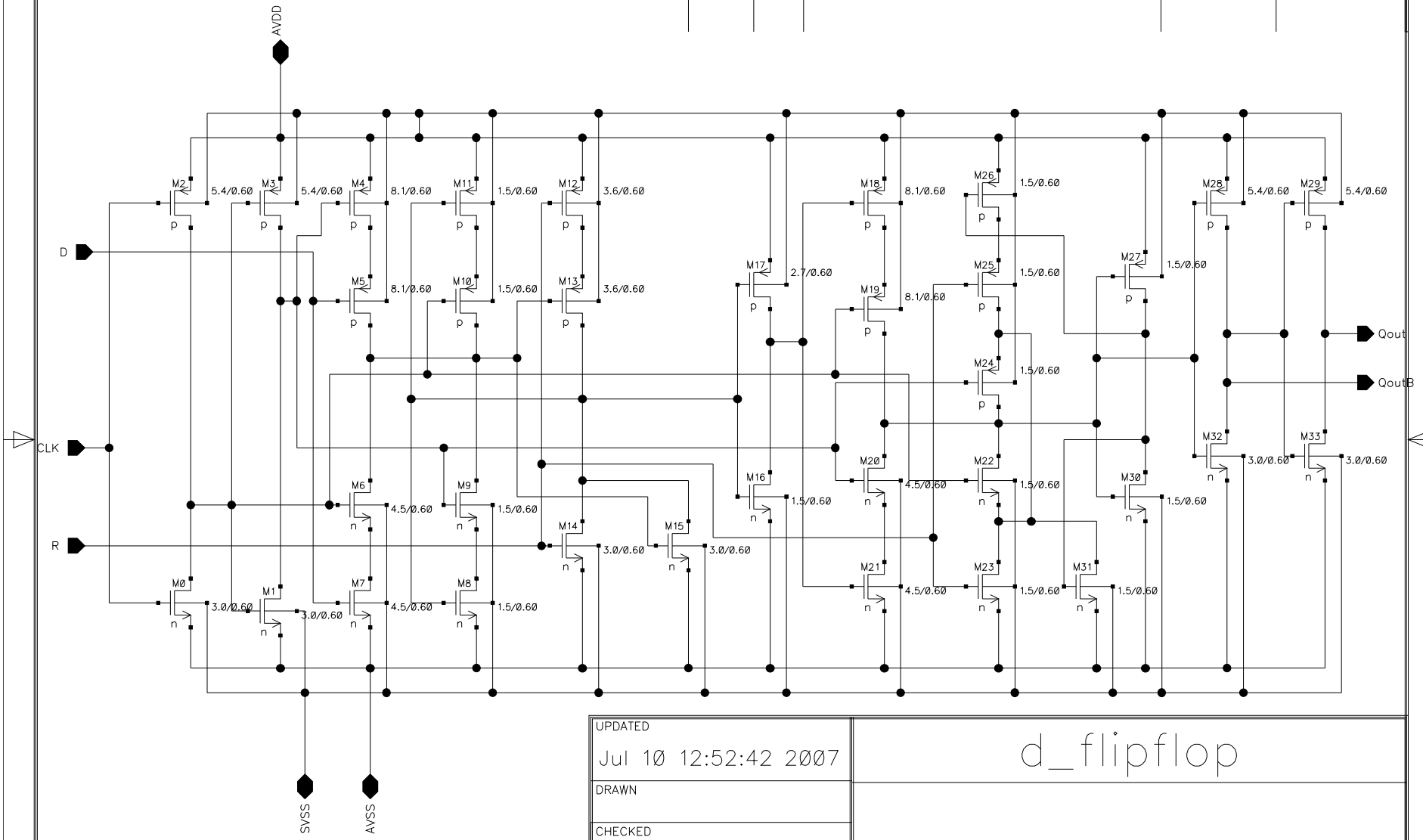
Resistor has l=83.85u and w=4.95u



UPDATED Jul 5 11:32:47 2011	unit_bias_res_2			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

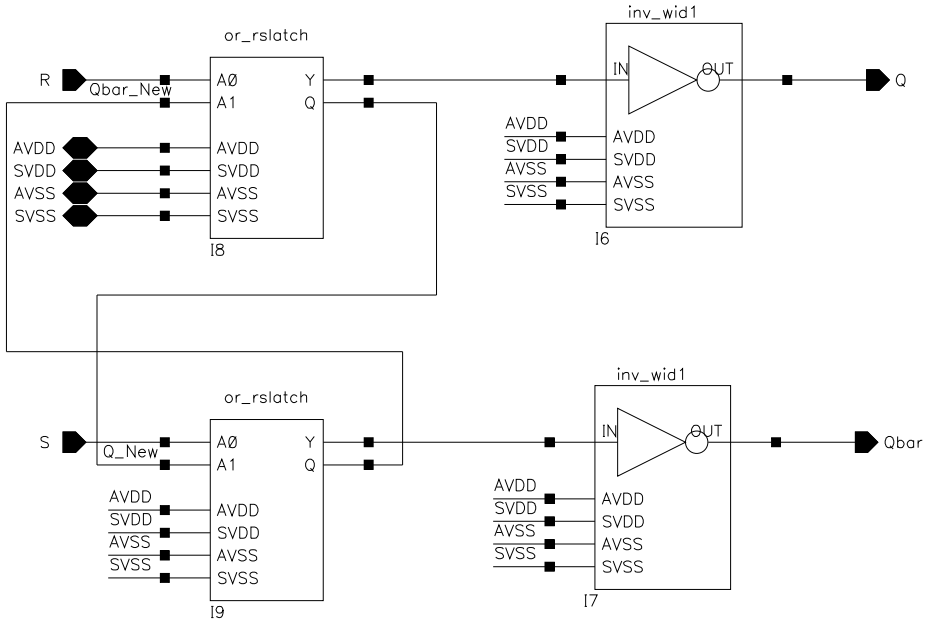


UPDATED	d_flipflop		
Jul 10 12:52:42 2007			
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

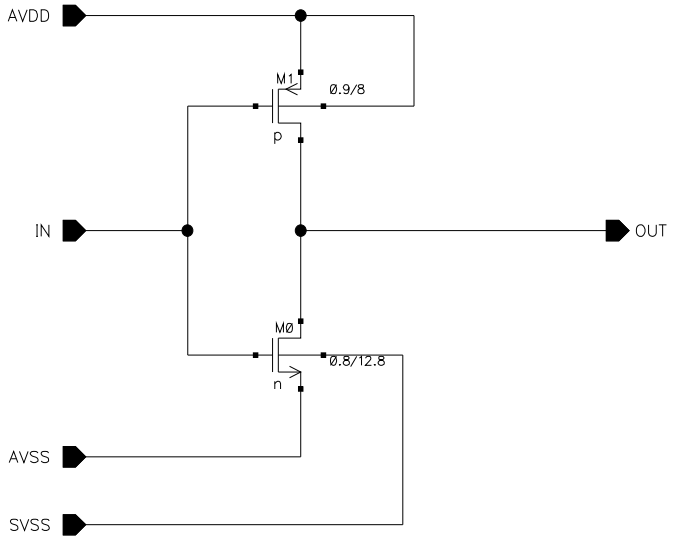


UPDATED Apr 18 15:40:41 2017	rs_latch			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

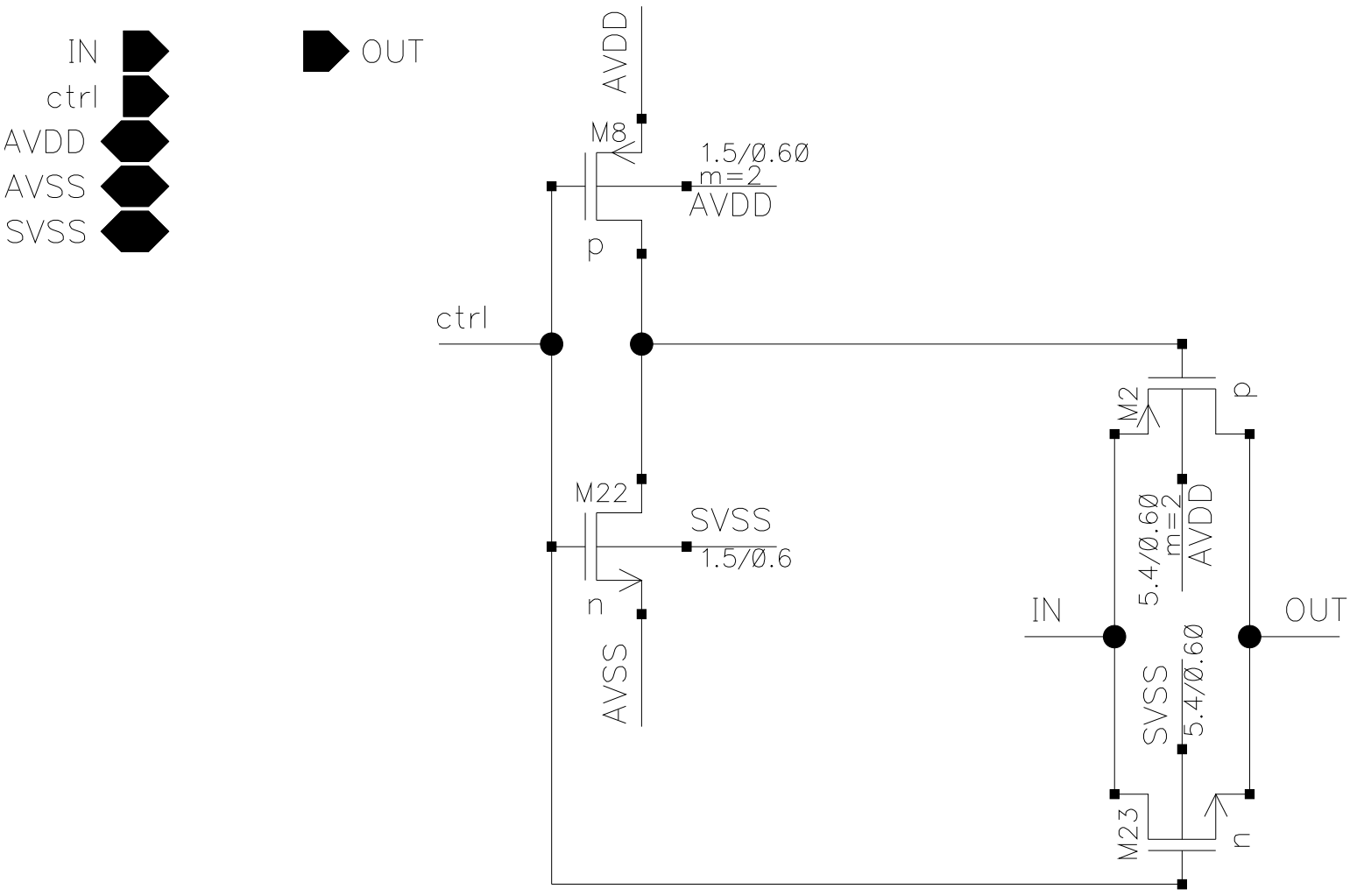
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



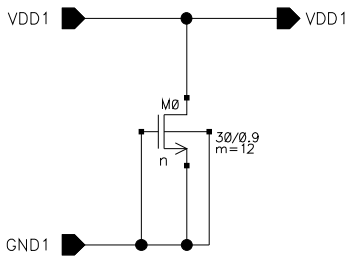
UPDATED Aug 17 15:50:28 2011	inv_wid1			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


IN
ctrl
AVDD
AVSS
SVSS
OUT
AVDD
M8
1.5/0.60
m=2
AVDD
p
ctrl
M22
SVSS
1.5/0.6
n
AVSS
M2
p
5.4/0.60
m=2
AVDD
IN
OUT
SVSS
5.4/0.60
M23
n

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

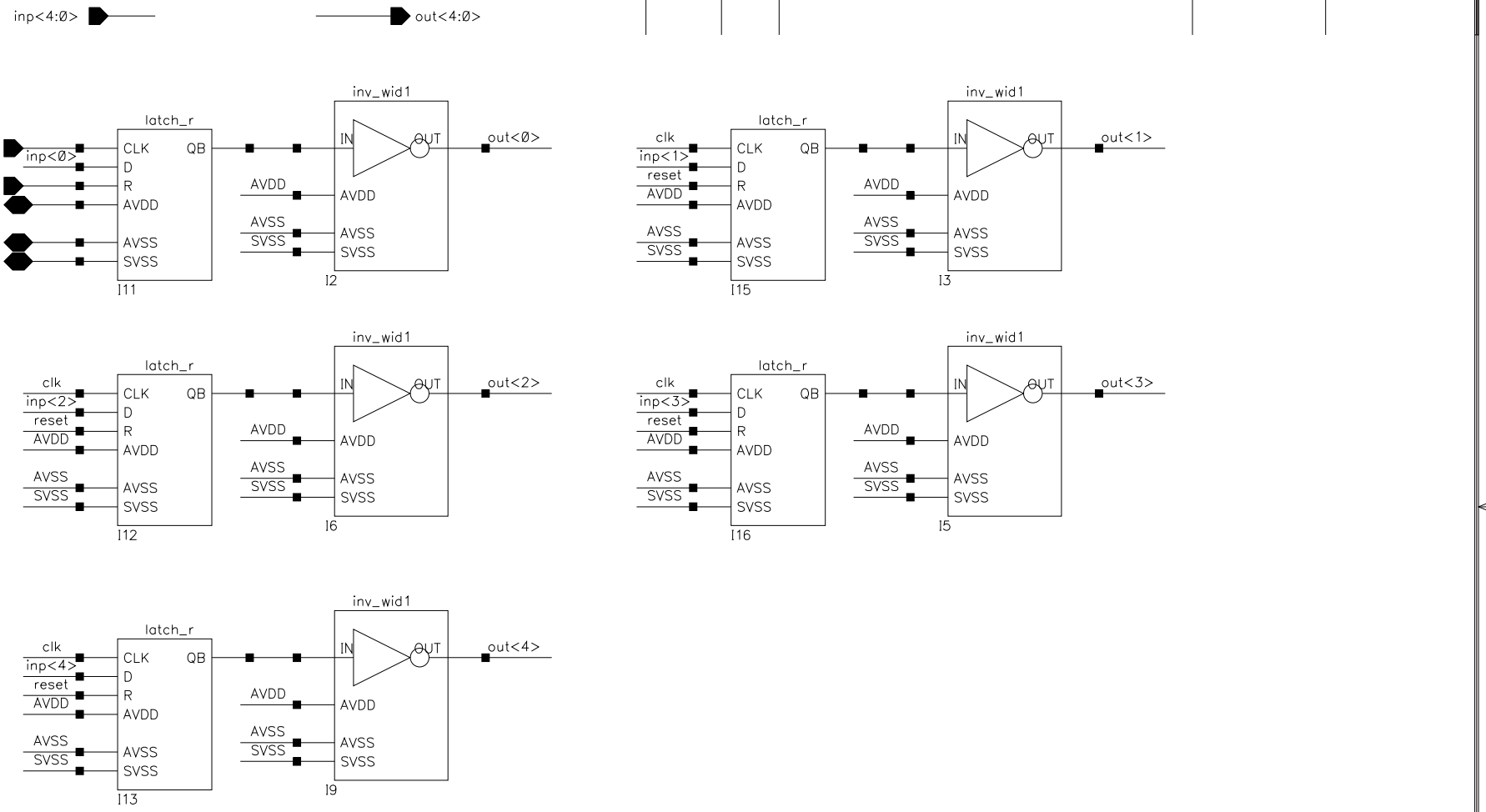


UPDATED Nov 11 15:36:54 2004	PadVdd			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

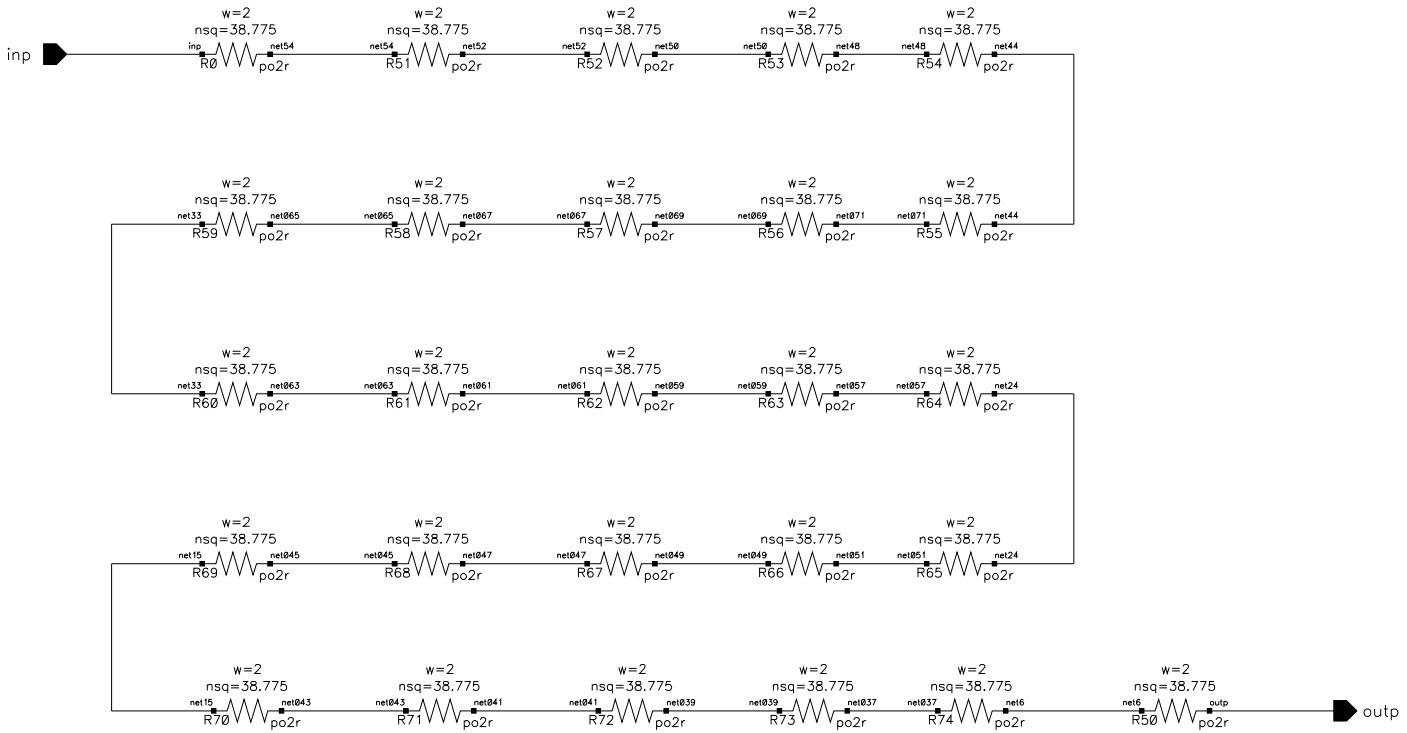


UPDATED Jun 25 14:07:41 2010	latch_5bit		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

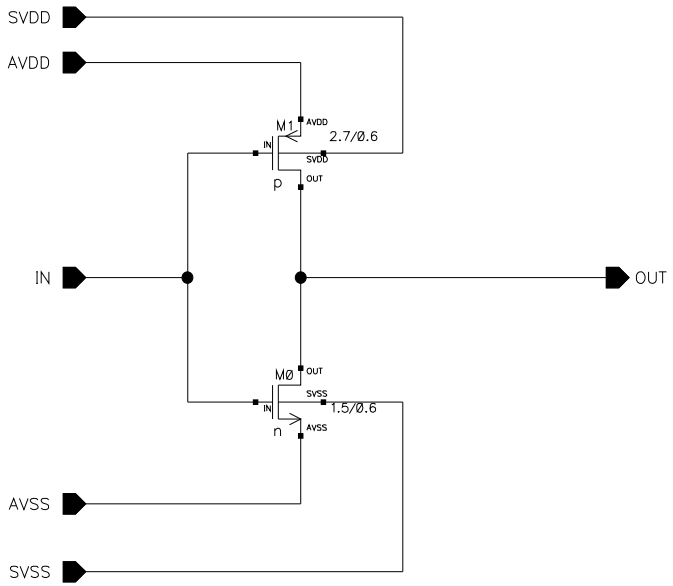


UPDATED Oct 11 10:50:29 2011	ny_res85k			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Sep 19 18:46:05 2002	inv_wid1			
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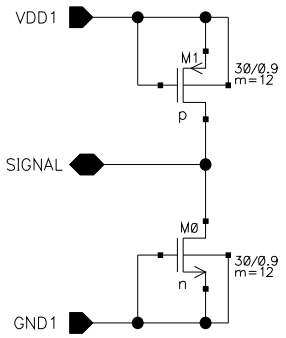
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

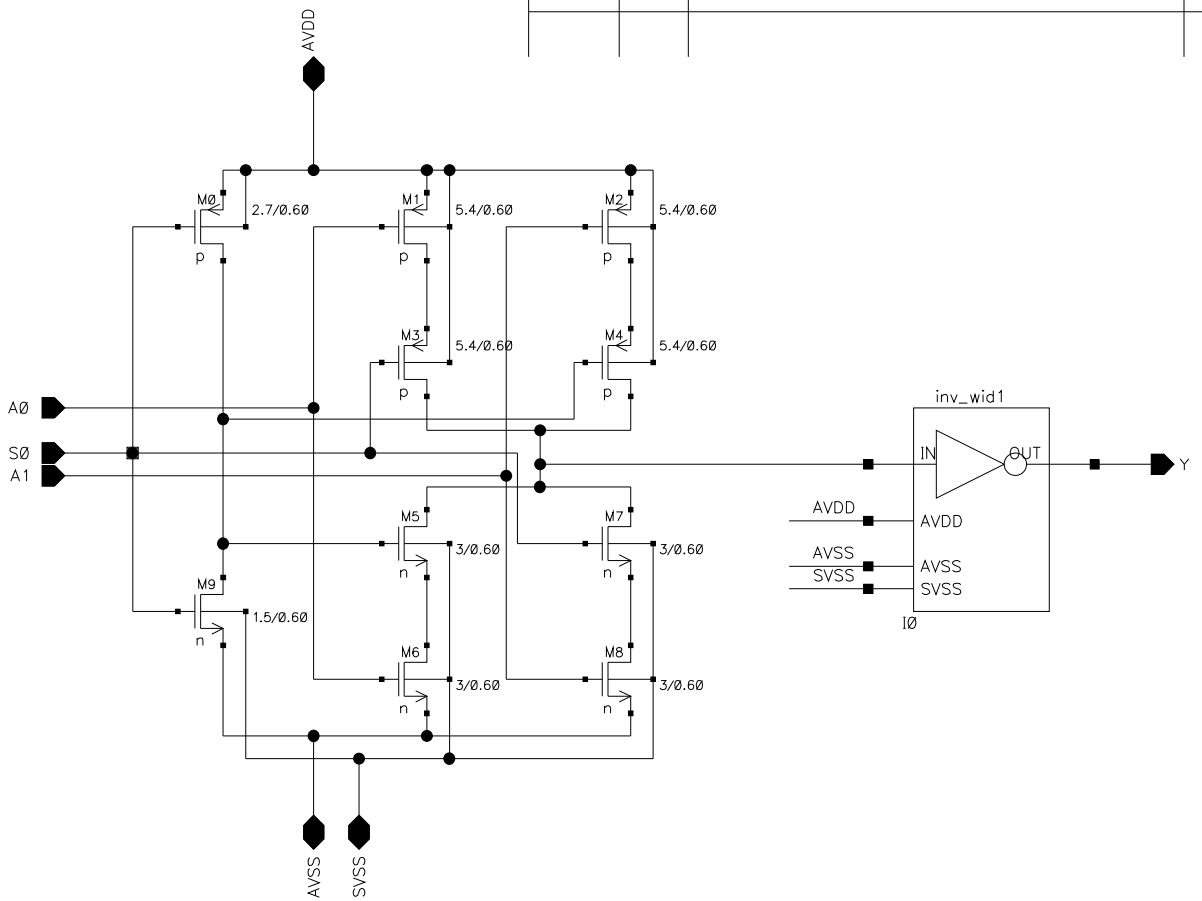


UPDATED Jan 25 15:54:23 2007	PadAref			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

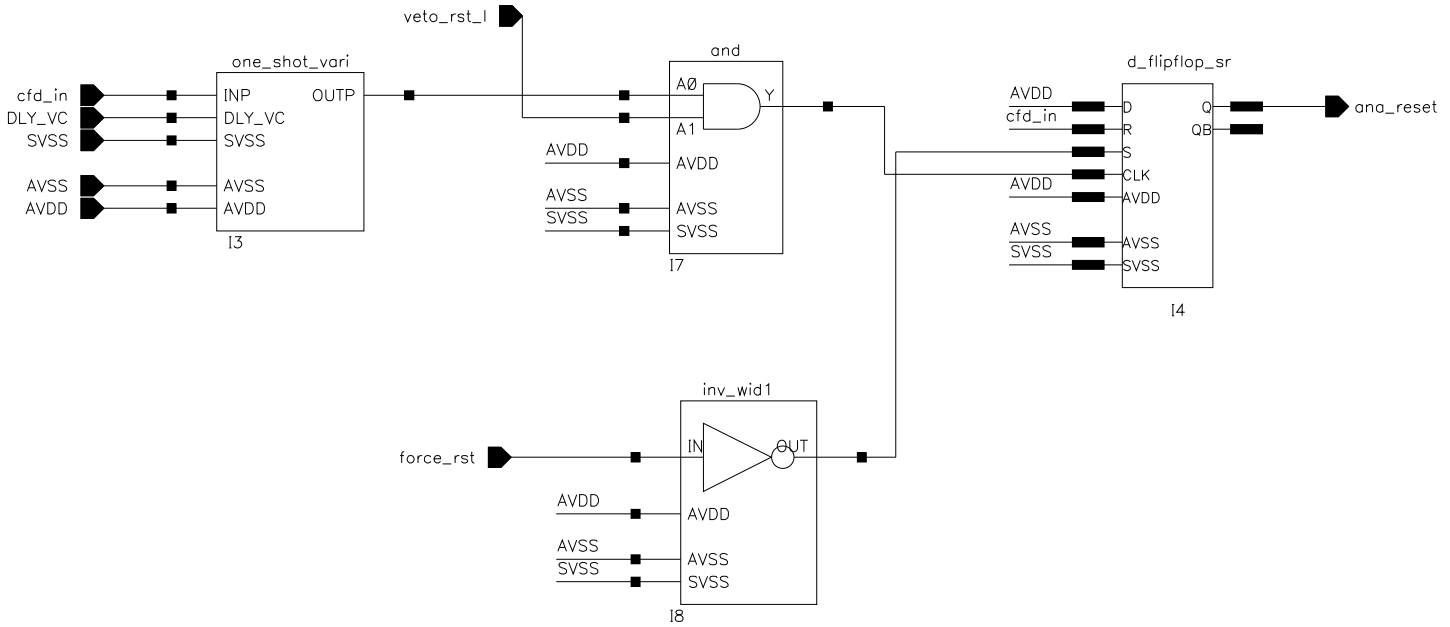


UPDATED Jun 25 14:12:18 2010	mux21			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV A

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

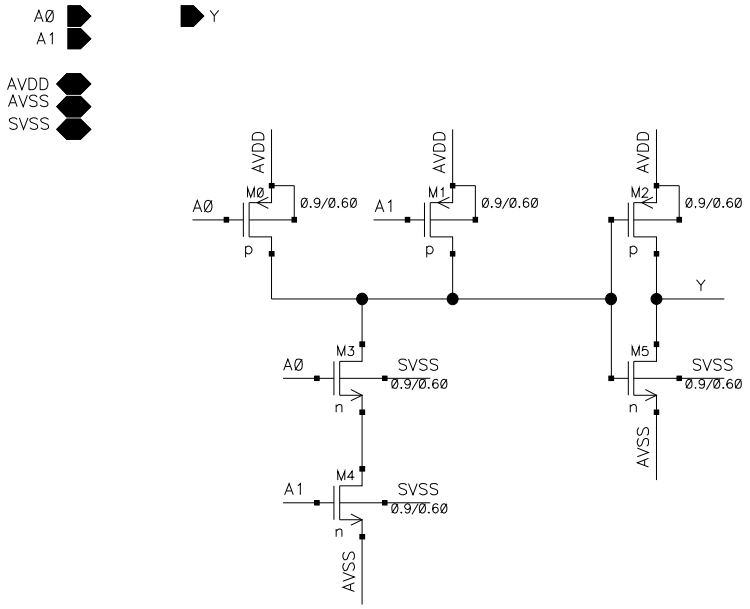


UPDATED	Jun 22 14:28:58 2010	SIUE IC Design Lab	
DRAWN		Reset Logic	
CHECKED			
CHECKED		SIZE A / CAGE NO. / DWG NO.	REV A
ISSUED		SCALE	SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

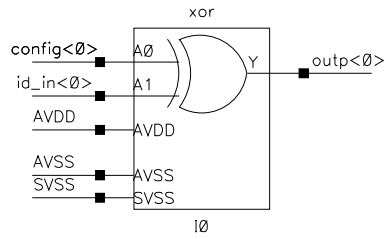


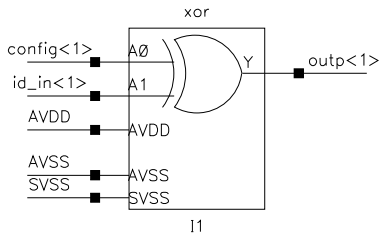
UPDATED Aug 8 14:14:18 2007	and			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

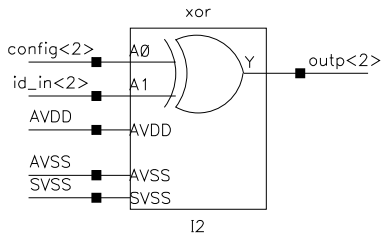
CAGE NO.	DWG NO.	SH 1	REV

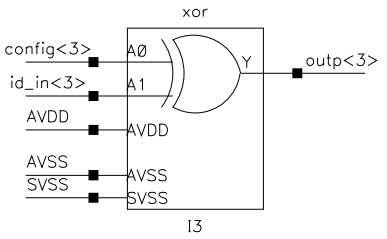
REVISIONS

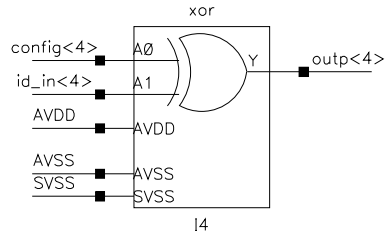
ZONE	REV	DESCRIPTION	DATE	APPROVED

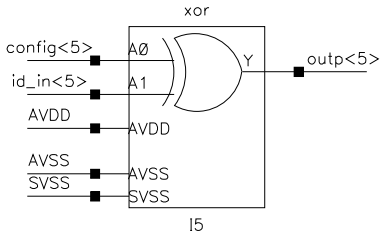


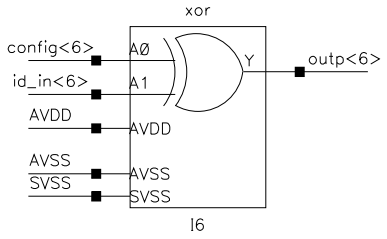


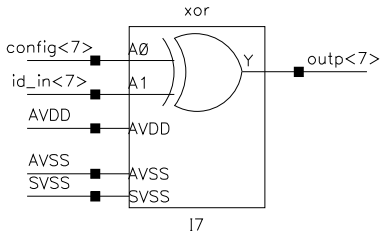


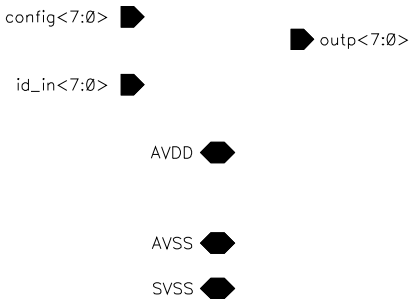












UPDATED	comparator		
Jun 25 13:52:10 2010			
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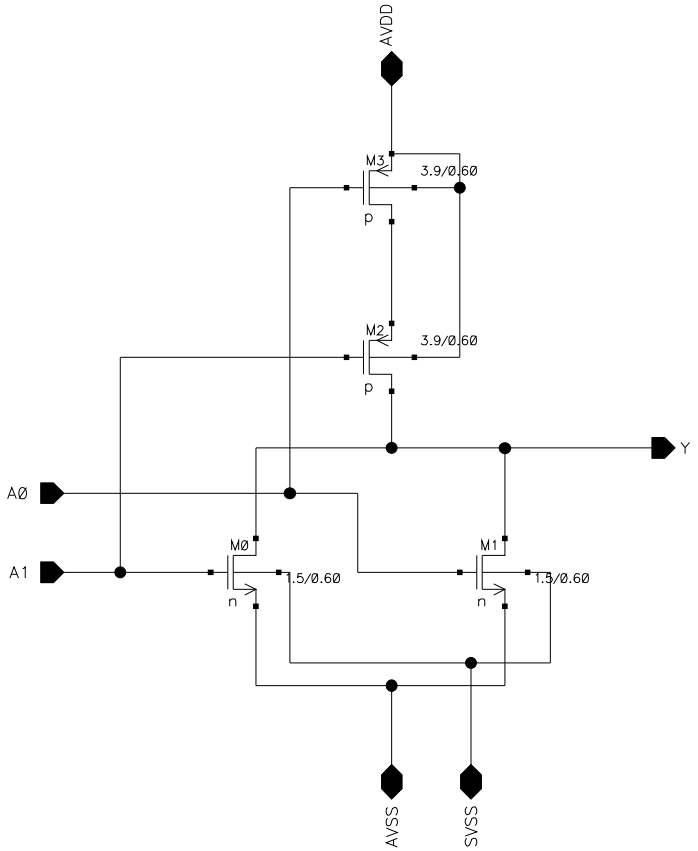
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

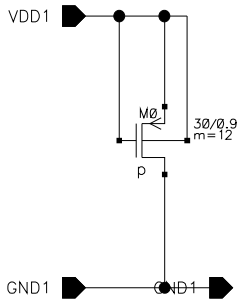


UPDATED Jun 22 12:47:58 2007	nor			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

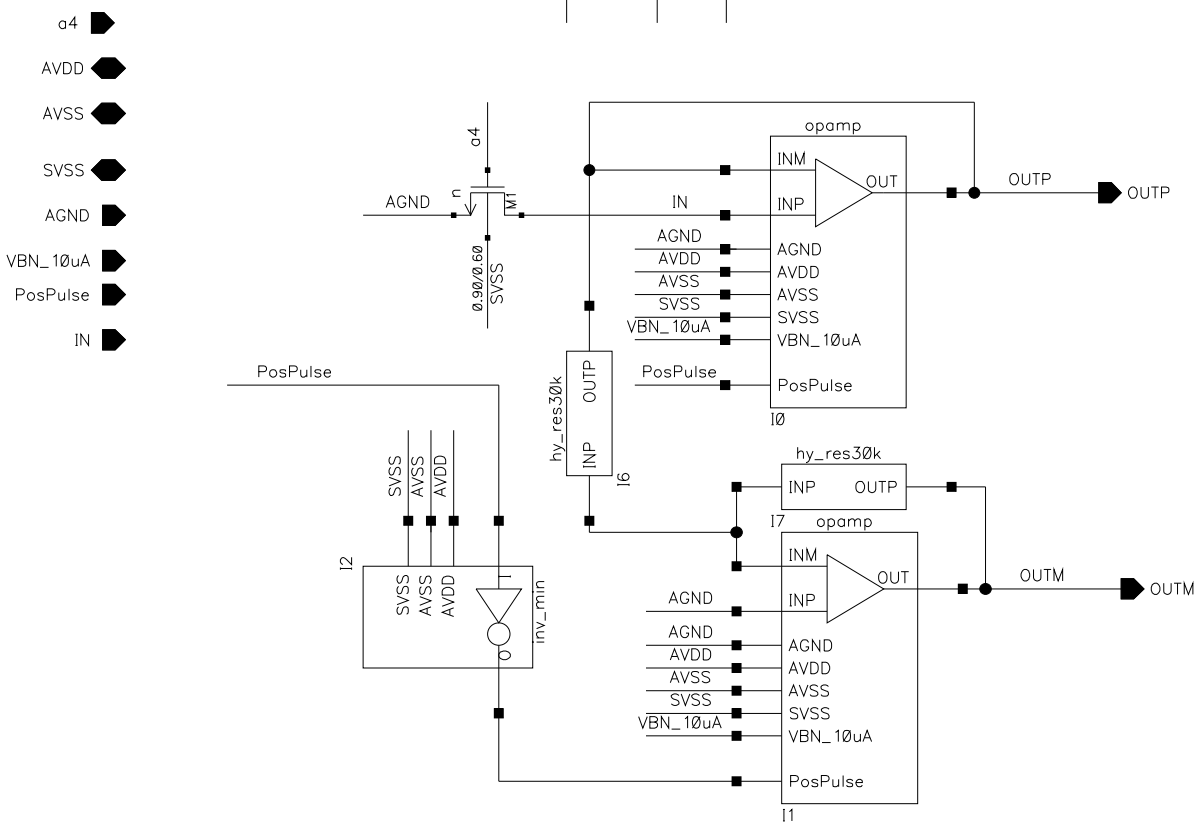


UPDATED Nov 11 15:38:19 2ØØ4	PadGnd			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

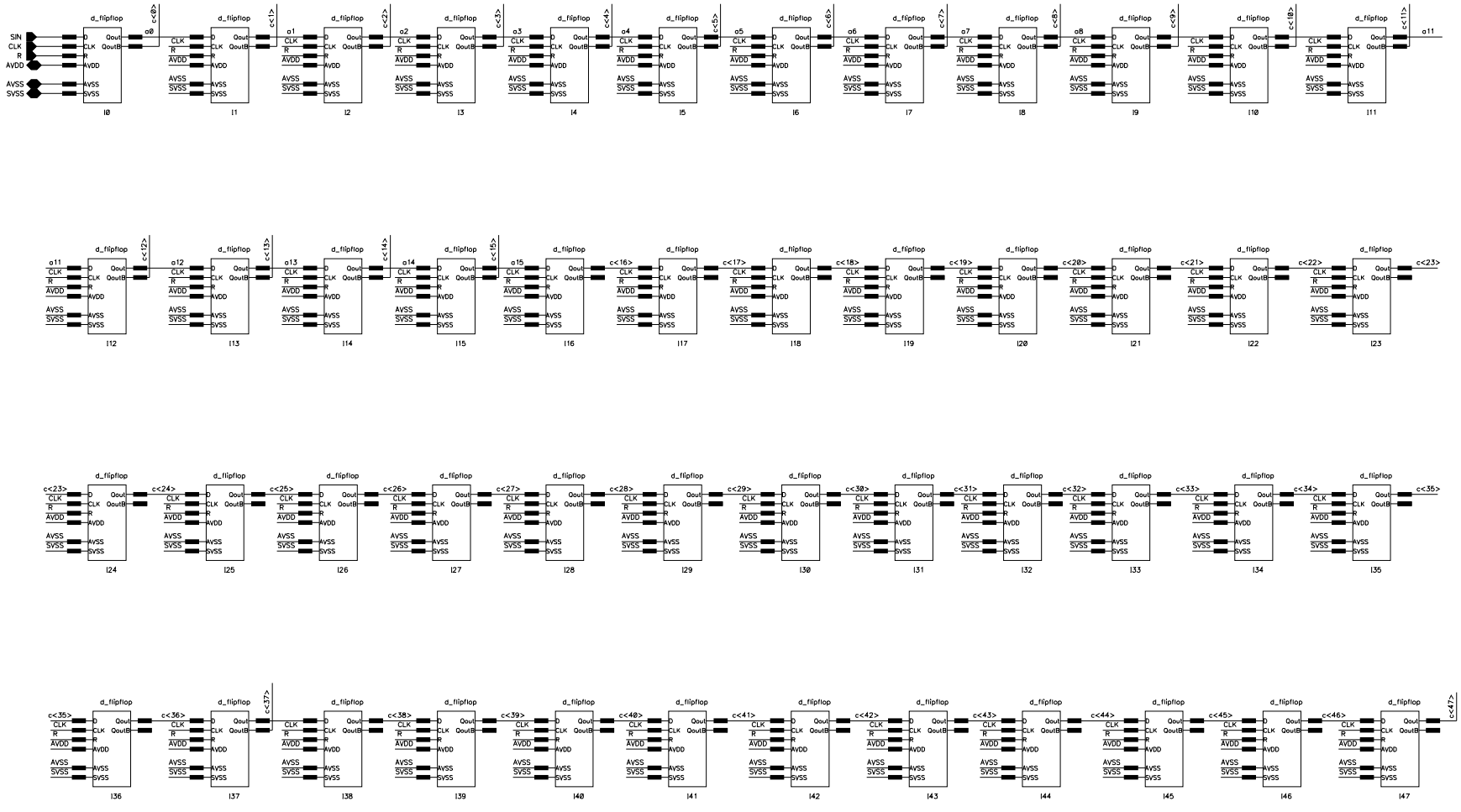
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED			
Jul 5 13:11:41 2011			
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



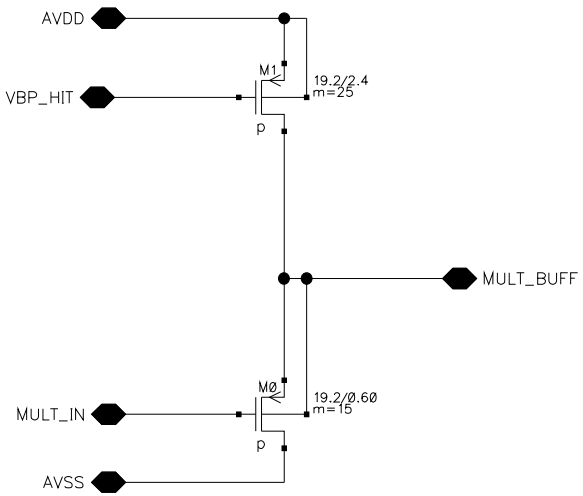
UPDATED	Jul 15 14:53:54 2010	config_reg	
DRAWN			
CHECKED			
CHECKED		SIZE C / CAGE NO. / DWG NO. / REV	
ISSUED		SCALE / SHEET 1 OF 1	

REV | SH 1 | DWG NO. | CAGE NO.

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Sep 12 17:19:01 2007	MULT_BUF			
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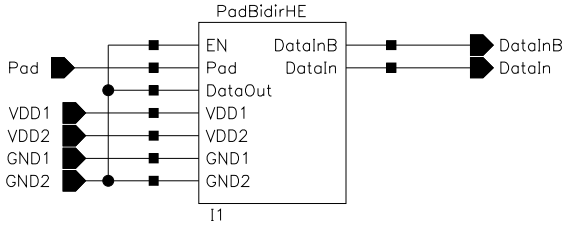
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

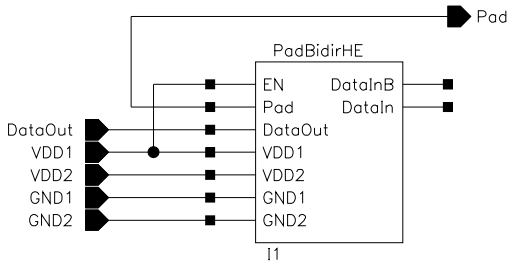


UPDATED Mar 2 14:46:22 2017	PadInc		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

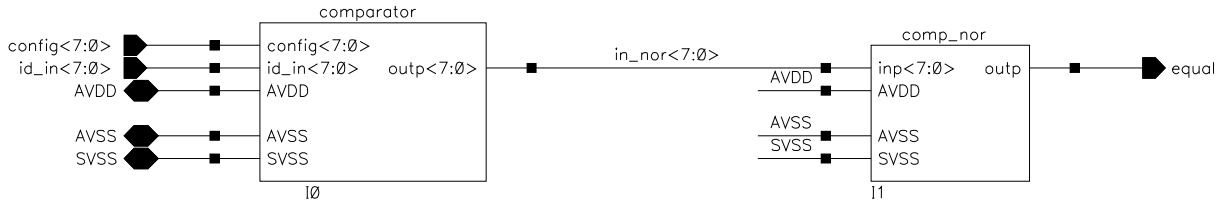


UPDATED Apr 28 16:14:10 2016	PadOut			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

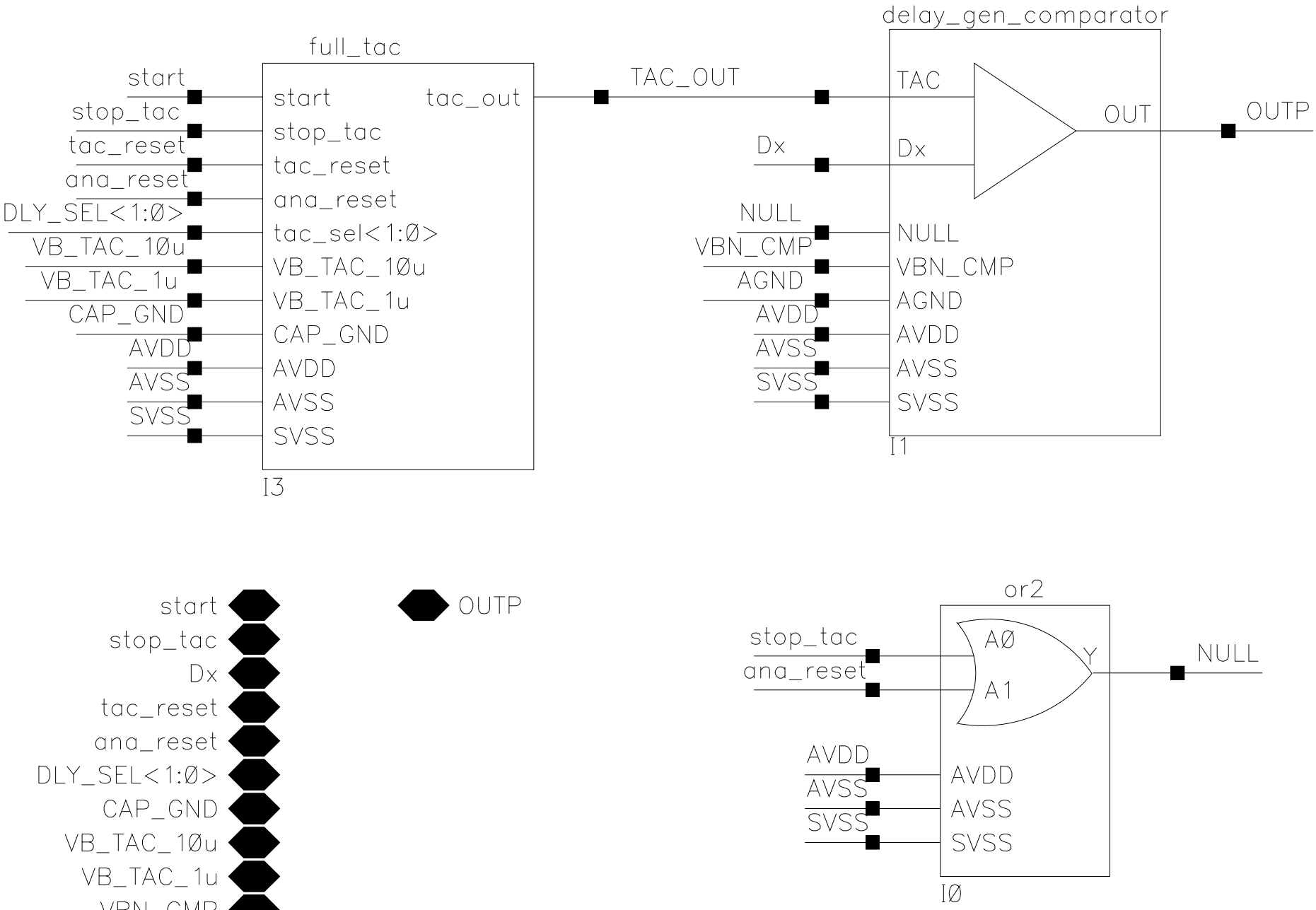
CAGE NO.	DWG NO.	SH 1	REV

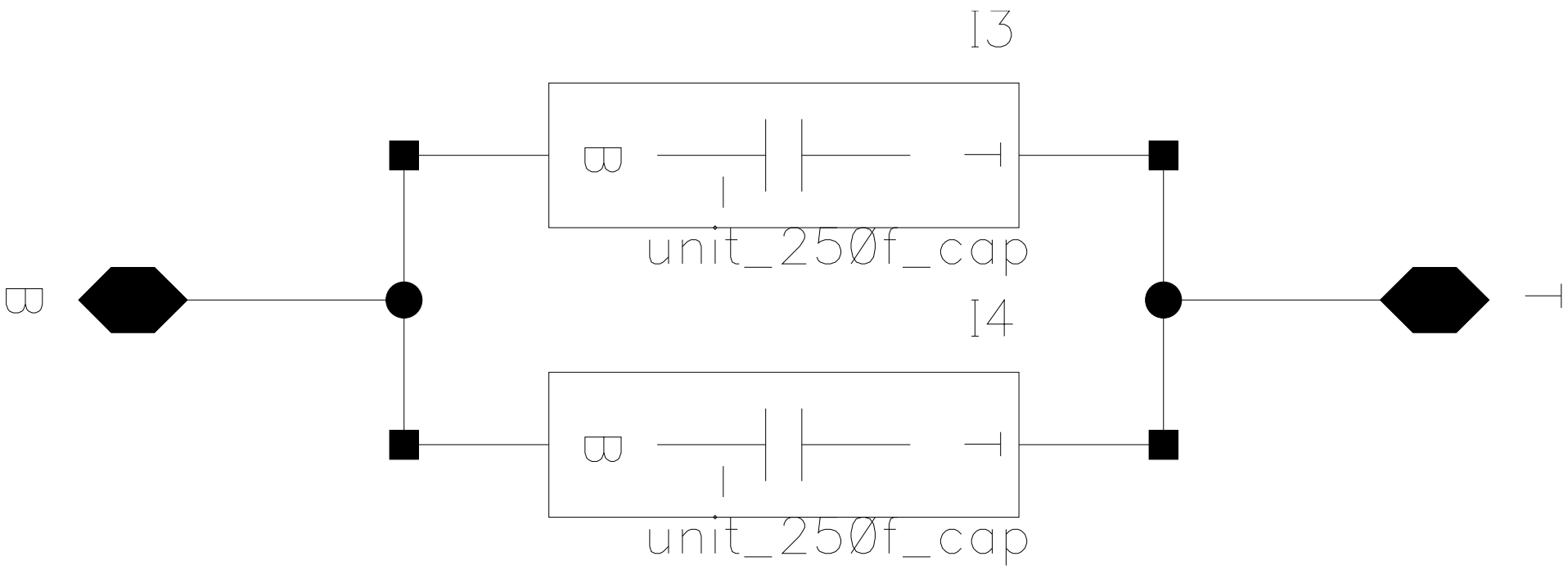
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jun 25 13:53:00 2010	equal_logic		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

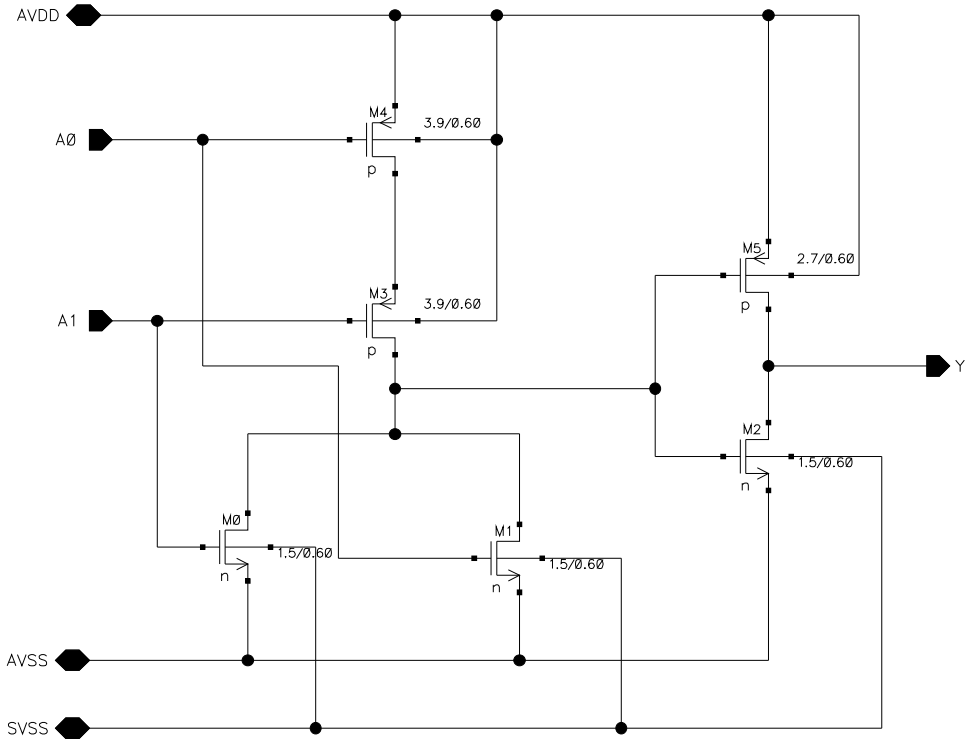

full_tac
start
stop_tac
tac_reset
ana_reset
DLY_SEL<1:0>
VB_TAC_10u
VB_TAC_1u
CAP_GND
AVDD
AVSS
SVSS
start
stop_tac
tac_reset
ana_reset
tac_sel<1:0>
VB_TAC_10u
VB_TAC_1u
CAP_GND
AVDD
AVSS
SVSS
tac_out
I3
TAC_OUT
delay_gen_comparator
TAC
Dx
NULL
VBN_CMP
AGND
AVDD
AVSS
SVSS
TAC
Dx
NULL
VBN_CMP
AGND
AVDD
AVSS
SVSS
OUT
OUTP
I1
start
stop_tac
Dx
tac_reset
ana_reset
DLY_SEL<1:0>
CAP_GND
VB_TAC_10u
VB_TAC_1u
VBN_CMP
AGND
AVDD
AVSS
SVSS
OUTP
or2
stop_tac
ana_reset
AVDD
AVSS
SVSS
A0
A1
Y
AVDD
AVSS
SVSS
NULL
I0


I3
B
unit_250f_cap
B
I4
B
unit_250f_cap
B
T

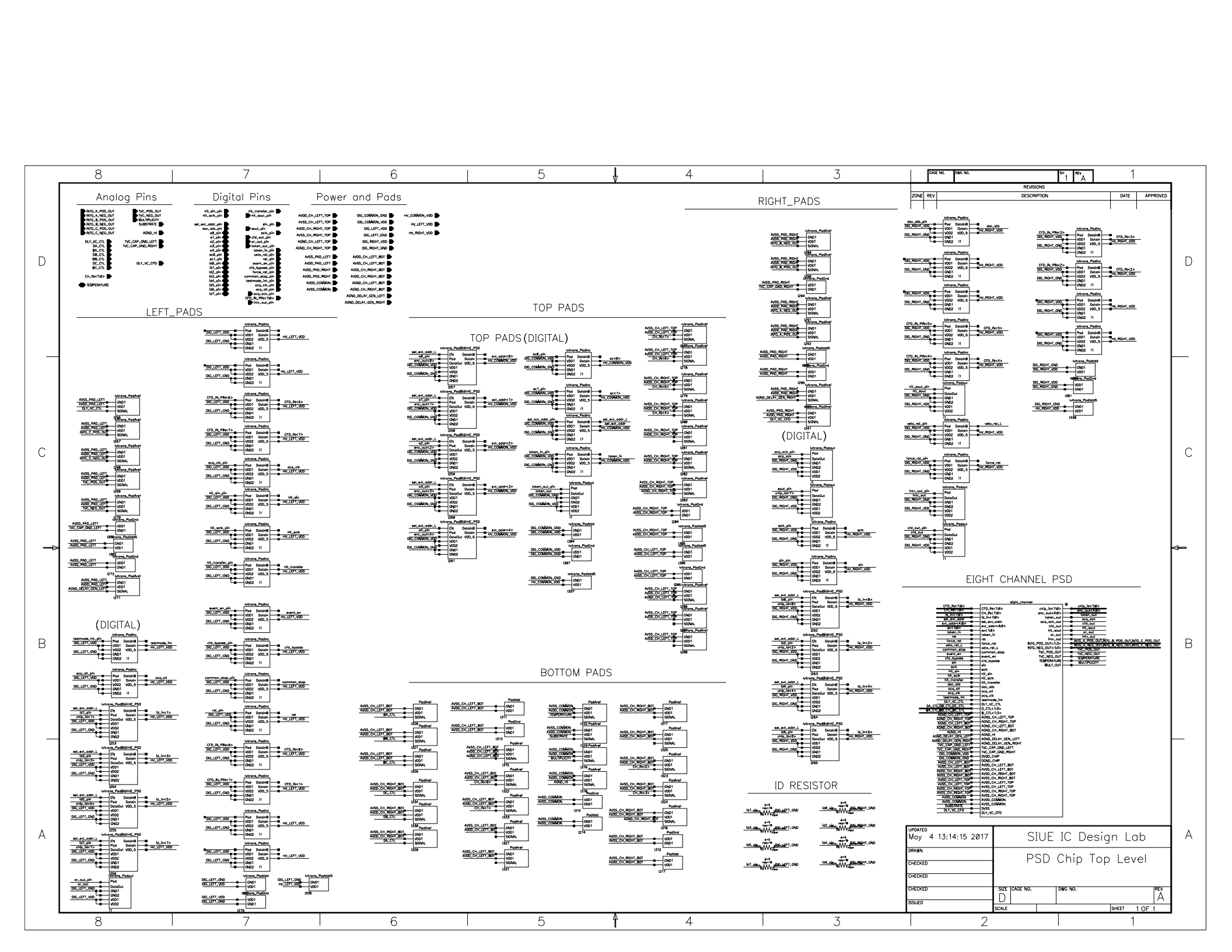
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



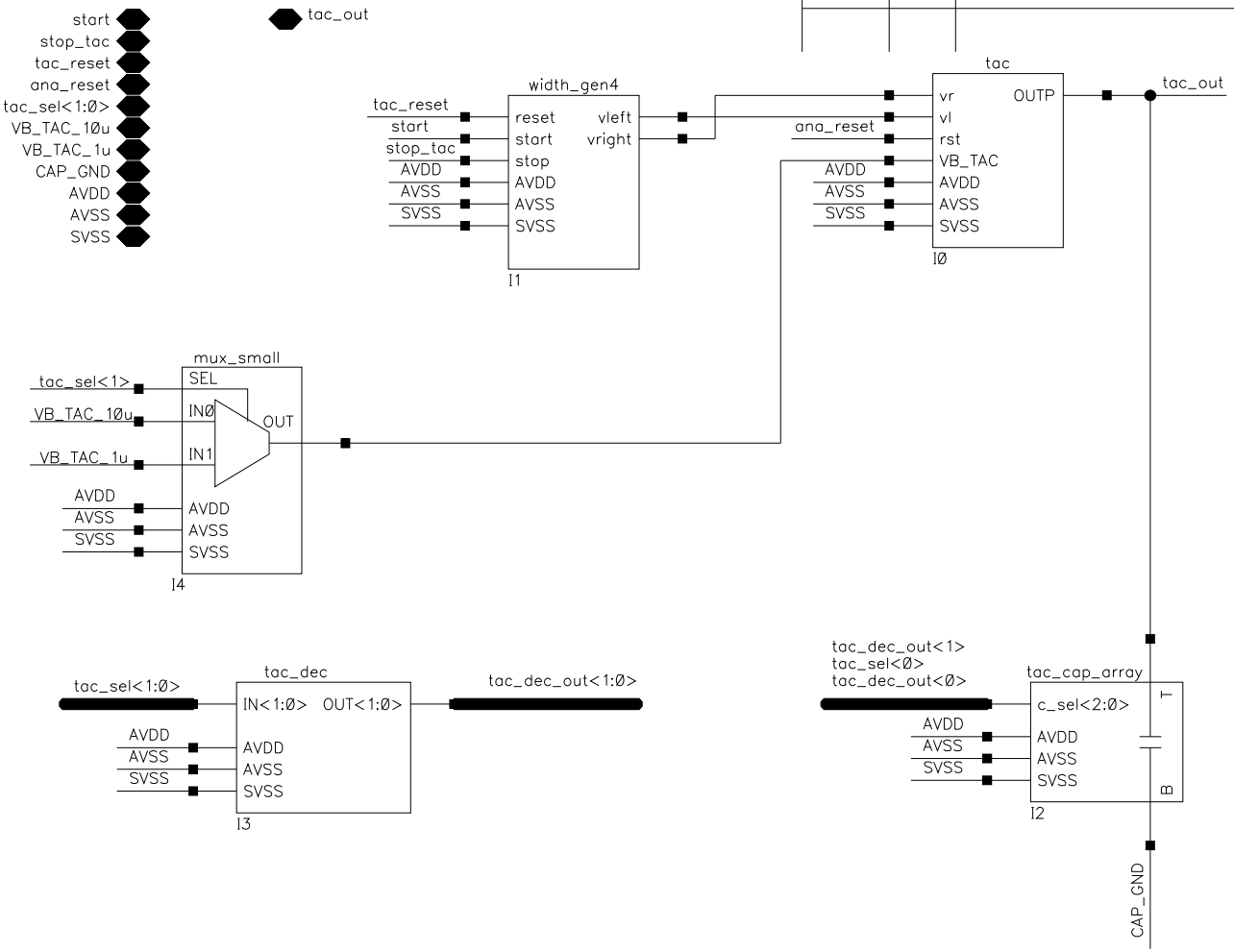
UPDATED	Or		
Jul 6 11:07:39 2007			
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1


Analog Pins
Digital Pins
Power and Pads
LEFT_PADS
TOP PADS
TOP PADS (DIGITAL)
BOTTOM PADS
RIGHT_PADS
(DIGITAL)
ID RESISTOR
EIGHT CHANNEL PSD
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
CAGE NO.
DWG NO.
SH 1
REV A
UPDATED
May 4 13:14:15 2017
DRAWN
CHECKED
CHECKED
CHECKED
ISSUED
SIUE IC Design Lab
PSD Chip Top Level
SIZE D
CAGE NO.
DWG NO.
REV A
SCALE
SHEET 1 OF 1

CAGE NO.	DWG NO.	SH	REV
		1	

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



tac_sel	I (uA)	C (pf)	Tmax (ns)	Tmin (ns)
00	10	0.2	50	5
01	10	1.0	250	25
10	1	0.6	1500	150
11	1	4.0	10000	1000

Note: Assume Vmax = 2.5 and Vmin = 0.25

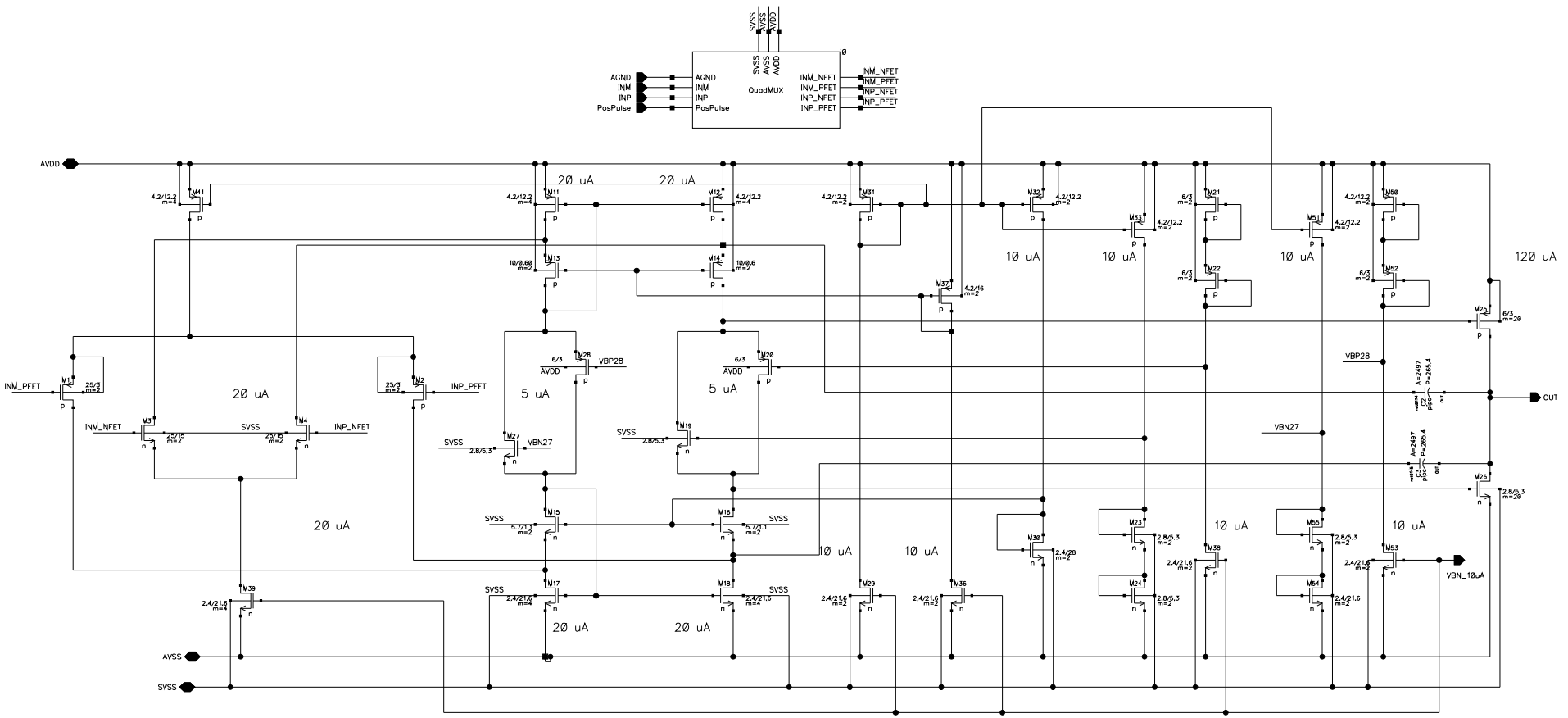
UPDATED Jul 9 12:33:14 2007	full_tac		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

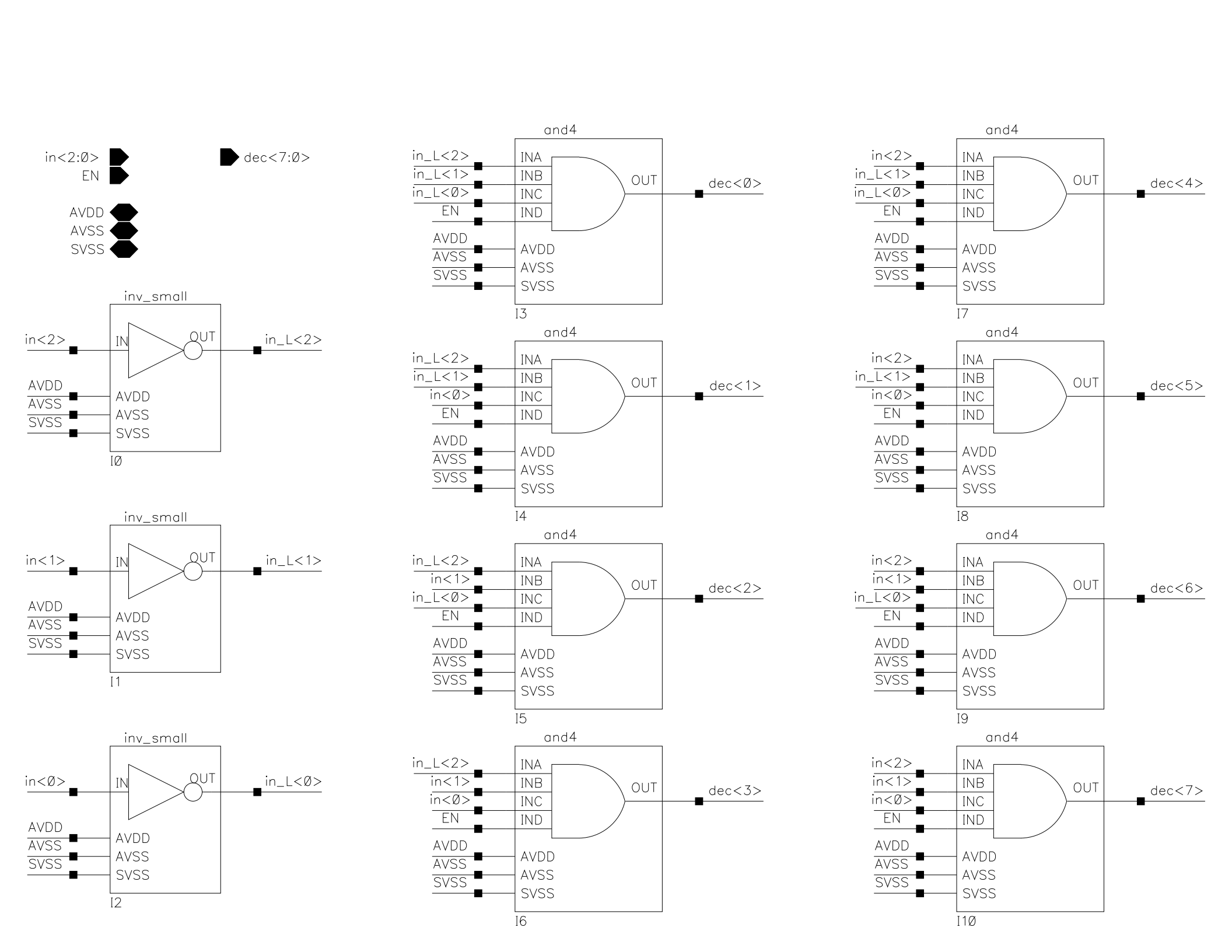
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

UPDATED Jul 5 11:28:47 2011	hy_res5k			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	



AGND
INM
INP
PosPulse
QuadMUX
INM_NFET
INM_PFET
INP_NFET
INP_PFET
SVSS
AVSS
AVDD
I0
AVDD
AVSS
SVSS
OUT
VBN_10uA
VBP28
VBN27
20 uA
5 uA
10 uA
120 uA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EN
dec<7:0>
AVDD
AVSS
SVSS
inv_small
in<2>
IN
OUT
in_L<2>
AVDD
AVSS
SVSS
I0
inv_small
in<1>
IN
OUT
in_L<1>
AVDD
AVSS
SVSS
I1
inv_small
in<0>
IN
OUT
in_L<0>
AVDD
AVSS
SVSS
I2
and4
in_L<2>
in_L<1>
in_L<0>
EN
AVDD
AVSS
SVSS
INA
INB
INC
IND
OUT
dec<0>
AVDD
AVSS
SVSS
I3
and4
in_L<2>
in_L<1>
in<0>
EN
AVDD
AVSS
SVSS
INA
INB
INC
IND
OUT
dec<1>
AVDD
AVSS
SVSS
I4
and4
in_L<2>
in<1>
in_L<0>
EN
AVDD
AVSS
SVSS
INA
INB
INC
IND
OUT
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AVSS
SVSS
I5
and4
in_L<2>
in<1>
in<0>
EN
AVDD
AVSS
SVSS
INA
INB
INC
IND
OUT
dec<3>
AVDD
AVSS
SVSS
I6
and4
in<2>
in_L<1>
in_L<0>
EN
AVDD
AVSS
SVSS
INA
INB
INC
IND
OUT
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AVSS
SVSS
I7
and4
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in_L<1>
in<0>
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AVDD
AVSS
SVSS
INA
INB
INC
IND
OUT
dec<5>
AVDD
AVSS
SVSS
I8
and4
in<2>
in<1>
in_L<0>
EN
AVDD
AVSS
SVSS
INA
INB
INC
IND
OUT
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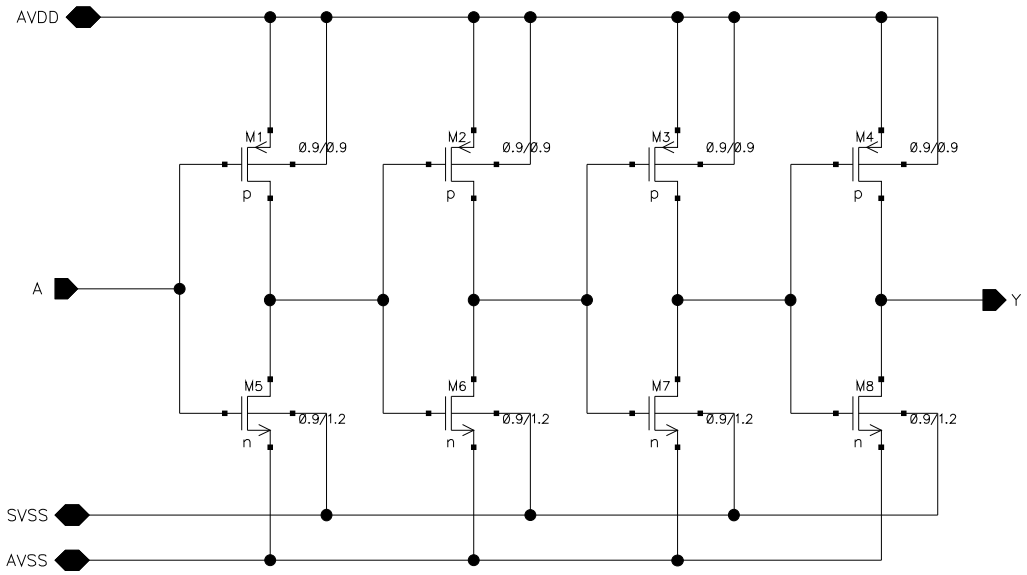
AVDD
AVSS
SVSS
I9
and4
in<2>
in<1>
in<0>
EN
AVDD
AVSS
SVSS
INA
INB
INC
IND
OUT
dec<7>
AVDD
AVSS
SVSS
I10

CAGE NO.	DWG NO.	SH 1	REV

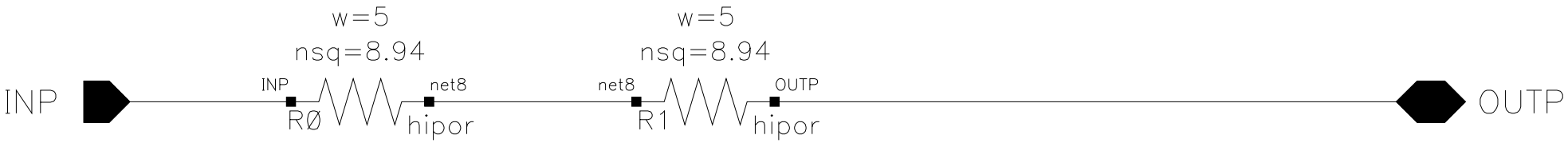
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	inv_12			
Mar 24 09:53:31 2010				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

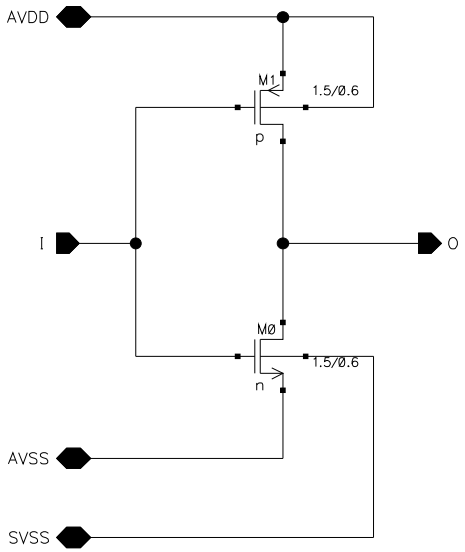
17k Resistor l = 85 & w = 5 (1.7 is overlap)



CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

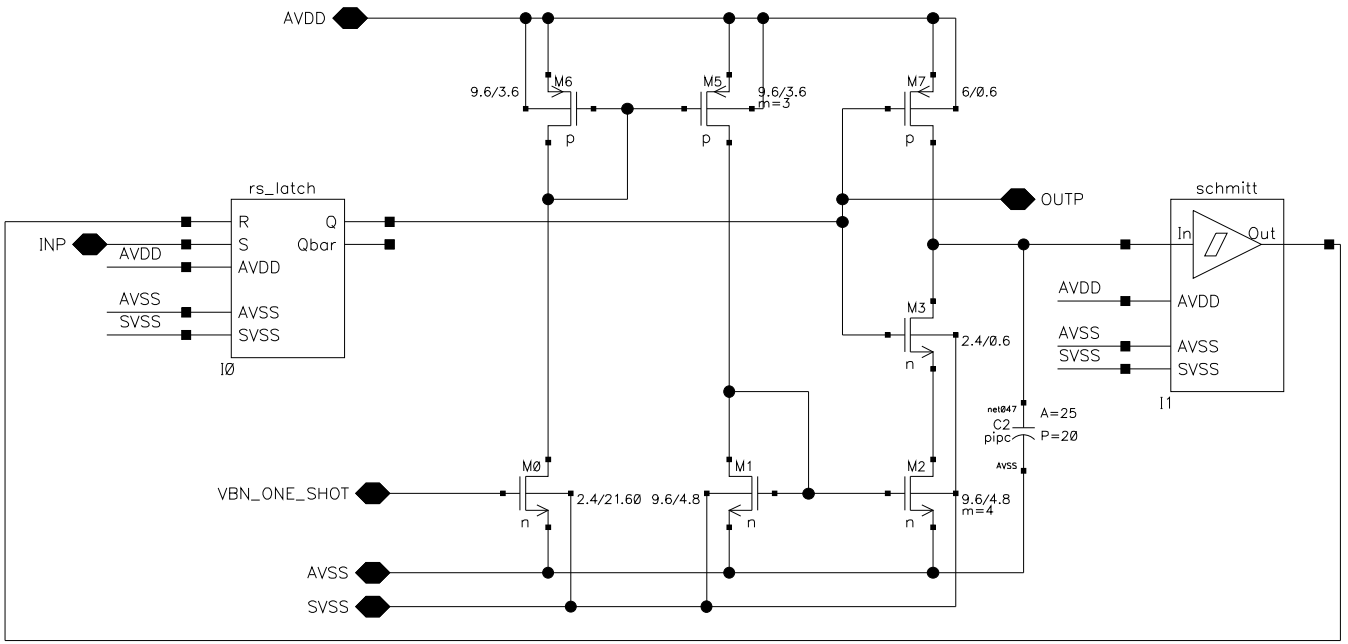


UPDATED	inv_min		
Jul 21 14:40:02 2011			
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. REV
ISSUED	SCALE		SHEET 1 OF 1

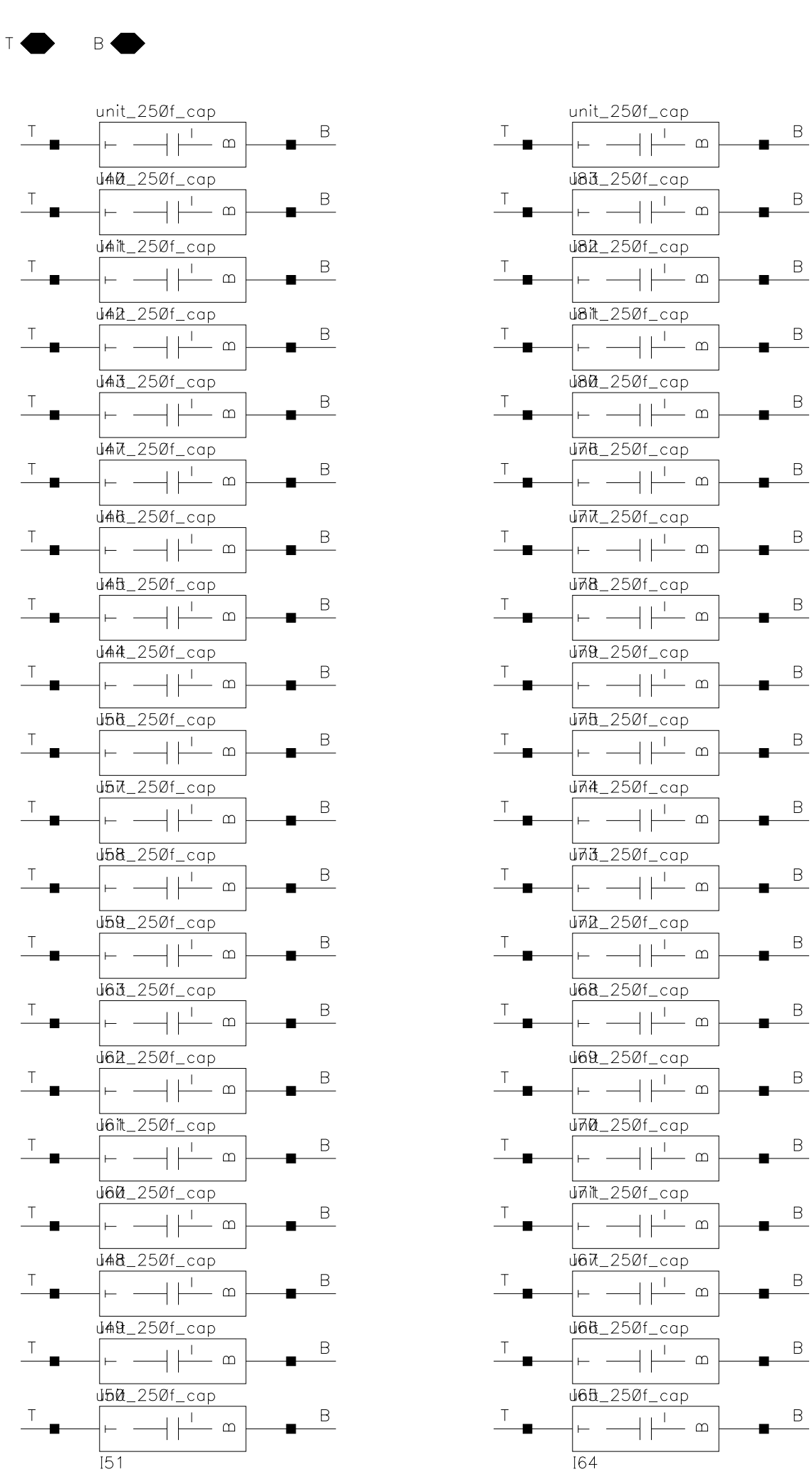
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



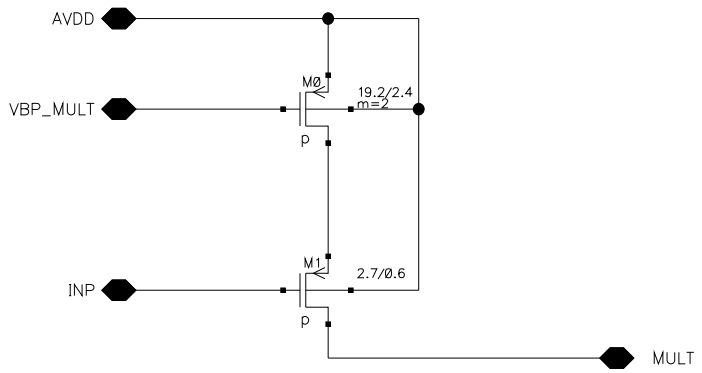
UPDATED Jul 25 17:41:17 2011	one_shot_100ns			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


T
B
unit_250f_cap
I51
I64

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

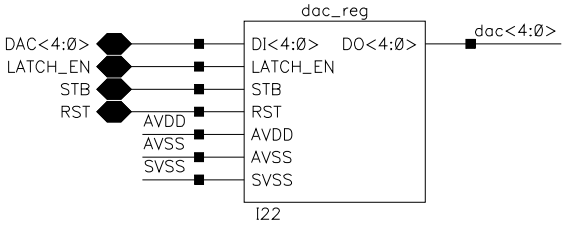


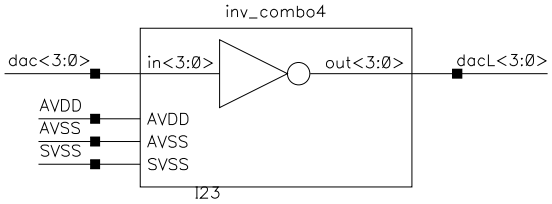
UPDATED Apr 11 15:35:44 2011	single_mult			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

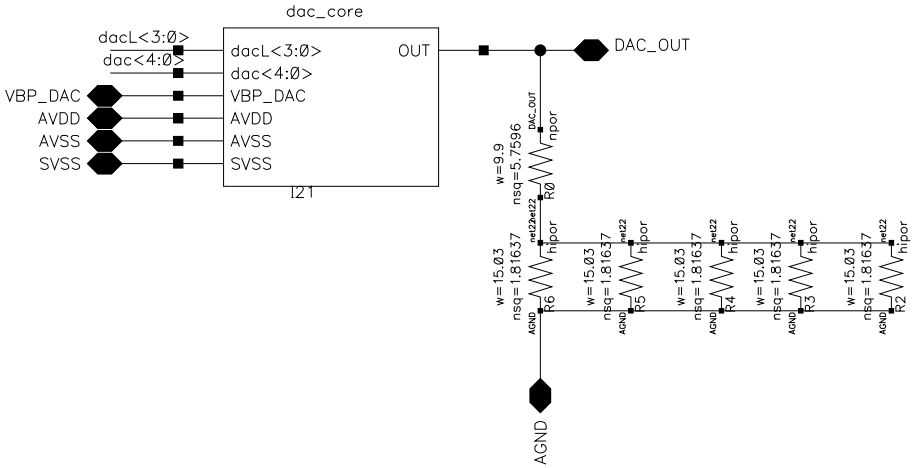
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED





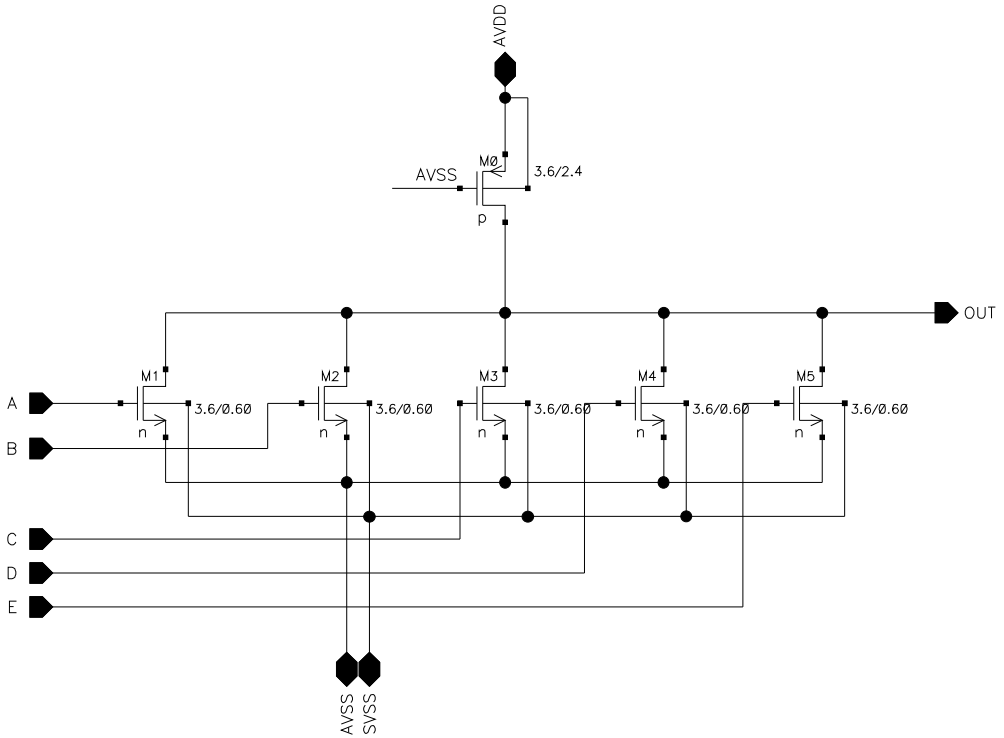


UPDATED Jul 6 12:17:24 2011	dac			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

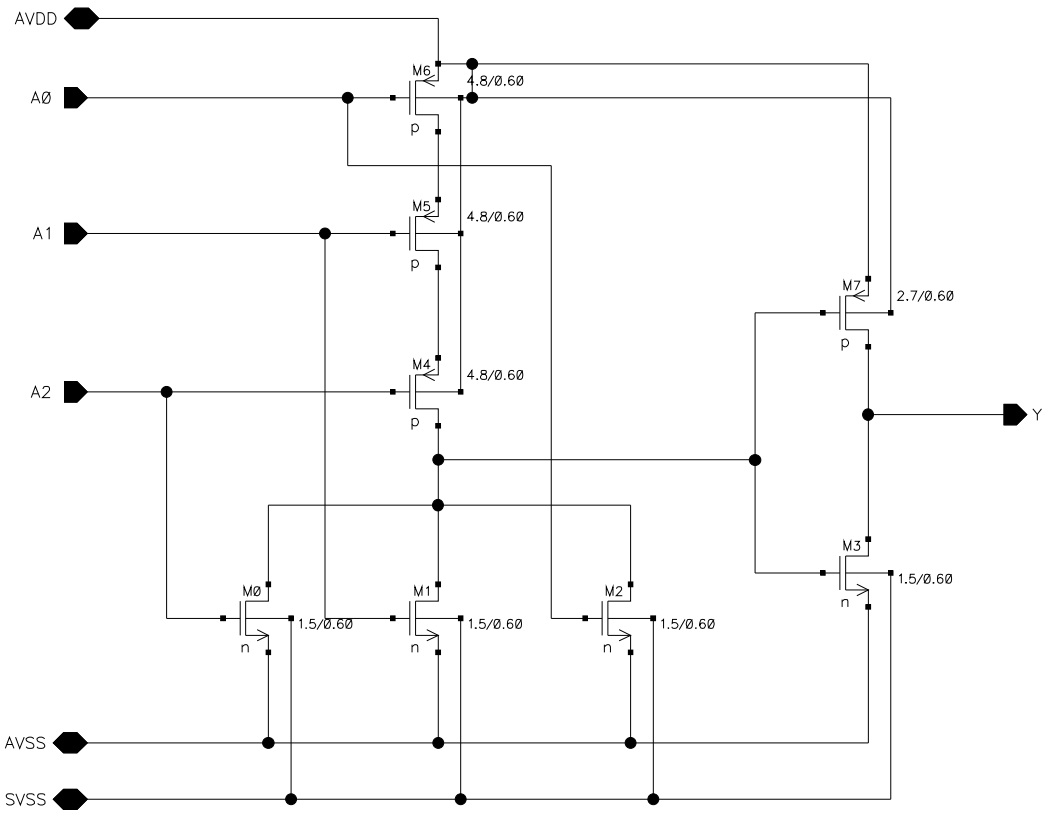


UPDATED Jul 11 13:37:50 2007	pseudo_nor		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

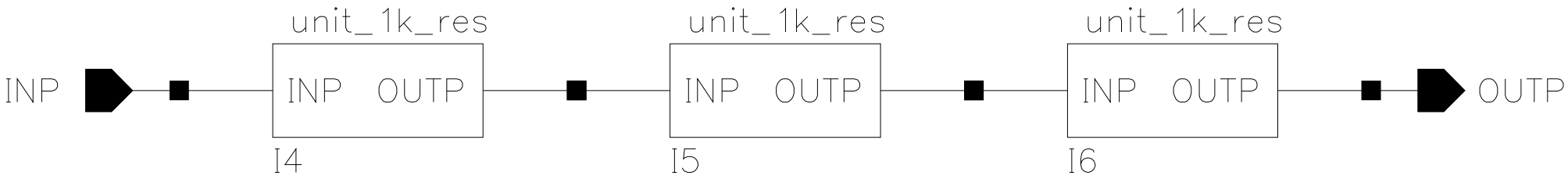
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



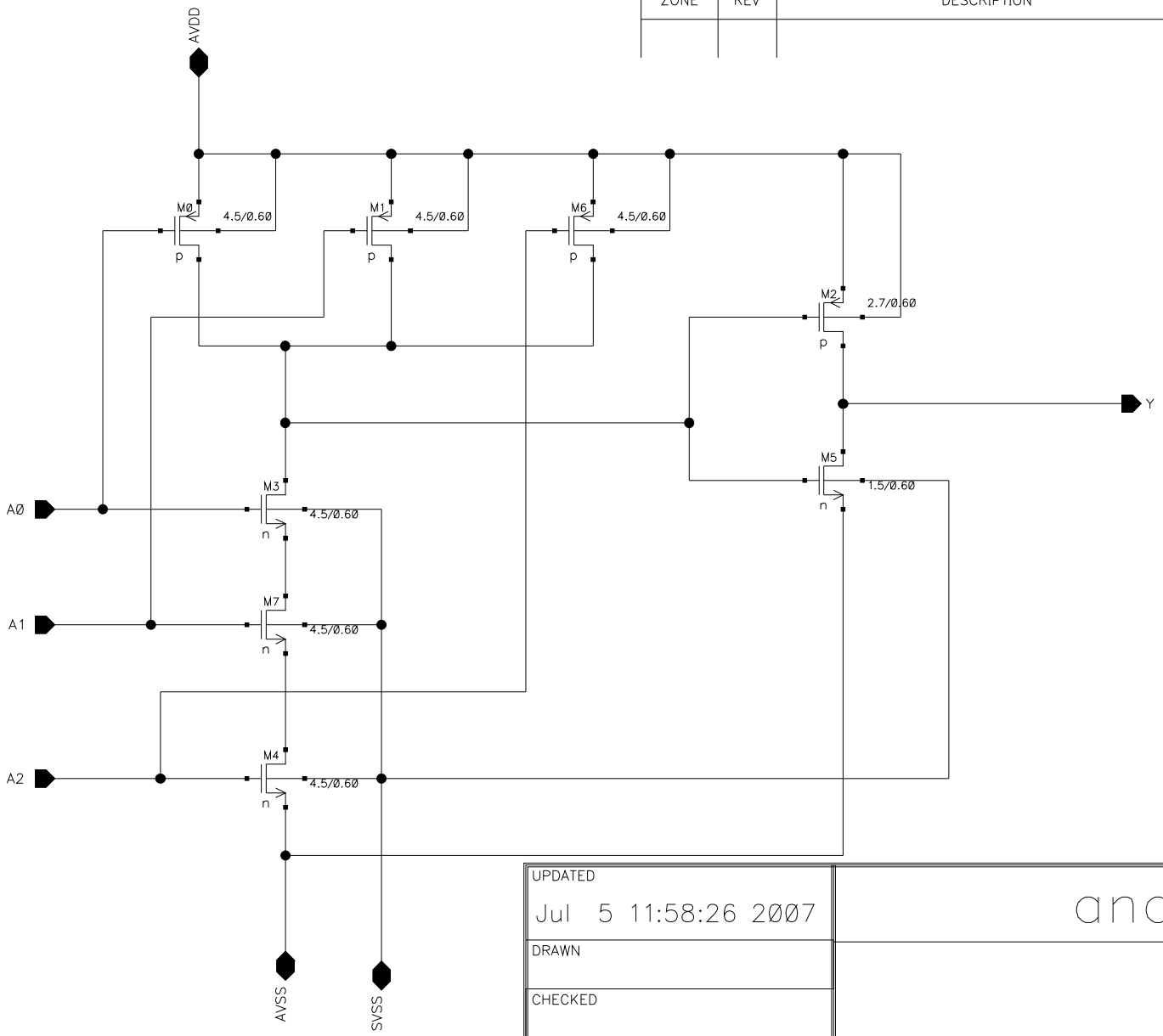
UPDATED Jun 11 15:46:50 2007	or_3inp			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


unit_1k_res
unit_1k_res
unit_1k_res
INP
INP OUTP
INP OUTP
INP OUTP
OUTP
I4
I5
I6

CAGE NO.	DWG NO.	SH	REV
		1	

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

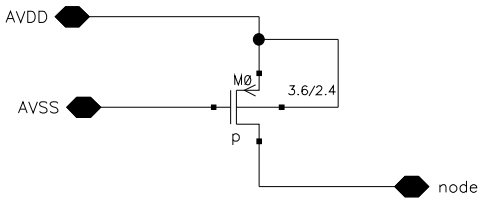


UPDATED Jul 5 11:58:26 2007	and03		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

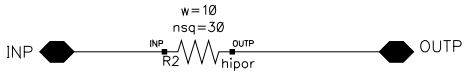
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Aug 3 14:33:16 2007	p_fet			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

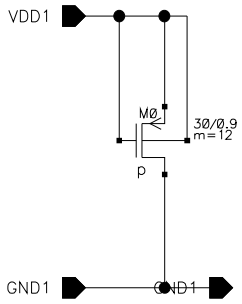


UPDATED Jul 5 13:09:10 2011	hy_res30k
DRAWN	
CHECKED	
CHECKED	SIZE A | CAGE NO. | DWG NO. | REV
ISSUED	SCALE | SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

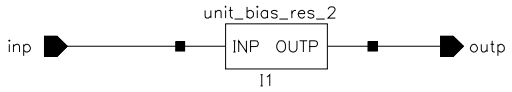


UPDATED Nov 11 15:38:19 2ØØ4	PadGnd			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

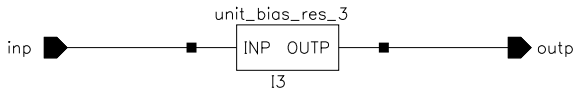


UPDATED Jul 5 11:32:50 2011	hy_res17k		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

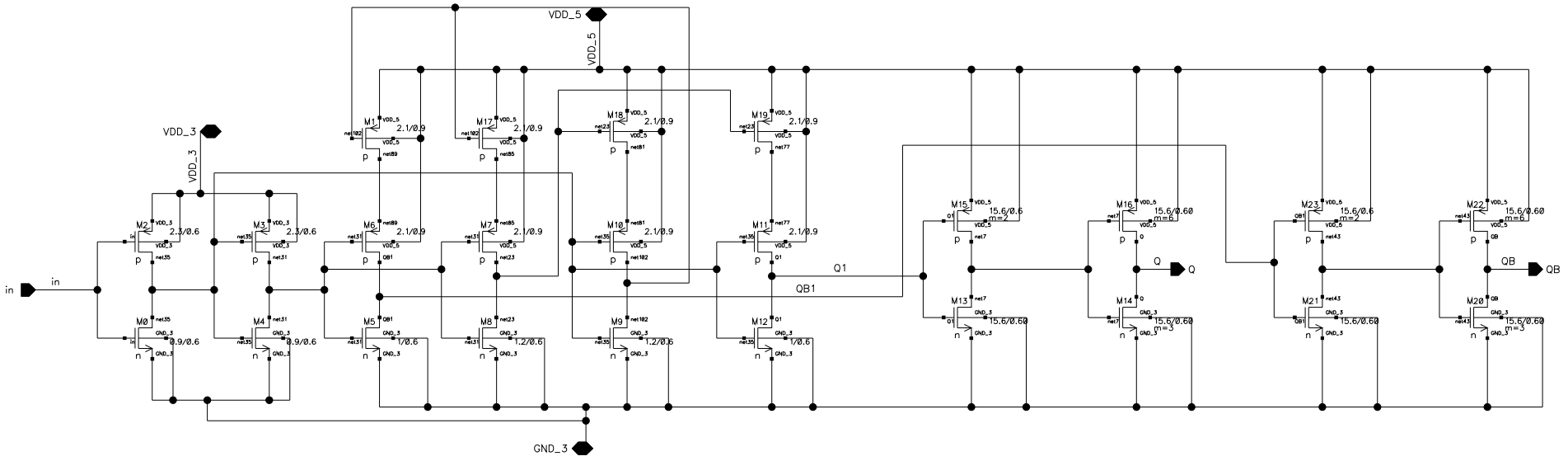
CAGE NO.	DWG NO.	SH 1	REV

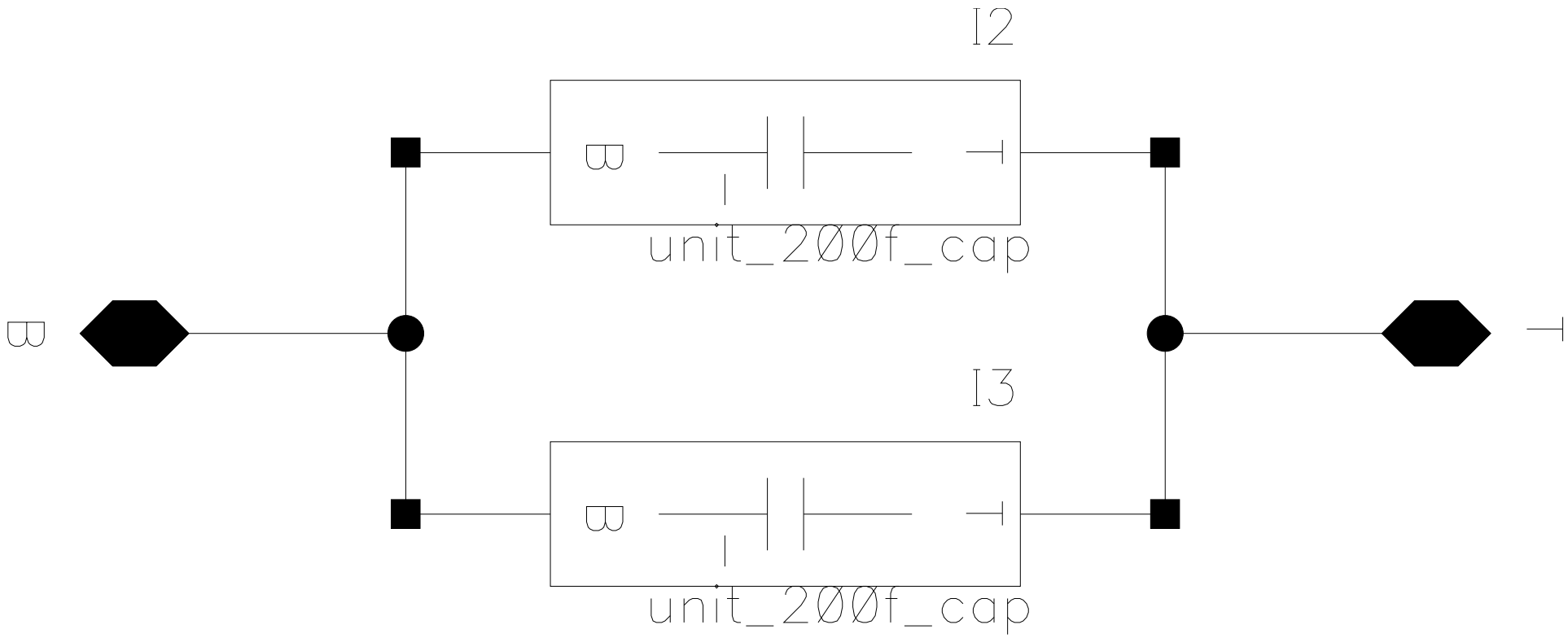
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jul 5 11:23:56 2011	hy_res0_59k			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

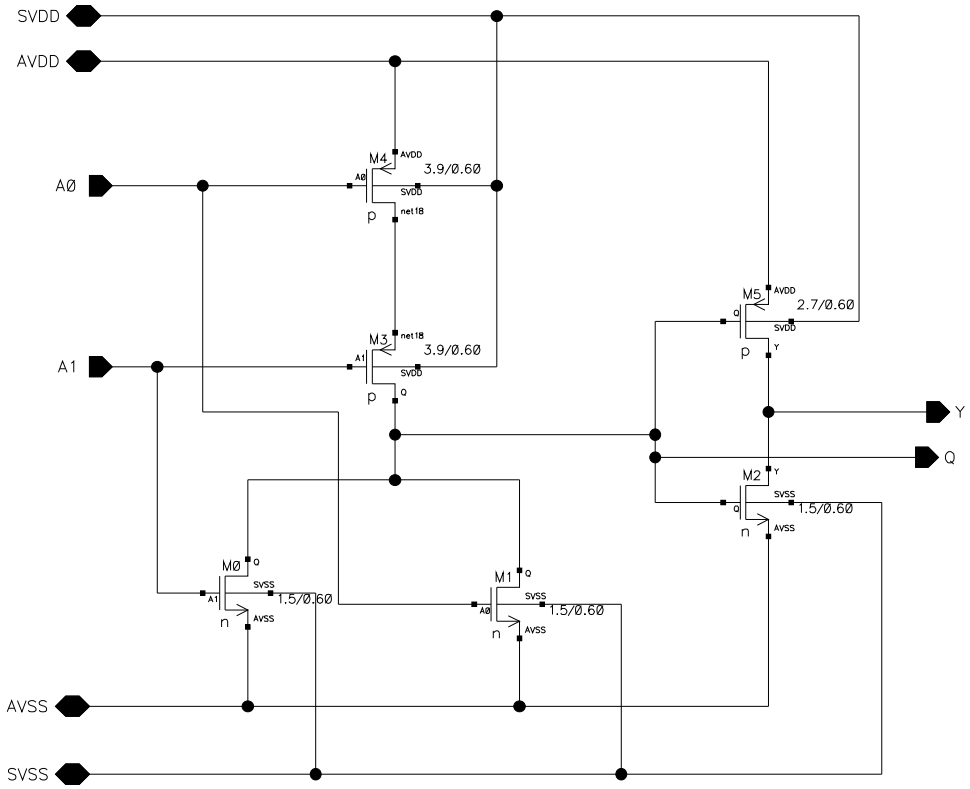

VDD_5
VDD_3
GND_3
in
Q1
QB1
Q
QB
M0
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M23
0.9/0.6
2.1/0.9
2.3/0.6
1/0.6
1.2/0.6
15.6/0.6
15.6/0.60
m=2
m=6
m=3


I2
B
T
unit_200f_cap
B
T
I3
B
T
unit_200f_cap
B
T

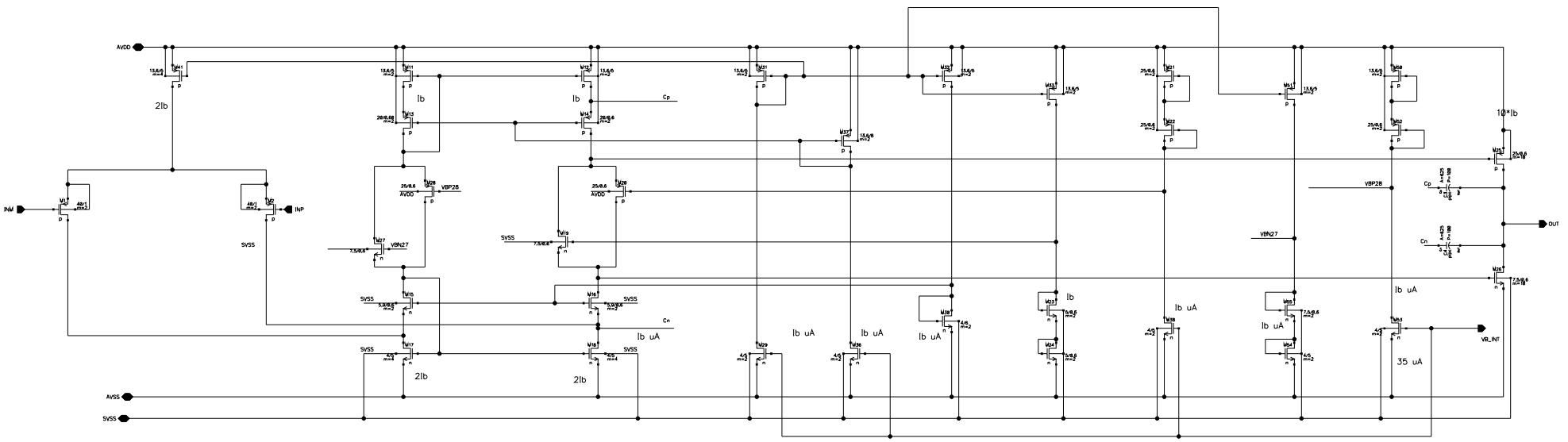
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



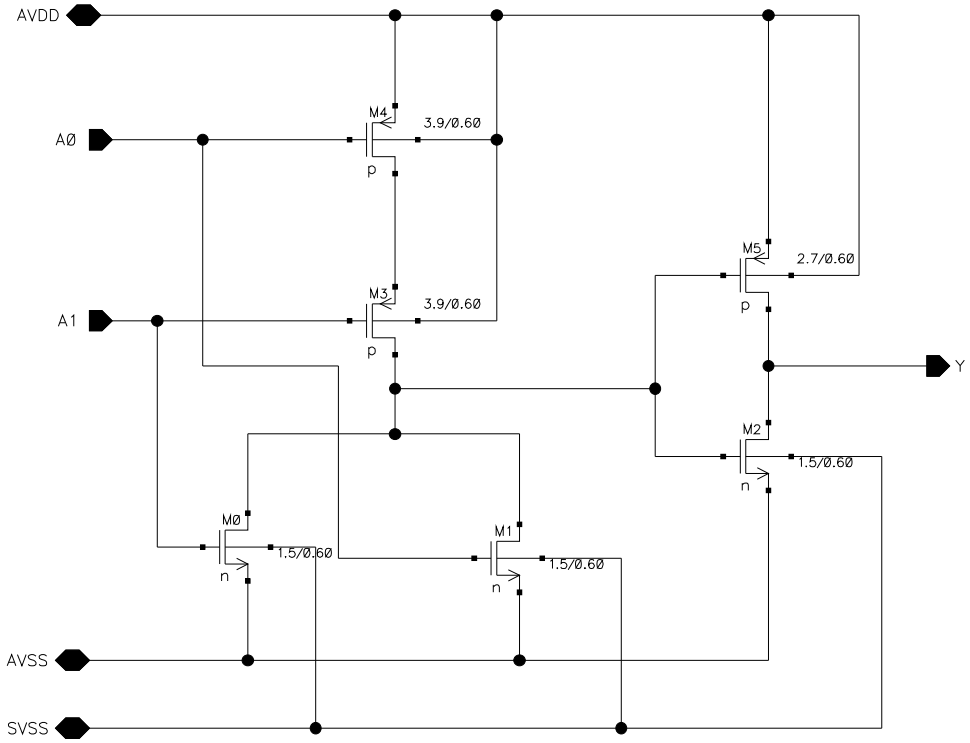
UPDATED Jul 30 12:40:16 2003	or_rslatch			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


AVDD
AVSS
SVSS
INM
INP
OUT
2Ib
Ib
Cp
Cn
VBP28
VBN27
10*Ib
35 uA
VB_INT

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

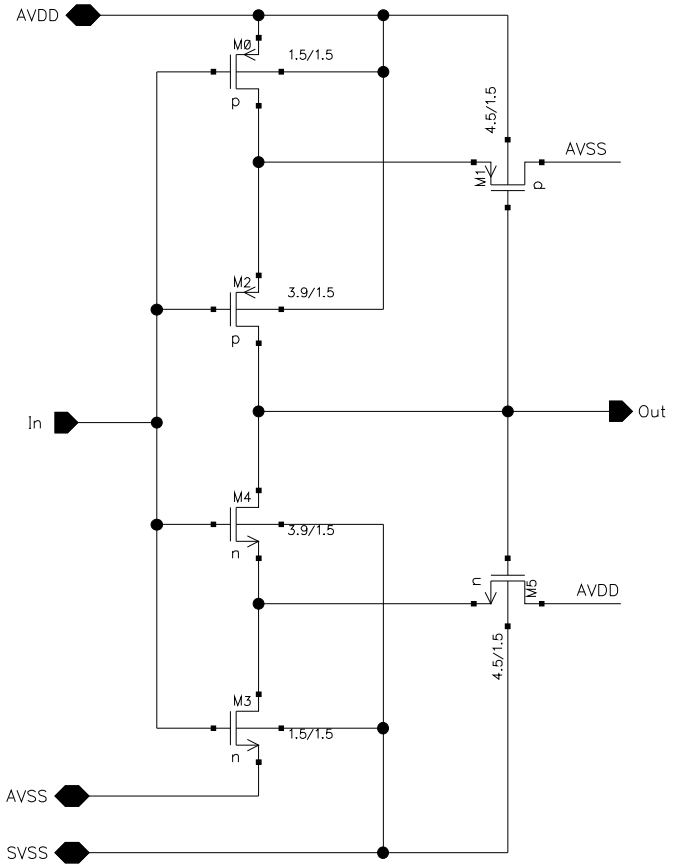


UPDATED Jun 11 15:23:02 2007	Or			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

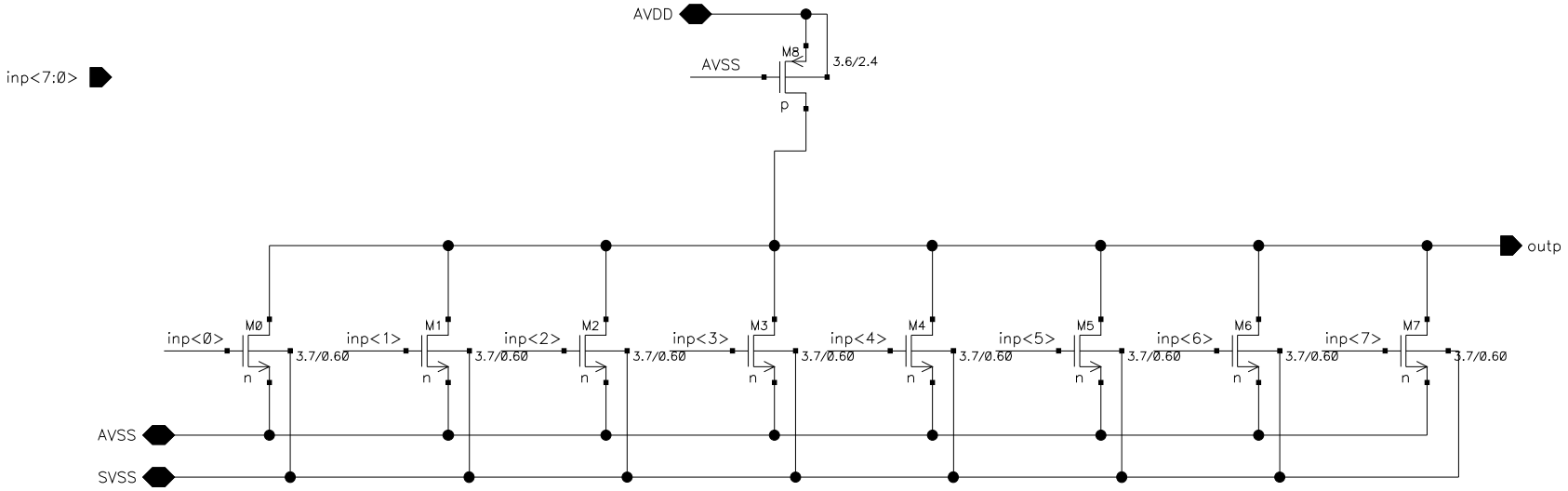


UPDATED Aug 13 11:29:31 2007	schmitt			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

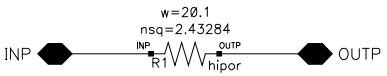


UPDATED Jul 6 10:56:07 2007	comp_nor			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

Resistor has l=48.9u and w=20.1u

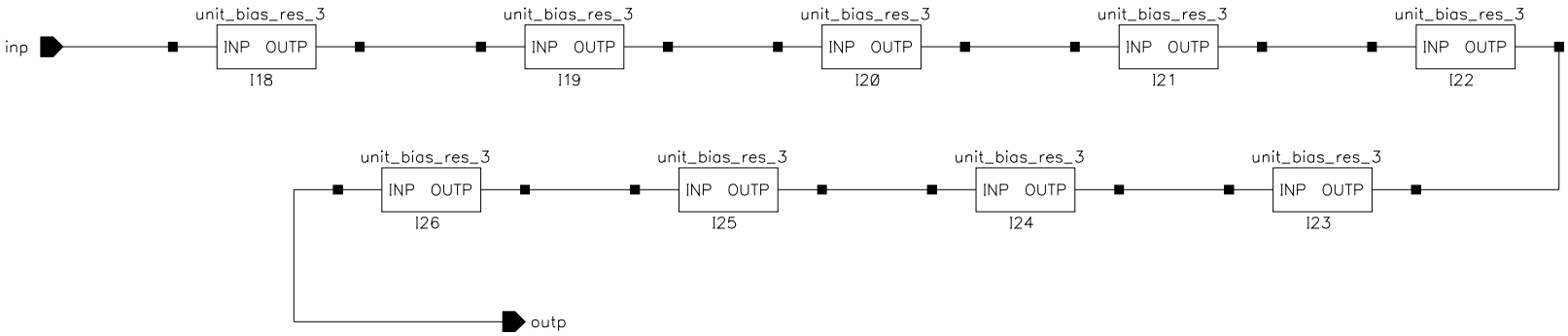


UPDATED	unit_bias_res			
Jul 5 11:28:43 2011				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

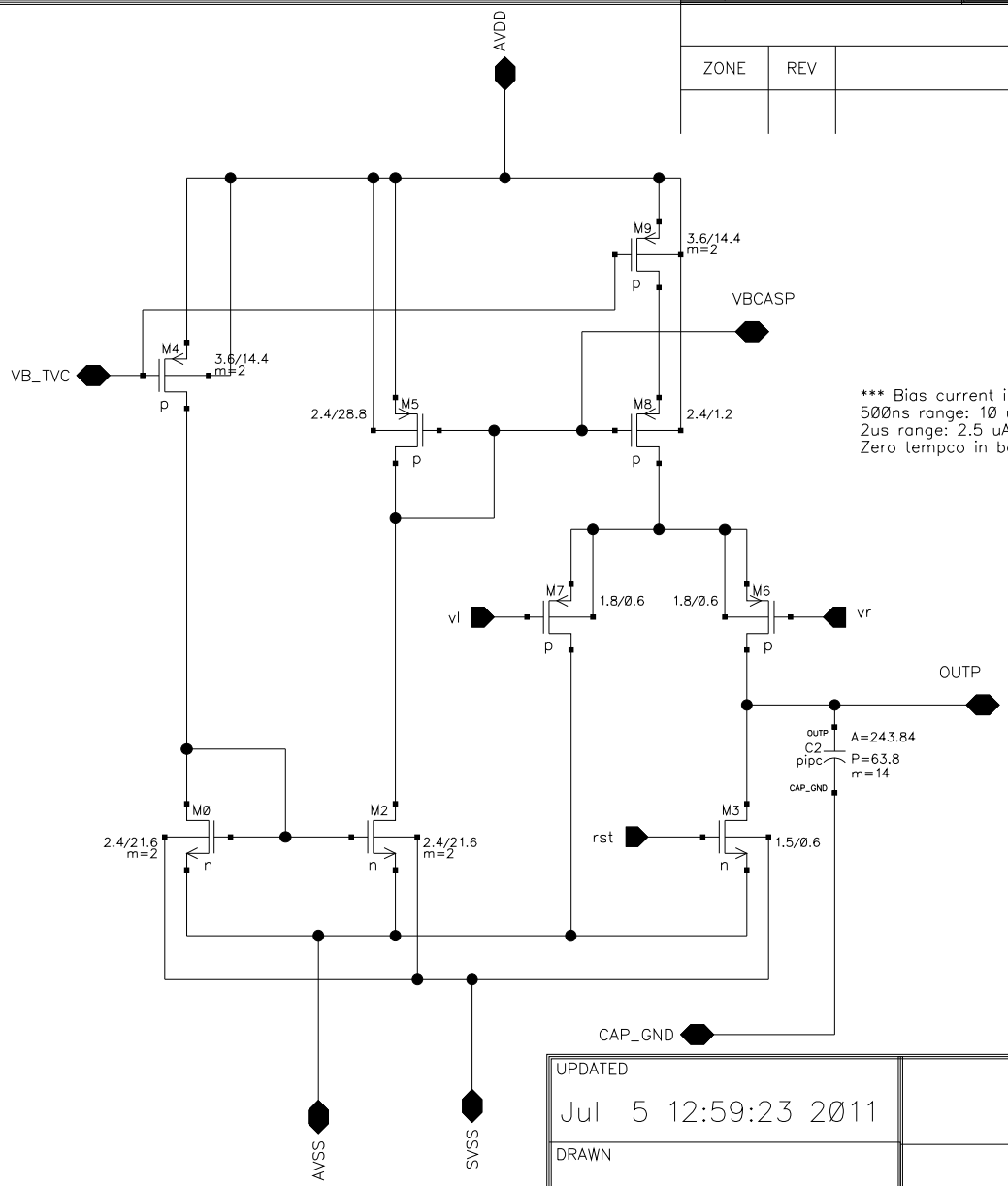


UPDATED Jul 5 11:36:07 2011	hy_res9x0_59k		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



*** Bias current in M4 and M9 ****
500ns range: 10 uA
2us range: 2.5 uA
Zero tempco in both cases.

Full-scale in either mode is about a 2 Volt change.

The capacitor is about 3.1 pF.

UPDATED	Jul 5 12:59:23 2011
DRAWN	
CHECKED	
CHECKED	
ISSUED	

SIUE

TVC core

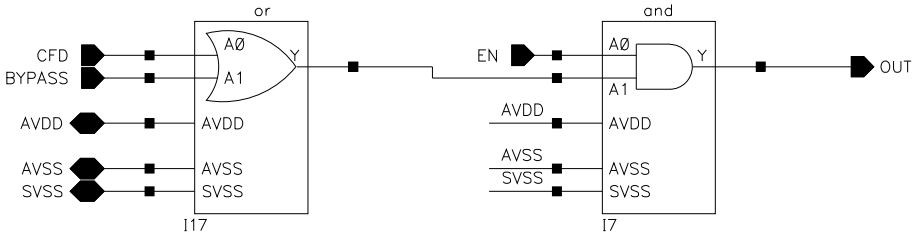
SIZE	CAGE NO.	DWG NO.	REV
A			

SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH	REV
		1	A

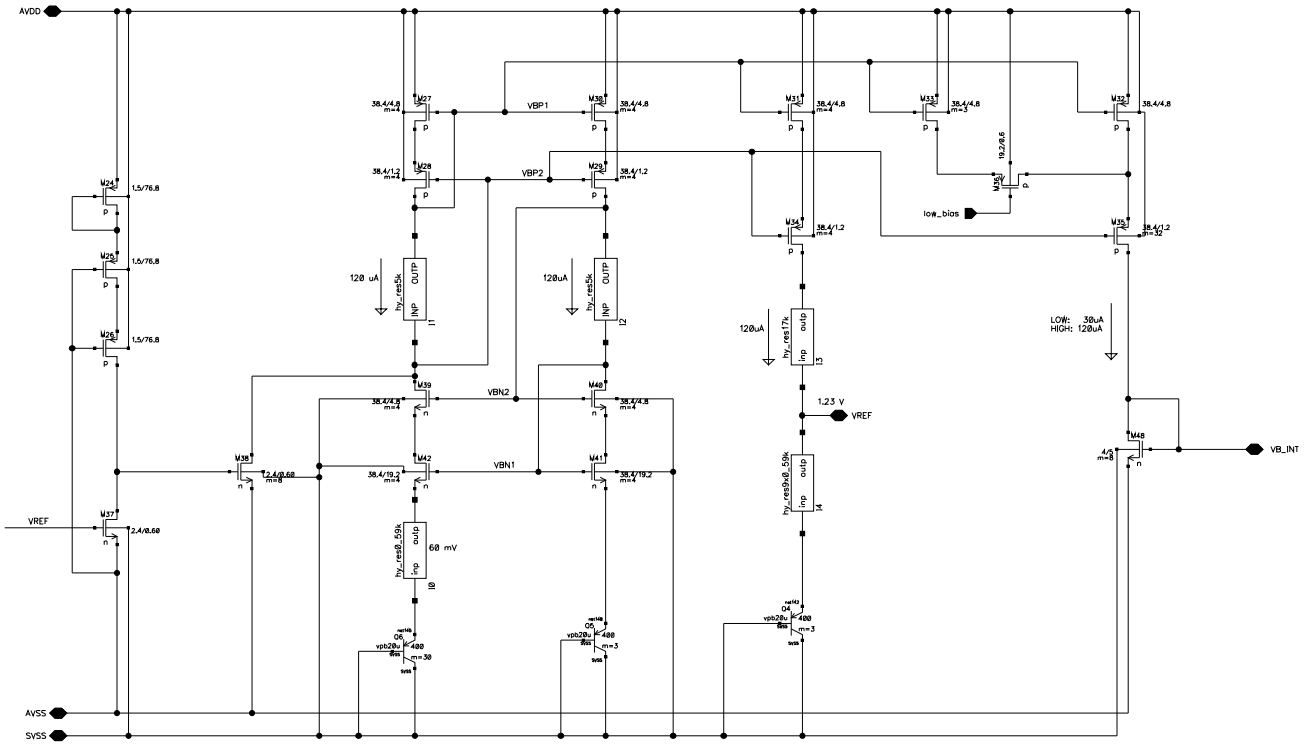
REVISIONS

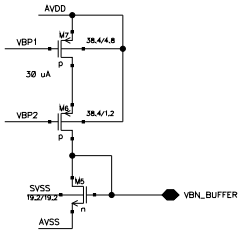
ZONE	REV	DESCRIPTION	DATE	APPROVED

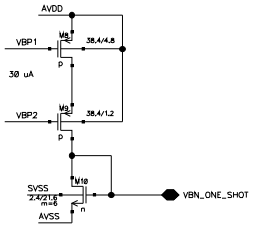


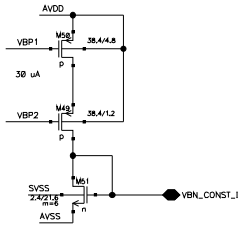
UPDATED: Jun 22 14:20:12 2010	SIUE IC Design Lab			
DRAWN	Triggering Logic			
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV A
ISSUED	SCALE		SHEET 1 OF 1	

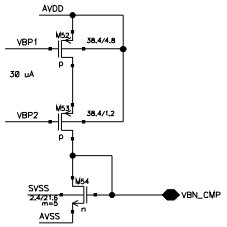
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED











UPDATED	Jul 5 13:19:57 2011
DRAWN	
CHECKED	
CHECKED	
ISSUED	

bias

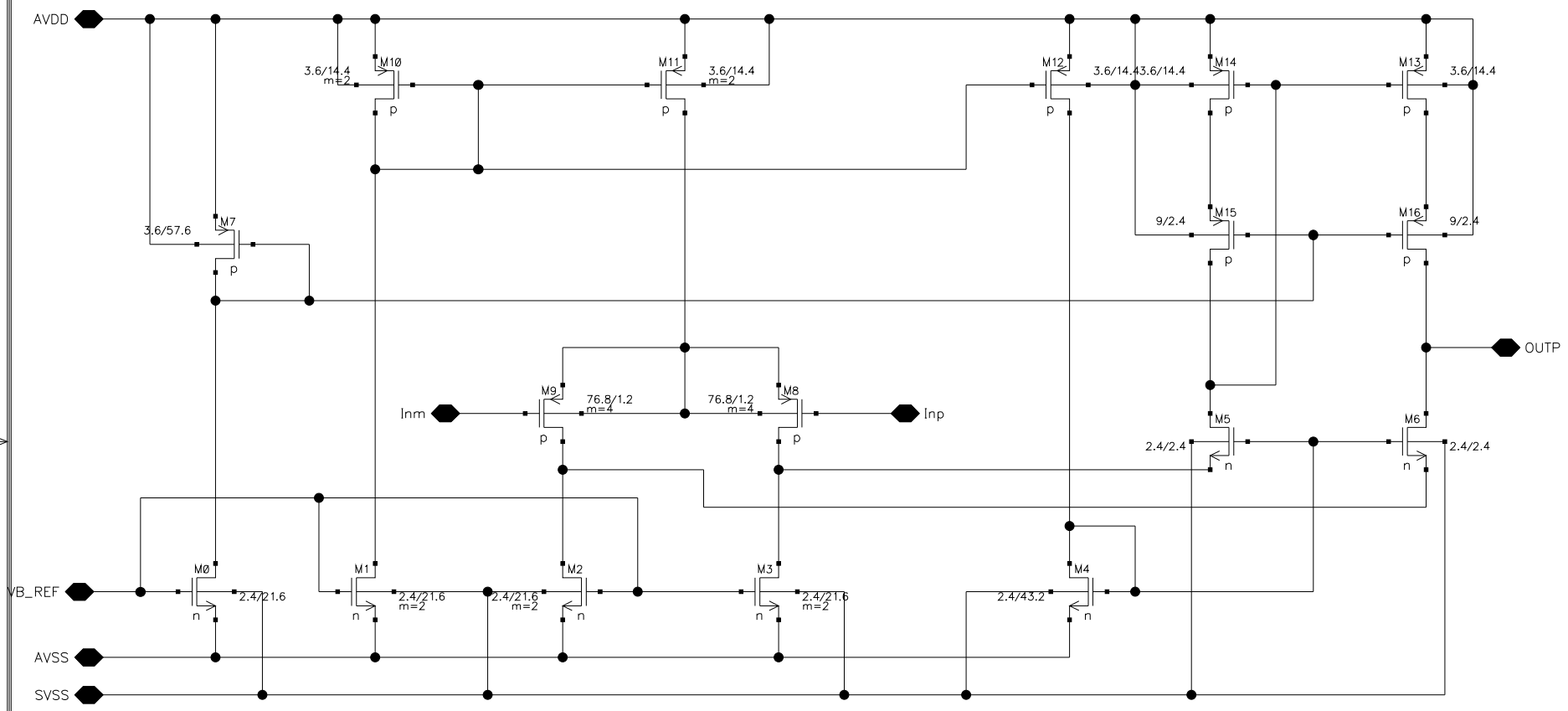
SIZE	CAGE NO.	DWG NO.	REV
C			
SCALE		SHEET	1 OF 1

REV	SH 1
DWG NO.	
CAGE NO.	

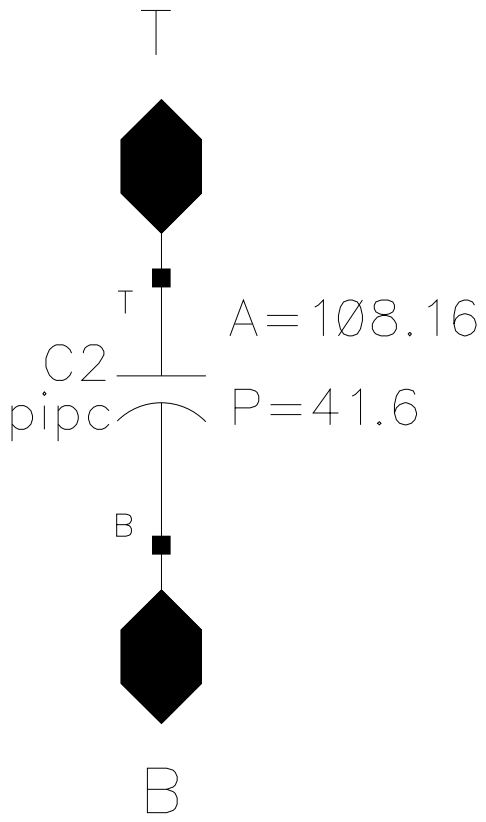
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



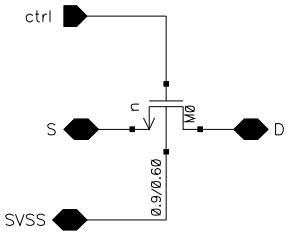
UPDATED Jul 16 13:51:14 2007	vref_buffer		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1


T
T
A=1Ø8.16
C2
pipc
P=41.6
B
B

CAGE NO.	DWG NO.	SH	REV
		1	A

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

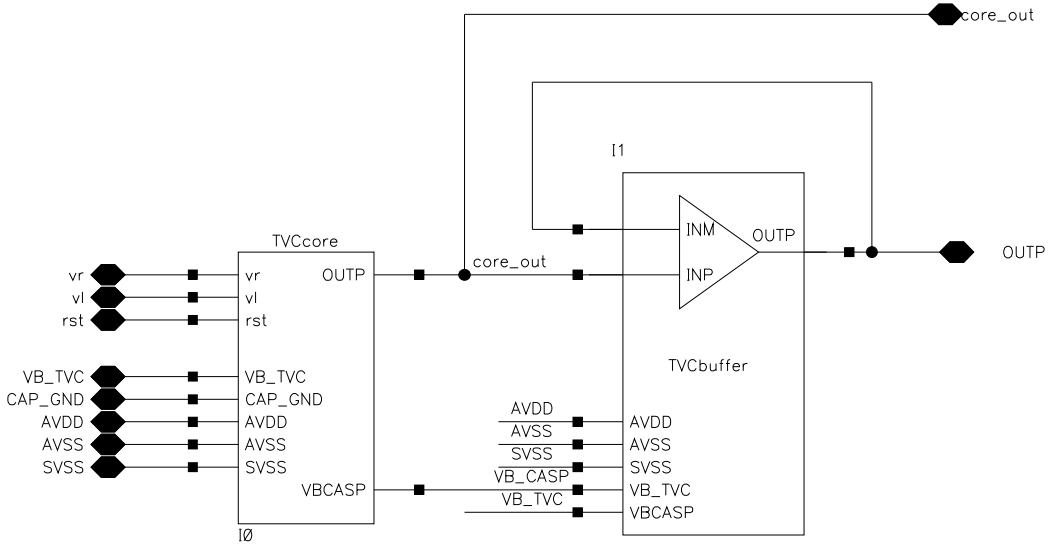


UPDATED	SIUE IC Design Lab		
Apr 1 21:23:24 2007	n-FET Switch		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV A
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH	REV
		1	

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



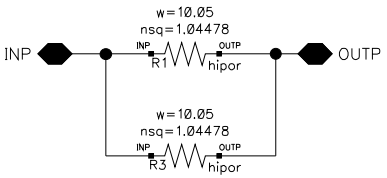
UPDATED Jun 18 14:45:51 2010	revisedTVC			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

Resistor has l=10.5u and w=10.05u m=2

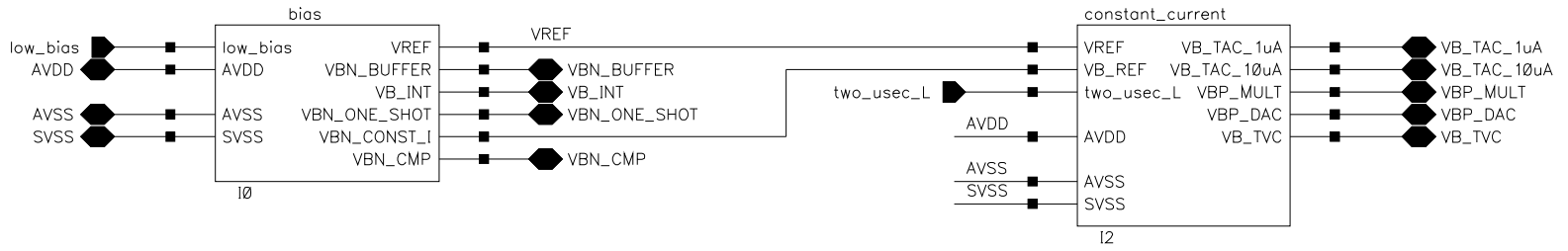


UPDATED	unit_bias_res_3			
Jul 5 11:23:47 2011				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

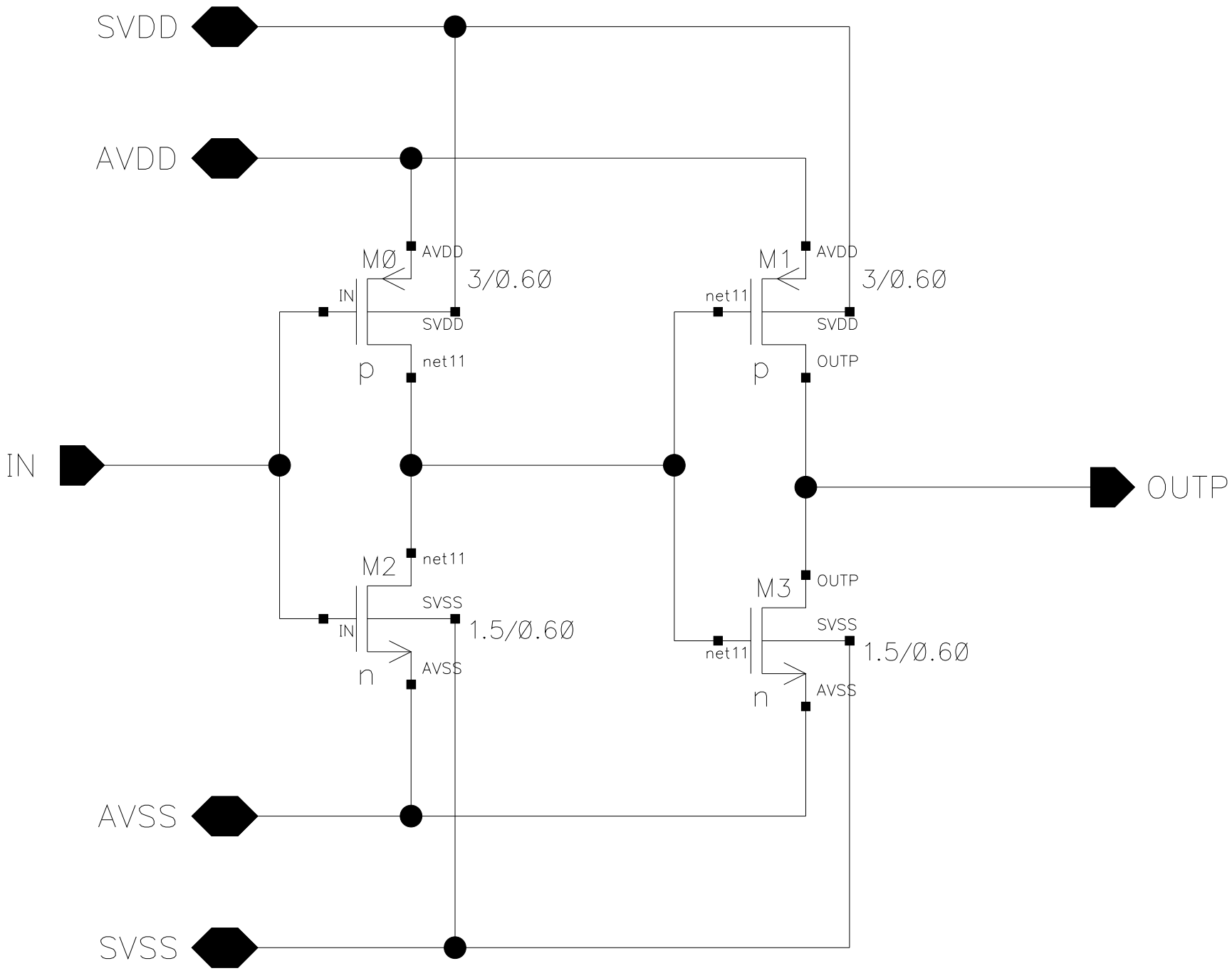
CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

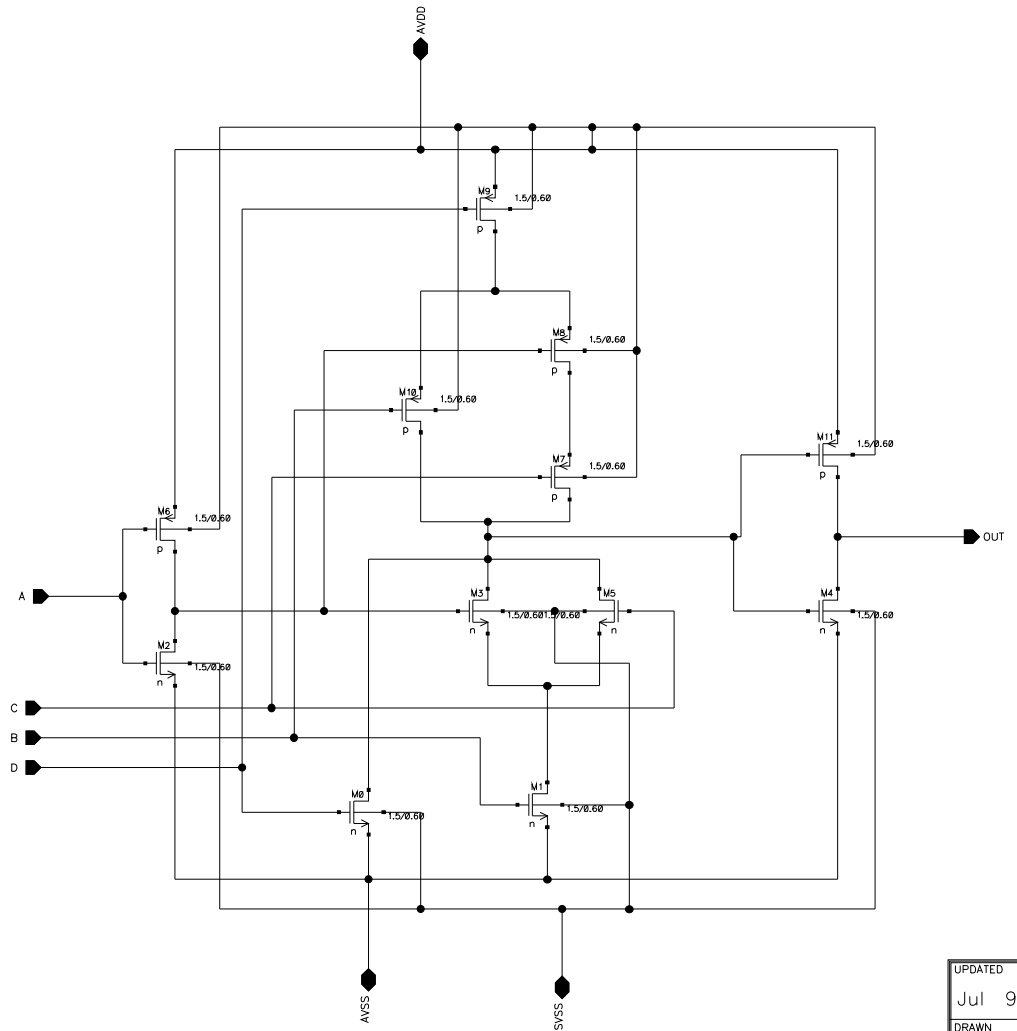


UPDATED Oct 10 14:25:37 2011	full_bias
DRAWN	
CHECKED	
CHECKED	SIZE A | CAGE NO. | DWG NO. | REV
ISSUED	SCALE | SHEET 1 OF 1


SVDD
AVDD
M0
AVDD
3/0.60
IN
SVDD
p
net11
M1
AVDD
3/0.60
net11
SVDD
p
OUTP
IN
OUTP
M2
net11
SVSS
1.5/0.60
IN
n
AVSS
M3
OUTP
SVSS
1.5/0.60
net11
n
AVSS
AVSS
SVSS

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

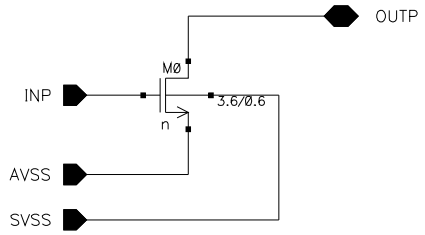


UPDATED	andor		
Jul 9 11:16:30 2007			
DRAWN			
CHECKED			
CHECKED	SIZE B	CAGE NO.	DWG NO. REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

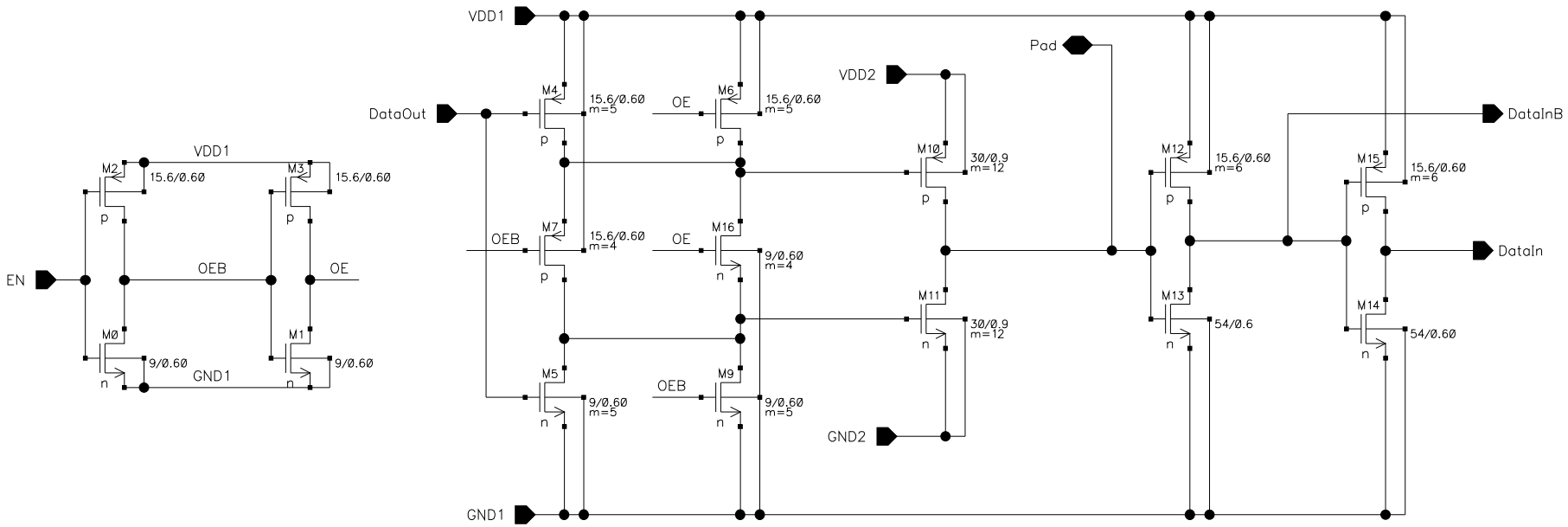


UPDATED Jul 24 14:51:53 2003	n_fet			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

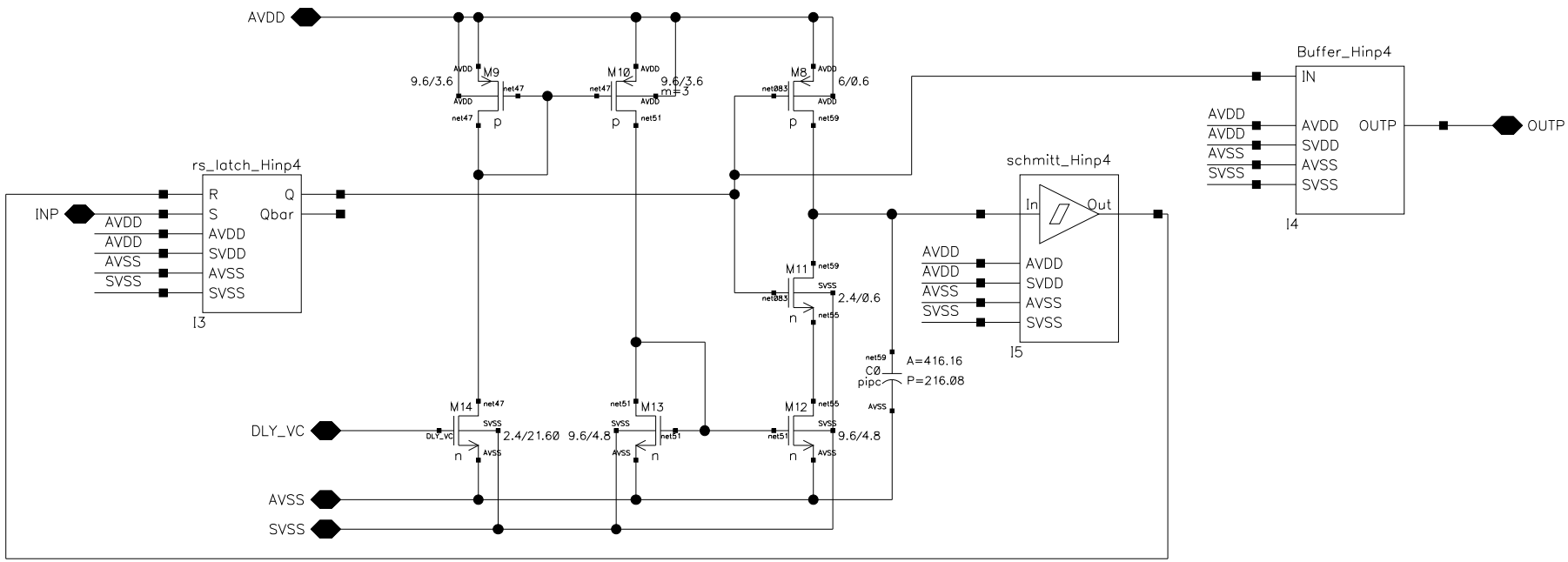


UPDATED Apr 28 16:14:02 2016	PadBidirHE		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

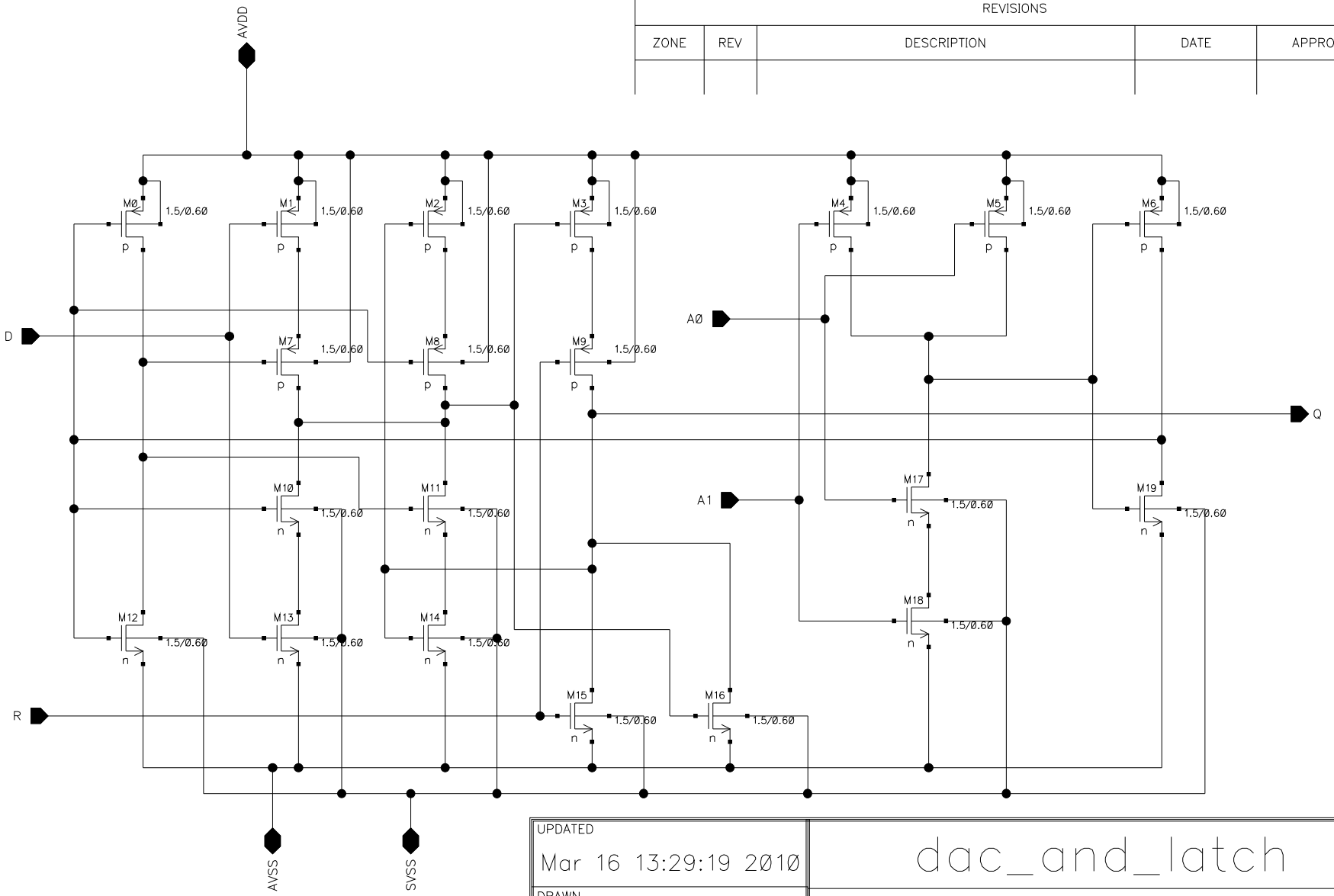


UPDATED	one_shot_vari_hitlogic		
Apr 25 14:54:35 2017			
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

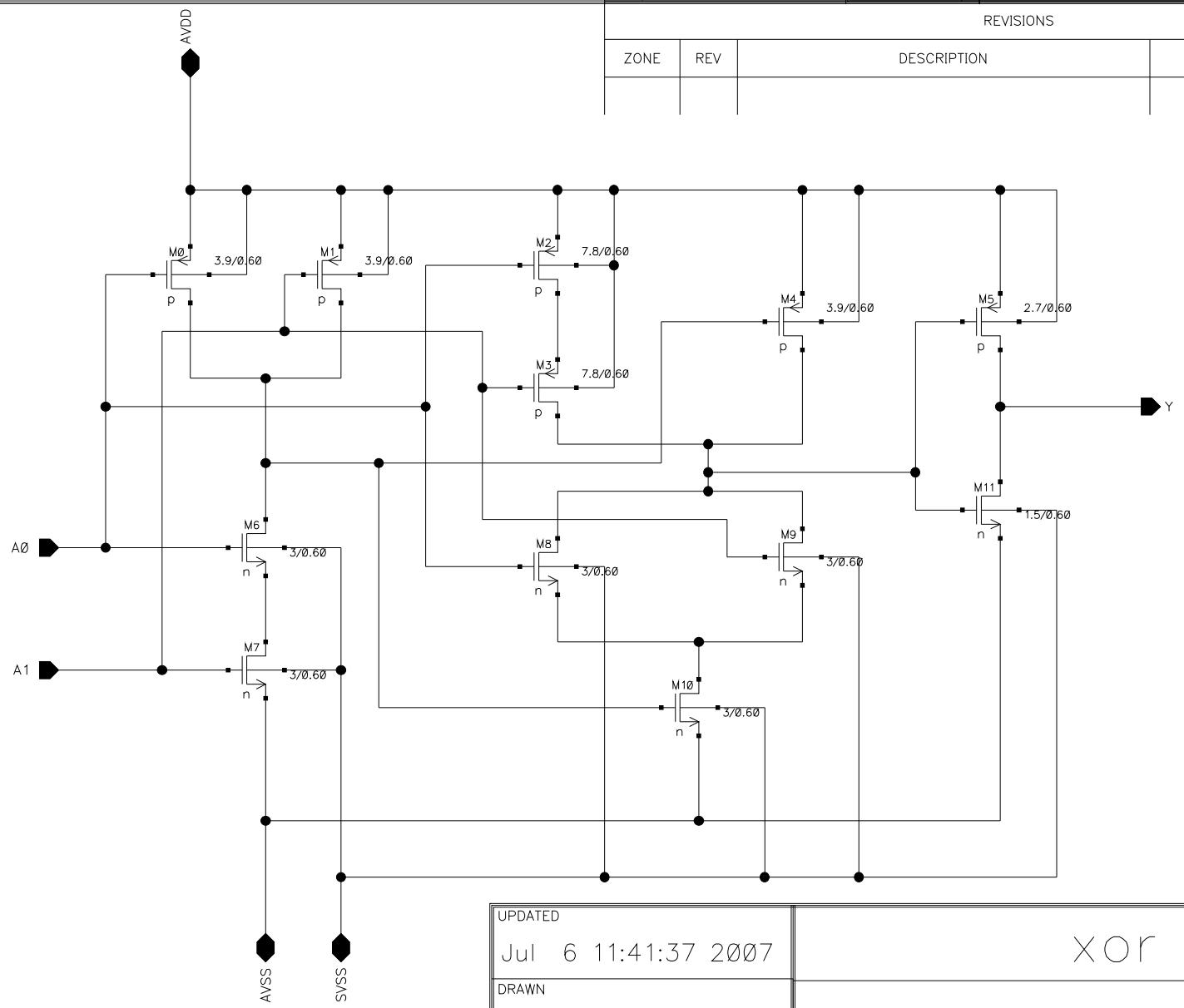


UPDATED Mar 16 13:29:19 2010	dac_and_latch		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

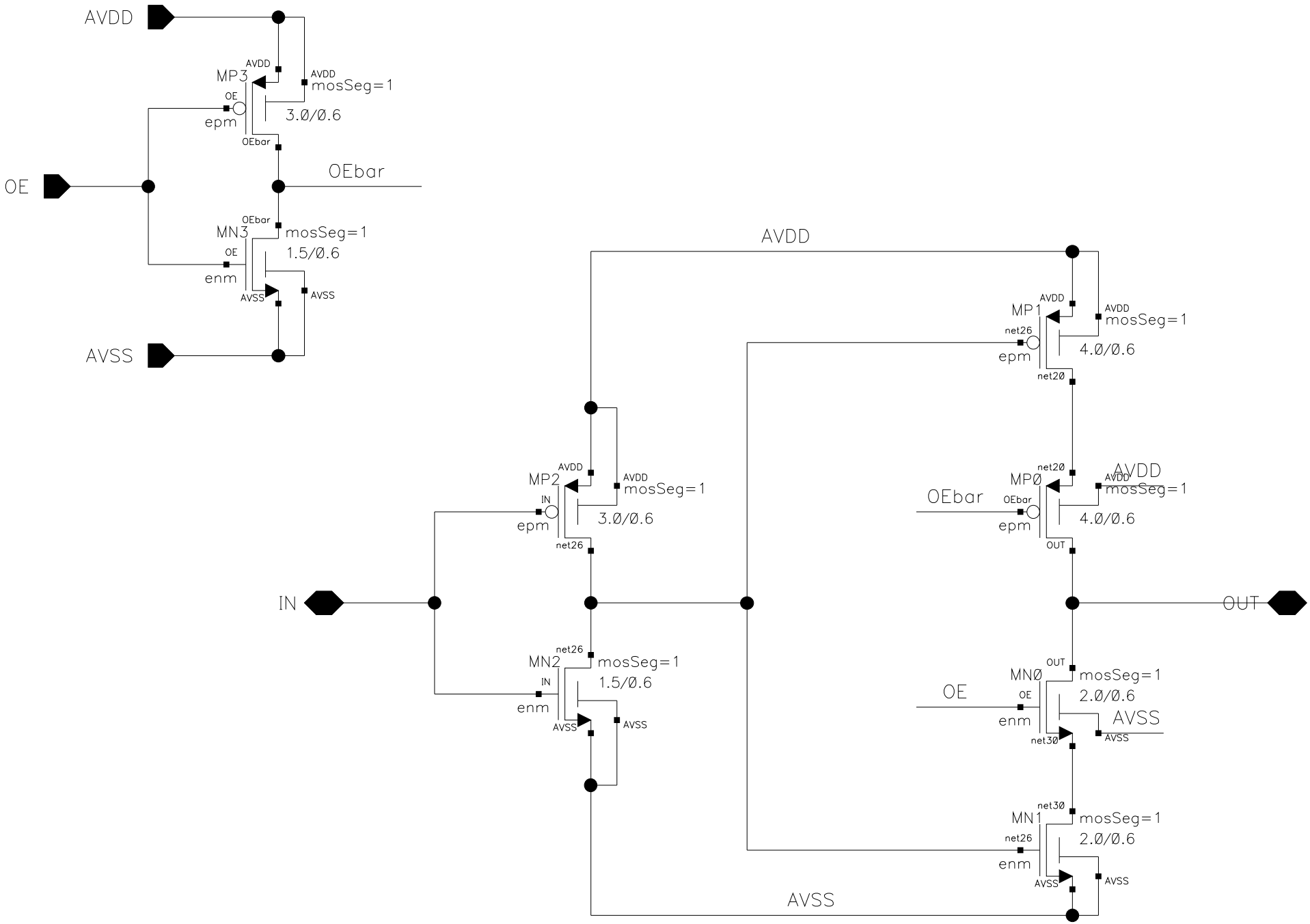
CAGE NO.	DWG NO.	SH 1	REV

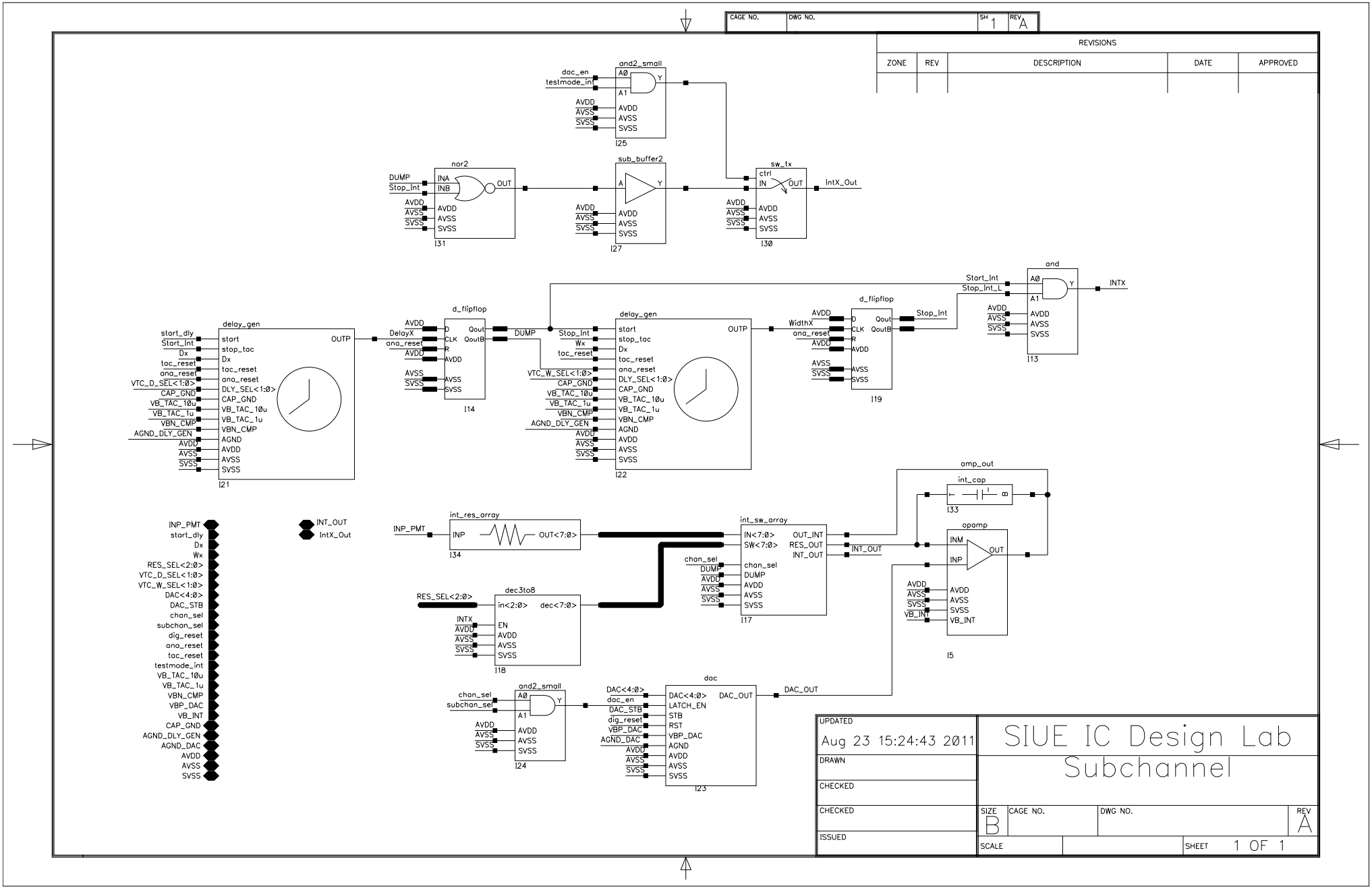
REVISIONS

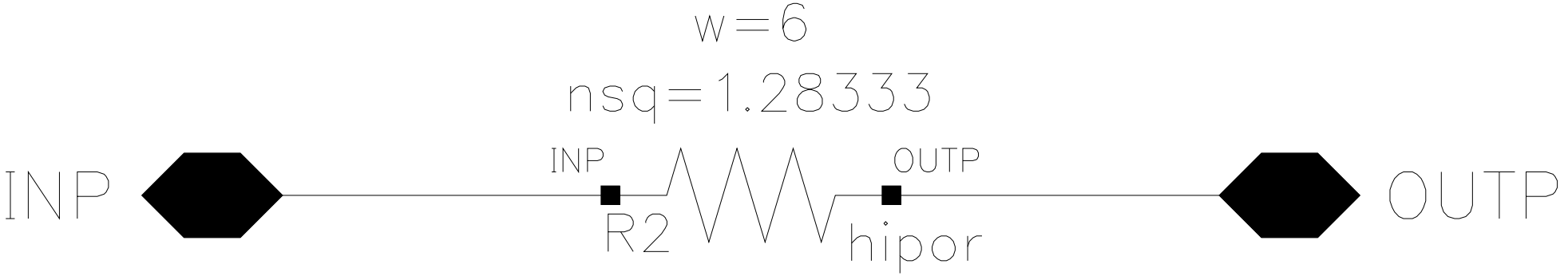
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	xor			
Jul 6 11:41:37 2007				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


AVDD
MP3
AVDD
AVDD
mosSeg=1
OE
epm
3.0/0.6
OEbar
OE
OEbar
MN3
OEbar
mosSeg=1
OE
1.5/0.6
enm
AVSS
AVSS
AVSS
AVDD
MP1
AVDD
AVDD
mosSeg=1
net26
epm
4.0/0.6
net20
MP2
AVDD
AVDD
mosSeg=1
IN
epm
3.0/0.6
net26
MP0
net20
AVDD
AVDD
mosSeg=1
OEbar
OEbar
epm
4.0/0.6
OUT
IN
OUT
MN2
net26
mosSeg=1
IN
1.5/0.6
enm
AVSS
AVSS
MN0
OUT
mosSeg=1
OE
OE
2.0/0.6
enm
AVSS
net30
AVSS
MN1
net30
mosSeg=1
net26
2.0/0.6
enm
AVSS
AVSS
AVSS

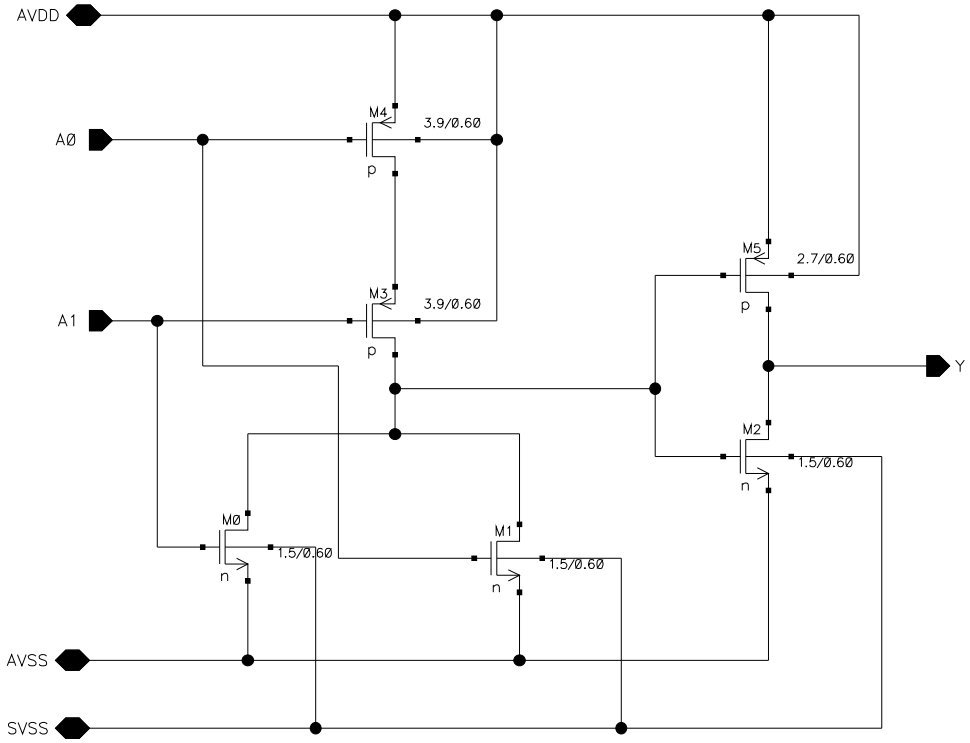

CAGE NO.
DWG NO.
SH 1
REV A
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
and2_small
dac_en
testmode_int
I25
nor2
DUMP
Stop_Int
I31
sub_buffer2
I27
sw_tx
IntX_Out
I30
and
Start_Int
Stop_Int_L
INTX
I13
d_flipflop
I14
I19
delay_gen
start_dly
Start_Int
Dx
tac_reset
ana_reset
VTC_D_SEL<1:0>
CAP_GND
VB_TAC_10u
VB_TAC_1u
VBN_CMP
AGND_DLY_GEN
I21
I22
INP_PMT
start_dly
Dx
Wx
RES_SEL<2:0>
VTC_D_SEL<1:0>
VTC_W_SEL<1:0>
DAC<4:0>
DAC_STB
chan_sel
subchan_sel
dig_reset
ana_reset
tac_reset
testmode_int
VB_TAC_10u
VB_TAC_1u
VBN_CMP
VBP_DAC
VB_INT
CAP_GND
AGND_DLY_GEN
AGND_DAC
AVDD
AVSS
SVSS
INT_OUT
IntX_Out
int_res_array
I34
int_sw_array
I17
amp_out
int_cap
I33
opamp
I5
dec3to8
I18
and2_small
I24
dac
I23
UPDATED
Aug 23 15:24:43 2011
DRAWN
CHECKED
CHECKED
ISSUED
SIUE IC Design Lab
Subchannel
SIZE B
CAGE NO.
DWG NO.
REV A
SCALE
SHEET 1 OF 1


w=6
nsq=1.28333
INP
INP
OUTP
R2
hipor
OUTP

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

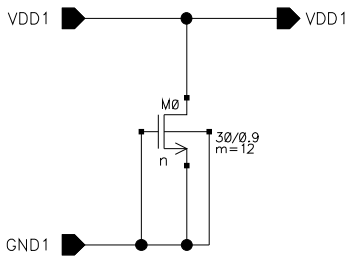


UPDATED	Or		
Jul 6 11:07:39 2007			
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

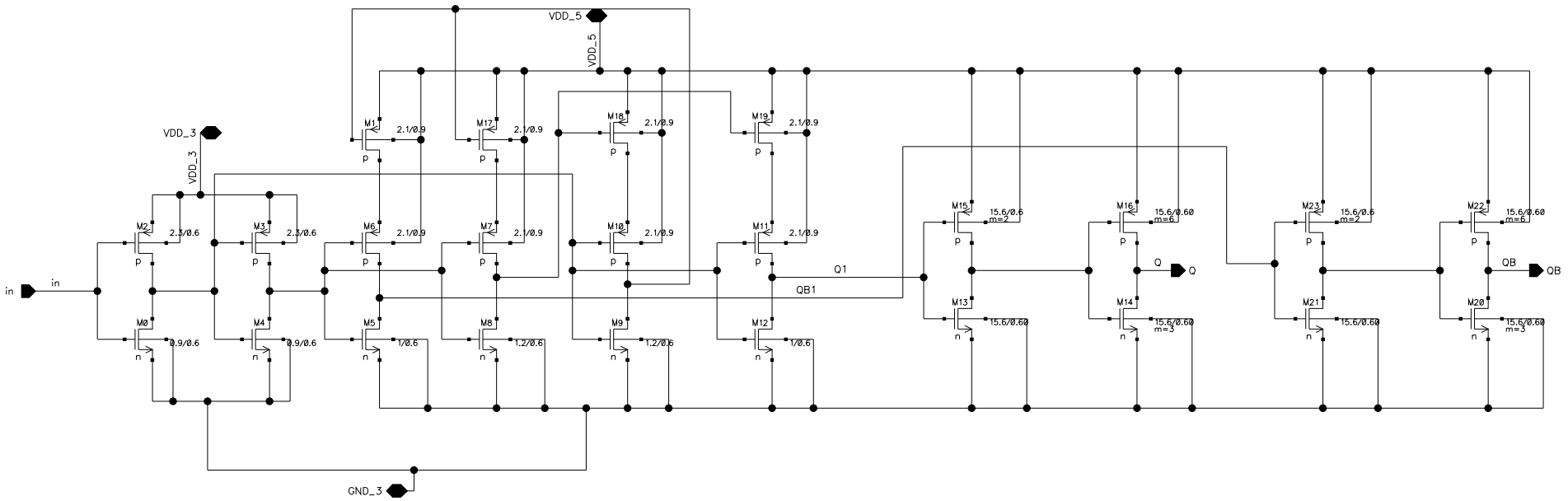
CAGE NO.	DWG NO.	SH 1	REV

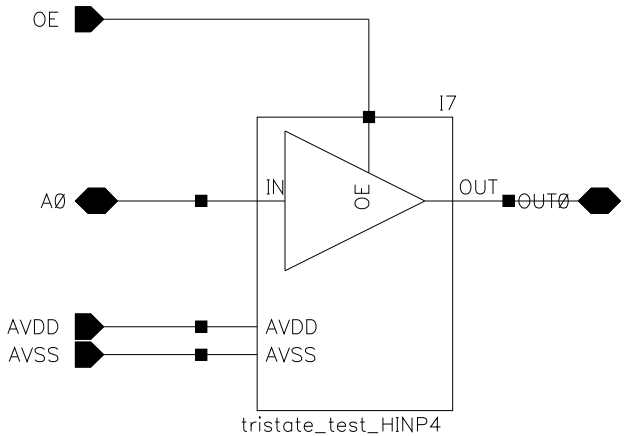
REVISIONS

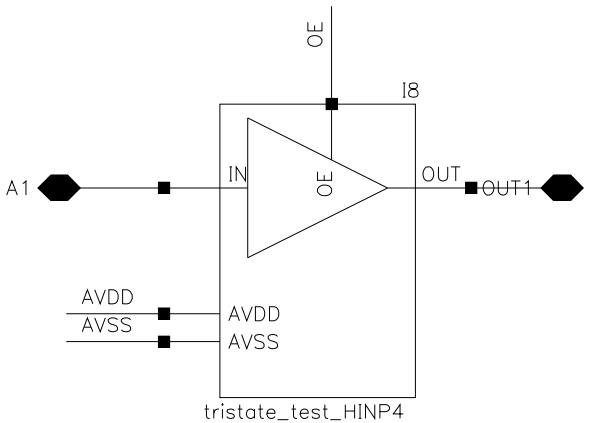
ZONE	REV	DESCRIPTION	DATE	APPROVED

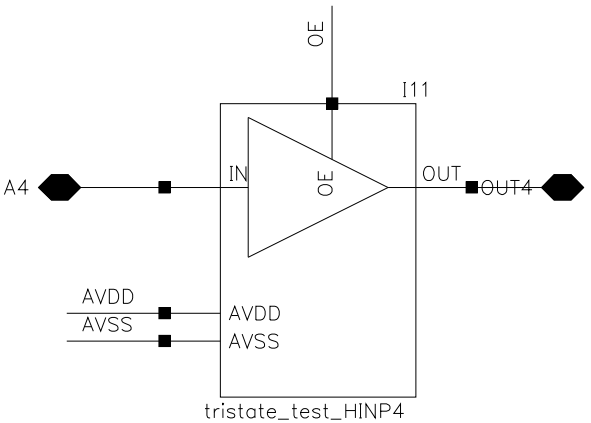


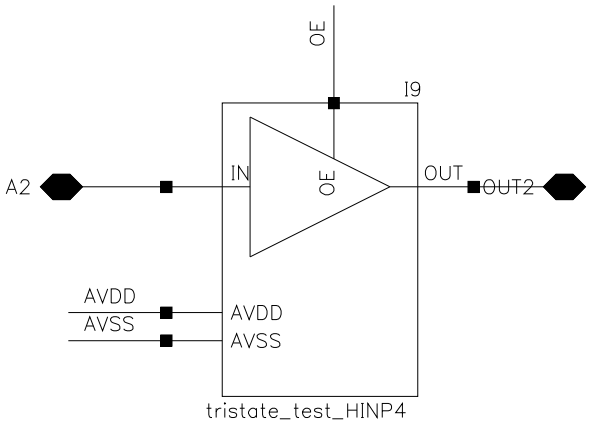
UPDATED Nov 11 15:36:54 2004	PadVdd			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

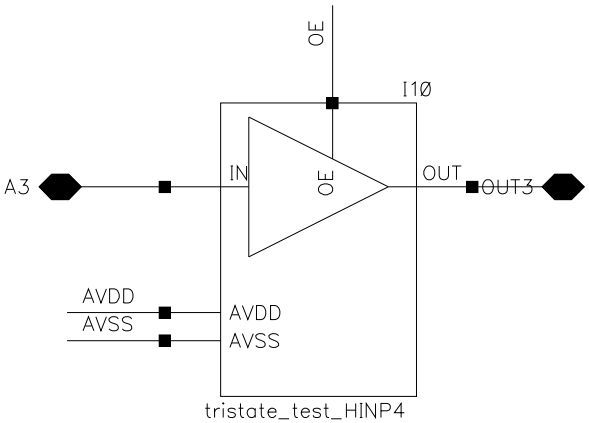

VDD_5
VDD_3
GND_3
in
M0
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M23
2.1/0.9
2.1/0.6
0.9/0.6
1/0.6
1.2/0.6
15.6/0.6
15.6/0.60
m=2
m=6
m=3
Q1
QB1
Q
QB


OE
I7
AØ
IN
OE
OUT
OUTØ
AVDD
AVSS
AVDD
AVSS
tristate_test_HINP4


OE
I8
A1
IN
OE
OUT
OUT1
AVDD
AVSS
AVDD
AVSS
tristate_test_HINP4


OE
I11
A4
IN
OE
OUT
OUT4
AVDD
AVSS
AVDD
AVSS
tristate_test_HINP4

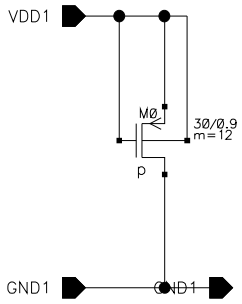

OE
I9
A2
IN
OE
OUT
OUT2
AVDD
AVSS
AVDD
AVSS
tristate_test_HINP4


OE
I1Ø
A3
IN
OE
OUT
OUT3
AVDD
AVSS
AVDD
AVSS
tristate_test_HINP4

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

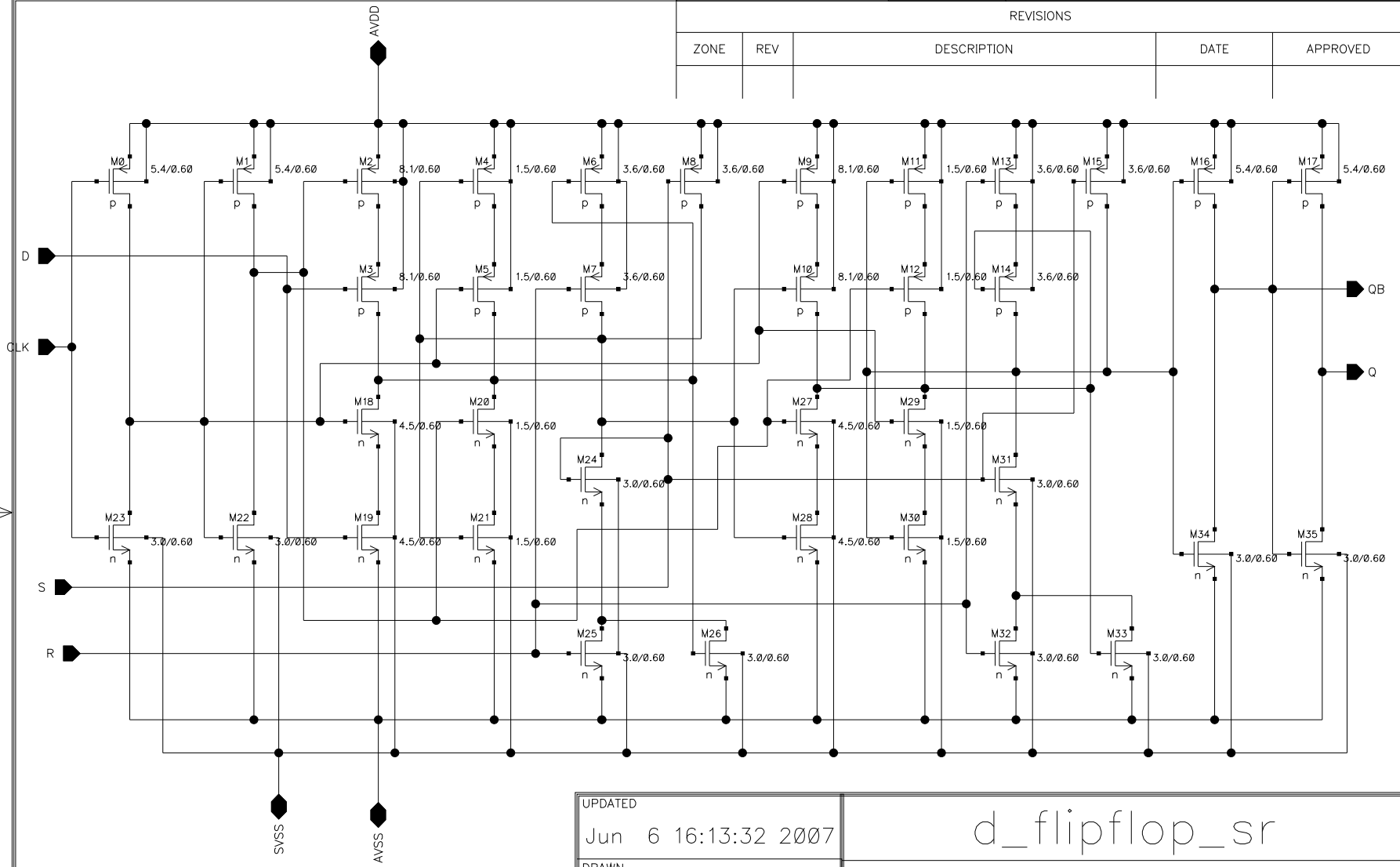


UPDATED Nov 11 15:38:19 2ØØ4	PadGnd			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

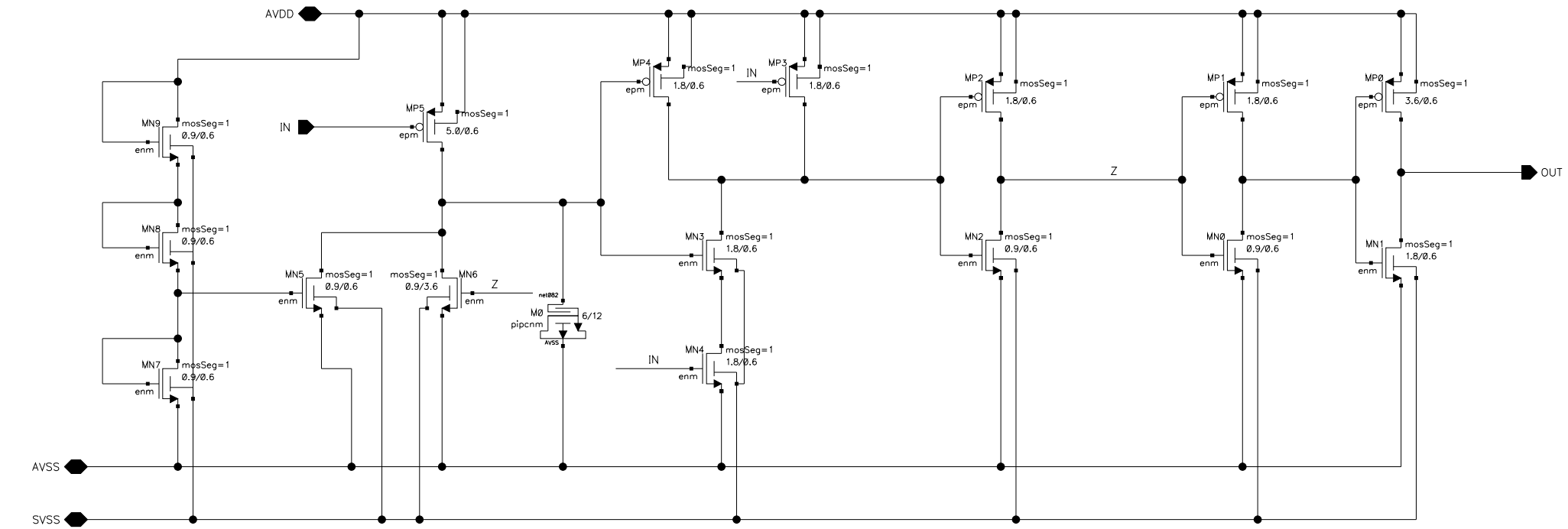


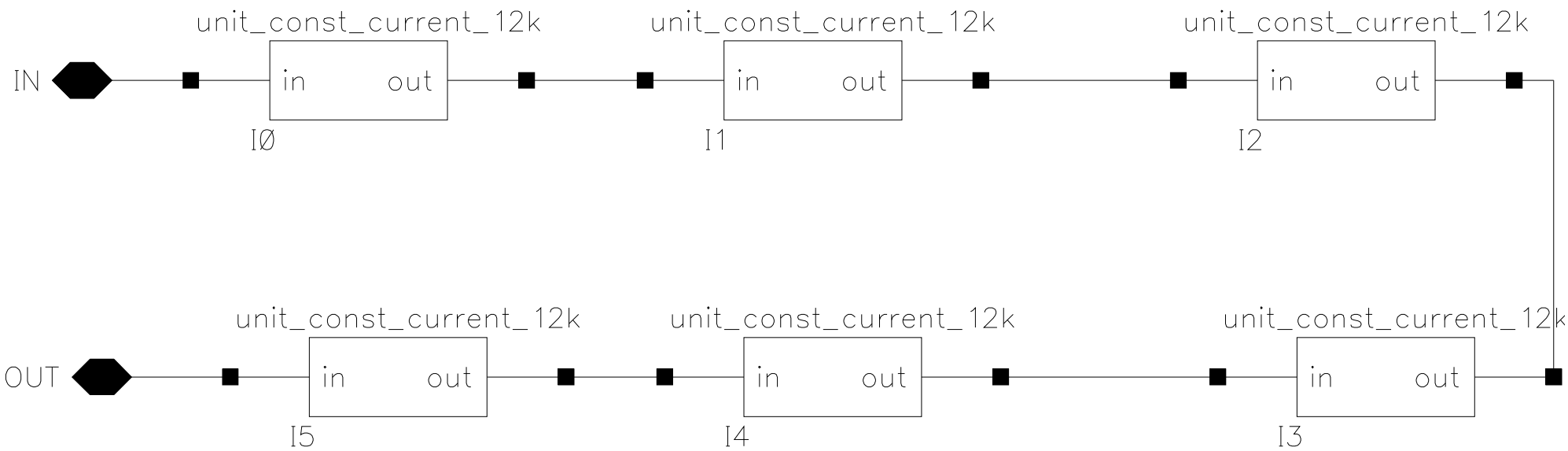
UPDATED	Jun 6 16:13:32 2007
DRAWN	
CHECKED	
CHECKED	
ISSUED	

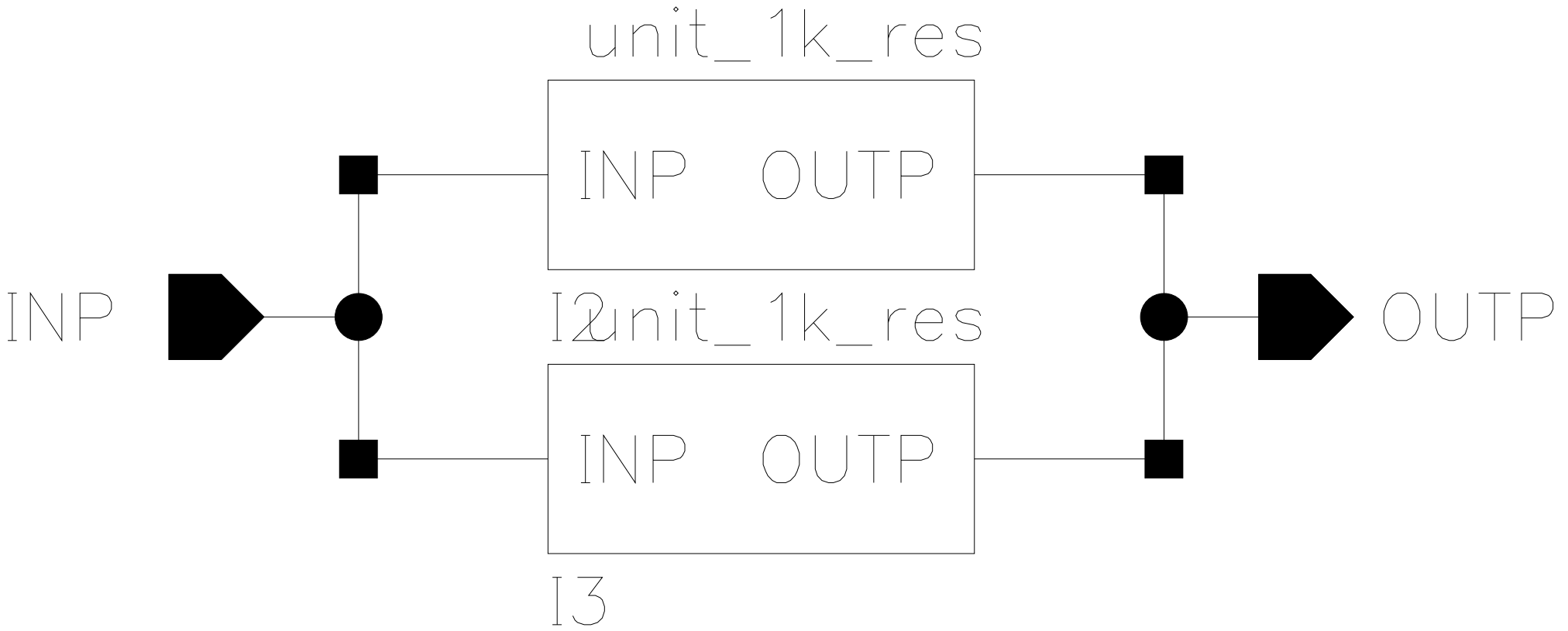
d_flipflop_sr

SIZE	CAGE NO.	DWG NO.	REV
A			

SCALE		SHEET 1 OF 1


AVDD
IN
MP5
mosSeg=1
5.0/0.6
epm
MP4
1.8/0.6
MP3
MP2
MP1
MP0
3.6/0.6
MN9
0.9/0.6
MN8
MN7
MN5
MN6
0.9/3.6
MN3
1.8/0.6
MN4
MN2
MN0
MN1
enm
Z
M0
pipcnm
6/12
net082
AVSS
SVSS
OUT

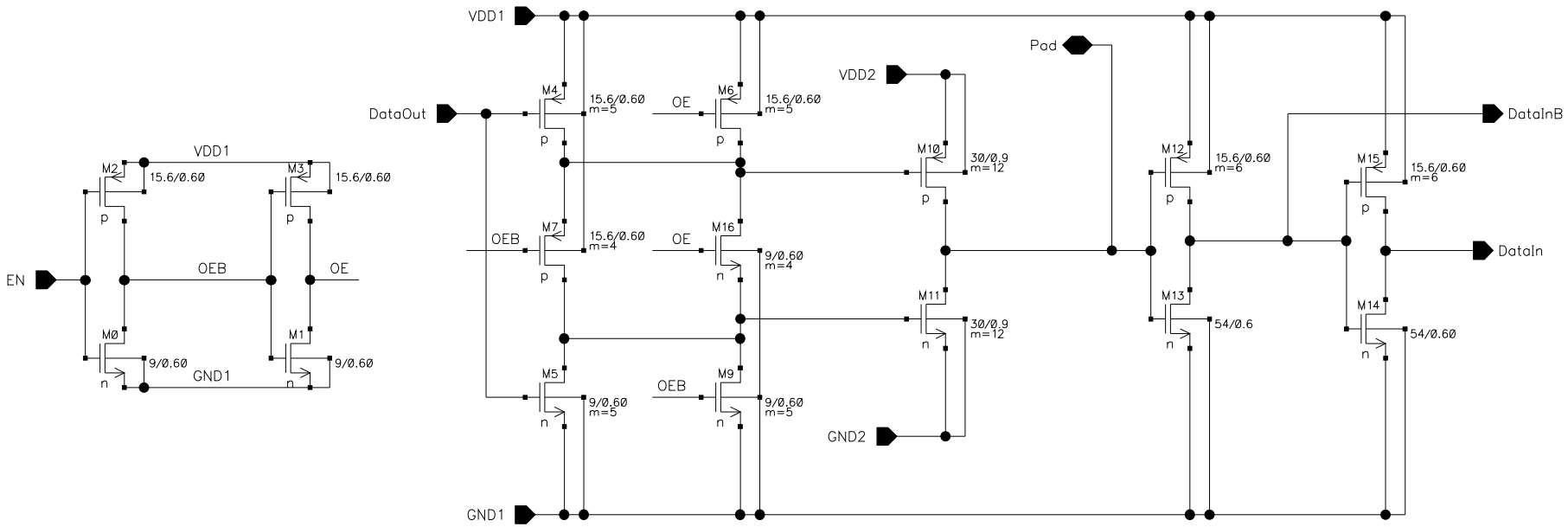

unit_const_current_12k
unit_const_current_12k
unit_const_current_12k
IN
in
out
in
out
in
out
I0
I1
I2
unit_const_current_12k
unit_const_current_12k
unit_const_current_12k
OUT
in
out
in
out
in
out
I5
I4
I3


unit_1k_res
INP OUTP
I2
unit_1k_res
INP OUTP
I3
INP
OUTP

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



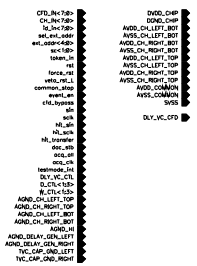
UPDATED Apr 28 16:14:02 2016	PadBidirHE		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH	REV
		1	A

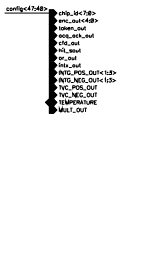
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

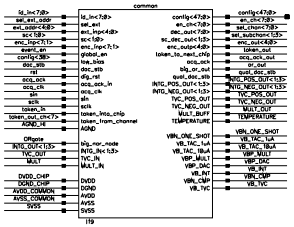
Inputs



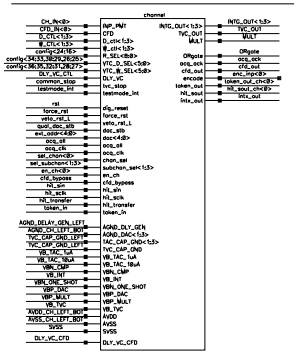
Outputs



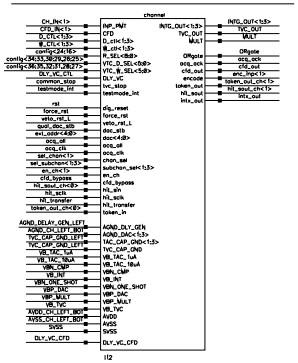
Common



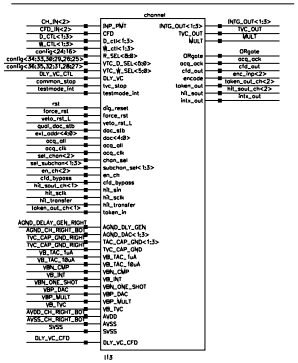
Channel Ø



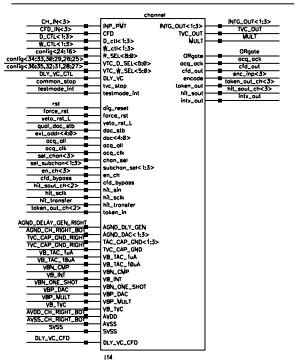
Channel 1



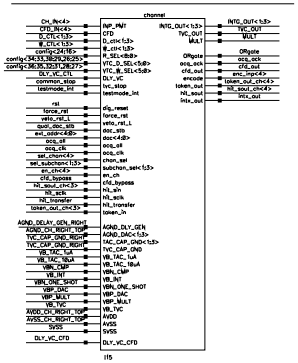
Channel 2



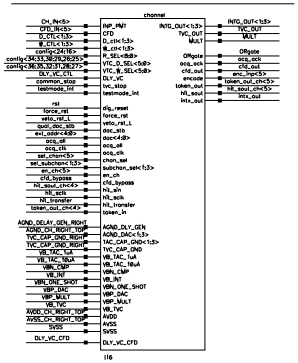
Channel 3



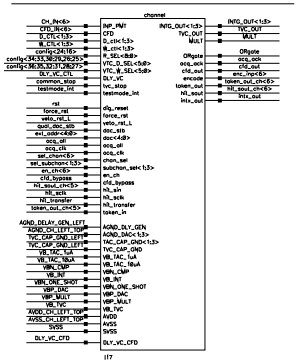
Channel 4



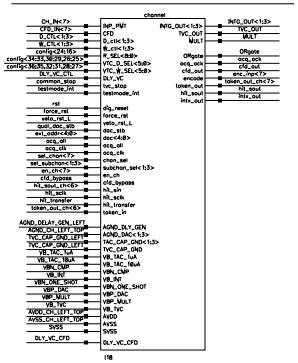
Channel 5



Channel 6



Channel 7

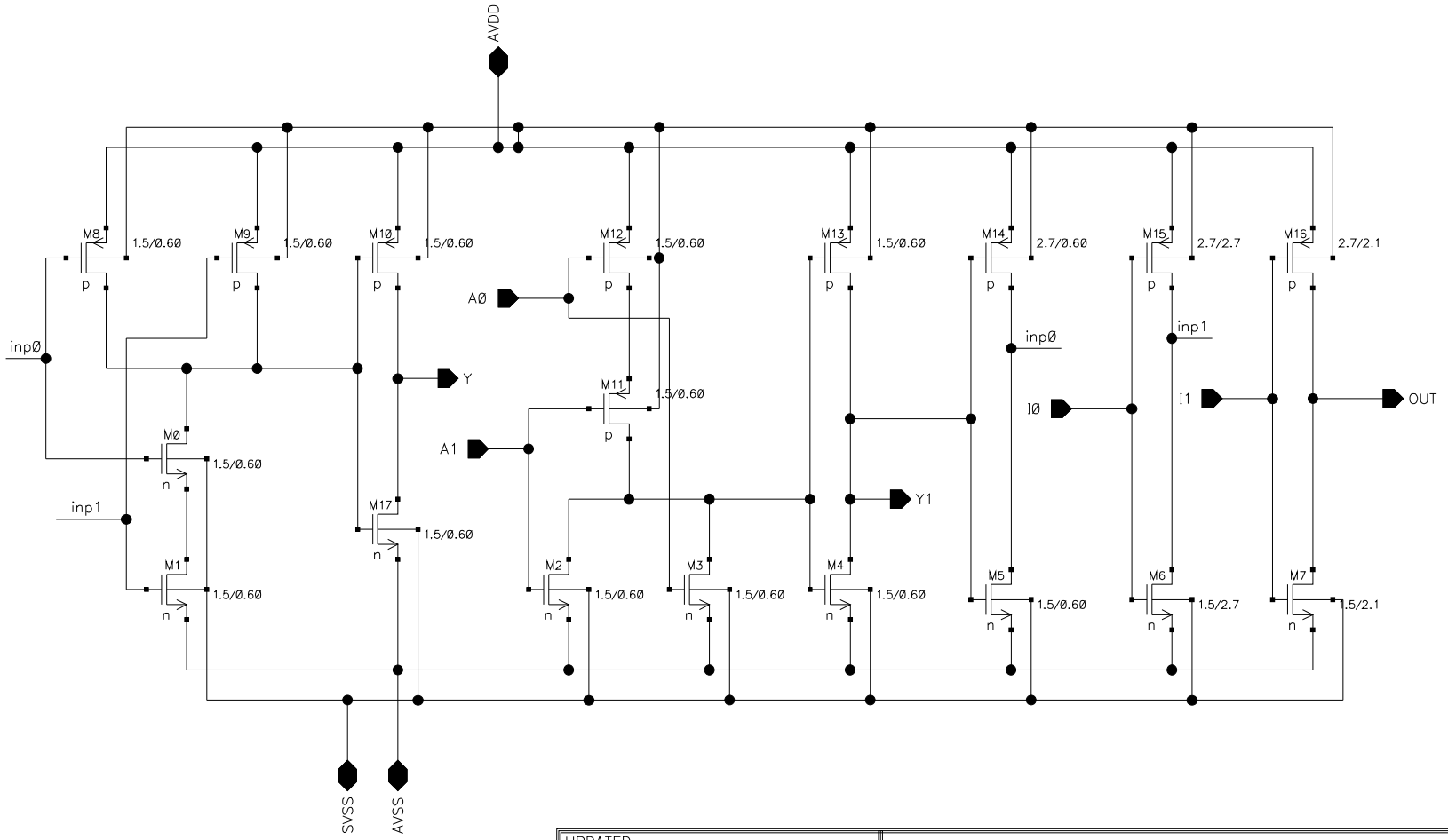


UPDATED	SIUE IC Design Lab
May 3 14:54:23 2017	
DRAWN	Eight Channel
CHECKED	
CHECKED	
CHECKED	SIZE D / CAGE NO. / DWG NO. / REV A
ISSUED	SCALE / SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

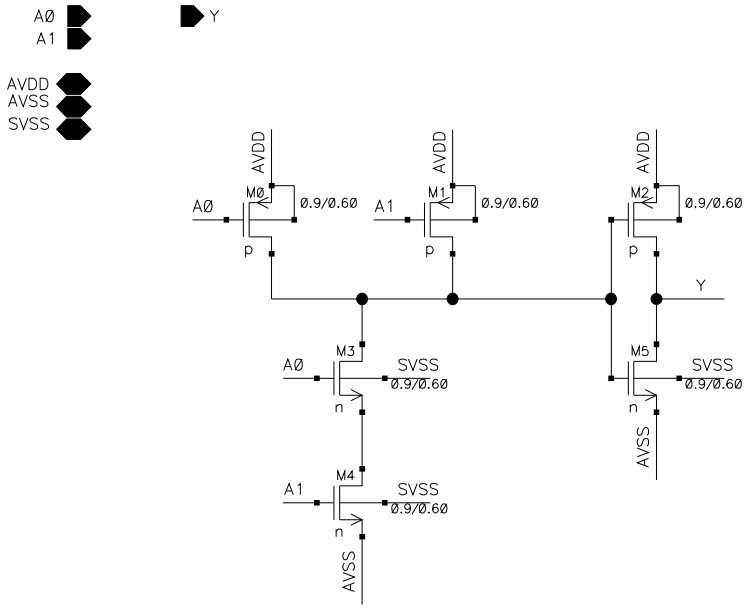


UPDATED Jul 9 10:40:23 2007				
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Aug 8 14:14:18 2007	and			
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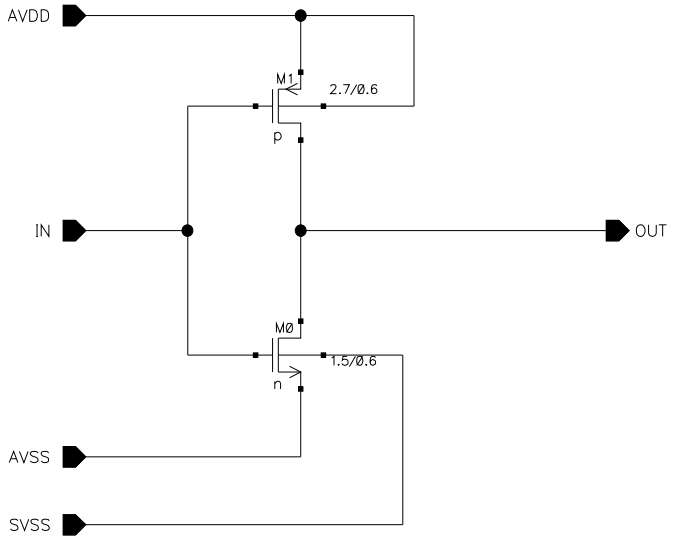
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jul 5 15:27:12 2007	inv_wid1			
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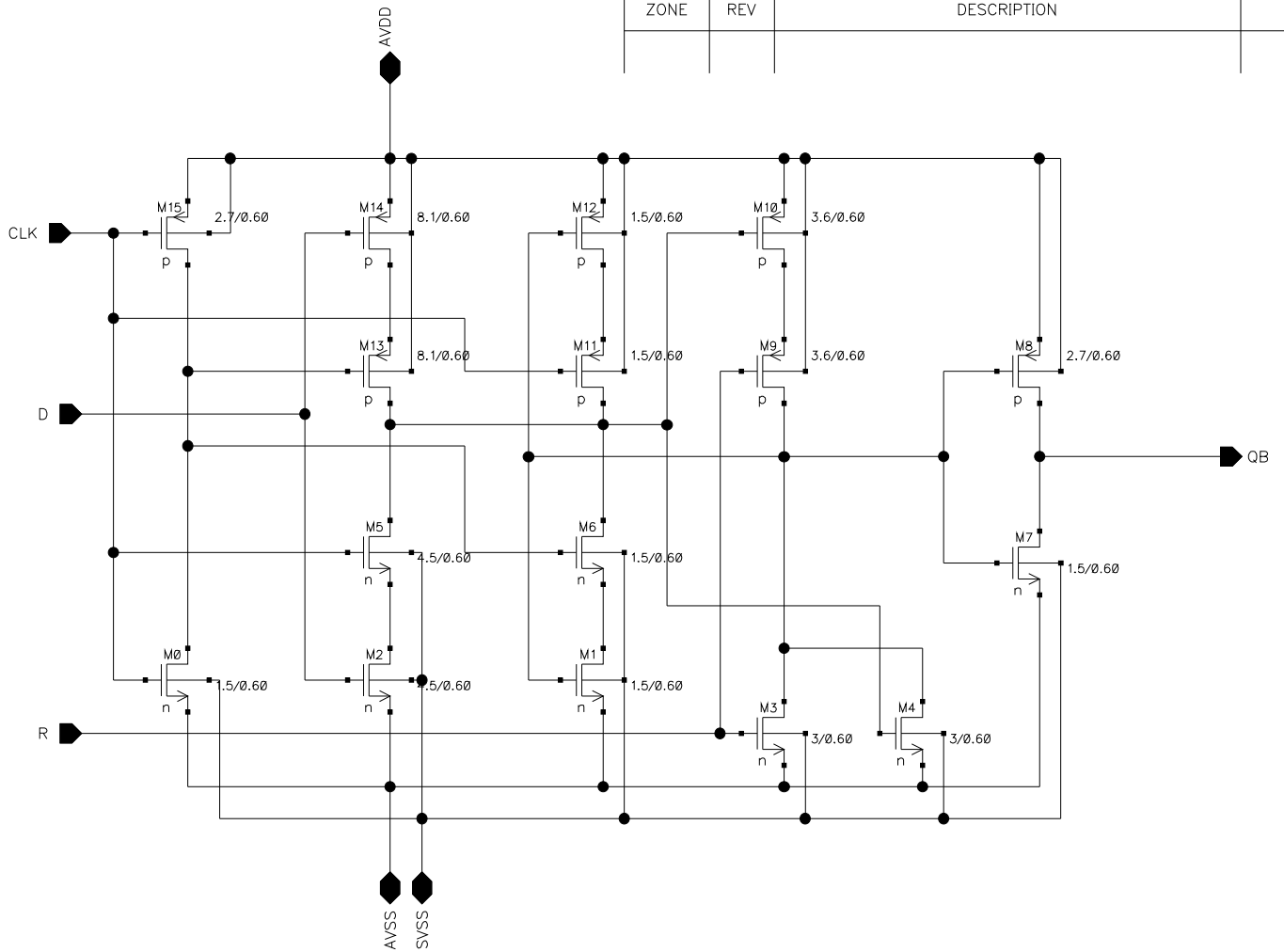
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

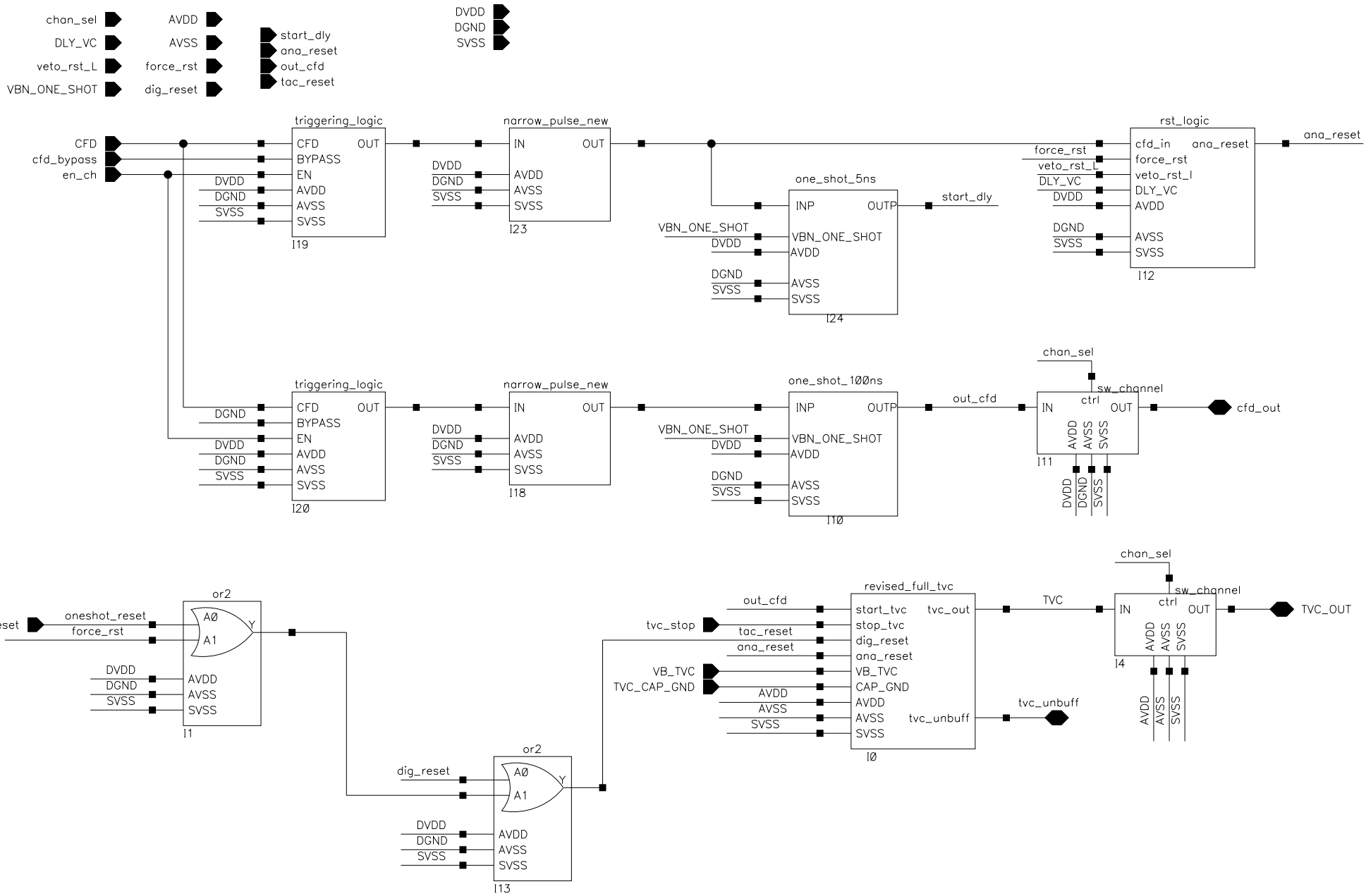
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED: Jul 9 10:44:29 2007	latch
DRAWN	
CHECKED	
CHECKED	
ISSUED	

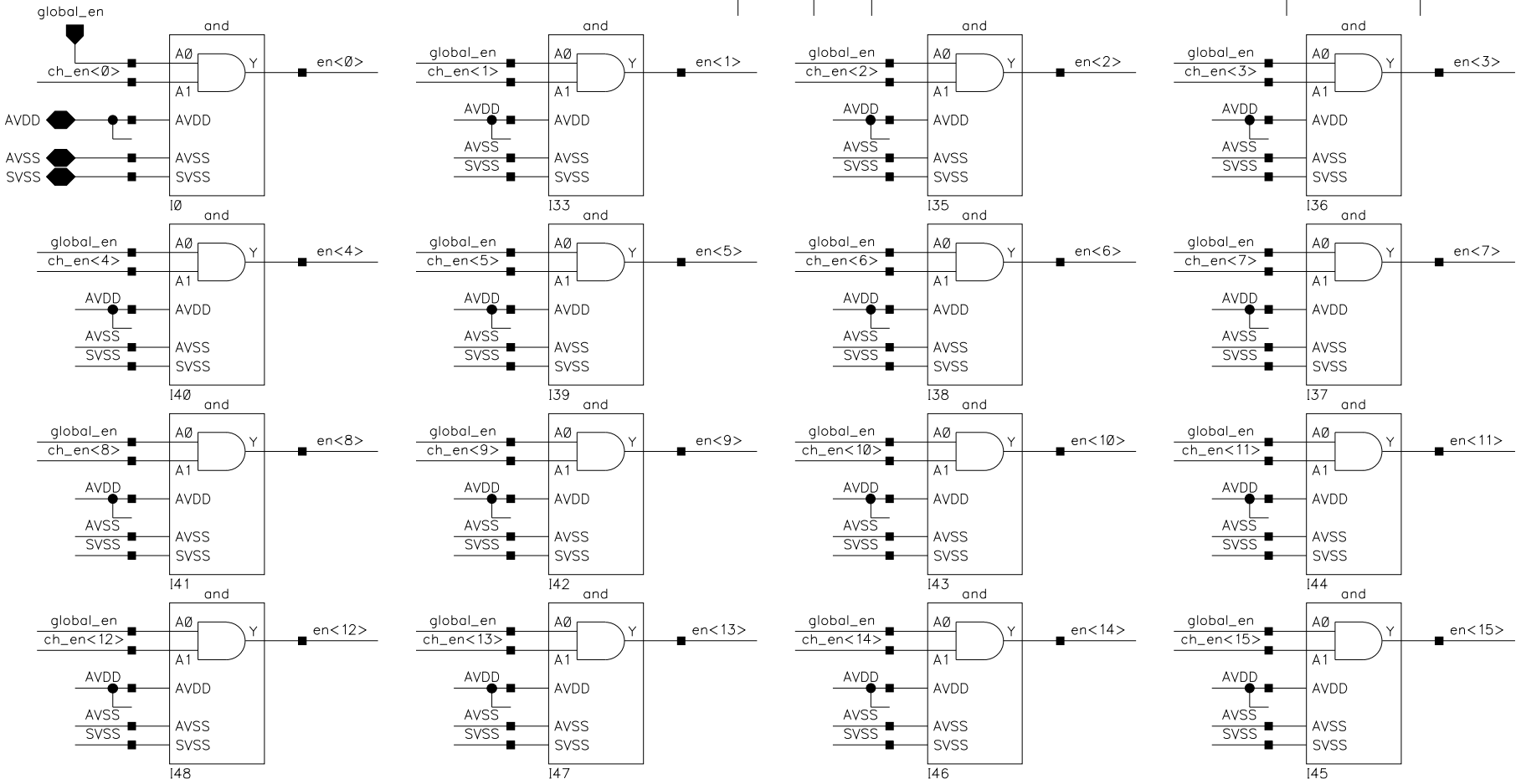
SIZE	CAGE NO.	DWG NO.	REV
A			
SCALE		SHEET 1 OF 1	


chan_sel
DLY_VC
veto_rst_L
VBN_ONE_SHOT
AVDD
AVSS
force_rst
dig_reset
start_dly
ana_reset
out_cfd
tac_reset
DVDD
DGND
SVSS
triggering_logic
CFD
cfd_bypass
en_ch
CFD
BYPASS
EN
OUT
I19
narrow_pulse_new
IN
OUT
I23
one_shot_5ns
INP
OUTP
VBN_ONE_SHOT
start_dly
I24
rst_logic
cfd_in
ana_reset
force_rst
veto_rst_l
DLY_VC
I12
triggering_logic
I20
narrow_pulse_new
I18
one_shot_100ns
out_cfd
I10
sw_channel
ctrl
I11
cfd_out
or2
Oneshot_reset
oneshot_reset
force_rst
A0
A1
Y
I1
dig_reset
I13
revised_full_tvc
out_cfd
tvc_stop
tac_reset
ana_reset
VB_TVC
TVC_CAP_GND
start_tvc
stop_tvc
dig_reset
ana_reset
VB_TVC
CAP_GND
tvc_out
tvc_unbuff
I0
TVC
I4
TVC_OUT

CAGE NO.	DWG NO.	SH 1	REV A

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



ch_en<15:0>

en<15:0>

UPDATED	SIUE IC Design Lab		
Jun 25 13:44:49 2010	Enable Logic		
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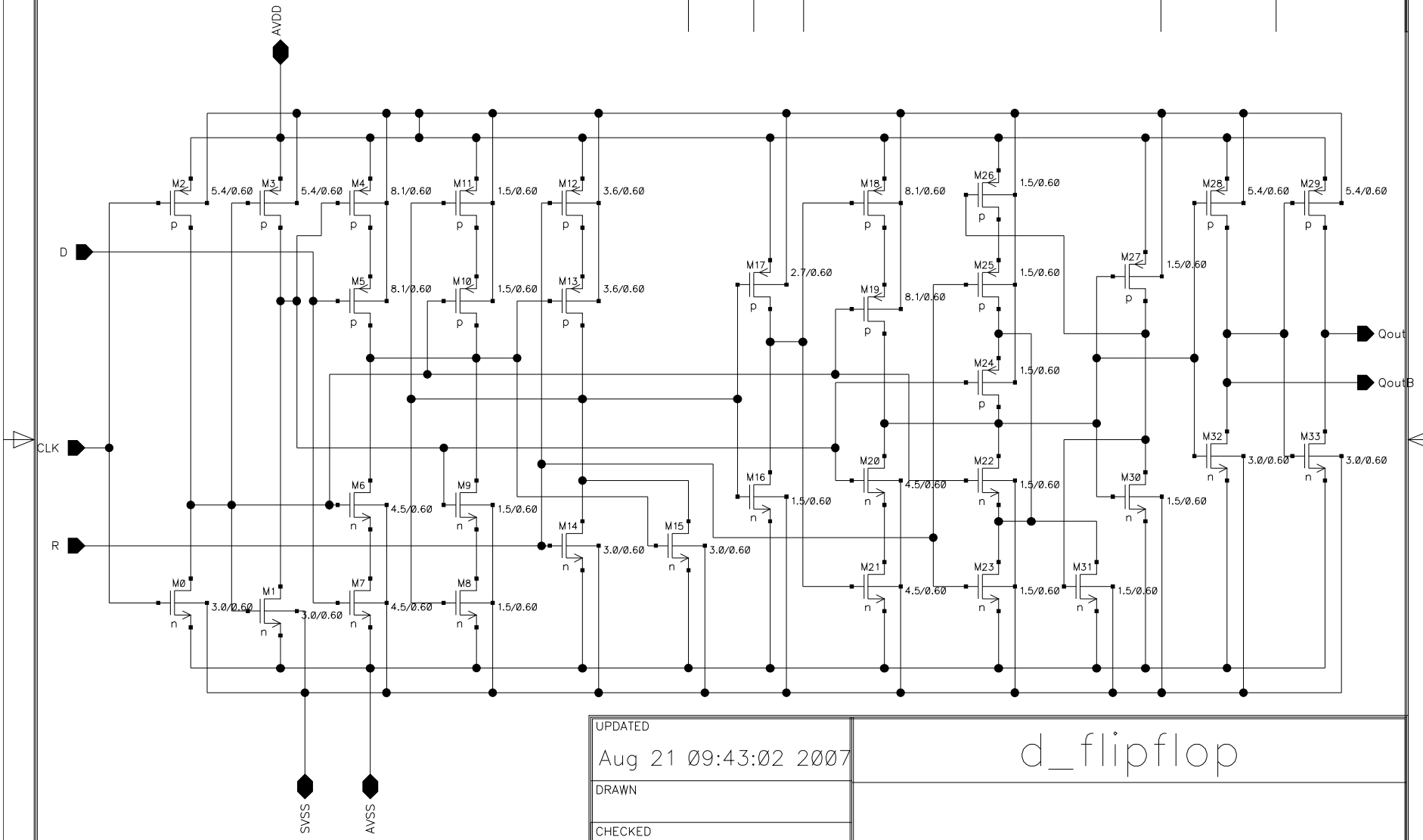
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV A
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	d_flipflop		
Aug 21 09:43:02 2007			
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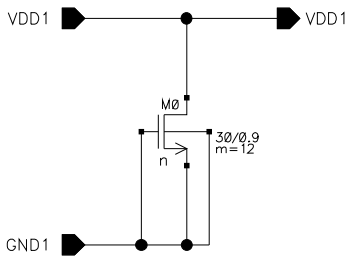
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Nov 11 15:36:54 2004	PadVdd			
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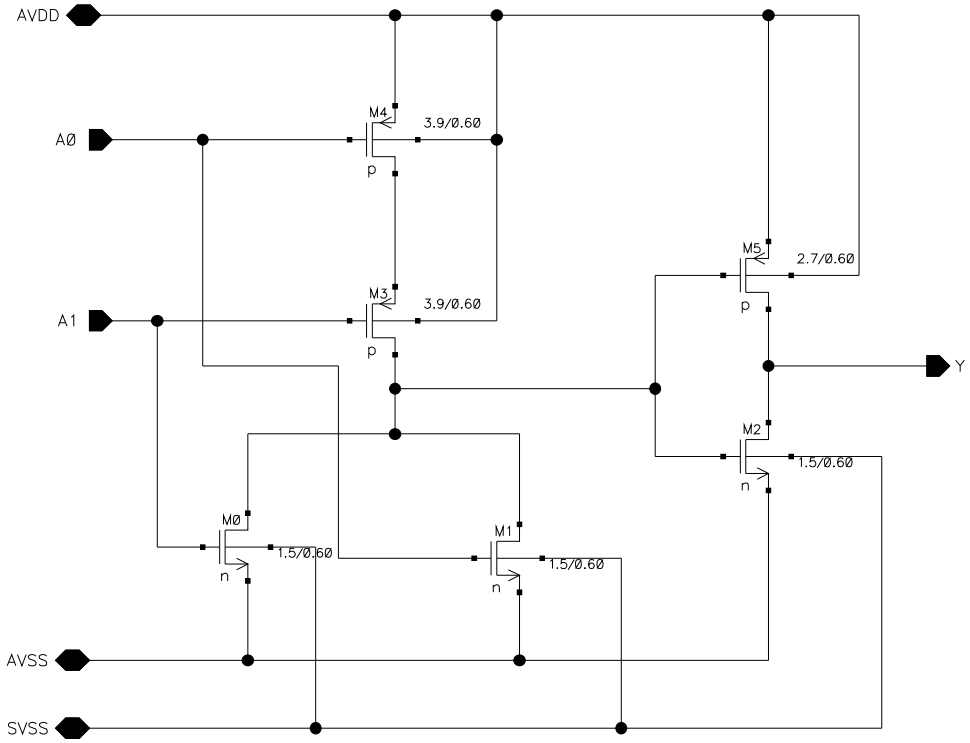
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

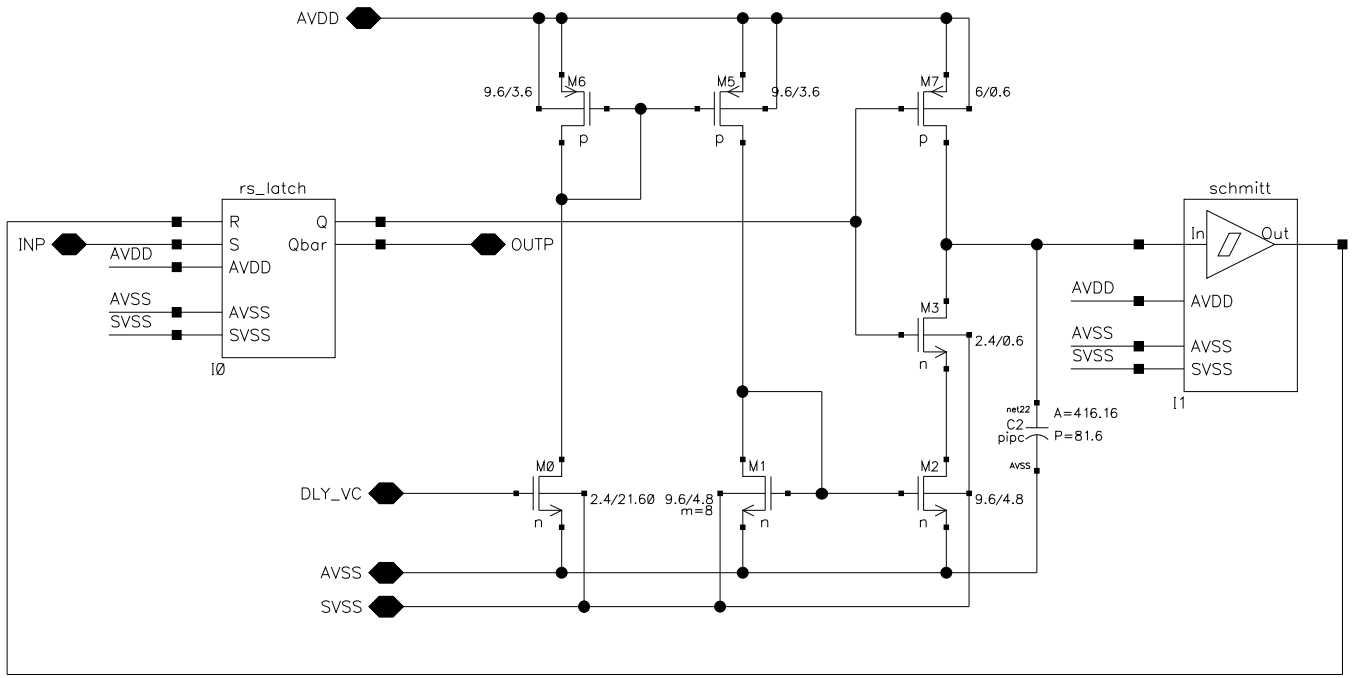


UPDATED Jun 5 12:02:59 2007	Or			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

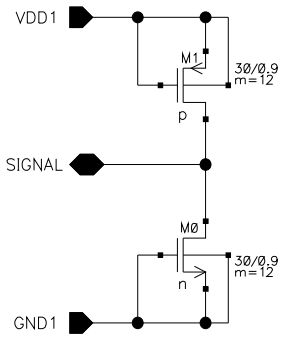


UPDATED	one_shot_vari		
Jul 5 12:56:Ø2 2Ø11			
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jan 25 15:54:23 2007	PadAref			
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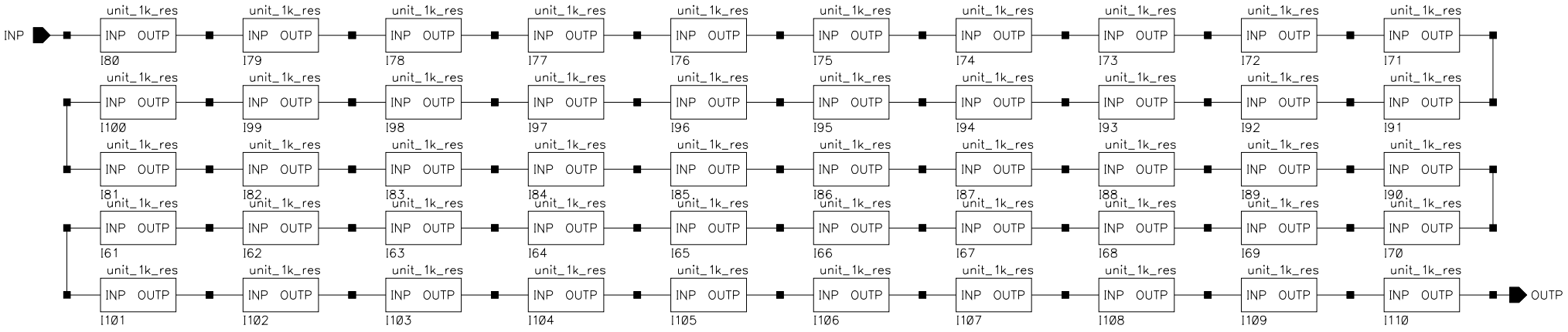
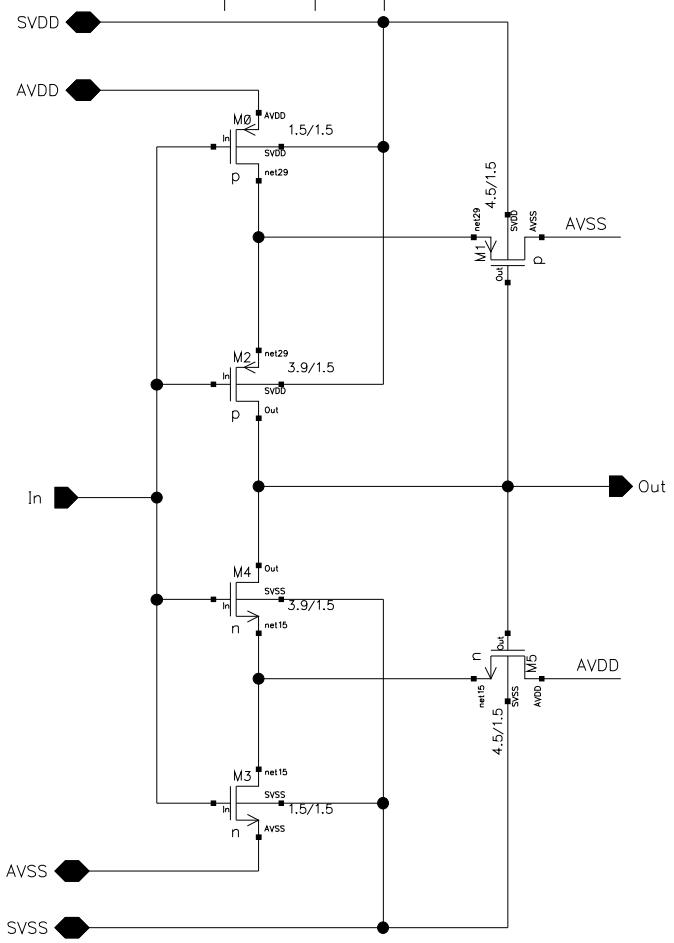
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


INP
OUTP
unit_1k_res
INP OUTP
I80
I79
I78
I77
I76
I75
I74
I73
I72
I71
I100
I99
I98
I97
I96
I95
I94
I93
I92
I91
I81
I82
I83
I84
I85
I86
I87
I88
I89
I90
I61
I62
I63
I64
I65
I66
I67
I68
I69
I70
I101
I102
I103
I104
I105
I106
I107
I108
I109
I110

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jul 24 14:48:04 2003	schmitt			
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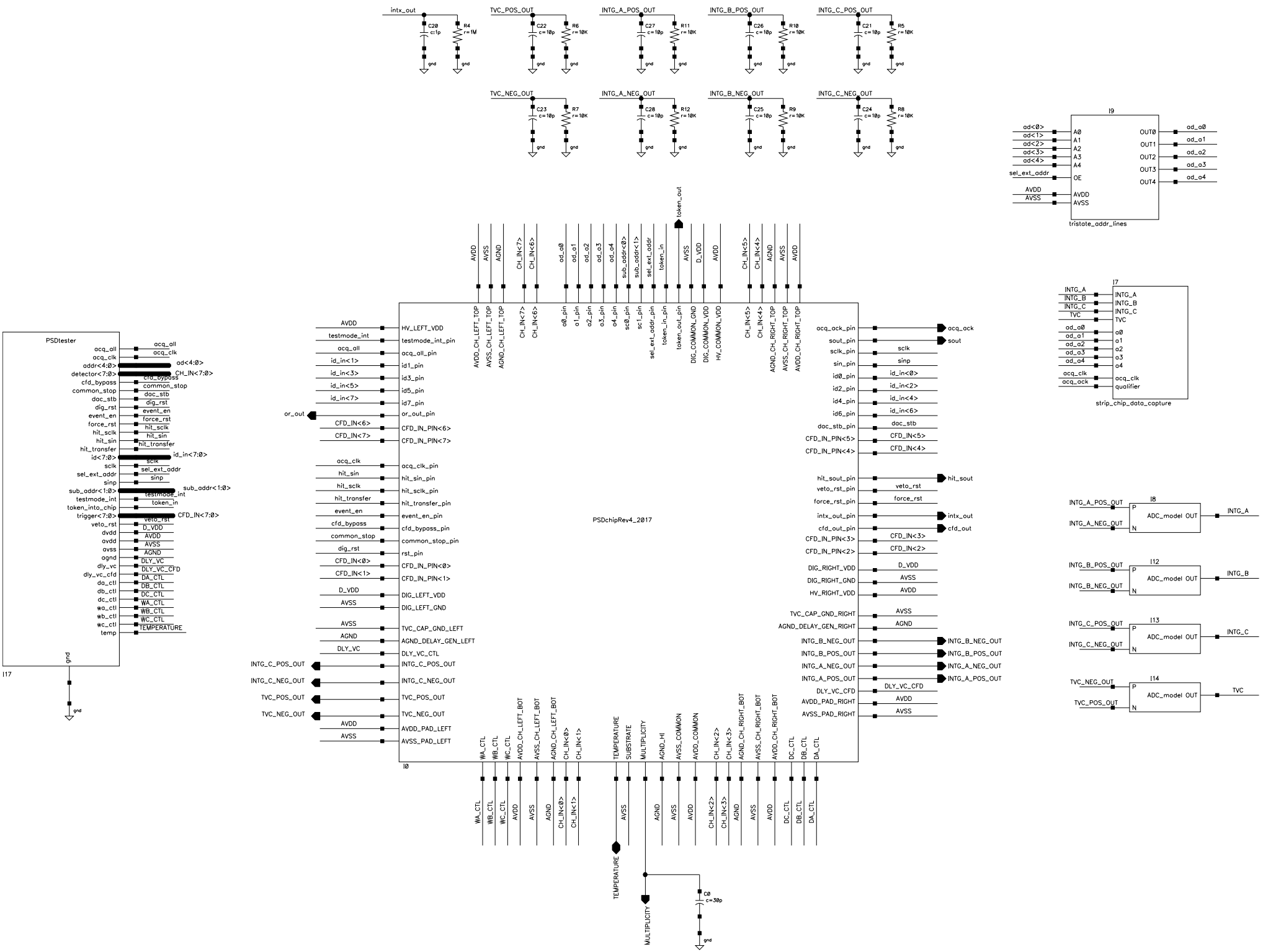
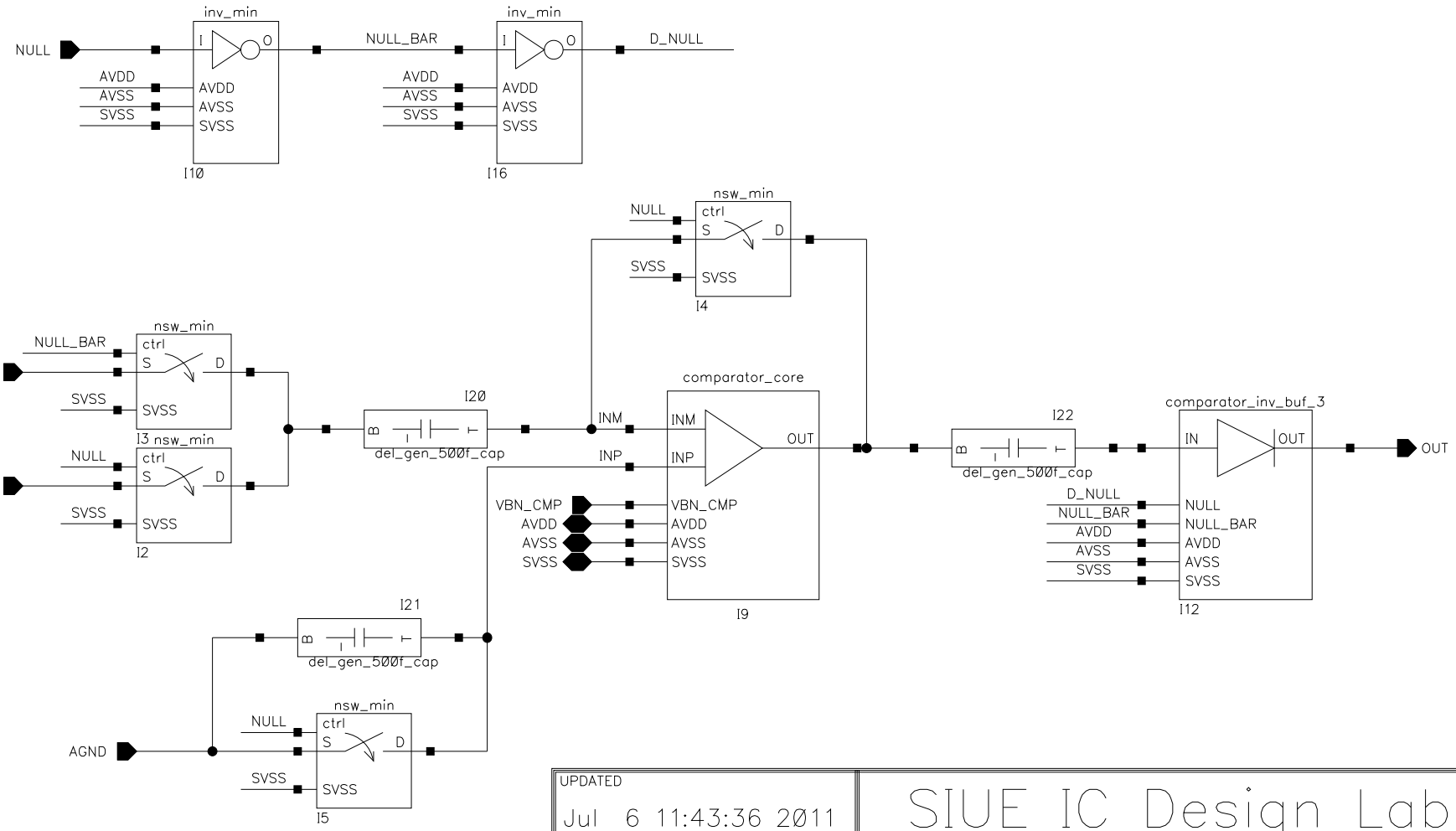
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


intx_out
C20 c:1p
R4 r=1M
TVC_POS_OUT
C22 c=10p
R6 r=10K
INTG_A_POS_OUT
C27 c=10p
R11 r=10K
INTG_B_POS_OUT
C26 c=10p
R10 r=10K
INTG_C_POS_OUT
C21 c=10p
R5 r=10K
TVC_NEG_OUT
C23 c=10p
R7 r=10K
INTG_A_NEG_OUT
C28 c=10p
R12 r=10K
INTG_B_NEG_OUT
C25 c=10p
R9 r=10K
INTG_C_NEG_OUT
C24 c=10p
R8 r=10K
gnd
I9
ad<0>
ad<1>
ad<2>
ad<3>
ad<4>
sel_ext_addr
AVDD
AVSS
A0
A1
A2
A3
A4
OE
AVDD
AVSS
OUT0
OUT1
OUT2
OUT3
OUT4
ad_a0
ad_a1
ad_a2
ad_a3
ad_a4
tristate_addr_lines
token_out
I7
INTG_A
INTG_B
INTG_C
TVC
ad_a0
ad_a1
ad_a2
ad_a3
ad_a4
acq_clk
acq_ack
qualifier
strip_chip_data_capture
PSDtester
acq_all
acq_clk
addr<4:0>
detector<7:0>
cfd_bypass
common_stop
dac_stb
dig_rst
event_en
force_rst
hit_sclk
hit_sin
hit_transfer
id<7:0>
sclk
sel_ext_addr
sinp
sub_addr<1:0>
testmode_int
token_into_chip
trigger<7:0>
veto_rst
dvdd
avdd
avss
agnd
dly_vc
dly_vc_cfd
da_ctl
db_ctl
dc_ctl
wa_ctl
wb_ctl
wc_ctl
temp
ad<4:0>
CH_IN<7:0>
common_stop
dac_stb
dig_rst
event_en
force_rst
hit_sclk
hit_sin
hit_transfer
id_in<7:0>
sclk
sel_ext_addr
sinp
sub_addr<1:0>
testmode_int
token_in
CFD_IN<7:0>
veto_rst
D_VDD
AVDD
AVSS
AGND
DLY_VC
DLY_VC_CFD
DA_CTL
DB_CTL
DC_CTL
WA_CTL
WB_CTL
WC_CTL
TEMPERATURE
I17
gnd
AVDD
AVSS
AGND
CH_IN<7>
CH_IN<6>
ad_a0
ad_a1
ad_a2
ad_a3
ad_a4
sub_addr<0>
sub_addr<1>
sel_ext_addr
token_in
token_out
AVSS
D_VDD
AVDD
CH_IN<5>
CH_IN<4>
AGND
AVSS
AVDD
AVDD_CH_LEFT_TOP
AVSS_CH_LEFT_TOP
AGND_CH_LEFT_TOP
CH_IN<7>
CH_IN<6>
a0_pin
a1_pin
a2_pin
a3_pin
a4_pin
sc0_pin
sc1_pin
sel_ext_addr_pin
token_in_pin
token_out_pin
DIG_COMMON_GND
DIG_COMMON_VDD
HV_COMMON_VDD
CH_IN<5>
CH_IN<4>
AGND_CH_RIGHT_TOP
AVSS_CH_RIGHT_TOP
AVDD_CH_RIGHT_TOP
AVDD
testmode_int
acq_all
id_in<1>
id_in<3>
id_in<5>
id_in<7>
or_out
CFD_IN<6>
CFD_IN<7>
acq_clk
hit_sin
hit_sclk
hit_transfer
event_en
cfd_bypass
common_stop
dig_rst
CFD_IN<0>
CFD_IN<1>
D_VDD
AVSS
AVSS
AGND
DLY_VC
INTG_C_POS_OUT
INTG_C_NEG_OUT
TVC_POS_OUT
TVC_NEG_OUT
AVDD
AVSS
HV_LEFT_VDD
testmode_int_pin
acq_all_pin
id1_pin
id3_pin
id5_pin
id7_pin
or_out_pin
CFD_IN_PIN<6>
CFD_IN_PIN<7>
acq_clk_pin
hit_sin_pin
hit_sclk_pin
hit_transfer_pin
event_en_pin
cfd_bypass_pin
common_stop_pin
rst_pin
CFD_IN_PIN<0>
CFD_IN_PIN<1>
DIG_LEFT_VDD
DIG_LEFT_GND
TVC_CAP_GND_LEFT
AGND_DELAY_GEN_LEFT
DLY_VC_CTL
INTG_C_POS_OUT
INTG_C_NEG_OUT
TVC_POS_OUT
TVC_NEG_OUT
AVDD_PAD_LEFT
AVSS_PAD_LEFT
PSDchipRev4_2017
acq_ack_pin
sout_pin
sclk_pin
sin_pin
id0_pin
id2_pin
id4_pin
id6_pin
dac_stb_pin
CFD_IN_PIN<5>
CFD_IN_PIN<4>
hit_sout_pin
veto_rst_pin
force_rst_pin
intx_out_pin
cfd_out_pin
CFD_IN_PIN<3>
CFD_IN_PIN<2>
DIG_RIGHT_VDD
DIG_RIGHT_GND
HV_RIGHT_VDD
TVC_CAP_GND_RIGHT
AGND_DELAY_GEN_RIGHT
INTG_B_NEG_OUT
INTG_B_POS_OUT
INTG_A_NEG_OUT
INTG_A_POS_OUT
DLY_VC_CFD
AVDD_PAD_RIGHT
AVSS_PAD_RIGHT
acq_ack
sout
sclk
sinp
id_in<0>
id_in<2>
id_in<4>
id_in<6>
dac_stb
CFD_IN<5>
CFD_IN<4>
hit_sout
veto_rst
force_rst
intx_out
cfd_out
CFD_IN<3>
CFD_IN<2>
D_VDD
AVSS
AVDD
AVSS
AGND
INTG_B_NEG_OUT
INTG_B_POS_OUT
INTG_A_NEG_OUT
INTG_A_POS_OUT
DLY_VC_CFD
AVDD
AVSS
I0
WA_CTL
WB_CTL
WC_CTL
AVDD_CH_LEFT_BOT
AVSS_CH_LEFT_BOT
AGND_CH_LEFT_BOT
CH_IN<0>
CH_IN<1>
TEMPERATURE
SUBSTRATE
MULTIPLICITY
AGND_HI
AVSS_COMMON
AVDD_COMMON
CH_IN<2>
CH_IN<3>
AGND_CH_RIGHT_BOT
AVSS_CH_RIGHT_BOT
AVDD_CH_RIGHT_BOT
DC_CTL
DB_CTL
DA_CTL
WA_CTL
WB_CTL
WC_CTL
AVDD
AVSS
AGND
CH_IN<0>
CH_IN<1>
TEMPERATURE
AVSS
AGND
AVSS
AVDD
CH_IN<2>
CH_IN<3>
AGND
AVSS
AVDD
DC_CTL
DB_CTL
DA_CTL
MULTIPLICITY
C0 c=30p
gnd
I8
INTG_A_POS_OUT
INTG_A_NEG_OUT
P
N
ADC_model OUT
INTG_A
I12
INTG_B_POS_OUT
INTG_B_NEG_OUT
INTG_B
I13
INTG_C_POS_OUT
INTG_C_NEG_OUT
INTG_C
I14
TVC_NEG_OUT
TVC_POS_OUT
TVC

CAGE NO.	DWG NO.	SH 1	REV A

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	Jul 6 11:43:36 2011
DRAWN	
CHECKED	
CHECKED	
ISSUED	

SIUE IC Design Lab

Delay Gen Comparator

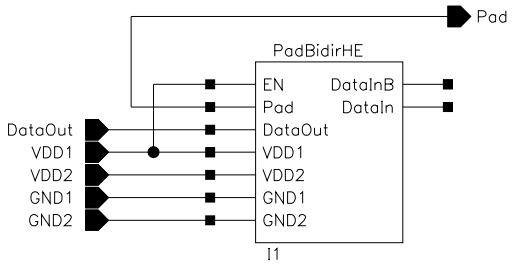
SIZE	CAGE NO.	DWG NO.	REV
A			A

SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Feb 28 11:31:10 2017	PadOut			
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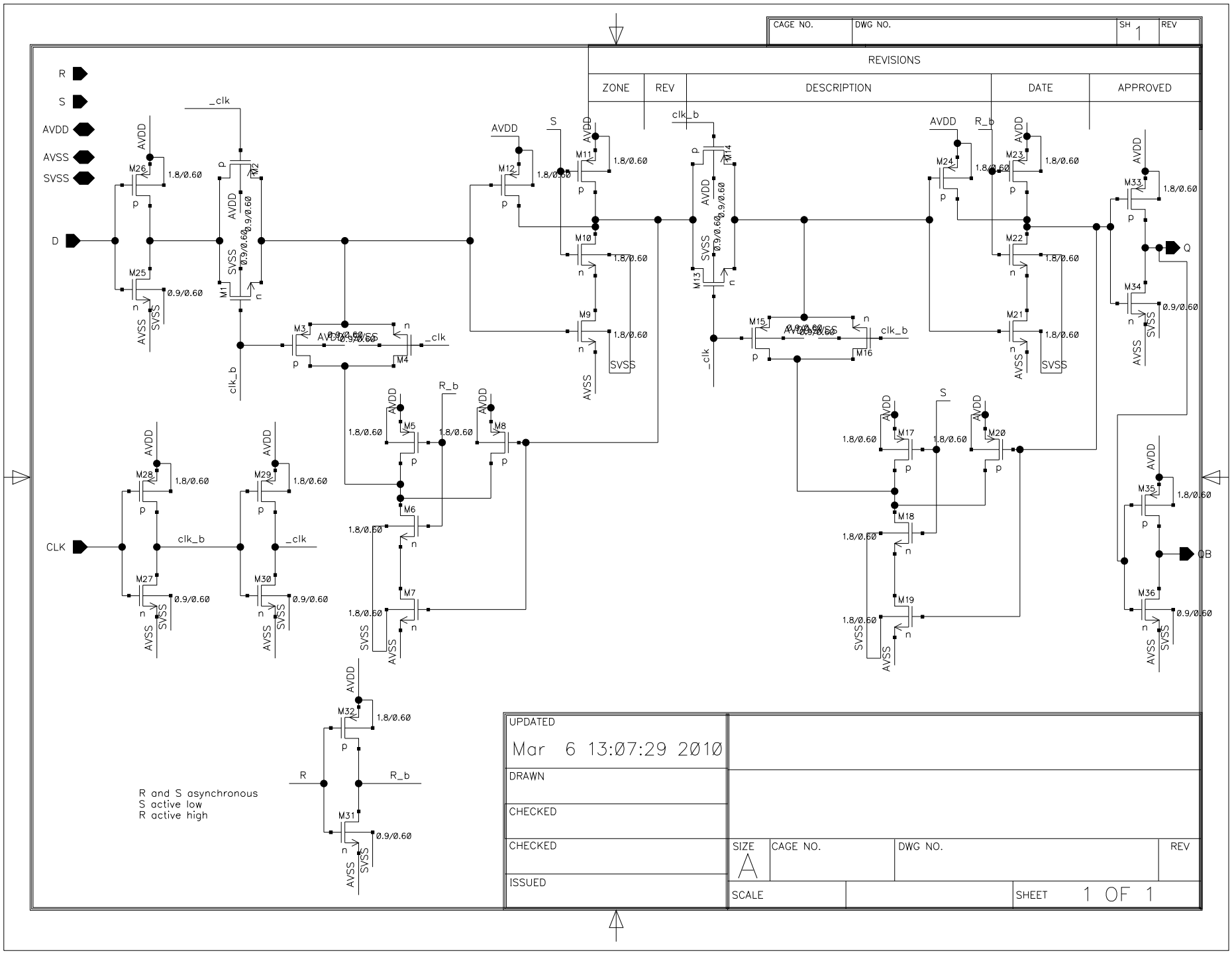
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


CAGE NO.
DWG NO.
SH 1
REV
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
R
S
AVDD
AVSS
SVSS
D
CLK
Q
QB
_clk
clk_b
R_b
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
M15
M16
M17
M18
M19
M20
M21
M22
M23
M24
M25
M26
M27
M28
M29
M30
M31
M32
M33
M34
M35
M36
1.8/0.60
0.9/0.60
R and S asynchronous
S active low
R active high
UPDATED
Mar 6 13:07:29 2010
DRAWN
CHECKED
CHECKED
ISSUED
SIZE
A
CAGE NO.
DWG NO.
REV
SCALE
SHEET 1 OF 1

T
B
unit_200f_cap
T
B
116
117
118
119
120
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122
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124
125
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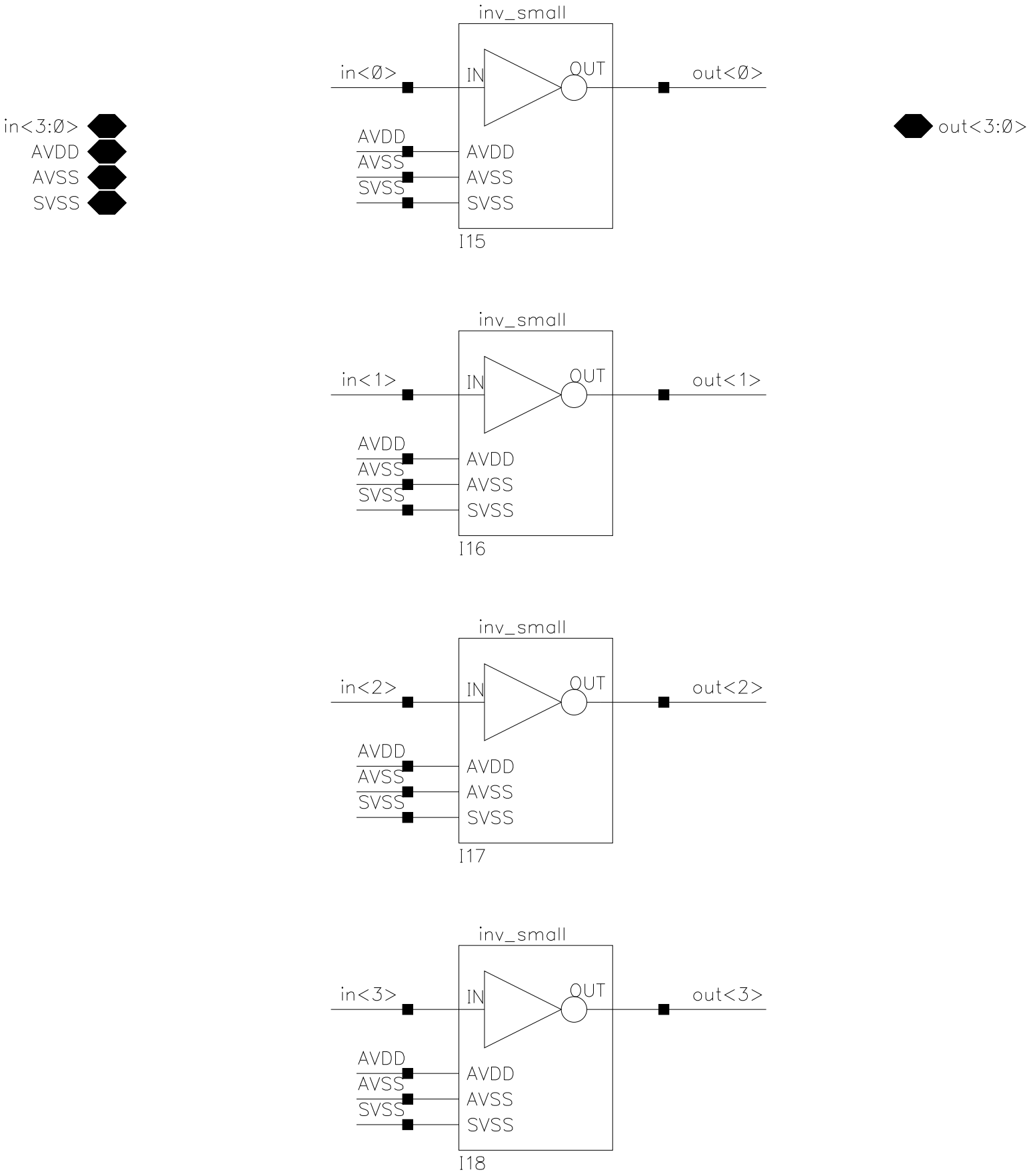
128
129
130
131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AVSS
SVSS
out<3:0>
inv_small
in<0>
IN
OUT
out<0>
AVDD
AVSS
SVSS
I15
inv_small
in<1>
IN
OUT
out<1>
AVDD
AVSS
SVSS
I16
inv_small
in<2>
IN
OUT
out<2>
AVDD
AVSS
SVSS
I17
inv_small
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IN
OUT
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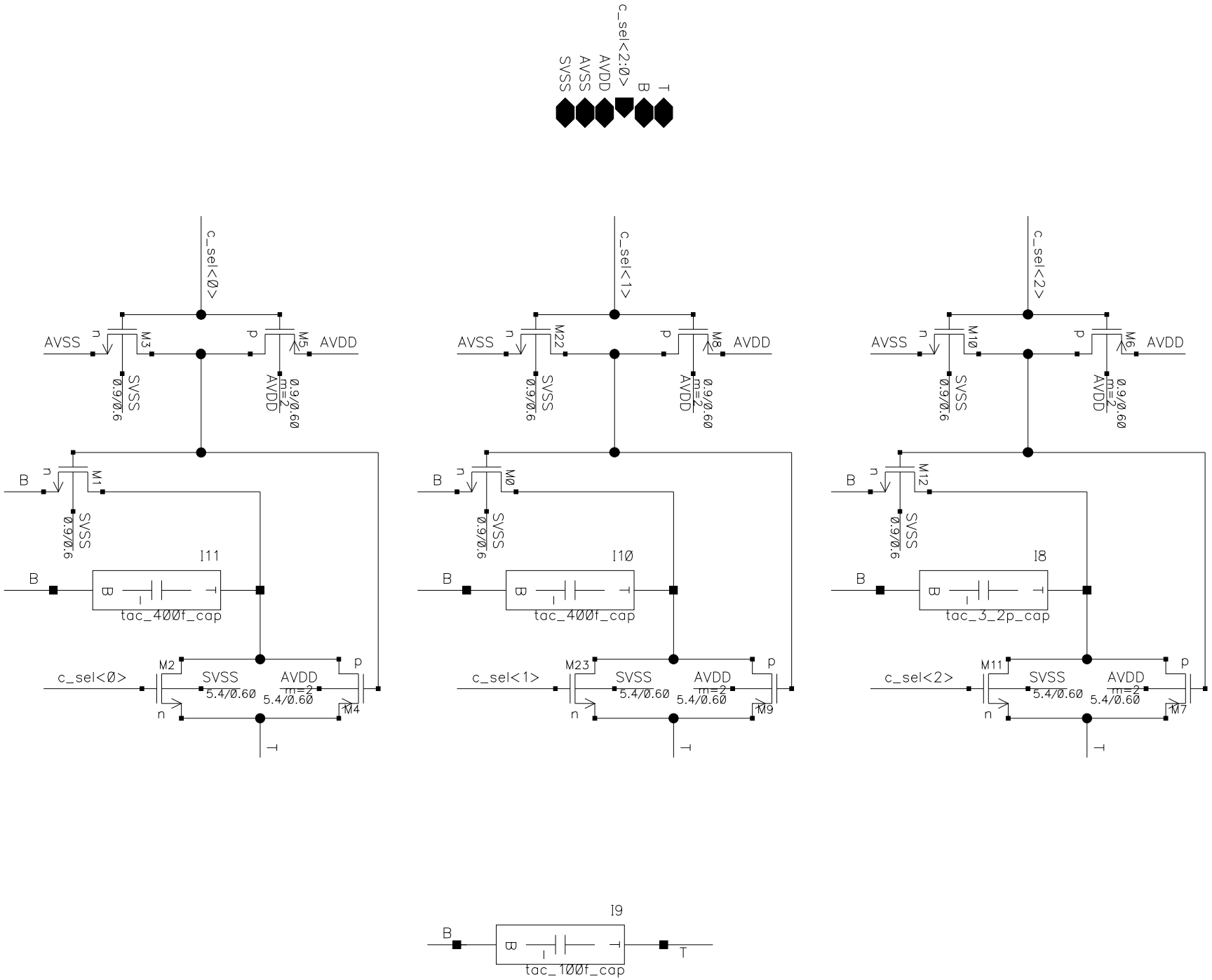
AVDD
AVSS
SVSS
I18


c_sel<2:0>
SVSS
AVSS
AVDD
B
T
c_sel<0>
c_sel<1>
c_sel<2>
AVSS
AVDD
M3
M5
M22
M8
M10
M6
M1
M0
M12
M2
M23
M11
M4
M9
M7
SVSS
0.9/0.6
0.9/0.60
m=2
5.4/0.60
I11
I10
I8
I9
tac_400f_cap
tac_3_2p_cap
tac_100f_cap

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

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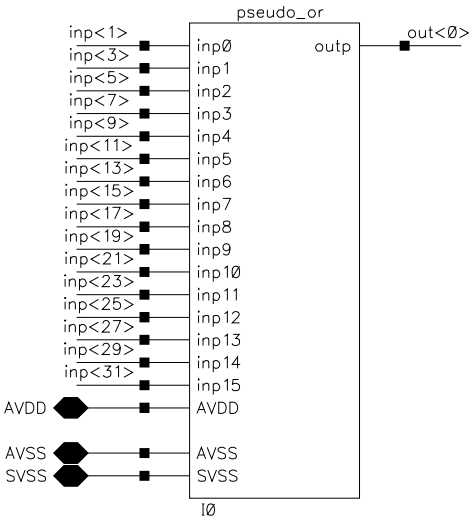
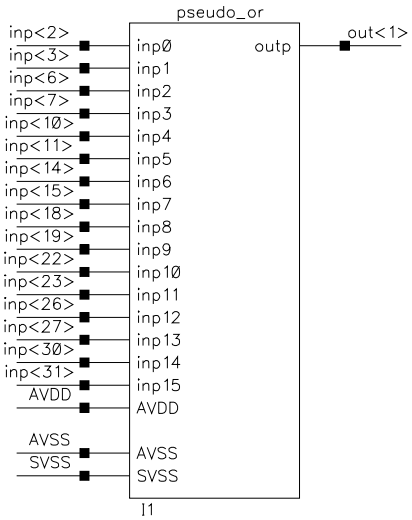
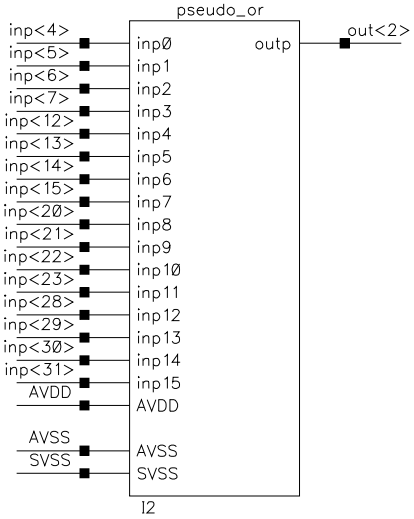
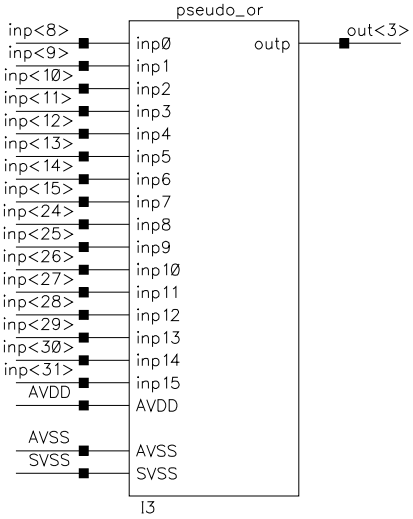
inp<31:8>

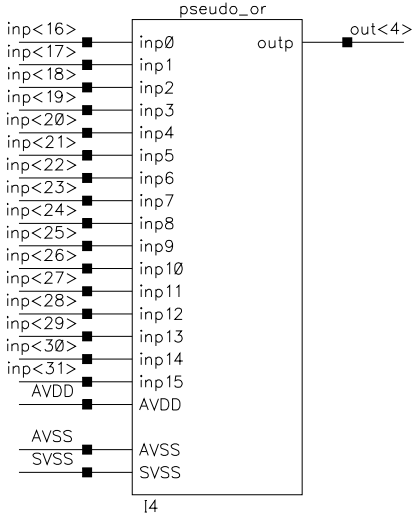
out<4:0>











UPDATED	enc32to5		
Jul 15 14:47:49 2010			
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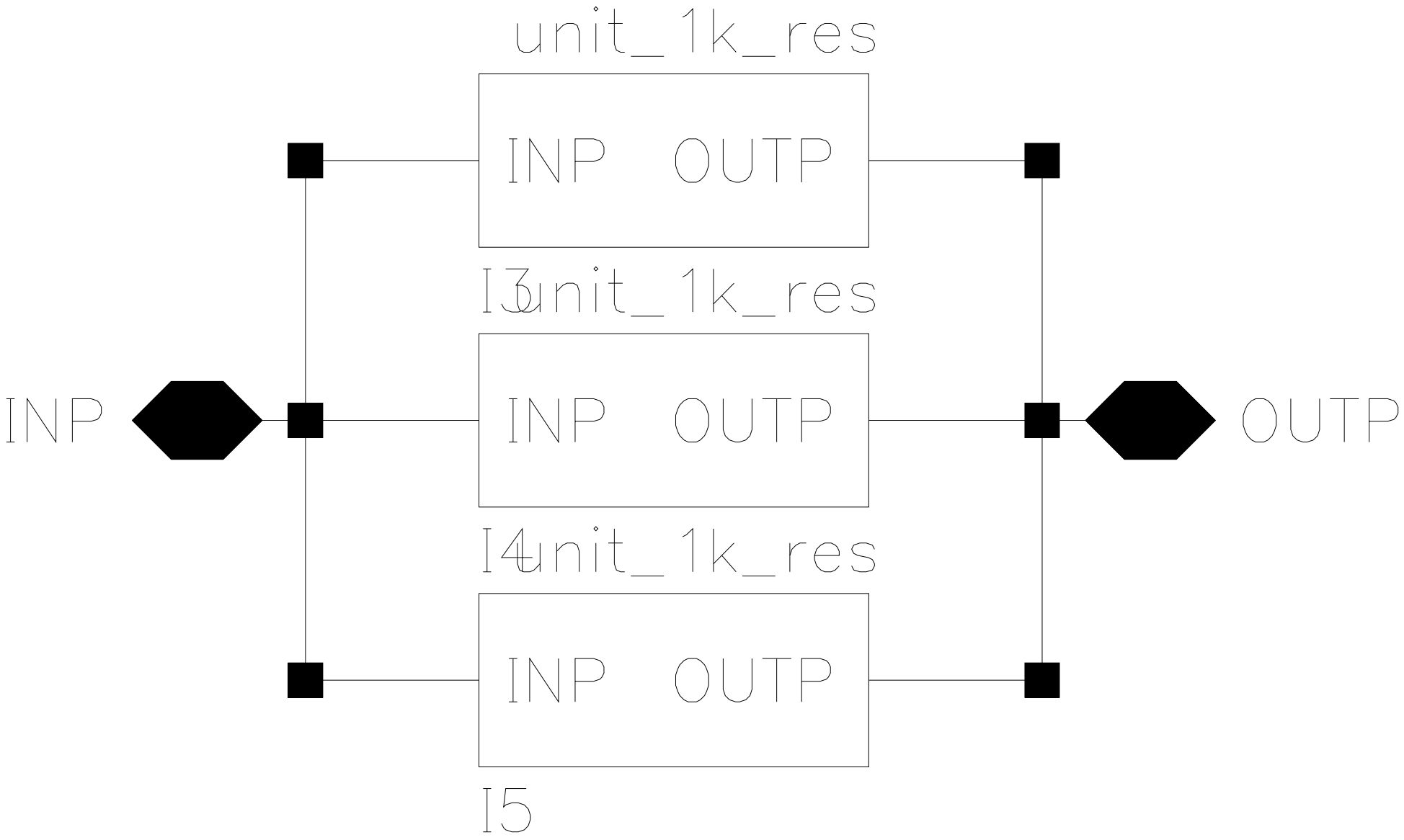
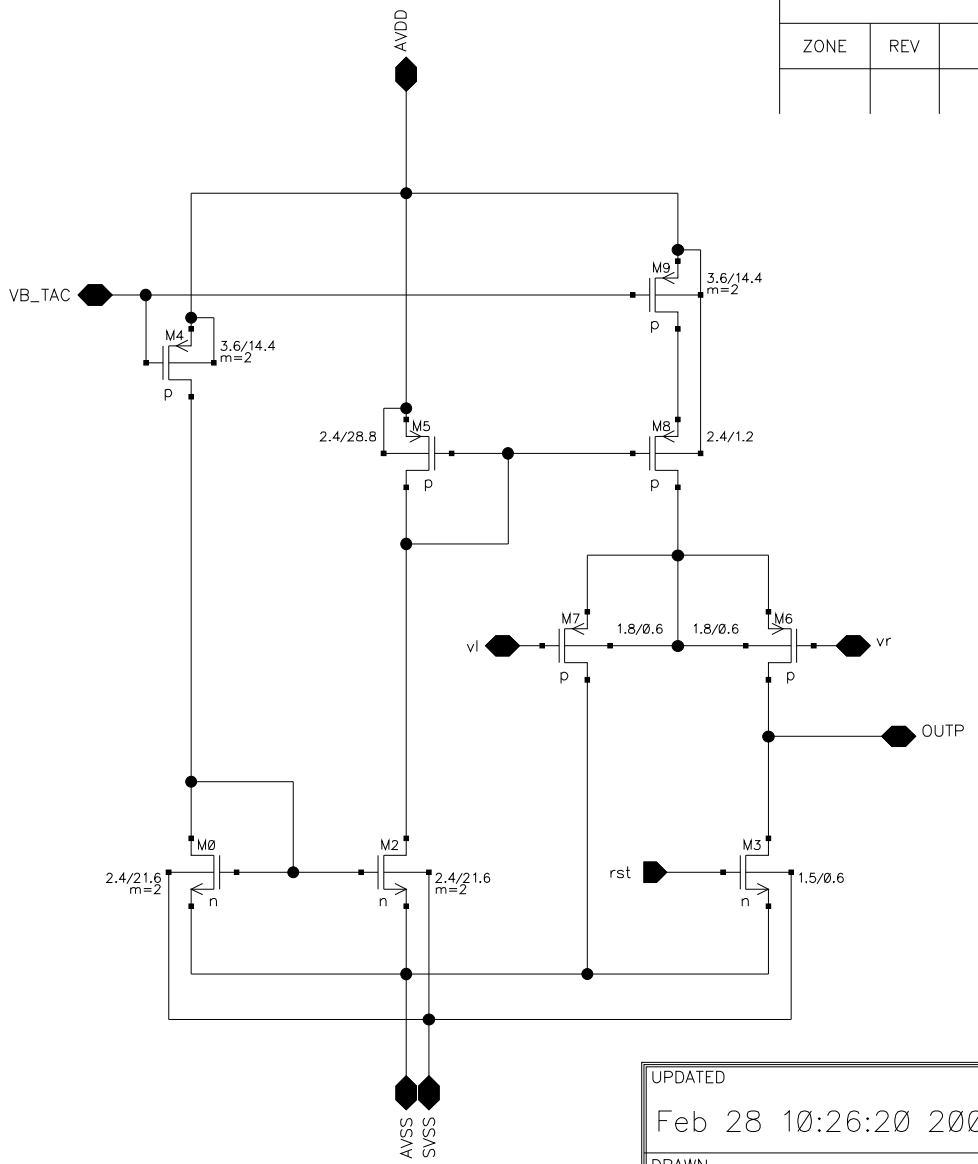
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. REV
ISSUED	SCALE		SHEET 1 OF 1


unit_1k_res
INP OUTP
I3
unit_1k_res
INP OUTP
INP
OUTP
I4
unit_1k_res
INP OUTP
I5

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED	tac			
Feb 28 10:26:20 2007				
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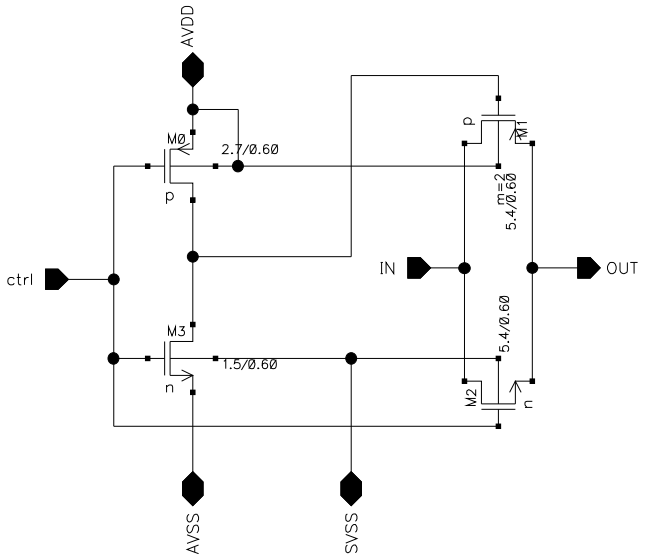
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



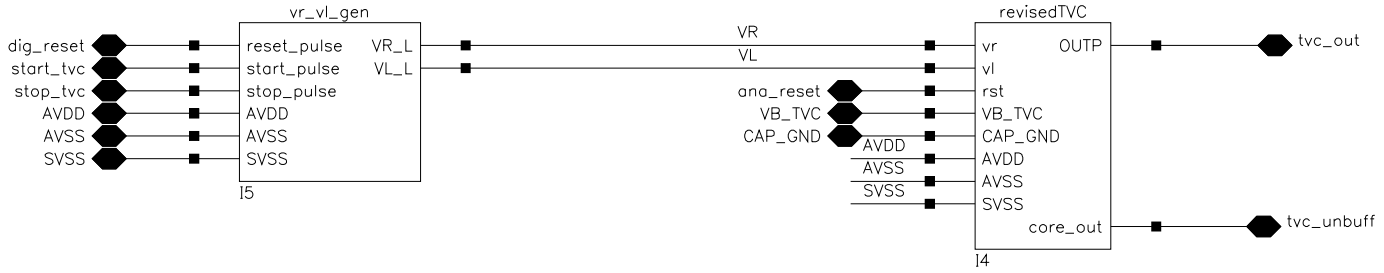
UPDATED Aug 13 15:55:31 2007	sw_channel		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

VR and VL are active low signals.
They drive the gates of PFETs.

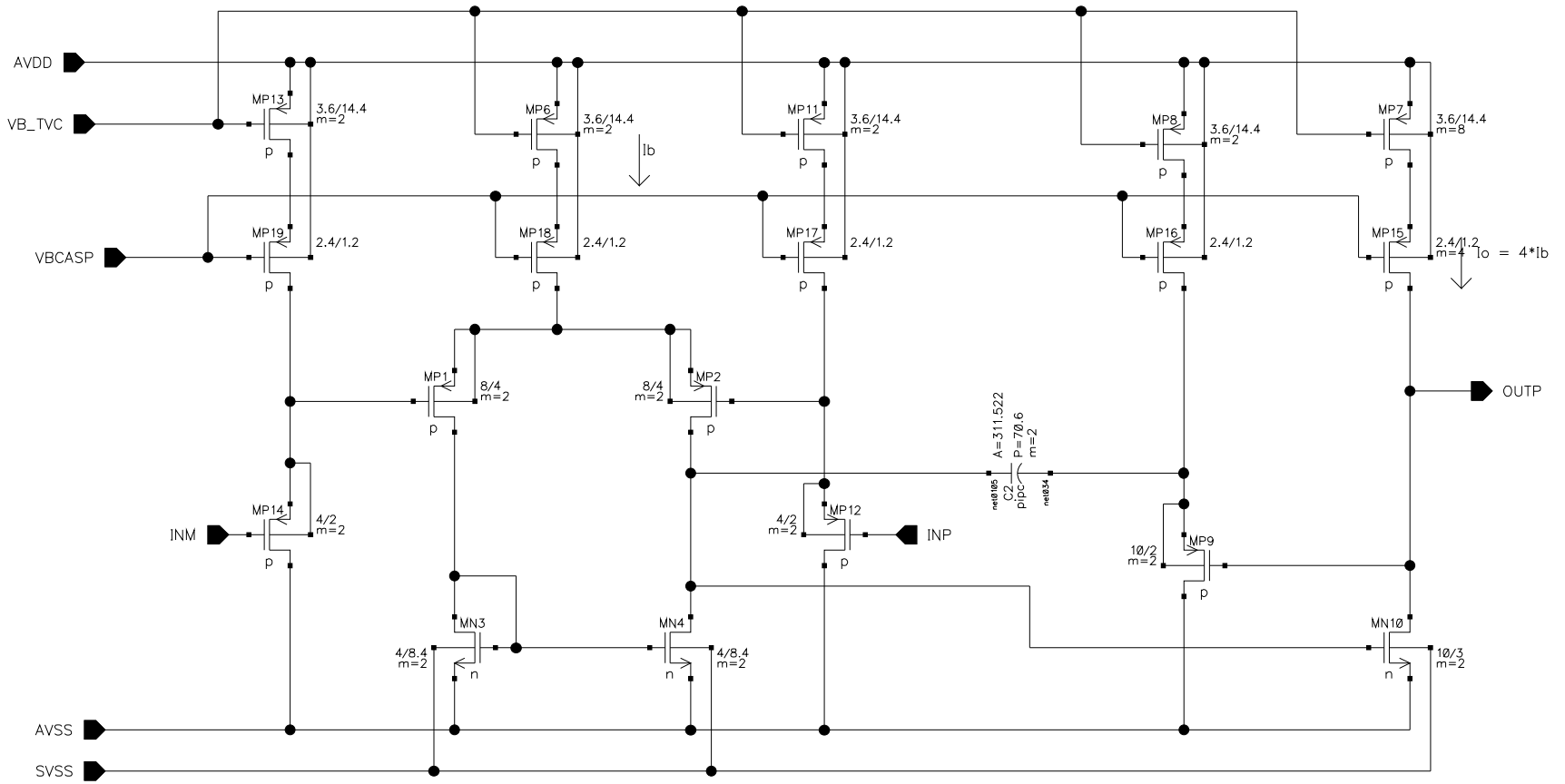


UPDATED Aug 17 15:02:46 2011	SIUE		
DRAWN	Revised full TVC		
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



Bias current:
500 ns range: 10 uA
2 us range: 2.5 uA

UPDATED	Jul 5 13:00:33 2011
DRAWN	
CHECKED	
CHECKED	
ISSUED	

SIUE

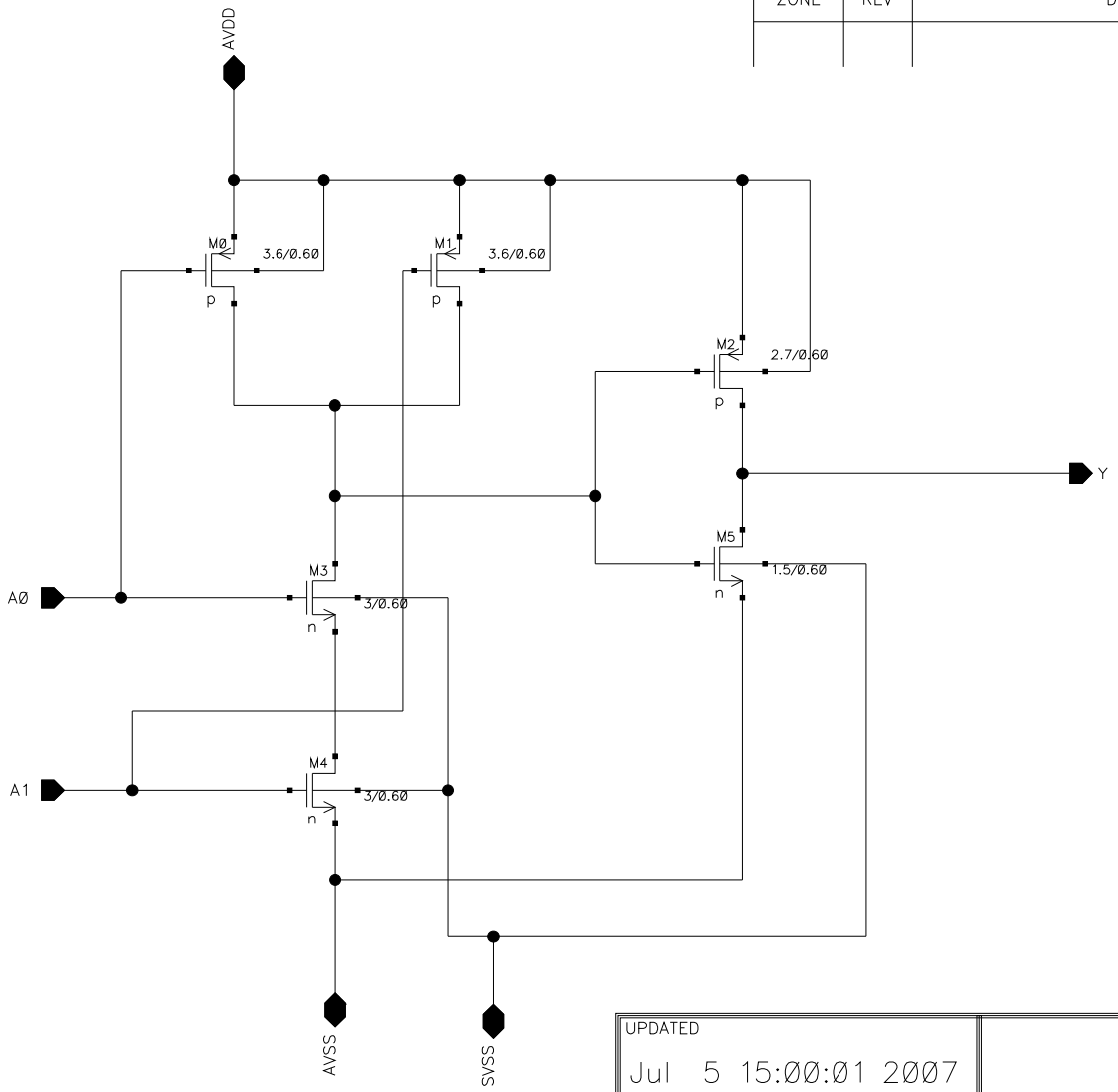
TVC local buffer

SIZE	CAGE NO.	DWG NO.	REV
A			
SCALE		SHEET	1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

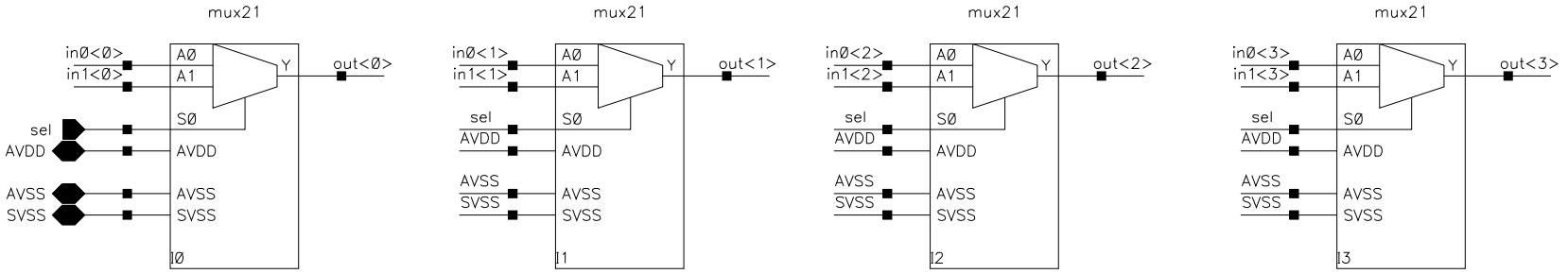


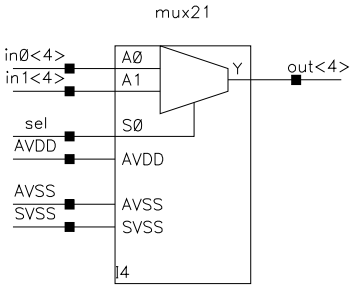
UPDATED Jul 5 15:00:01 2007	and			
DRAWN				
CHECKED				
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	

CAGE NO.	DWG NO.	SH 1	REV

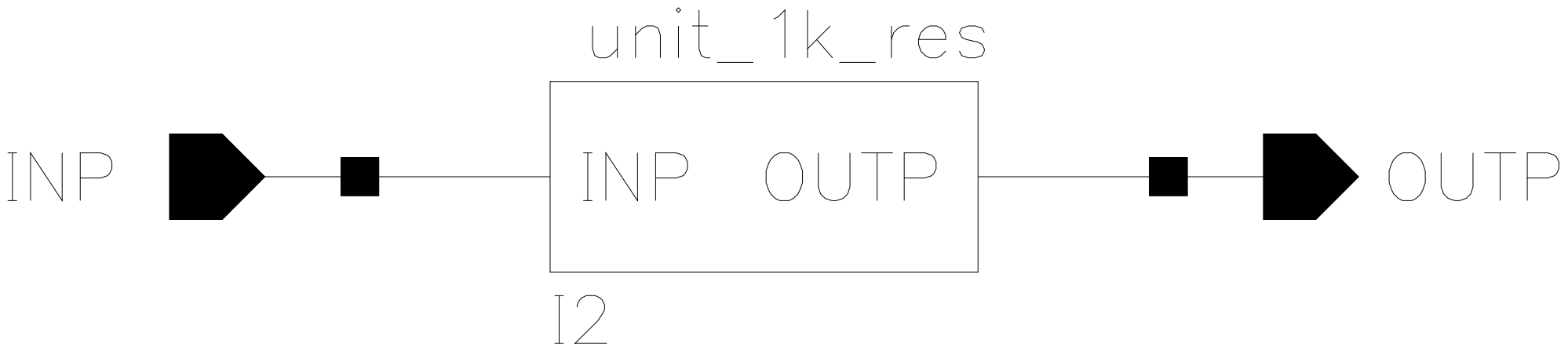
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED





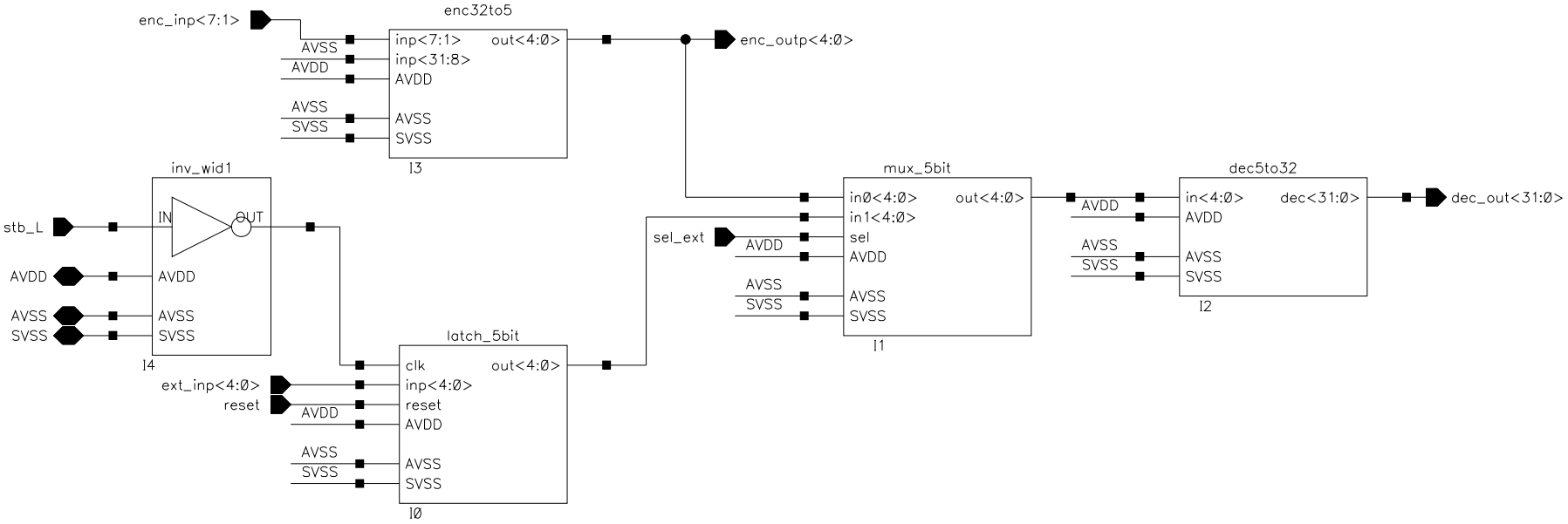
UPDATED Jun 25 14:14:01 2010	mux_5bit		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1


unit_1k_res
INP
INP
OUTP
OUTP
I2

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

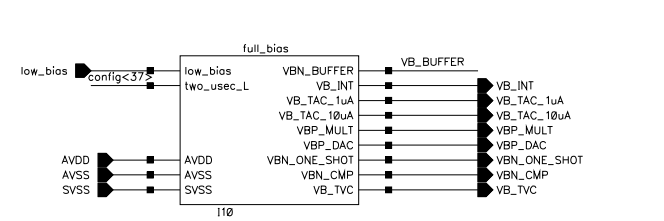
ZONE	REV	DESCRIPTION	DATE	APPROVED

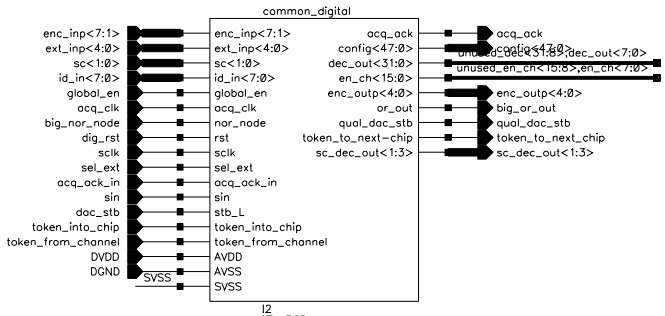


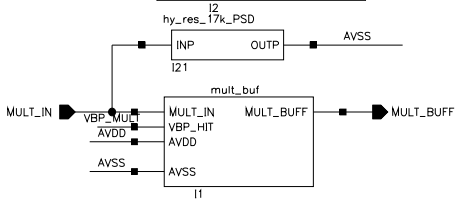
UPDATED Jun 28 07:56:50 2010	enc_dec_logic		
DRAWN			
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. / REV
ISSUED	SCALE		SHEET 1 OF 1

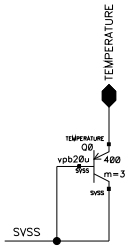
CAGE NO.	DWG NO.	SH	REV
		1	A

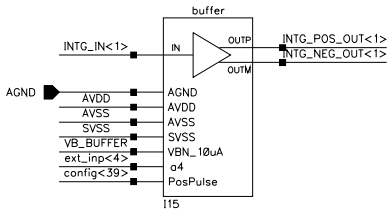
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

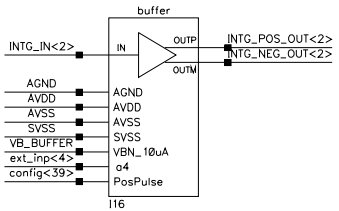


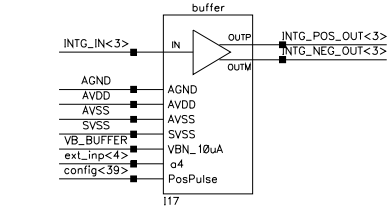


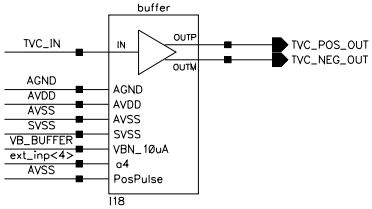










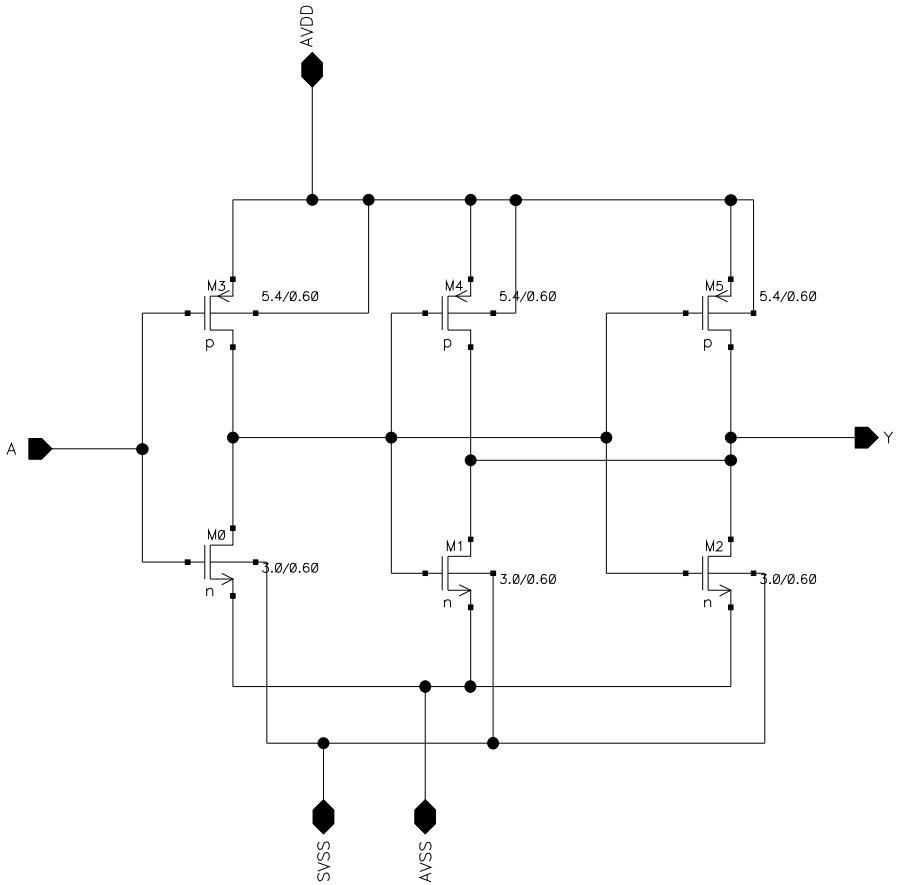


UPDATED	May 3 16:19:39 2017	SIUE IC Design Lab	
DRAWN		Common	
CHECKED			
CHECKED		SIZE B	CAGE NO. / DWG NO. / REV A
ISSUED		SCALE	SHEET 1 OF 1

CAGE NO.	DWG NO.	SH 1	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



UPDATED Jun 15 14:49:33 2007	buffer_4			
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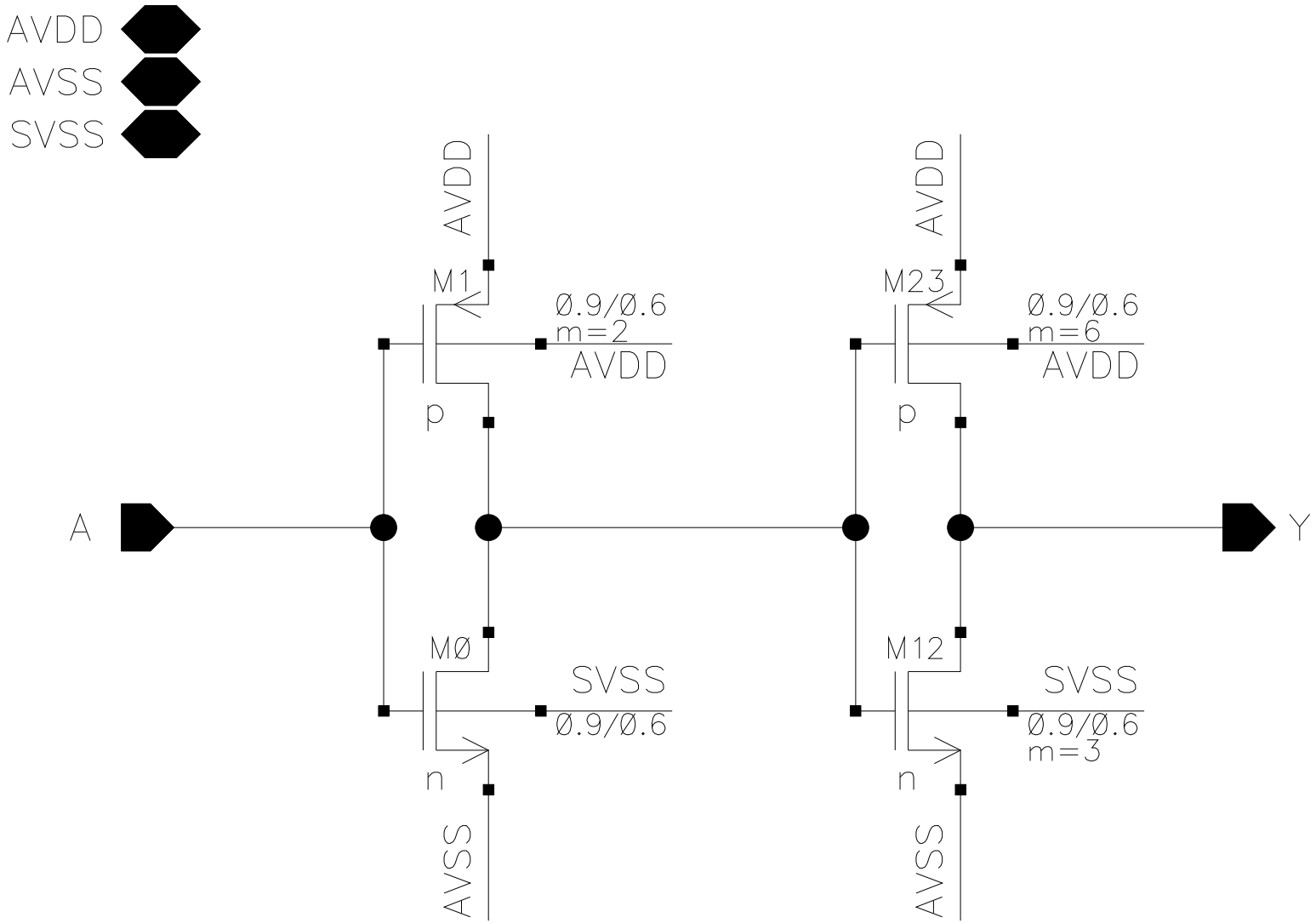
CHECKED	SIZE A	CAGE NO.	DWG NO.	REV
ISSUED	SCALE		SHEET 1 OF 1	


AVDD
AVSS
SVSS
AVDD
M1
Ø.9/Ø.6
m=2
AVDD
p
A
M0
SVSS
Ø.9/Ø.6
n
AVSS
AVDD
M23
Ø.9/Ø.6
m=6
AVDD
p
Y
M12
SVSS
Ø.9/Ø.6
m=3
n
AVSS