EEE 4483

Digital Electronics and Pulse Techniques

Lecture 0: Intro to the Course

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Referred Textbook:

Digital Integrated Circuits: A Design Perspective, 2nd edition

by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic

Early Digital Computers: Mechanical

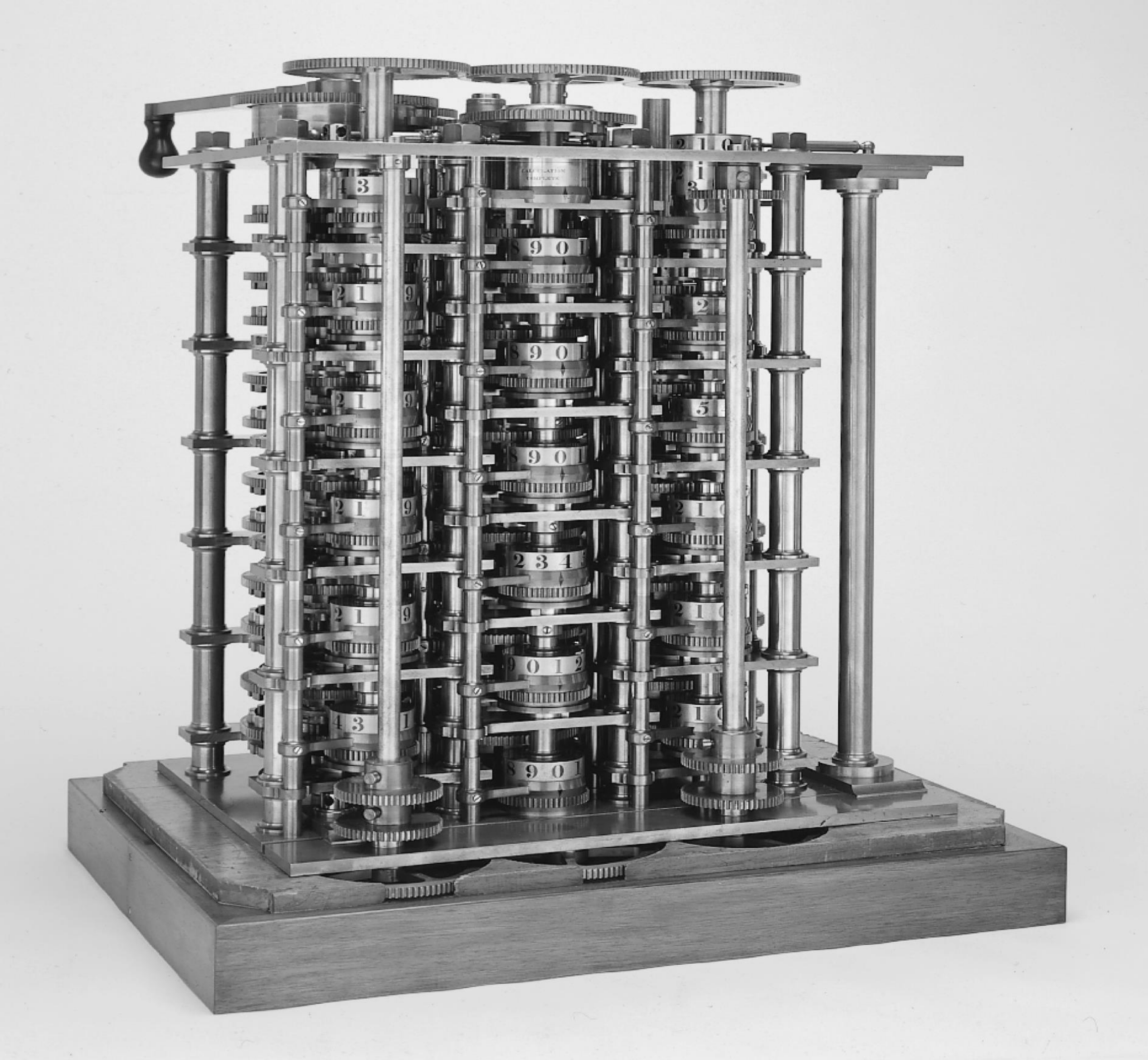


Fig: Working part of Babbage's Difference Engine I

- In the early nineteenth century, Babbage envisioned largescale mechanical computing devices, called Difference Engines
- The Analytical Engine was developed in 1834
  - Basic arithmetic operations
  - Operated in a two-cycle sequence, called "store" and "mill" (execute)
  - Used pipelining
- Impractical because of complexity and the cost:
  - Design of Difference Engine I required 25,000 mechanical parts at a total cost of £17,470 (in 1834!).

Birth of Digital "Electronic" Computing

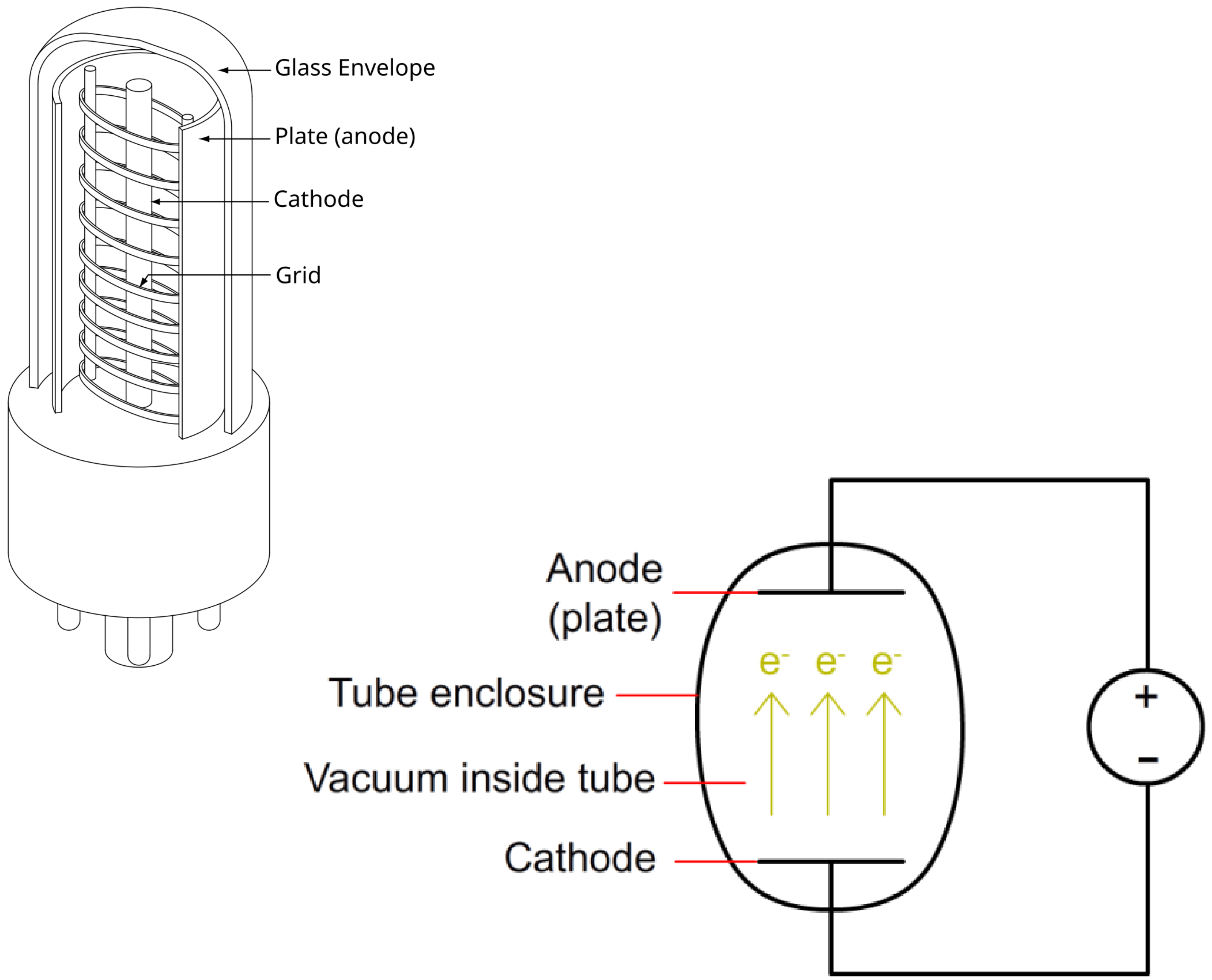


Fig: Vacuum tube

- The age of digital electronic computing started in full with the introduction of the vacuum tube
- Vacuum tube based computers –
  - ENIAC (for computing artillery firing tables)
  - UNIVAC I (first successful commercial computer)
- Infeasible because Reliability problems and excessive power consumption:
  - The ENIAC was 80 feet long, 8.5 feet high and several feet wide and incorporated 18,000 vacuum tubes

Evolution of Digital Logic Technologies

- 1947–1960s: Birth of Transistor-Based Logic
  - Invention of the transistor (1947, Bell Labs) and bipolar transistor (1949)
  - First bipolar logic gate (1956) → Fairchild Micrologic (1960)
  - TTL (Transistor-Transistor Logic) introduced in 1962; dominated market till 1980s

- 1960s–1970s: Toward MOS Technology
  - TTL offered high integration density, but still power-hungry
  - Efforts to reduce bipolar power (e.g., I^2L - Integrated Injection Logic) were limited
  - Shift toward MOSFET-based logic (originally patented in 1925–1935)

Evolution of Digital Logic Technologies (continued)

- MOS Logic Families
  - CMOS proposed in 1963; adoption delayed due to complexity
  - PMOS used first in calculators; **NMOS used in early microprocessors**:
    - Intel 4004 (1972), 8080 (1974)
    - Enabled high-density memory (e.g., 4 Kbit MOS memory in 1970)

- 1980s–Today: Rise of CMOS
  - NMOS faced power issues → industry shift to CMOS in late 1970s
  - CMOS became dominant due to lower power and scalability
  - Power concerns persist in modern CMOS design

Evolution of Integration Density

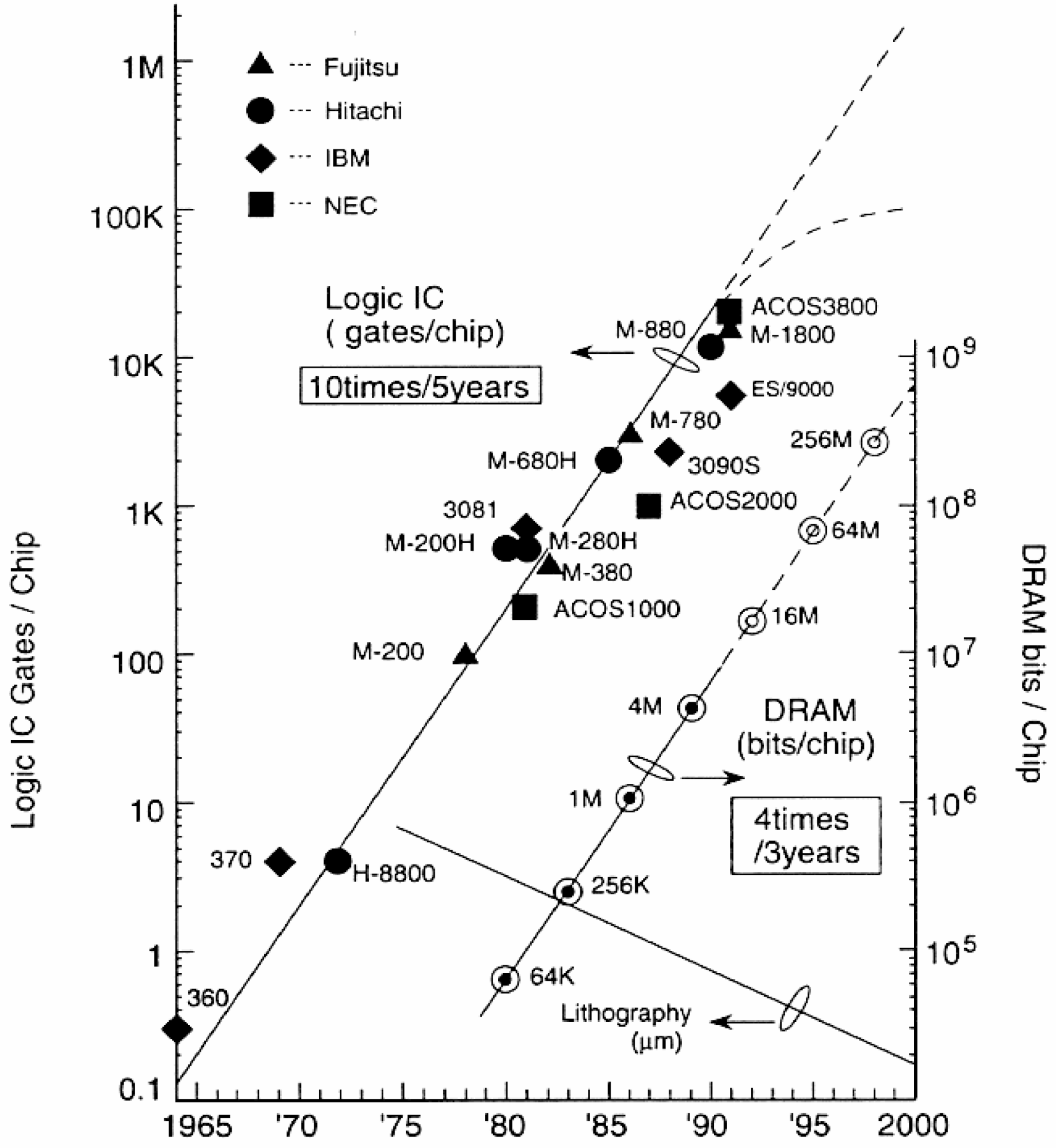
Moore's Law

Gordon Moore predicted in the 1960s –

"The number of transistors in an integrated circuit (IC) doubles about every two years"

- Transistor count has steadily increased since the 1970s –
  - Memory density has increased over 1000× since 1970
  - Million-transistor milestone crossed in late 1980s
  - Clock speed doubled every 3 years, reaching GHz range
- Recent Trend –
  - Moore's Law is slowing down due to physical and economic limits
  - Scaling beyond 5nm faces challenges like power density, heat, and cost

Evolution of Integration Density (continued)



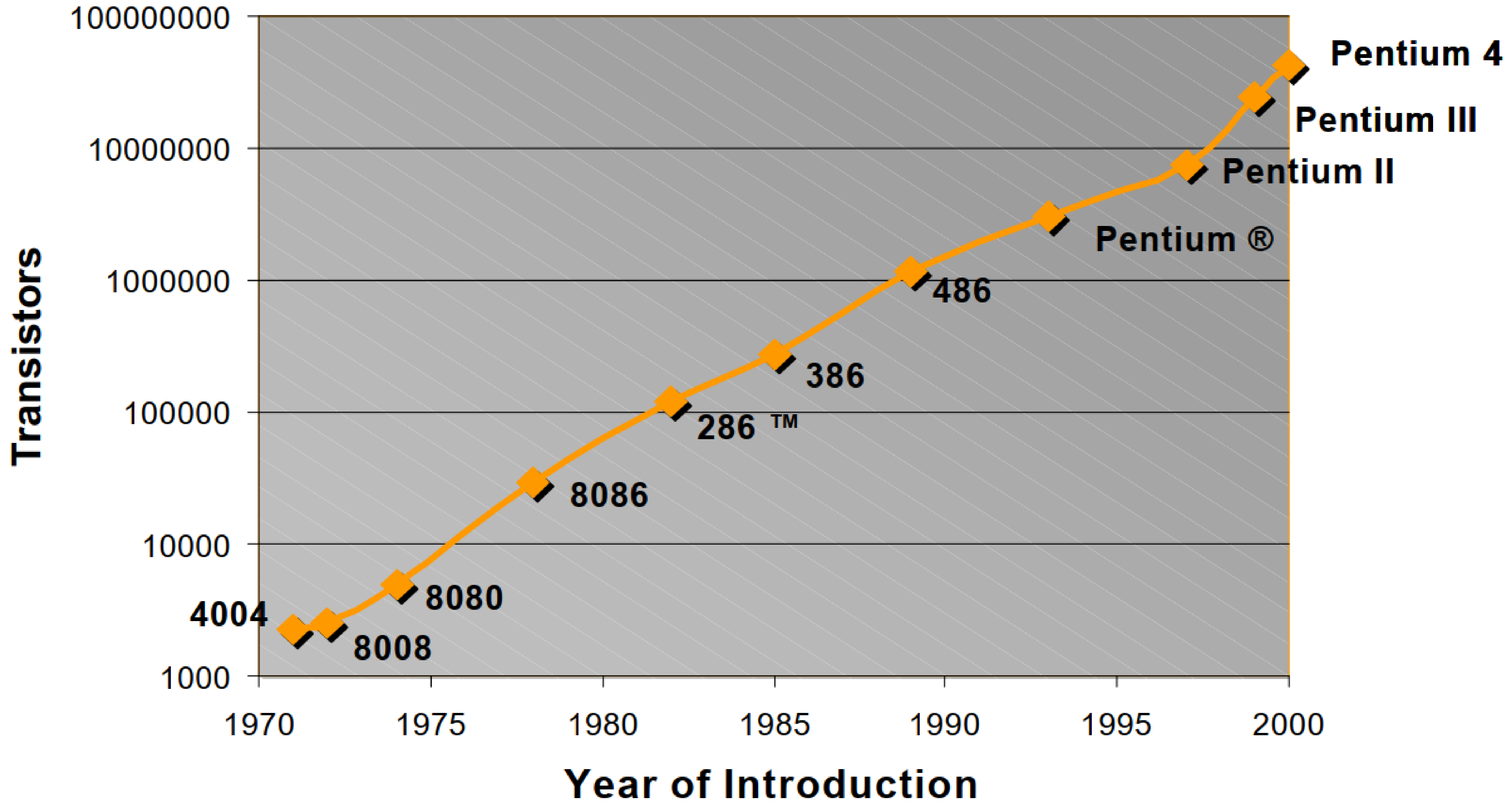


Fig: Evolution of Integration Density of Logic ICs

Design Methodology Shift

Early Designs – Manual Approach

- In the early days of IC design, each transistor was manually laid out and optimized
- Engineers treated each circuit as a custom, handcrafted entity, with full control over geometry and placement
- Example: The Intel 4004 microprocessor (1971) was designed entirely at the transistor level, with immense effort invested into fitting each element into limited silicon area
- This method was time-consuming, error-prone, and non-scalable, especially as transistor counts increased

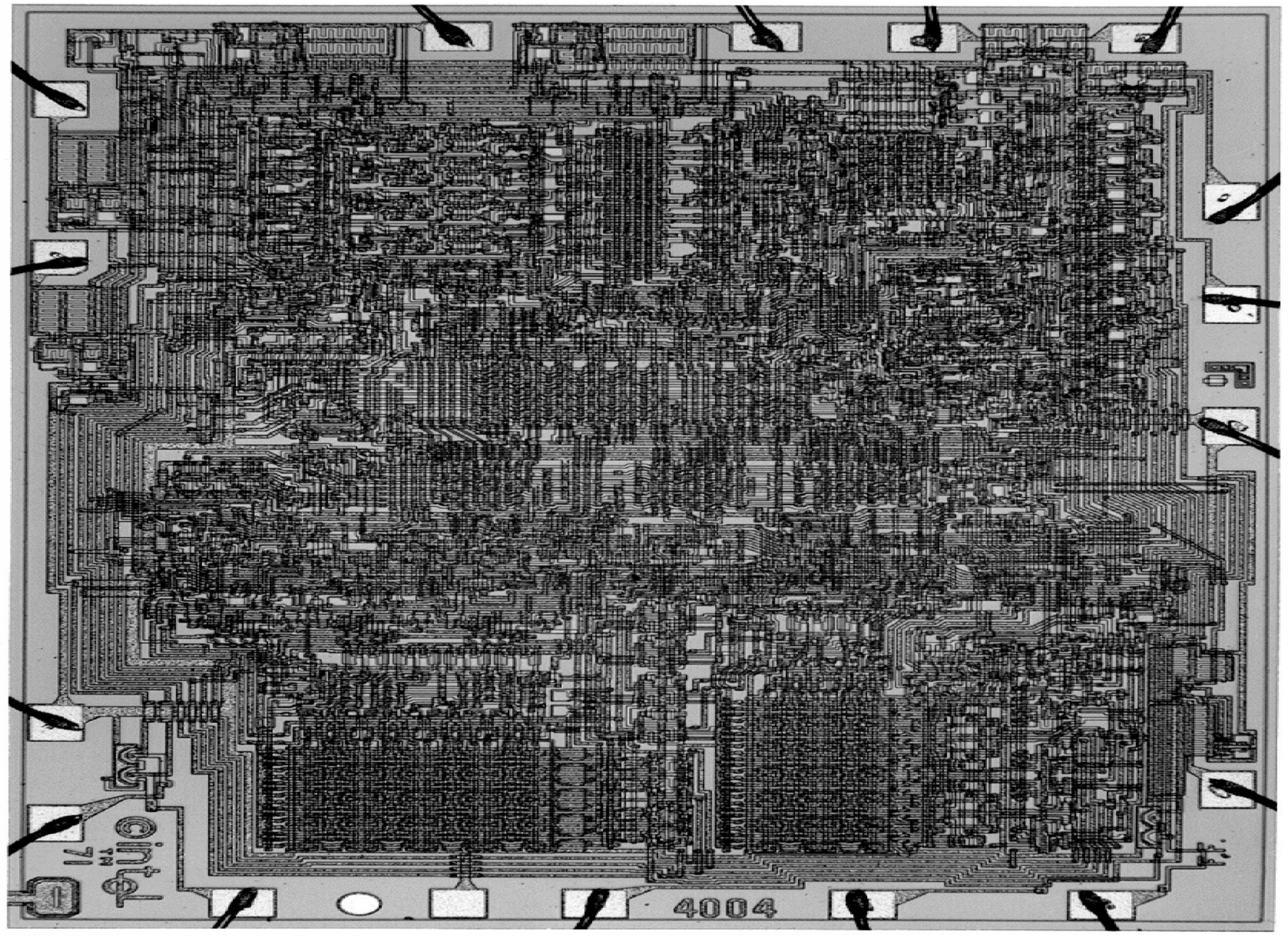


Fig: Intel 4004 microprocessor

Design Methodology Shift (continued)

Modern Designs – Automated Approach

- As integration complexity grew, a manual design approach became impractical
- Modern ICs are designed using a hierarchical methodology –
  - The chip is divided into functional modules (e.g., ALU, memory blocks, I/O controllers)
  - Each module is composed of standard cells like logic gates, flip-flops, multiplexers, etc
  - These cells are reused across the design to reduce effort and ensure consistency

Example: Intel Pentium® 4 (2000)

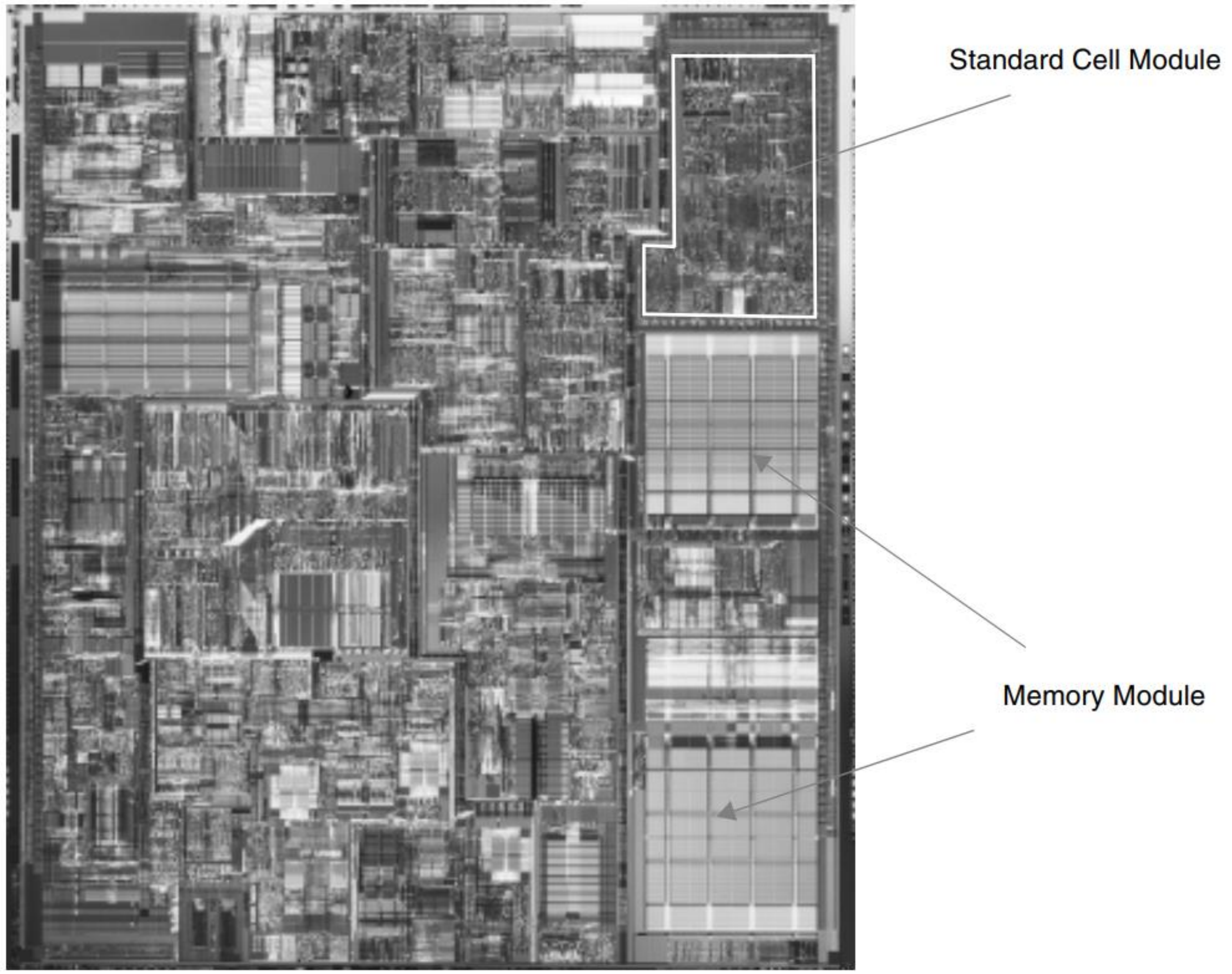


Fig: Intel Pentium® 4 microprocessor

Abstraction in Digital Design

- Abstraction allows designers to hide internal complexities of modules and work with simplified models.
- Once a digital block is implemented, it can be treated as a black box –
  - Only key characteristics (delay, power, functionality) are needed
  - Internal structure doesn’t affect system-level behavior significantly

› This approach reduces design complexity by focusing only on inter-module interaction

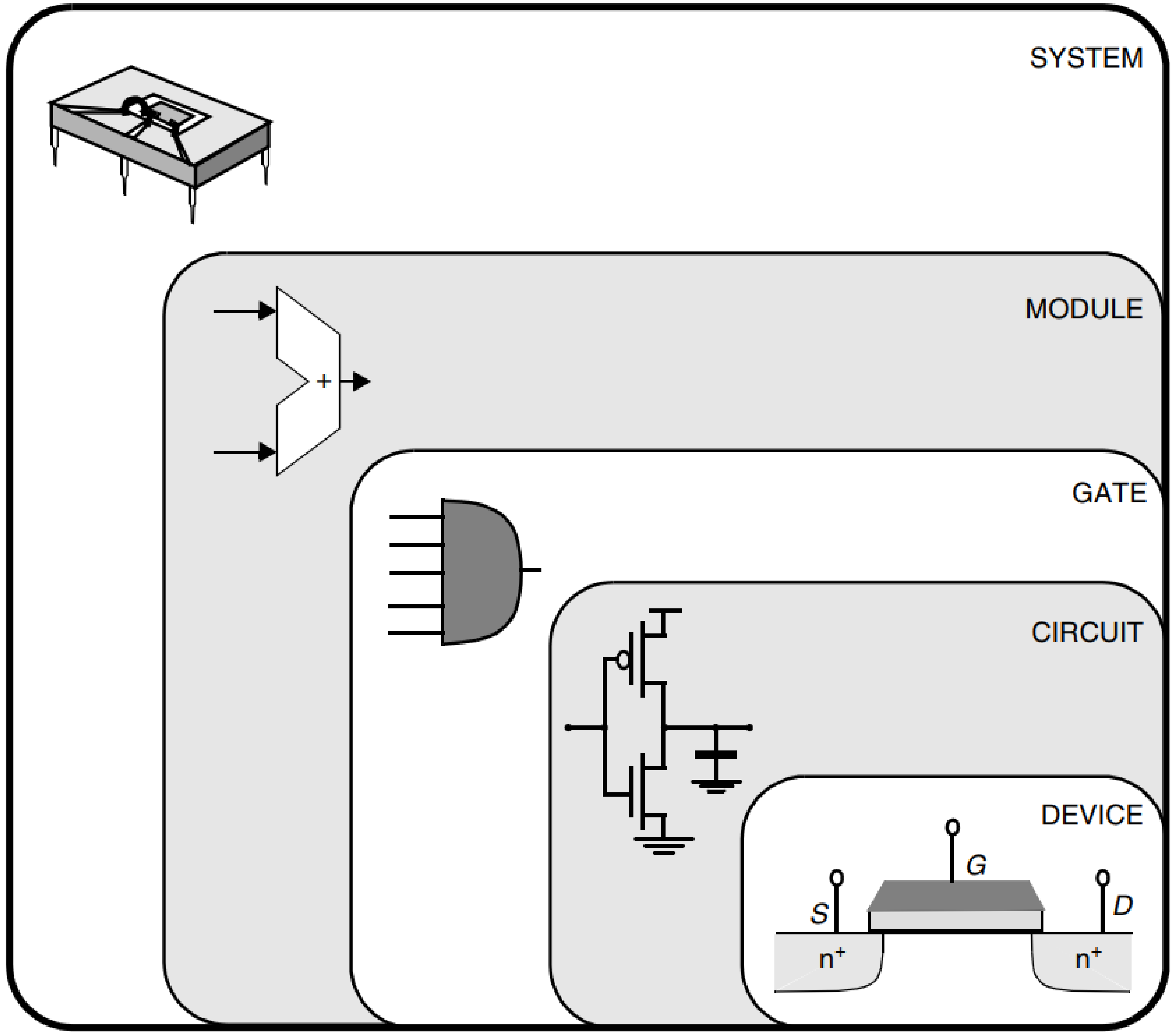


Fig: Design abstraction levels in digital circuits

Course Details

Course Contents

Diode logic gates, Transistor switches, Transistor gates, MOS gates, Logic Families: TTL, ECL, IIL and CMOS logic with operation details, Propagation delay, Product and noise immunity

Electronic circuits for flipflops, Counters and register, Memory systems, PLAs, A/D and D/A converters with applications, S/H circuits, LED, LCD and optically coupled oscillators, Non-linear applications of OP AMPs, Analog switches.

Linear wave shaping: Diode wave shaping techniques, Clipping and Clamping circuits, Comparator circuits, switching circuits, Pulse transformers, Pulse transmission, Pulse generation, Monostable, bistable and astable Multivibrators, Schmitt trigger, Blocking oscillators and time-base circuit, Timing circuits, Simple voltage sweeps, Linear current sweeps.

Course Details (continued)

Suggested Textbooks

- Digital Integrated Electronics by Herbert Taub and Donald Schilling
- Digital Integrated Circuits: A Design Perspective, 2^{nd} edition by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic
- Digital Electronics: Principles, Devices and Applications by Anil K. Maini

Prerequisite Courses

- CSE 4205: Digital Logic Design
- EEE 4383: Electronic Devices and Circuits