EEE 4483

Digital Electronics and Pulse Techniques

Lecture 1: Review of Electronic Devices

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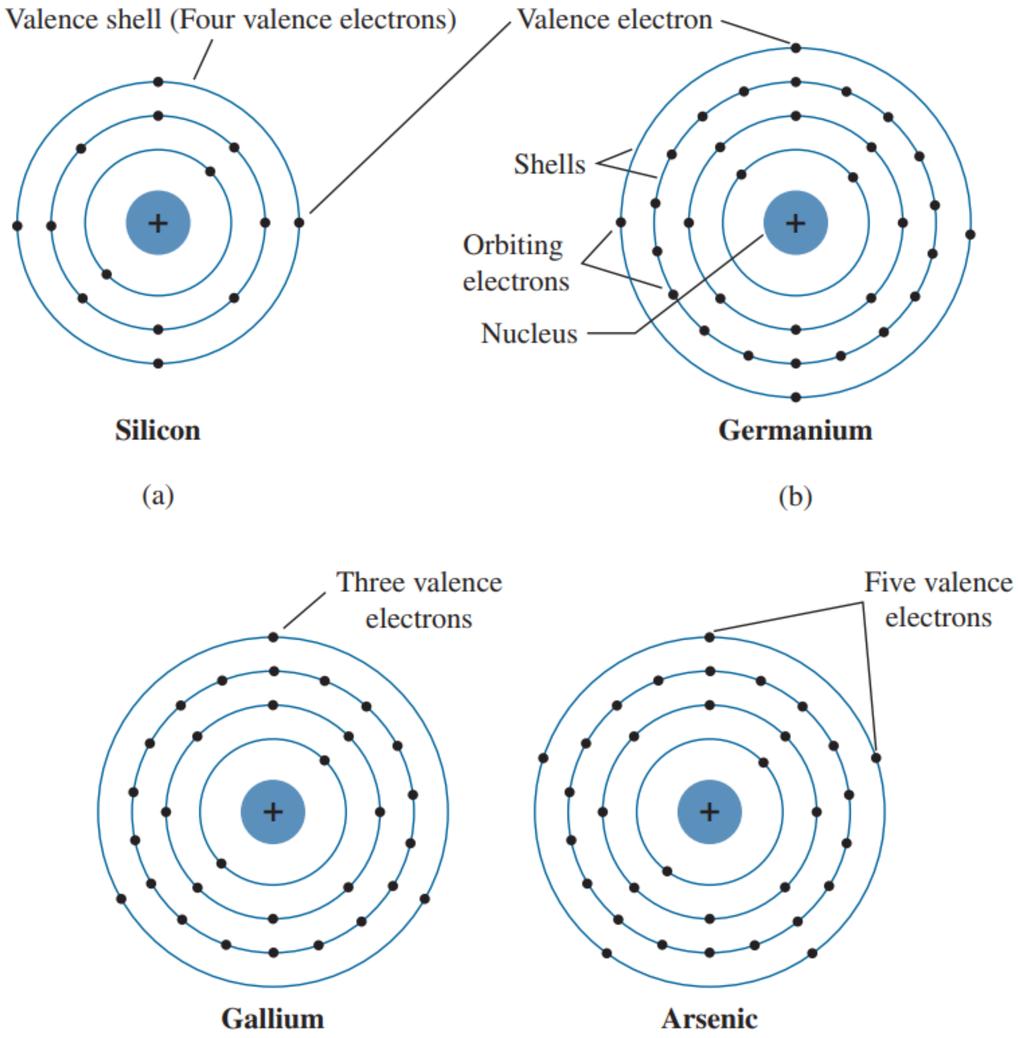
Referred Textbook:

Electronic Devices and Circuit Theory, 11th edition
by Robert L. Boylestad and Louis Nashelsky

Microelectronic Circuits, 6th edition
by Adel S. Sedra and Kenneth C. Smith

Microelectronics: Circuit Analysis and Design, 4th edition
by Donald A. Neamen

Semiconductor Basics



- Semiconductors are a special class of elements having a conductivity between that of a good conductor and that of an insulator
- At room temperature or when heated, some valence electrons gain enough energy to jump across the bandgap into the conduction band
- These free electrons in the conduction band, and the holes left behind in the valence band, enable current flow — acting like a conductor
  - Intrinsic Semiconductor: Highly pure form (very low impurity levels)
  - Intrinsic Carriers: Electrons/holes generated only by thermal energy

Doping: n-Type and p-Type Materials

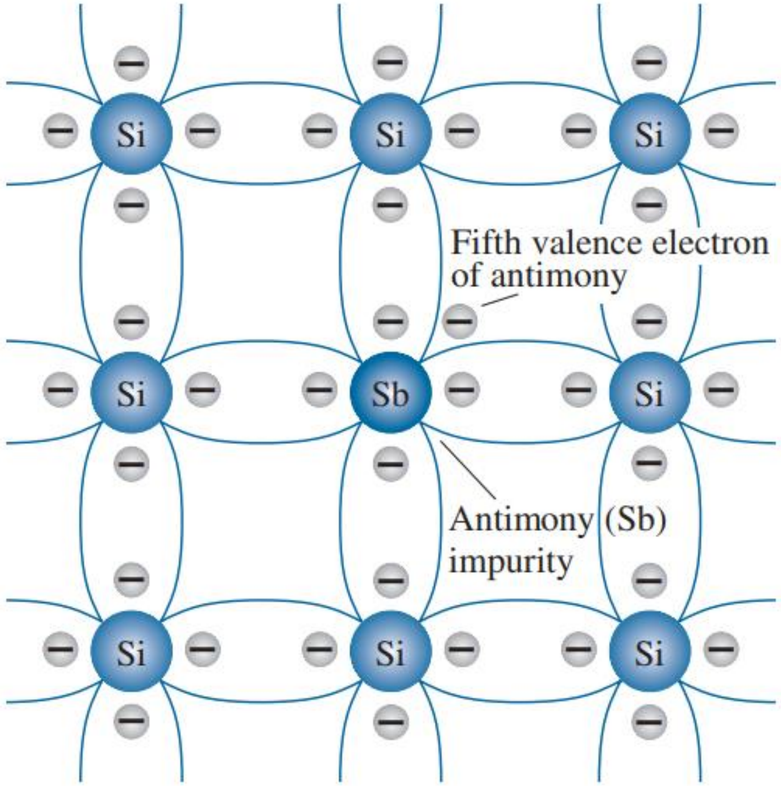


Fig: Antimony impurity in n-type material

n-Type Materials

- Formed by doping pure semiconductor with Group V elements (e.g., P, As, Sb) that have five valence electrons
- Each dopant forms four covalent bonds, leaving one free electron that is loosely bound and easily moves
- These pentavalent atoms are called donor atoms because they donate free electrons to the conduction band
- The free electrons are the majority carriers, enabling high conductivity in n-type material

Doping: n-Type and p-Type Materials (continued)

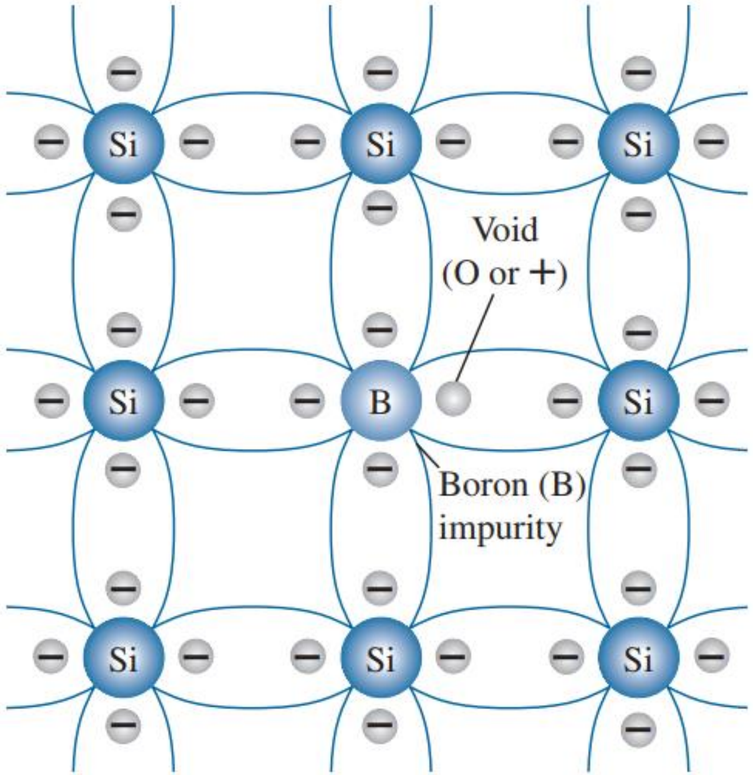


Fig: Boron impurity in p-type material

p-Type Materials

- Formed by doping pure semiconductor with Group III elements (e.g., B, Al, Ga) that have three valence electrons
- Each dopant forms three covalent bonds, leaving one bond incomplete, creating a hole
- These trivalent atoms are called acceptor atoms because they accept electrons to fill the missing bond
- The holes are the majority carriers, enabling high conductivity in p-type material

Minority Carriers in Doped Semiconductors

- In n-type material –
  - Doping adds many electrons (via donor atoms), making electrons the majority carriers.
  - Thermal generation still creates electron-hole pairs → holes are present but in very small numbers → minority carriers.
  - Majority carriers (electrons) = Electrons from donor atoms (doping) + electrons from thermal generation

- In p-type material –
  - Doping adds many holes (via acceptor atoms), making holes the majority carriers.
  - Thermal generation still creates electron-hole pairs → electrons are present in small numbers → minority carriers.
  - Majority carriers (holes) = Holes from acceptor atoms (doping) + Holes from thermal generation

Minority Carriers in Doped Semiconductors (continued)

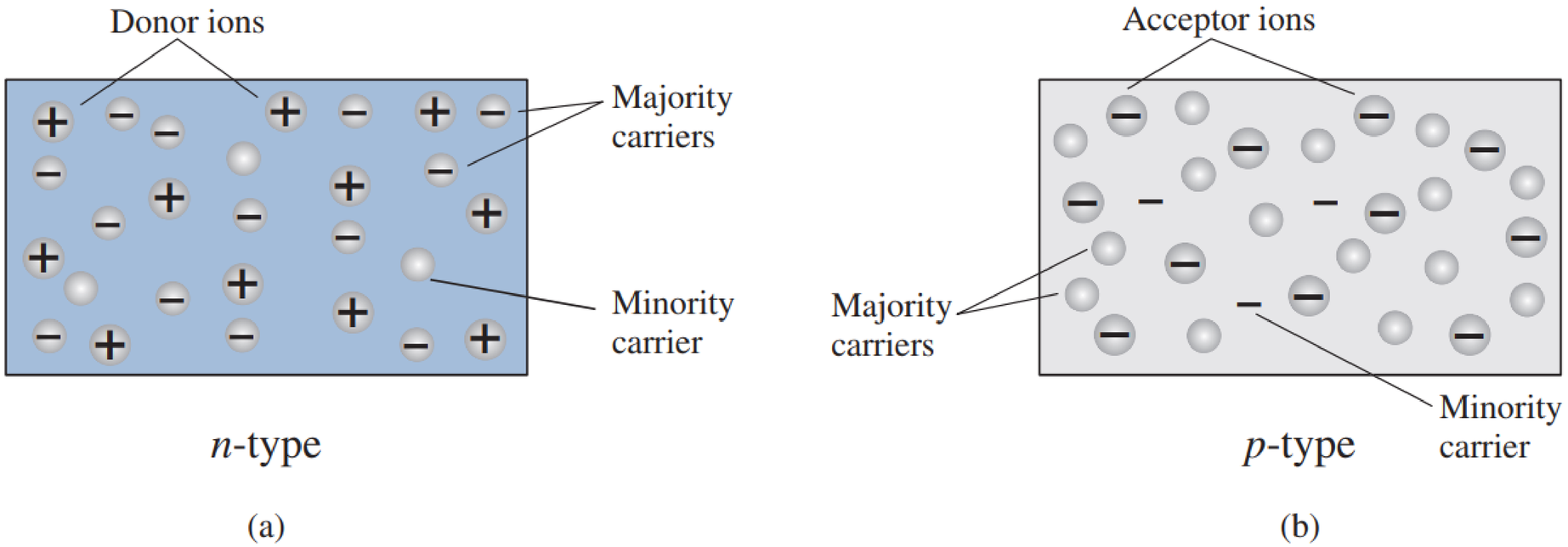


Fig: (a) n-type material, (b) p-type material

Semiconductor Diode

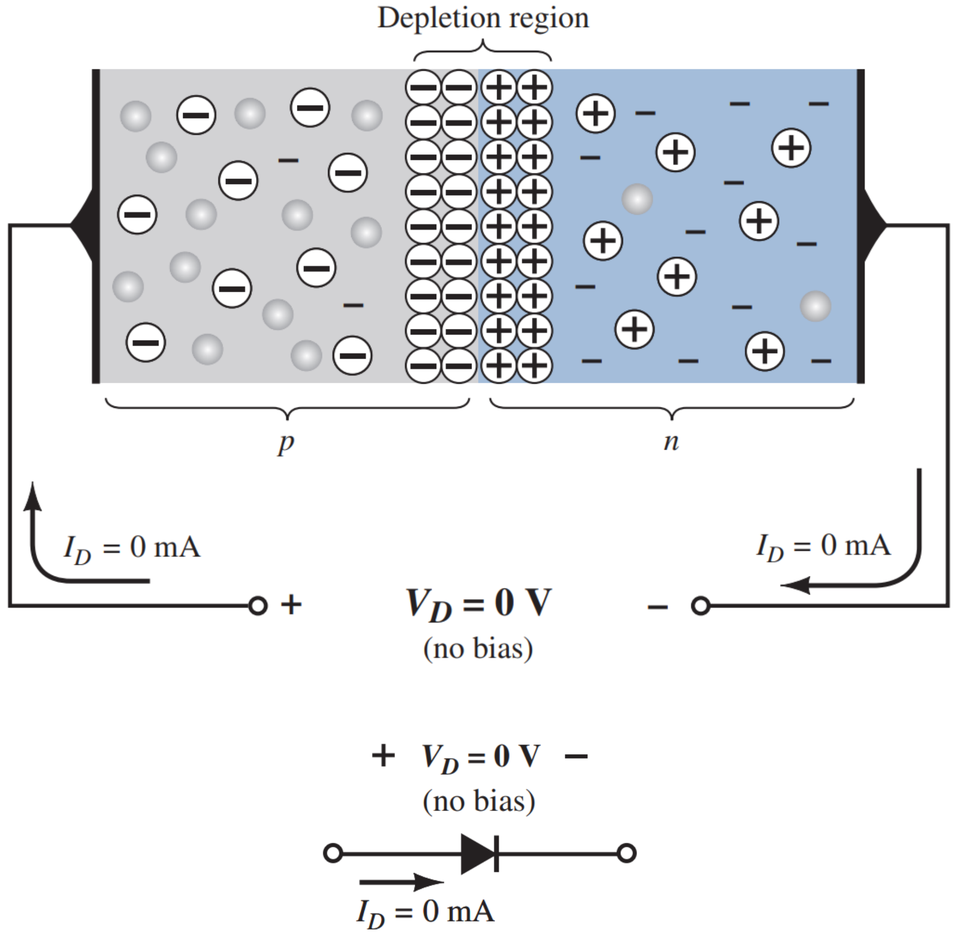


Fig: A p–n junction with no external bias

No Applied Bias (Voltage = 0 V)

- When p-type and n-type materials join, electrons diffuse from n to p, and holes from p to n, due to carrier concentration differences
- This diffusion causes recombination near the junction, depleting free carriers
- Left behind: immobile ions (negative on p-side, positive on n-side)
- An electric field builds up → opposes further diffusion
- System reaches equilibrium when –

diffusion current = drift current

Semiconductor Diode (continued)

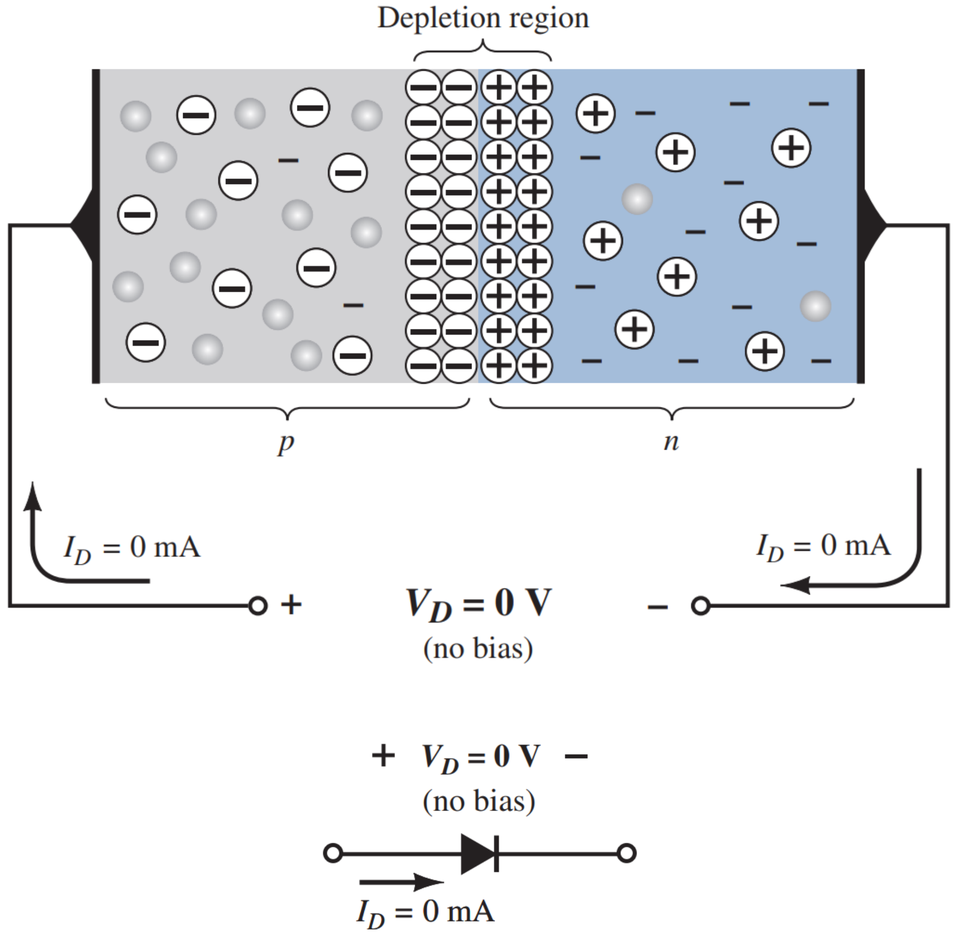


Fig: A p–n junction with no external bias

- Diffusion Current
  - Caused by concentration gradient of majority carriers
  - Electrons move from high (n-side) to low (p-side) concentration
  - Holes move from p-side → n-side
  - This movement creates current from carrier movement
- Drift Current
  - Caused by electric field in the depletion region
  - The field pushes electrons toward n-side, and holes toward p-side (acts on minority carriers)
  - It opposes the direction of diffusion

Semiconductor Diode (continued)

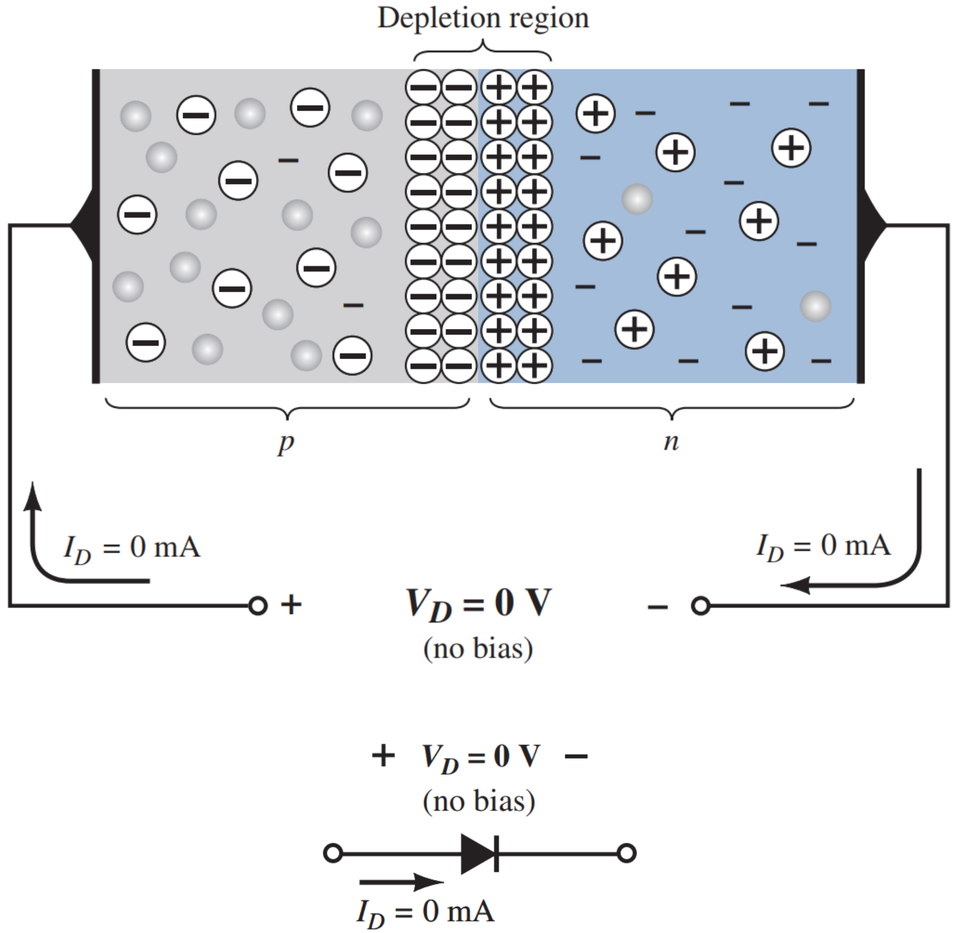


Fig: A p–n junction with no external bias

- At Equilibrium
  - As more carriers diffuse, the electric field gets stronger
  - Eventually, this field is strong enough to pull back carriers
  - Eventually, the drift current (caused by this electric field acting on minority carriers) exactly balances the diffusion current (from majority carriers)
  - Although electrons and holes are constantly moving, the opposing flows cancel each other
  - Result: No net current

Semiconductor Diode (continued)

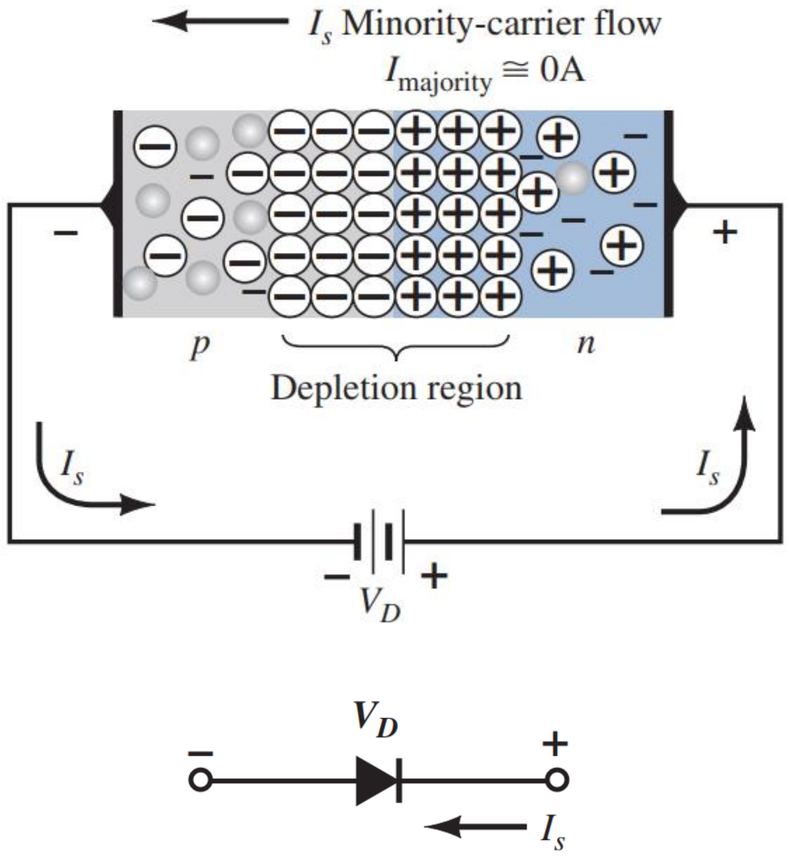


Fig: Reverse-biased p–n junction

Reverse-Bias Condition ($V_D < 0$ V)

- Positive terminal connected to n-type, negative to p-type
- Electrons pulled toward the positive terminal
- Holes pulled toward the negative terminal

→ Depletion region widens

- Majority Carrier Flow Stops
  - Barrier becomes too wide
  - Majority carriers cannot cross → flow ≈ 0
- Minority Carrier Flow Continues
  - Minority carriers still drift across the junction
  - Results in a small reverse current, called reverse saturation current (I_s)

Semiconductor Diode (continued)

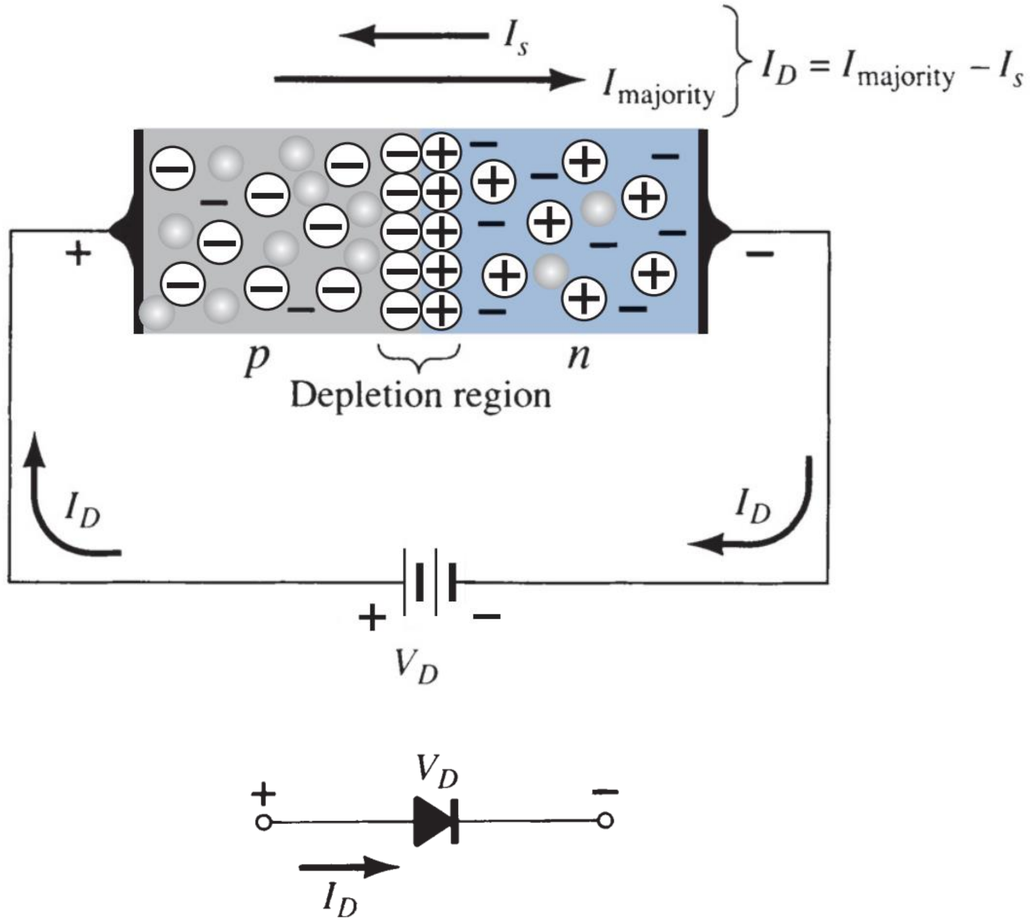


Fig: Forward-biased p–n junction

Forward-Bias Condition ($V_D > 0$ V)

- Positive terminal connected to p-type, negative to n-type
- This pushes electrons from n-side and holes from p-side toward the junction

- Depletion Region Narrows
  - Electrons and holes recombine with ions at the junction
  - Barrier height reduces, making it easier for majority carriers to cross

Semiconductor Diode (continued)

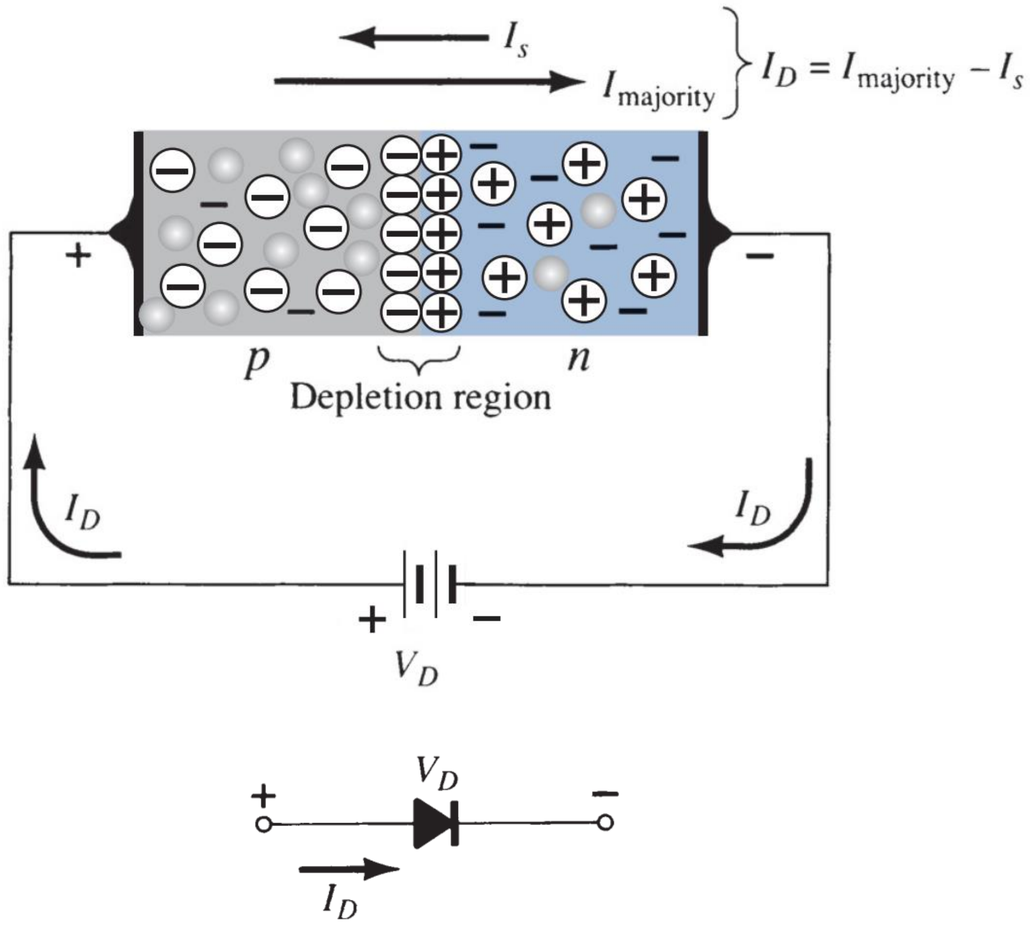


Fig: Forward-biased p–n junction

- Majority Carrier Flow Increases
  - Majority carriers now easily cross the junction
  - Large current flow begins
  - Minority carrier flow remains constant
- Exponential Current Increase
  - As forward voltage increases, depletion width shrinks more
  - Results in exponential rise in current after threshold (knee voltage/cut-in voltage)

Semiconductor Diode (continued)

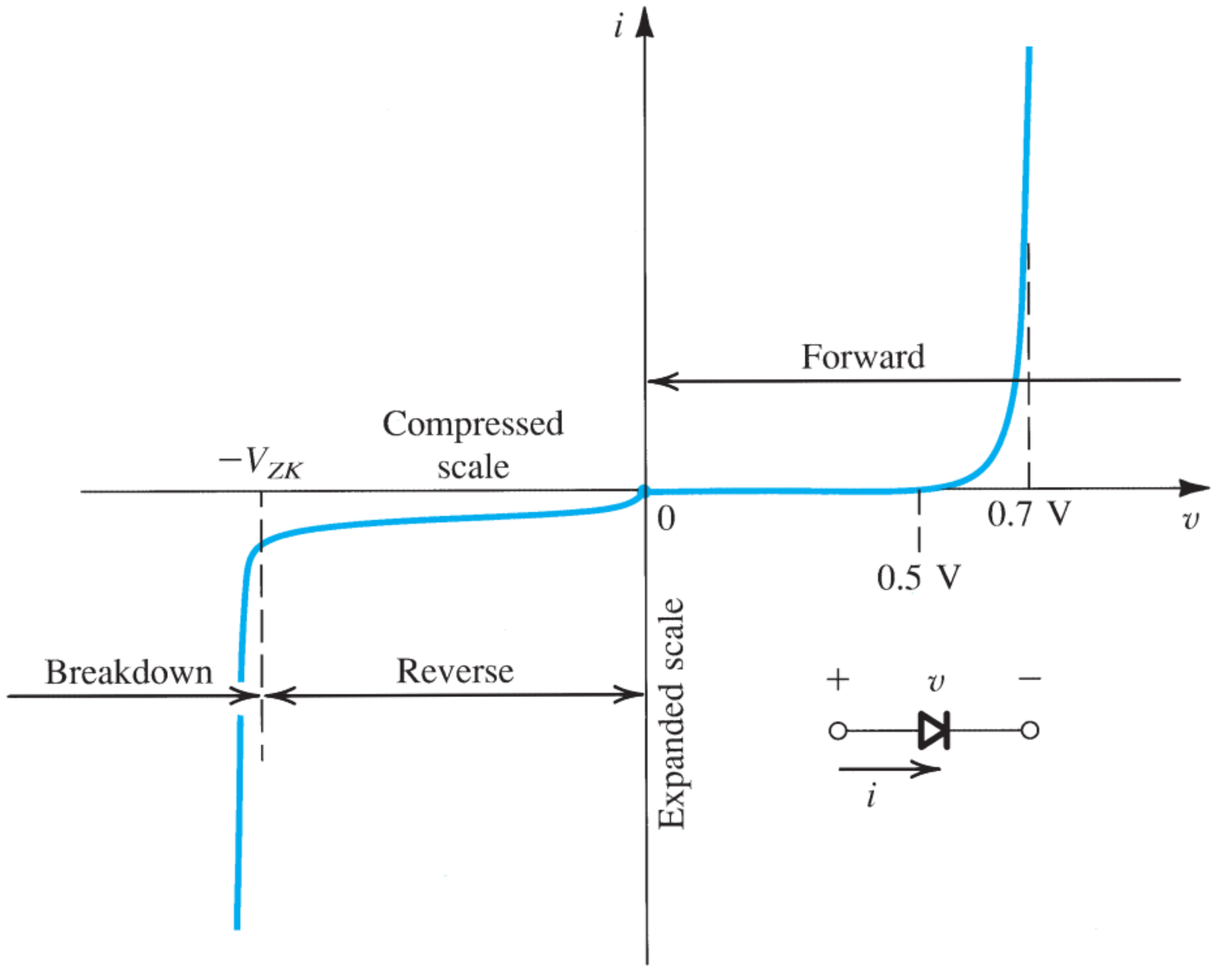


Fig: I-V characteristics of diode

Shockley's Diode Equation

The current through a diode is given by the Shockley equation –

$$I_D = I_S\left(e^{V_D/nV_T} - 1\right)$$

Where,

I_D = Diode current

I_S = Reverse saturation current

V_D = Applied forward-bias voltage

n = Ideality factor (typically $1 - 2$)

V_T = Thermal voltage = $\frac{kT}{q}$

k = Boltzmann's constant = $1.38 \times 10^{-23}\ J/K$

T = Absolute temperature in kelvin = $273 +\ ^\circ C$

q = Charge of an electron = $1.6 \times 10^{-19} C$

Diode Models

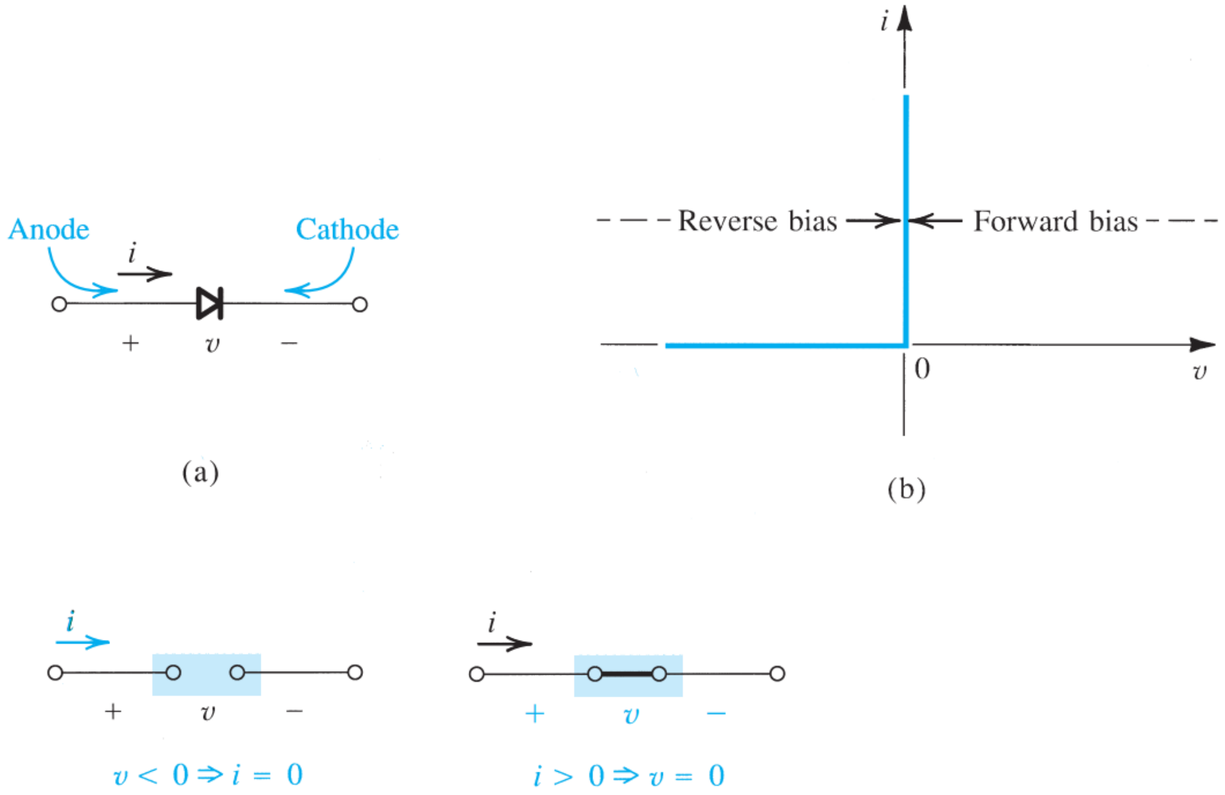


Fig: Ideal diode model

The Ideal Model

- Forward Bias (ON State)
  - Diode acts as a perfect conductor
  - Voltage drop across diode: $V_D = 0\ \text{V}$
  - Current flows freely: $I_D > 0$
- Reverse Bias (OFF State)
  - Diode acts as a perfect insulator
  - No current flow: $I_D = 0$, regardless of reverse voltage

This model is best for basic switching behavior and introductory analysis

Diode Models (continued)

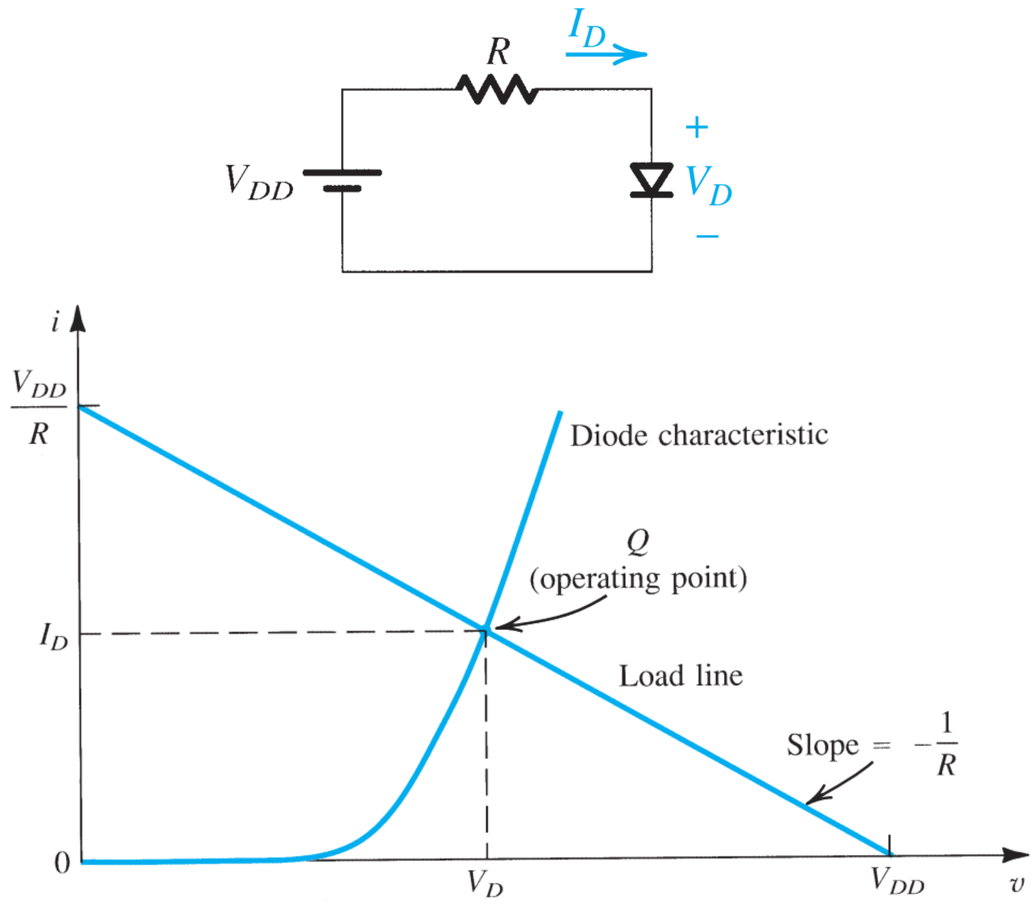


Fig: Exponential model of diode

The Exponential Model

Shockley's Diode Eqn. (approximated) –

$$I_D = I_S\, e^{V_D/V_T}$$

- Diode model is generated by following this equation
- Most accurate model for diode behavior
- Highly nonlinear, making it difficult to solve analytically

Diode Models (continued)

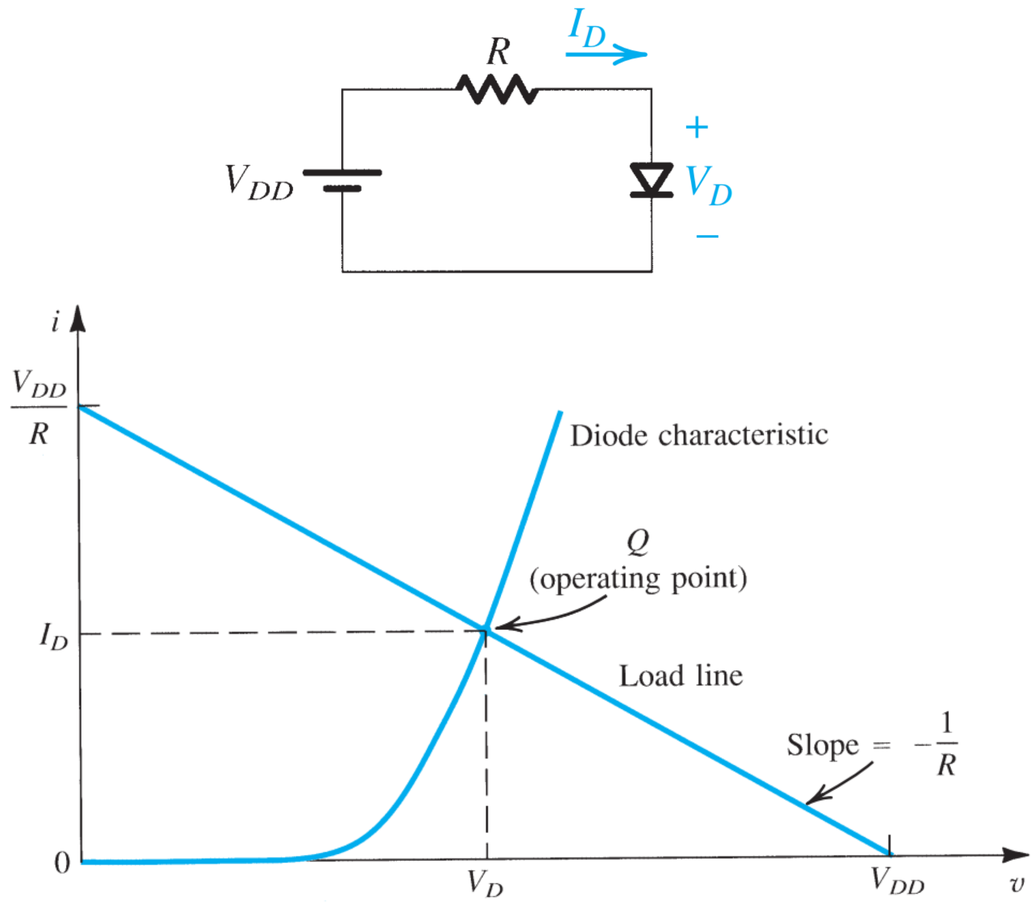


Fig: Exponential model of diode

The Exponential Model

Step 1: Circuit Analysis

- Using KVL in the circuit at the top –

$$I_D = \frac{V_{DD} - V_D}{R}$$

- Now we have two equations –

  Diode equation: $I_D = I_S\, e^{V_D/V_T}$

  Load line equation: $I_D = \frac{V_{DD} - V_D}{R}$

- Two unknowns: I_D and V_D

Diode Models (continued)

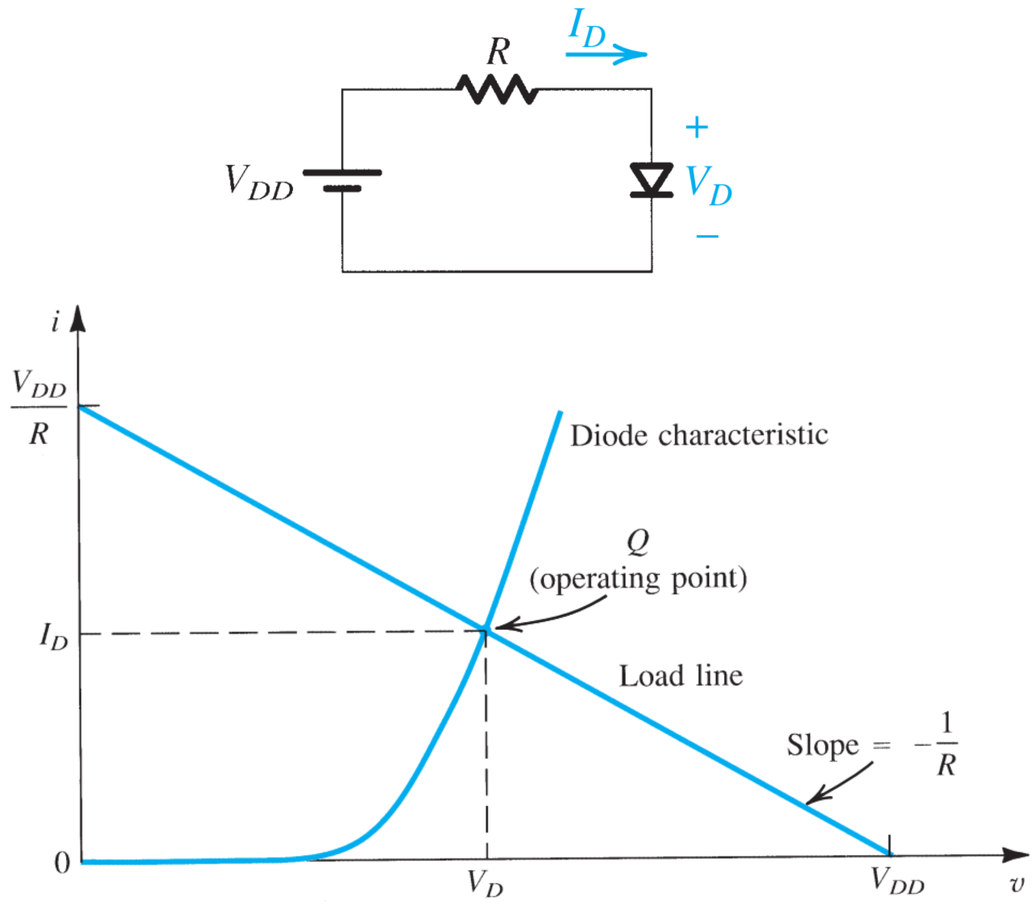


Fig: Exponential model of diode

The Exponential Model

Step 2: Graphical Analysis

- Plot both equations on the I-V plane –

  Exponential Curve → Diode equation

  Straight Line → Load line

- Operating Point (Q-point) is the intersection of the two curves
- Q-point gives actual values of I_D and V_D

Diode Models (continued)

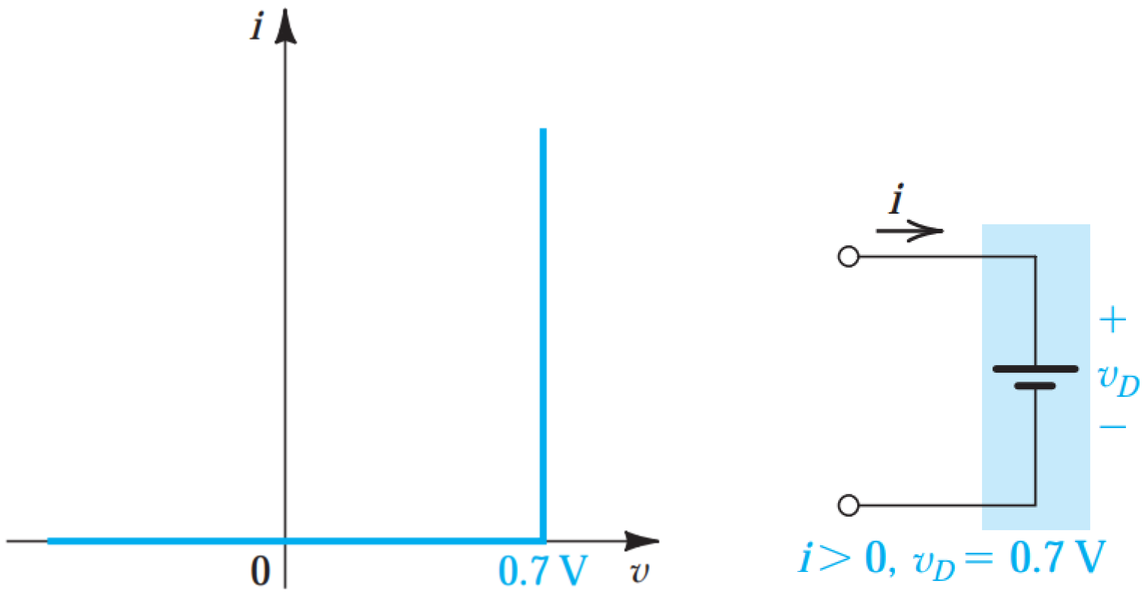


Fig: Constant-Voltage-Drop model of diode

The Constant-Voltage-Drop Model

- Assumes a fixed voltage drop across a forward-biased diode –

$$V_D \approx 0.7 \text{ V} \text{ (for Silicon)}$$

- Based on practical observation –
  - Actual forward voltage ranges from 0.6 V to 0.8 V
  - Simplified to a constant value for ease of analysis

Diode Models (continued)

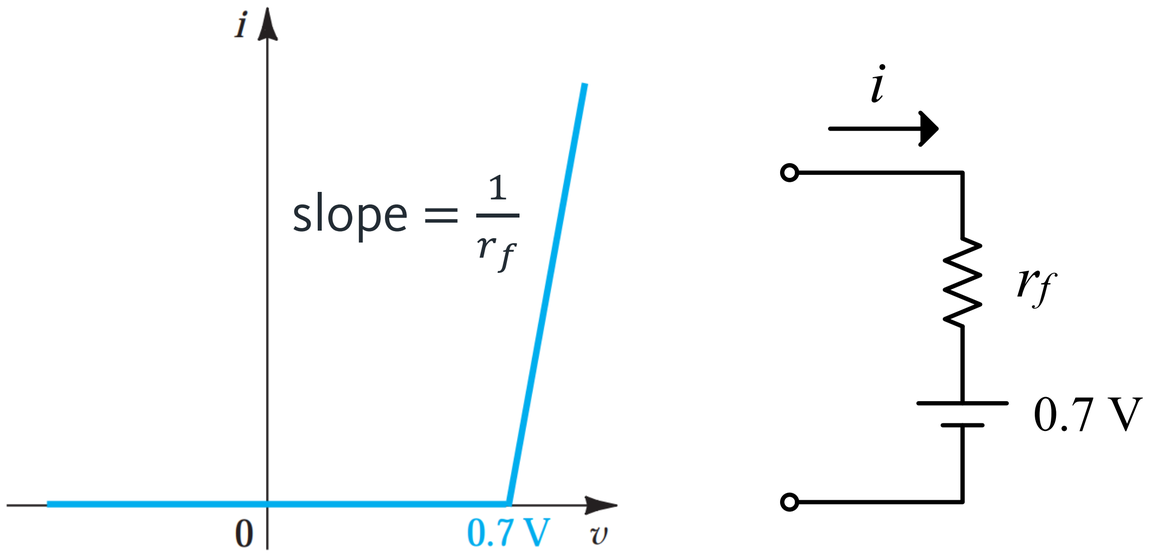


Fig: Piecewise Linear model of diode

Piecewise Linear Model

Improves upon the constant-voltage-drop model by adding a small forward resistance.

Diode is modeled as –

$$V_D = 0.7 + I_D \cdot r_f \quad \text{(for silicon)}$$

Here, r_f is small resistance when the diode is ON (typically a few ohms)

Bipolar Junction Transistor (BJT)

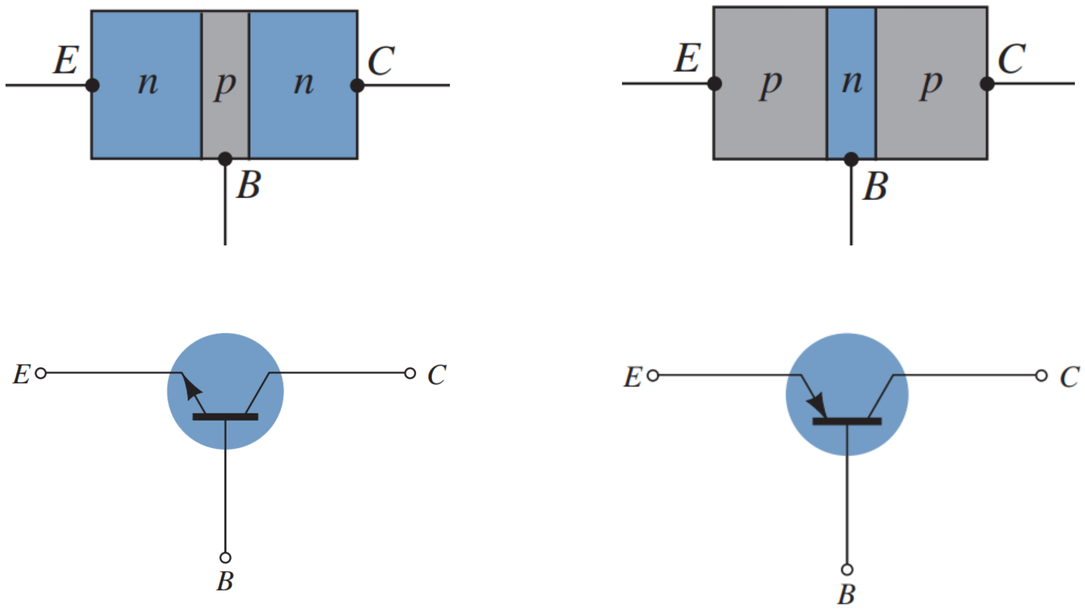
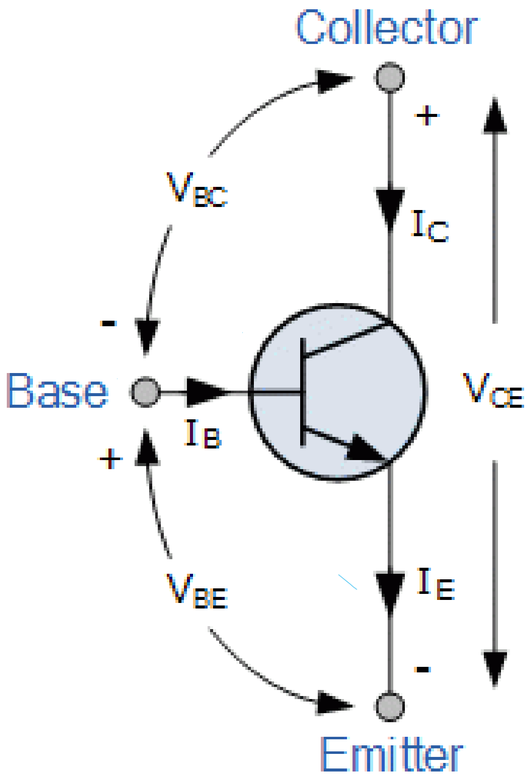


Fig: NPN and PNP Transistor

- A current-controlled semiconductor device → A small base current I_B controls a much larger collector current I_C
- Has three terminals – Emitter (E), Base (B) and Collector (C)
- Comes in two types – NPN and PNP
- Two main application – Amplification and Switching

**Why is it called “bipolar”?

BJT: Modes of Operation

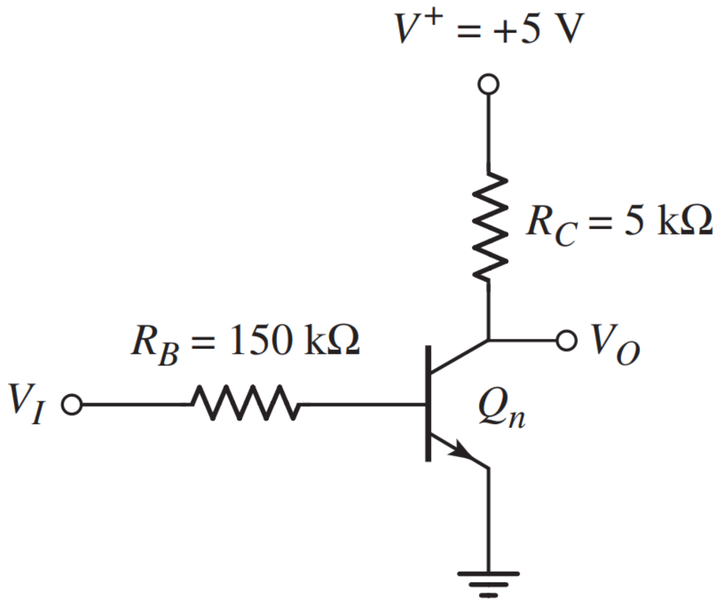


Modes	EB Junction	CB Junction	Application
Cutoff	Reverse	Reverse	Switching
Saturation	Forward	Forward	
Active	Forward	Reverse	Amplifier
Inverse-active	Reverse	Forward	??

Current Relationships	Voltage Relationships	
	Active Mode	Saturation Mode
$I_E = I_B + I_C$ $I_C = \beta I_B$ β = current gain (typically 20-200)	$V_{BE} \approx 0.7$ V $V_{CE} > V_{BE}$	$V_{BE} \approx 0.7$ V $V_{CE} \approx 0.2$ V

Voltage Transfer Characteristics of BJT

Objective: Develop the voltage transfer curves for the circuits shown in the figure below. Assume npn transistor parameters of $V_{BE}(\text{on}) = 0.7\ \text{V},\ \beta = 120,\ V_{CE}(\text{on}) = 0.2\ \text{V}$ (Neamen, Page 311)



Solution:

- For $V_I \leq 0.7$ V :

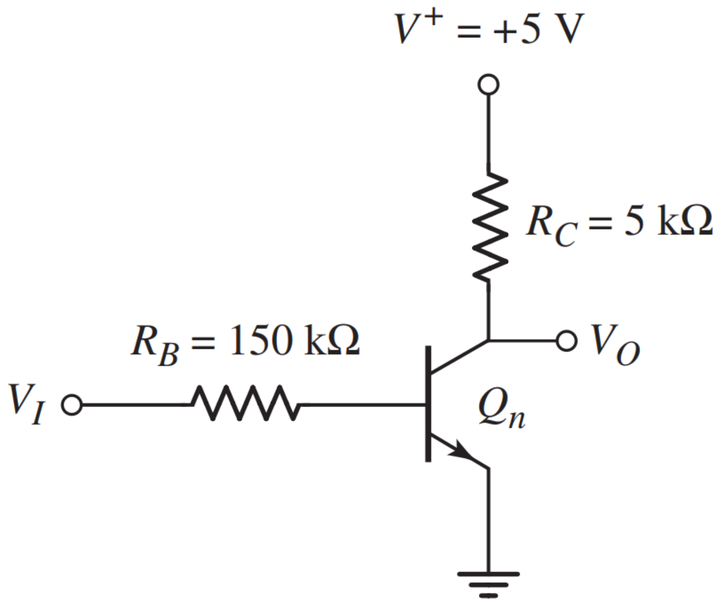
  Transistor Q_n is cut off, so that $I_B = I_C = 0$. The output voltage is then $V_O = V^+ = 5$ V.

- For $V_I > 0.7$ V :

  Transistor Q_n turns on and is initially biased in the active mode. We have –

$$I_B = \frac{V_I - 0.7}{R_B}$$

Voltage Transfer Characteristics of BJT (continued)



- For $V_I > 0.7$ V :

  Transistor Q_n turns on and is initially biased in the active mode. We have –

$$I_B = \frac{V_I - 0.7}{R_B}$$

  And,

$$I_C = \beta I_B = \frac{\beta(V_I - 0.7)}{R_B}$$

  Then,

$$V_O = 5 - I_C R_C = 5 - \frac{\beta(V_I - 0.7)R_C}{R_B}$$

  This equation is valid for $0.2 \leq V_O \leq 5$ V. When $V_O = 0.2$ V, the transistor Q_n goes into saturation.

Voltage Transfer Characteristics of BJT (continued)

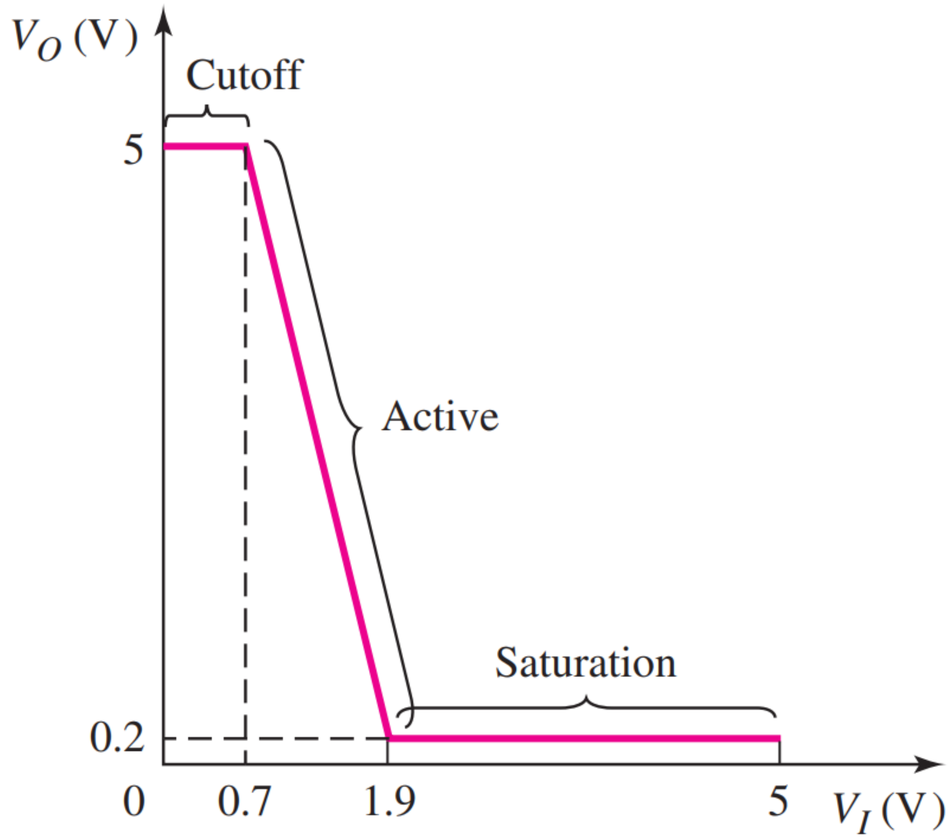


Fig: Voltage transfer characteristics

- For $V_O = 0.2\ \text{V}$:

  When $V_O = 0.2\ \text{V}$, transistor Q_n goes into saturation. When $V_O = 0.2\ \text{V}$, the input voltage is found from –

$$0.2 = 5 - \frac{(120)(V_I - 0.7)(5)}{150}$$

  Which yields $V_I = 1.9\ \text{V}$. For $V_I \geq 1.9\ \text{V}$, the transistor Q_n remains biased in the saturation region.

  The voltage transfer curve is shown in the left Figure.

Field Effect Transistor (FET)

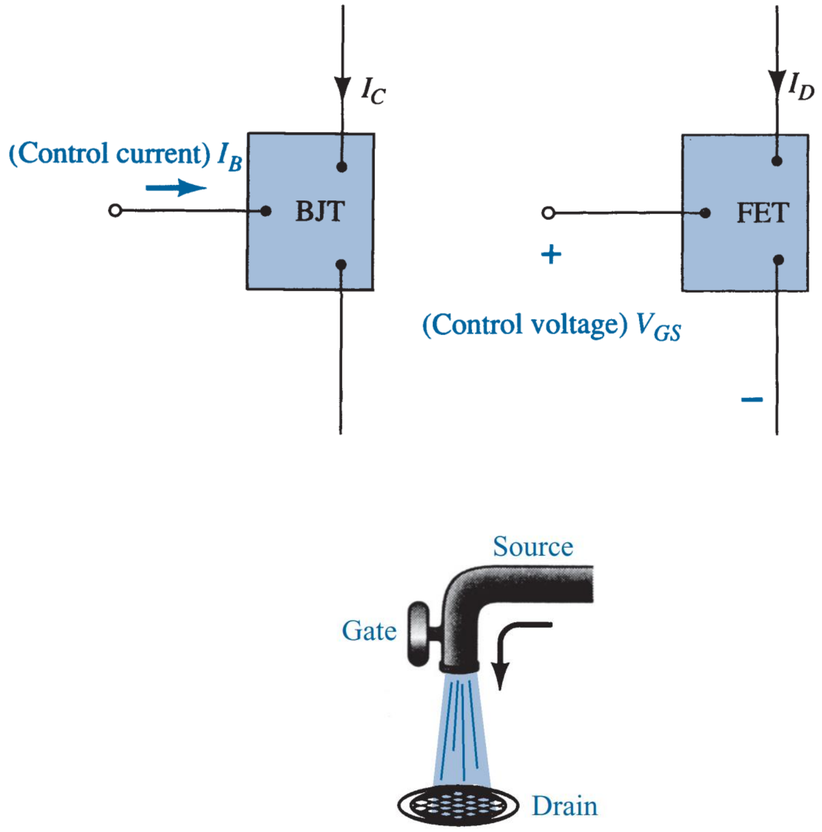


Fig: Field Effect Transistor

Field Effect Transistor (FET) is a three-terminal, voltage-controlled device. FET is comparable to BJTs but differs in control mechanism and carrier type.

Key Differences between FET and BJT –

Feature	BJT	FET
Control Type	Current-controlled	Voltage-controlled
Conduction	Bipolar	Unipolar
Input Impedance	Low	Very high (MΩ range)
Voltage Gain	High	Lower than BJT
Temp. Stability	Less stable	More stable

MOSFETs

There are two main types of FETs: JFET and MOSFET.

In this course, we will focus on MOSFET, as it is widely used in digital logic gates (specifically enhancement-type MOSFETs).

MOSFET → Metal-Oxide-Semiconductor Field-Effect Transistor

- Metal-Oxide Refers to the gate structure, which consists of a metal layer separated from the semiconductor by an insulating oxide layer, typically silicon dioxide.
- Field-Effect describes how the device controls current using an electric field created by the gate voltage, rather than current injection.

Enhancement-type MOSFET

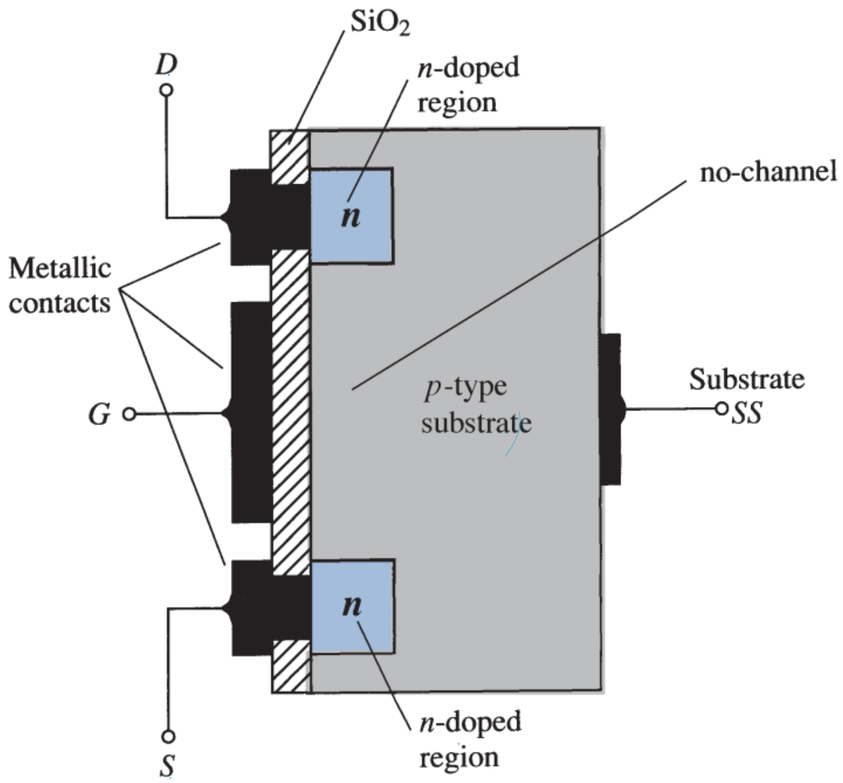


Fig: n-channel enhancement-type MOSFET

- In the left figure: n-channel enhancement-type MOSFET
- Built on a p-type silicon substrate
- Source (S) and Drain (D) formed by n-type material
- Gate (G) is insulated from the substrate by a thin SiO_2 layer
- No physical conducting channel between source and drain at zero gate voltage
- Control of conduction is achieved electrically via gate voltage

Enhancement-type MOSFET (continued)

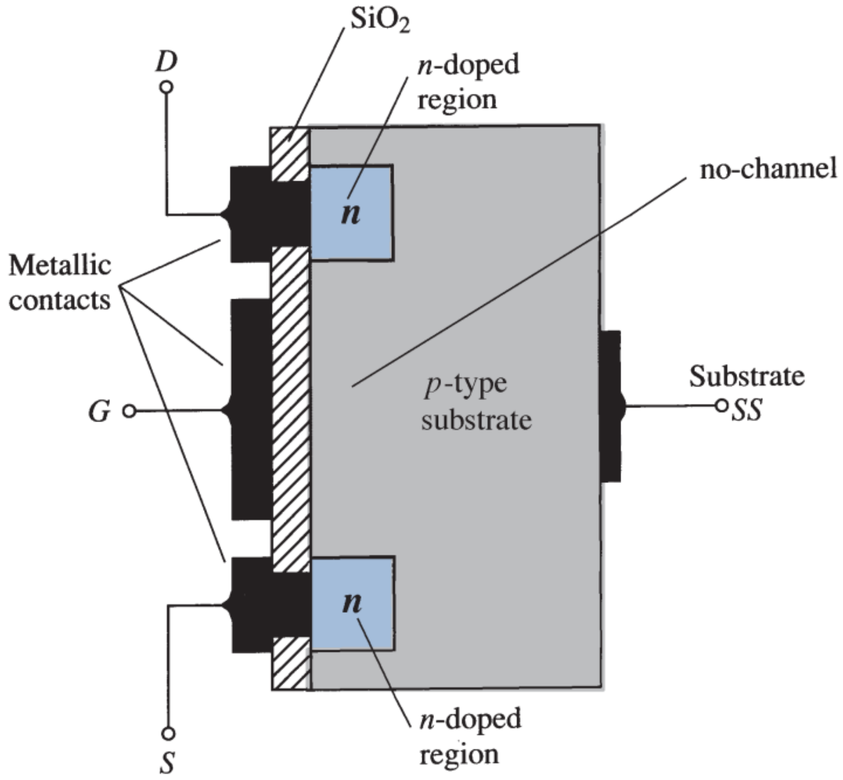


Fig: n-channel enhancement-type MOSFET

Key Construction Features

- Substrate:
  - May be internally connected to Source, or
  - Externally connected via a fourth terminal (often labeled SS or Body)
- In contrast to depletion-mode MOSFET:
  - No channel is pre-built
  - A channel must be induced by applying a suitable V_{GS}
- SiO_2 insulates Gate from underlying semiconductor → extremely high input impedance

Enhancement-type MOSFET

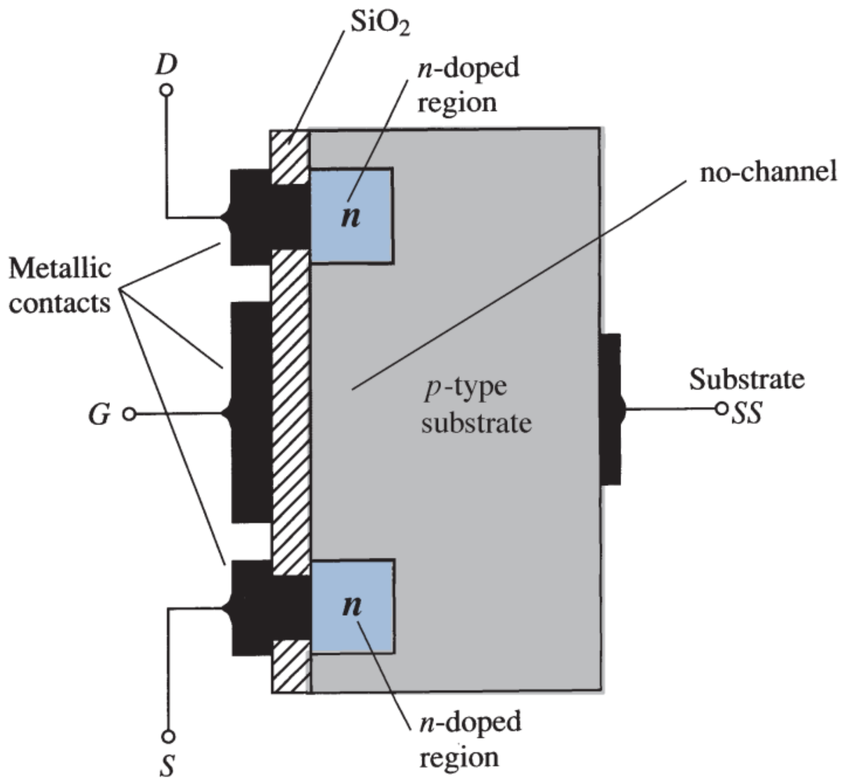


Fig: n-channel enhancement-type MOSFET

Behavior at $V_{GS} = 0$ V

- Apply a positive V_{DS}, but with $V_{GS} = 0$ V:
  - No channel ⟶ $I_D \approx 0$ A
- Electrons exist in n-doped Source and Drain region, but:
  - No conduction path due to absence of channel
  - Two reverse-biased p–n junctions block current flow

Enhancement-type MOSFET

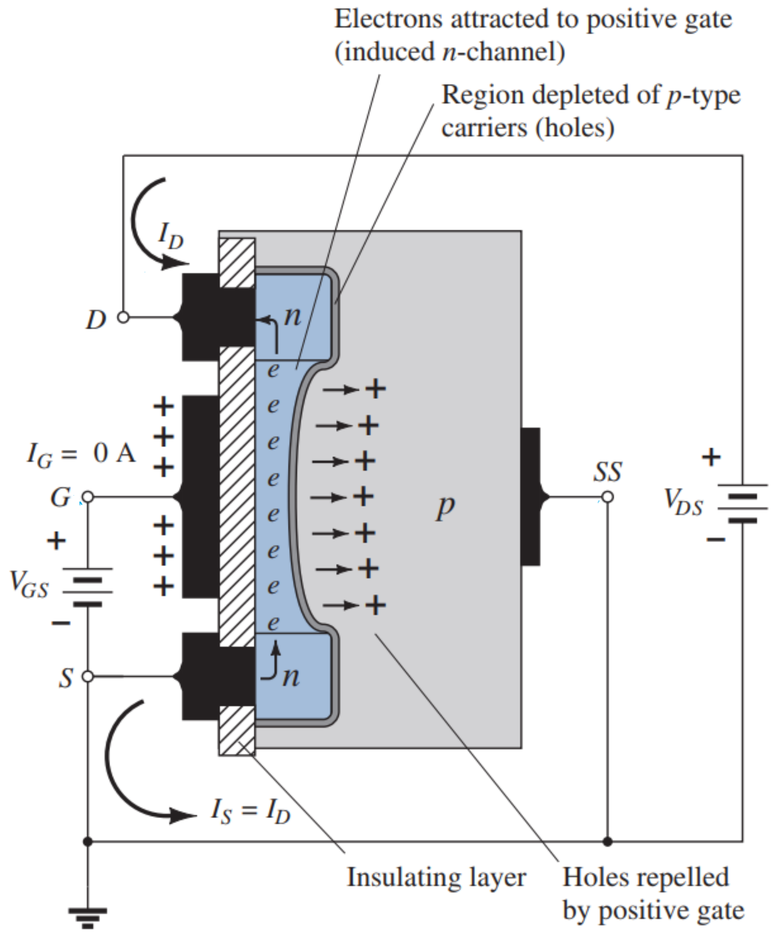


Fig: n-channel enhancement-type MOSFET

Behavior at $V_{GS} > 0$ V

- When $V_{GS} > 0$:
  - Positive gate voltage repels holes (majority carriers) along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p-substrate
  - Electrons are attracted and (minority carriers) accumulated near gate
  - An inversion layer (n-channel) forms, enabling conduction
  - Threshold Voltage (V_T or $V_{GS(th)}$): Minimum gate voltage to form a channel

Enhancement-type MOSFET

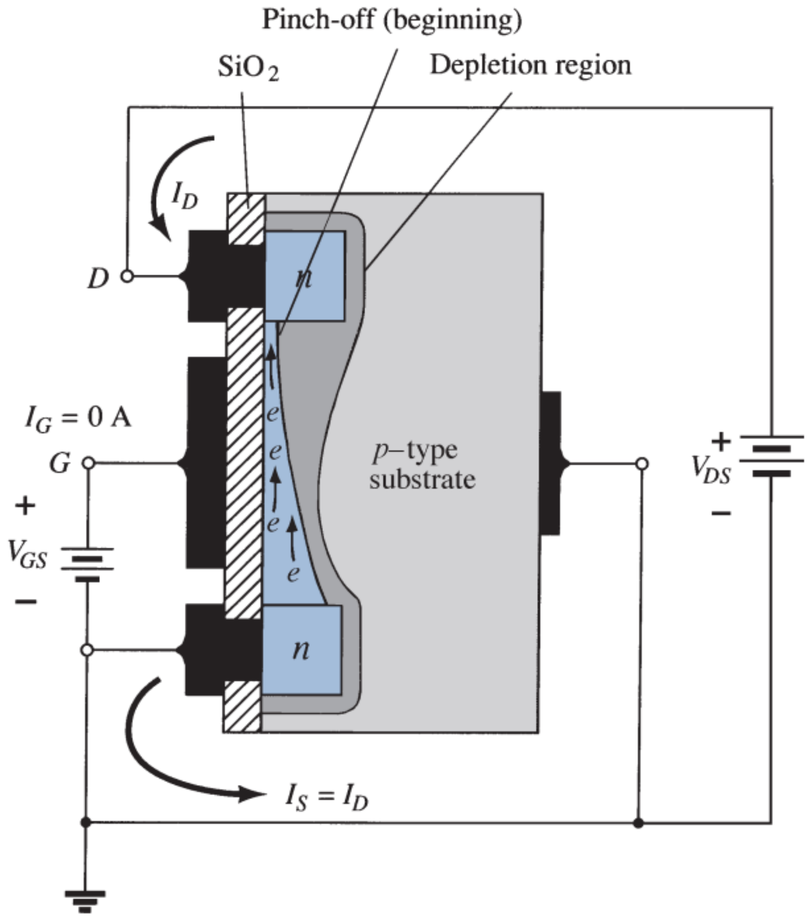


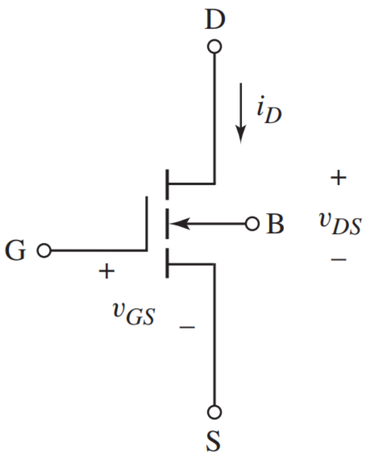
Fig: n-channel enhancement-type MOSFET

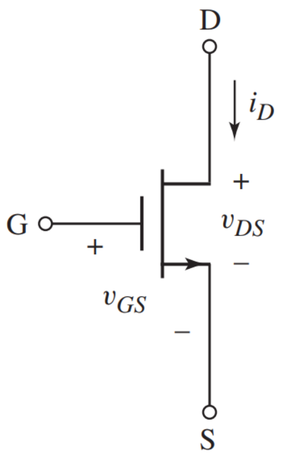
Behavior at $V_{GS} > 0$ V

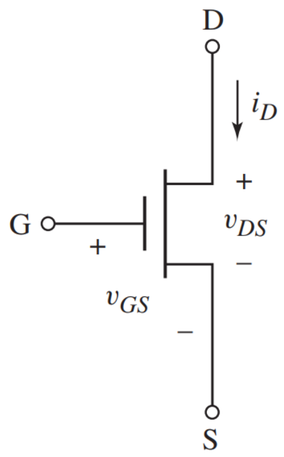
- Enhancement Mode Operation:
  - Channel forms only after V_{GS} exceeds V_T
  - Thus, called "Enhancement-type"
  - ID current increases as V_{GS} increases beyond V_T
- Saturation and Pinch-Off:
  - If V_{GS} is fixed, increasing V_{DS} causes V_{GD} to decrease, causing channel near Drain to pinch off
  - Beyond this, I_D saturates despite increasing V_{DS}

Enhancement-type MOSFET

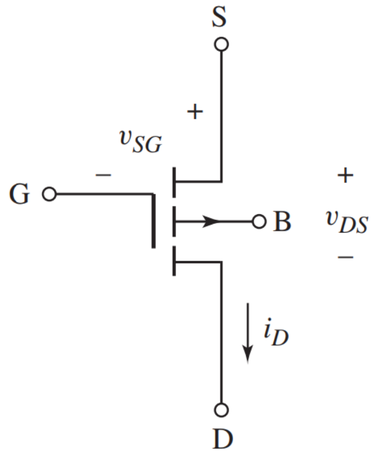
Commonly used Circuit Symbols

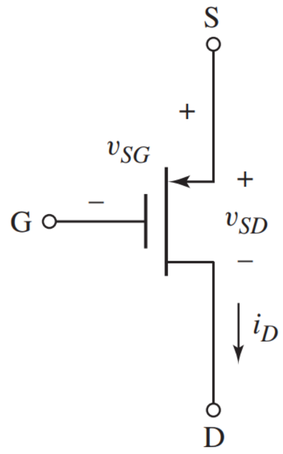


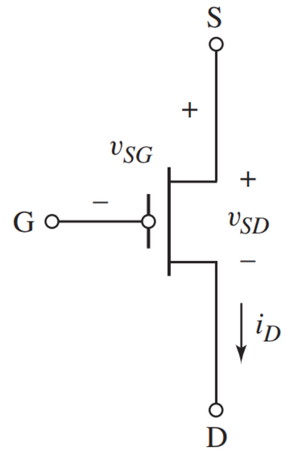




n-channel enhancement-type MOSFET







p-channel enhancement-type MOSFET

MOSFET Application: Logic Gates

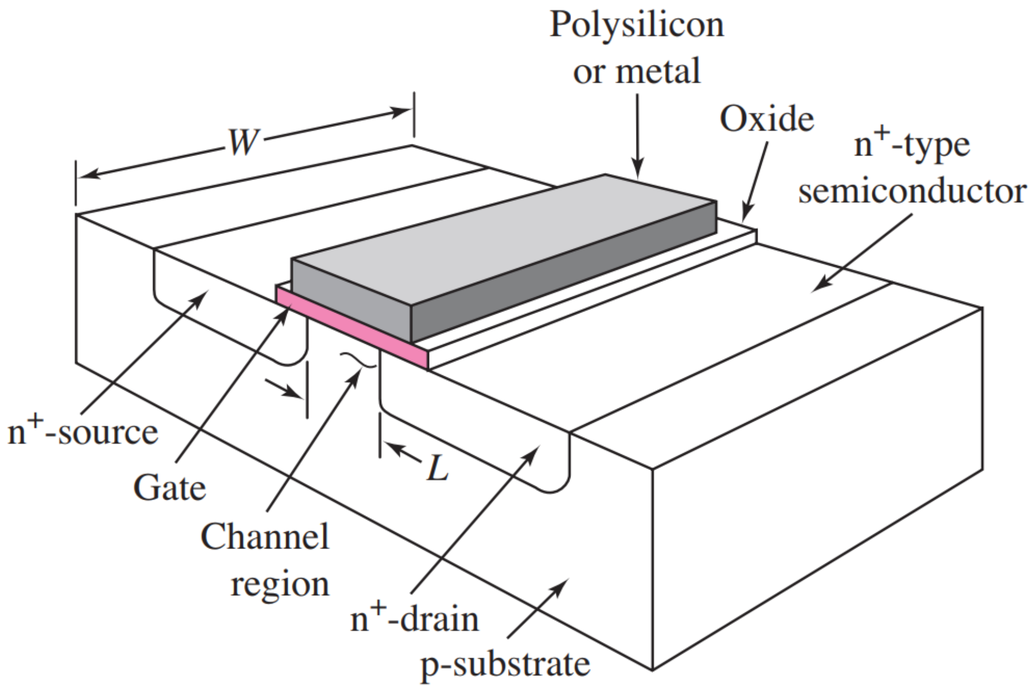


Fig: Structural diagram of an n-channel enhancement-type MOSFET

- Enhancement-type MOSFETs are the building blocks of digital logic –
  - n-channel enhancement MOSFET → NMOS
  - p-channel enhancement MOSFET → PMOS
- CMOS (Complementary MOS):
  - Combines NMOS + PMOS
  - Offers low power, high noise margin, high density
  - Used in nearly all modern digital logic ICs