

PARTICULARS OF THE EXPERIMENTS PERFORMED

S.NO.	EXPERIMENTS	DATE	PAGE	REMARKS
1.	To get familiarised with digital electronics equipment	26-08-2023	1-4	M 9/8
2.	To test the truth table of all the gates of - i) IC 7400(NAND), ii) IC7404 (NOT), iii) IC7408(AND), iv) IC7432(OR)	02-08-2023	5-7	M 9/8
3.	To test the truth table of all the gates of :- i) IC7402 (NOR) ii) IC7486(XOR) iii) IC7410 (3 i/p NAND) iv) IC7411(3 i/p AND) v) IC7420(4 i/p NAND)	09-08-2023	8-10	M 16/8
4.	To study & realise Half Adder using basic gates. To study & realise Full Adder using basic gates.	16-08-2023 23-08-2023	11	M 13/9
5.	To study & realise Half Subtractor using basic gates To study & realise Full Subtractor using basic gates.	16-08-2023 23-08-2023	12	M 13/9
6.	To study working of logic gates using NOR and NAND gate respectively.	13-09-2023	13-15	M 4/10
7.	To design and implement Multiplexer using logic gates.	04-10-2023	16-17	M 11/10
8.	To design and implement DeMultiplexer using logic gates.	04-10-2023	18-19	M 11/10
9.	To convert given binary numbers to gray codes & vice versa.	11-10-2023	20	M 8/11
10.	Truth Table verification of Flip Flops: SR and D FF	01-11-2023	21	M 8/11
11.	Truth Table verification of Flip Flops: JK and T FF	01-11-2023	22	M 8/11

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AIM : To get familiarised with digital electronics equipments.

APPARATUS : Breadboard, Trainer kit

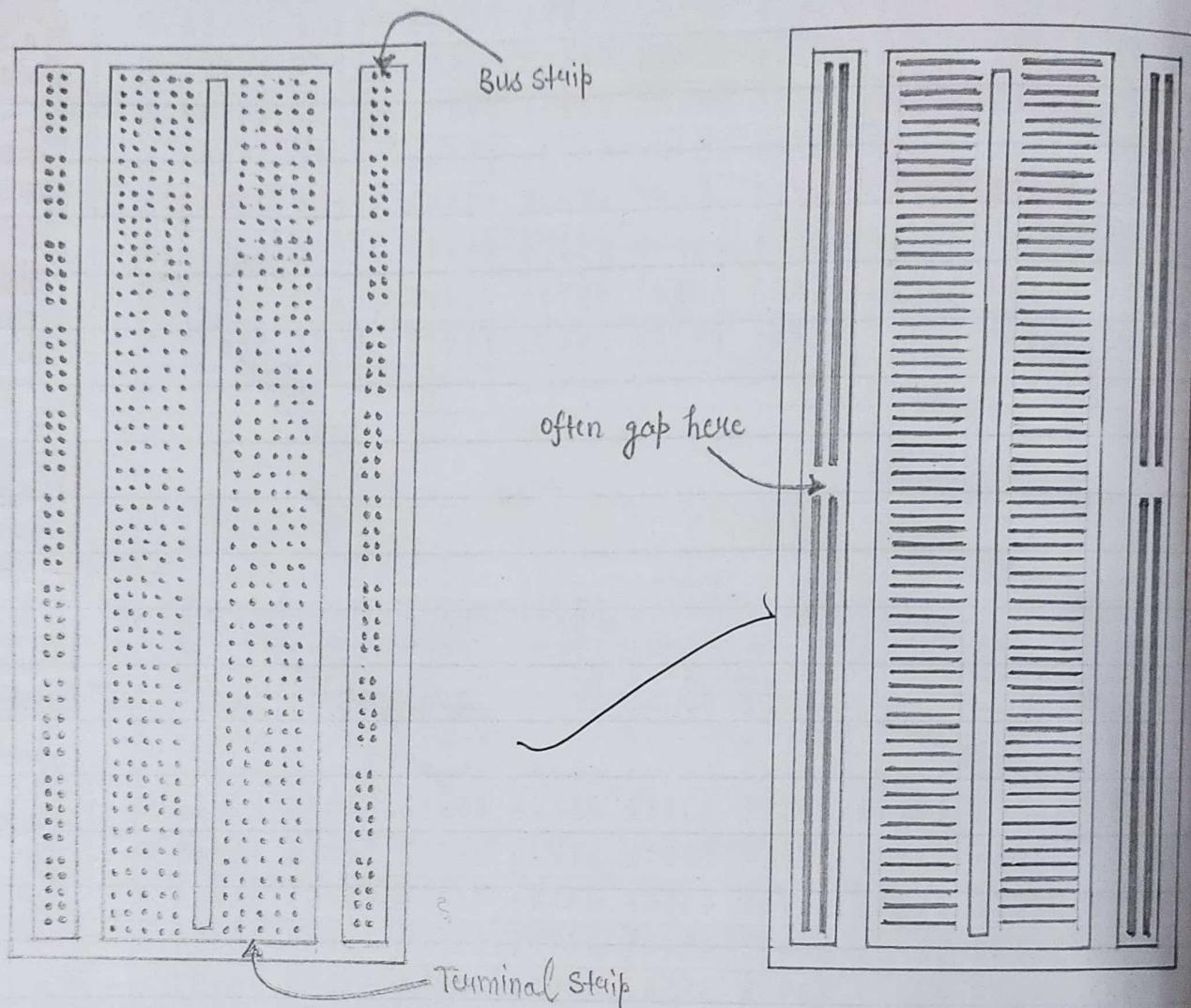


Fig:- The Breadboard. The lines indicate connected holes.

EXPERIMENT-1

AIM : To get familiarised with digital electronics equipments.

APPARATUS : Breadboard, trainer kit

THEORY : The breadboard consists of two terminal strips and two bus strips (often broken in the centre). Each bus strip has two rows of contact. Each of the two rows of contacts are a node. That is, each contact along a row on a bus strip is connected together (inside the breadboard). Bus strips are used primarily for power supply connections, but are also used for any node requiring a large number of connections. Each terminal strip has 60 rows and 5 columns of contacts on each side of the centre gap. Each row of 5 contacts is a node.

We will build our circuits on the terminal strips by inserting the leads of circuit components into the contact receptacles and making connections with 22-26 gauge wire. There are wire cutter/strippers and a spool of wire in the lab. It is a good practice to wire +5V and 0V power supply connections to separate bus strips.

The 5V supply MUST NOT BE EXCEEDED since this will damage the ICs (Integrated circuits) used during the experiments. Incorrect connections of power to the ICs could result in them exploding or becoming very hot.- with the possible serious injury occurring to the people working on the experiment! Ensure that the power supply polarity and all components

and connections are correct before switching on power.

- Trainer kit : Trainer kit has breadboard, power supply (fixed and variables), input switches, output LED, clock for frequency generation.
- Building the circuit : Throughout the experiment we will use TTL (Transistor Transistor logic) chips to build circuits. The steps for building a circuit should be completed in the order described below -
 1. Turn the power (trainer kit) off before building anything.
 2. Make sure the power is off before building anything in circuit.
 3. Connect the +5V and ground (GND) leads of the power supply to the power and ground bus strips on breadboard.
 4. Put the chips that will be used, into the breadboard.
 5. Point all the chips in the same direction with Pin 1 at the upper left corner.
 6. Select a connection on the schematic and plow a piece of hook-up wire between corresponding pins of the chips on the breadboard. It is better to make short connections before longer ones.
 7. Get one of the members of group to check the connections, before power is turned on.
 8. If an error is made and is not spotted before power is turned on, turn the power off immediately before reviving the circuit.

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9. At the end of the laboratory session collect your hook-up wires, chips and all equipments and return them to the demonstrator.
10. Tidy the area that you were working in and leave it in the same condition as it was before you started.

Common causes of Problems :

1. Not connecting the ground and power pins for all chips.
2. Not turning on the power supply before checking the operation of the circuit.
3. leaving out wires.
4. Plugging wires into the wrong holes.
5. Driving a single gate input with the outputs of two or more gates.
6. Modifying the circuit with the power on.

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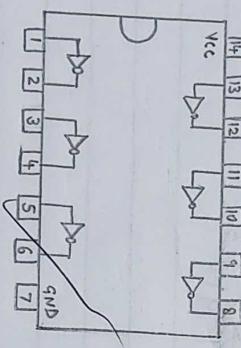
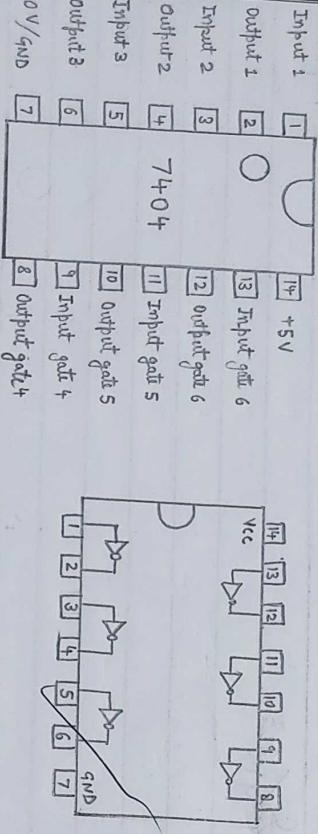
AIM: To test the truth table of all the gates of -

- i) IC 7400 (NAND)
- ii) IC 7404 (NOT)
- iii) IC 7408 (AND)
- iv) IC 7432 (OR)

APPARATUS REQUIRED :

Sr. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	NOT gate	IC 7404	1
2.	NAND gate	IC 7408	1
3.	OR gate	IC 7432	1
4.	NAND gate	IC 7400	1
5.	IC Trainer kit	-	1
6.	Patch cord	-	1

IC 7404: NOT gate



EXPERIMENT -2

AIM: To test the truth table of all the gates of -

- i) IC 7400 (NAND)
- ii) IC 7404 (NOT)
- iii) IC 7408 (AND)
- iv) IC 7432 (OR)

APPARATUS REQUIRED :

Sr. No.	COMPONENT	SPECIFICATION	QUANTITY
1.	NOT gate	IC 7404	1
2.	AND gate	IC 7408	1
3.	OR gate	IC 7432	1
4.	NAND gate	IC 7400	1
5.	IC Trainer kit	-	1
6.	Patch cord	-	1

Build a circuit to implement the Boolean function $F = \overline{A} \cdot \overline{B}$. Please note that the notation \overline{A} refers to \overline{A} . This notation should be used during the write up of laboratory experiments.

Sometimes the chip manufacturers may denote the first pin by a small indented circle above the first pin of the chip. Place the chip in the same direction to avoid confusion at a later stage. Remember to connect power to the chips to get them to work.

A	$Y = \overline{A}$	Color of LED
0	1	Red
1	0	Green

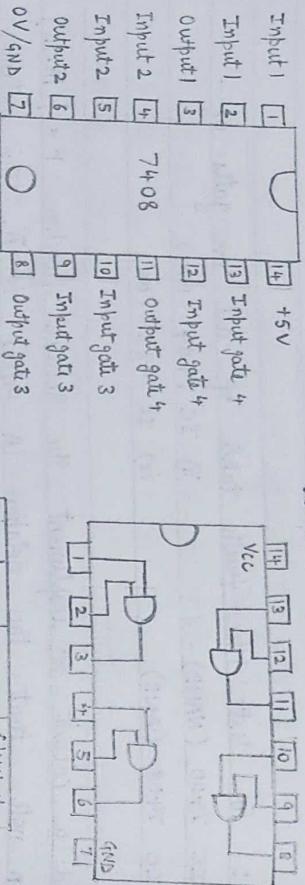
SYMBOL: A —→ Y = \overline{A}

TRUTH TABLE

IC 7408 : AND Gate

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SYMBOL: $A \overline{\wedge} B = Y = A \cdot B$

A	B	$Y = A \cdot B$	Output of
0	0	0	Ground
0	1	0	Ground
1	0	0	Ground
1	1	1	Set

SYMBOL: $A \overline{\vee} B = Y = A + B$

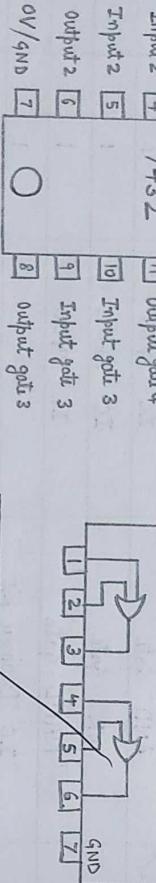
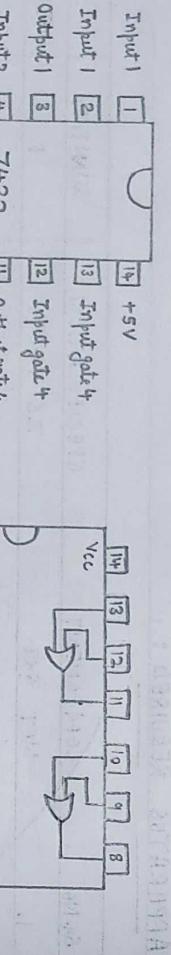
TRUTH
TABLE

IC 7432 : OR gate

NOT Gate : The NOT gate is called an inverter. The output is high when the input is low.

OR Gate : The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low when both the inputs are low.

AND Gate : The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low when any one of the inputs is low.



A	B	$Y = A + B$	Output of
0	0	0	Ground
0	1	1	Set
1	0	1	Set
1	1	1	Set

SYMBOL: $A \overline{\vee} B = Y = A + B$

TRUTH
TABLE

A	B	$Y = A + B$	Output of
0	0	0	Ground
0	1	1	Set
1	0	1	Set
1	1	1	Set

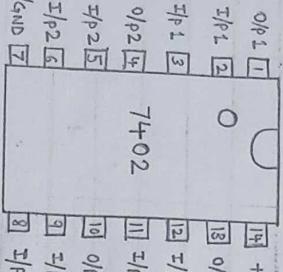
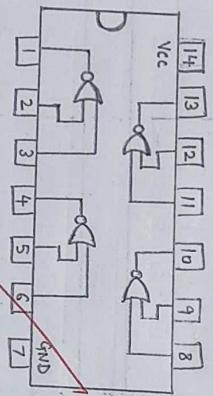
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EXPERIMENT - 3EXPERIMENT - 3

AIM: To study the truth table of all the gates of:-
 (i) IC 7402 (NOR) (ii) IC 7486 (XOR) (iii) IC 7410 (3-i/p NAND)
 (iv) IC 7411 (3-i/p AND) (v) IC 7420 (4-i/p NAND)

APPARATUS REQUIRED:
 (i) IC 7402 (NOR) (ii) IC 7486 (XOR) (iii) IC 7410 (3-i/p NAND)
 (iv) IC 7411 (3-i/p AND) (v) IC 7420 (4-i/p NAND)

SYN. NO.	COMPONENT	SPECIFICATION	QUANTITY
1.	NOR gate	IC 7402	1
2.	XOR gate	IC 7486	1
3.	3-i/p-NAND gate	IC 7410	1
4.	3-i/p AND gate	IC 7411	1
5.	4-i/p NAND gate	IC 7420	1
6.	IC Trainer kit	-	1
7.	Patch Cords	-	14

IC 7402 (NOR)APPARATUS REQUIRED:

AIM: To study the truth table of all the gates of:-
 (i) IC 7402 (NOR) (ii) IC 7486 (XOR) (iii) IC 7410 (3-i/p NAND)
 (iv) IC 7411 (3-i/p AND) (v) IC 7420 (4-i/p NAND)

Build a circuit to implement the Boolean Function $F = \overline{(A \cdot B)}$. Please note that the notation \overline{A} refers to \bar{A} . This notation should be used during the write up of laboratory experiments. Sometimes the chip manufacturers may denote the first pin by a small indented circle above the first pin of the chip. Place the chip in the same direction to avoid confusion at a later stage. Remember to connect power to the chips to get them to work.

SYMBOL:	A	B	$Y = \overline{A+B}$	Colour of LED
	0	0	1	Red
	0	1	0	Green
	1	0	0	Green
	1	1	0	Green

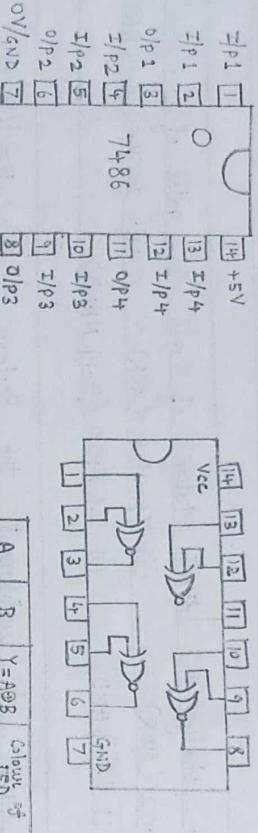
TRUTH TABLE

$$Y = \overline{A+B}$$

IC 7406 (XOR)

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SYMBOL: $A \xrightarrow{Y = A \oplus B} Y$

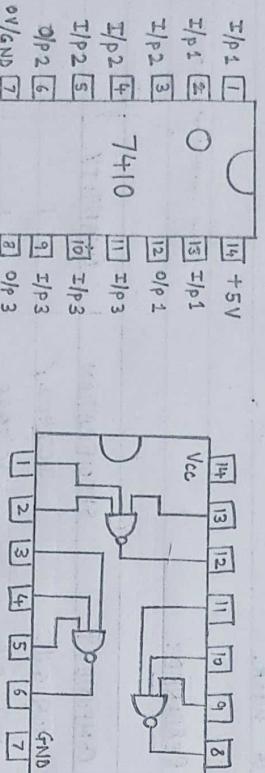
A	B	$Y = A \oplus B$	Color of LED
0	0	0	Green
0	1	1	Red
1	0	1	Red
1	1	0	Green

IC 7410 (3-i/p NAND)

TRUTH TABLE

Y = A ⊕ B

XOR gate: The output is high when one of the both inputs is high and other input is low. The output is low when both the inputs are low or both inputs are high.



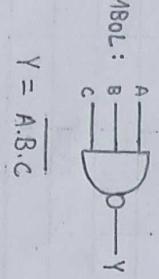
AND gate: The AND gate performs a logical multiplication commonly known as AND function. The output is high when all inputs are high. The output is low when any one of the input is low.

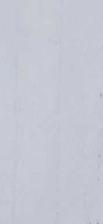
NAND gate: The NAND gate is a contradiction of AND-NOT.

It is a combination of AND and NOT gate respectively. The output is high when all inputs are low or any one of the inputs is high. The output is low when all the inputs are high.

A	B	C	$Y = \overline{ABC}$	Color of LED
0	0	0	1	Red
0	0	1	0	Red
0	1	0	0	Red
0	1	1	1	Red
1	0	0	1	Red
1	0	1	0	Red
1	1	0	0	Red
1	1	1	1	Red

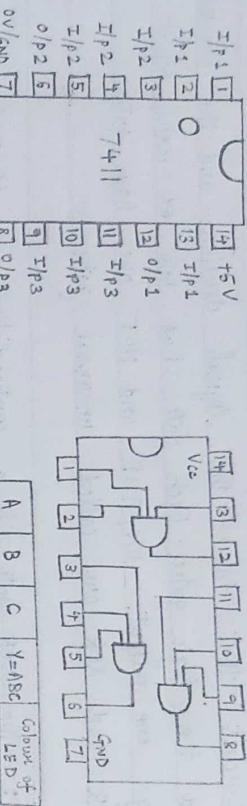
TRUTH TABLE



SYMBOL: 

$$Y = A \cdot B \cdot C$$

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PROCEDURE:

0V/GND

I/p 3

0/p 3

I/p 3

AIM: To study and realize half adder and full adder using X-OR and basic gates.

APPARATUS REQUIRED: IC 7486, IC 7408, IC 7404, IC Transistor kit, Patch cords

CIRCUIT DIAGRAM:

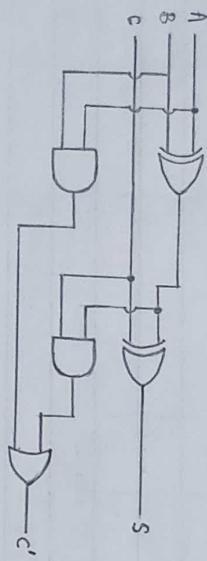
Half Adder using basic gates



$$S = A \oplus B = A\bar{B} + \bar{A}B$$

$$C' = A \cdot B$$

Full Adder using basic gates



A	B	S	C'
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

APPARATUS REQUIRED:

IC 7486, IC 7404, IC 7408, IC 7432, IC Transistor kit, Patch cord

PROCEDURE:

1. Verify the gates.
2. Make the connections as per the circuit diagram.

3. Switch on Vcc and apply various combination of input according to truth table.

4. Note down the output reading for half / full adder and carry bit for different combination of inputs.

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$$S = A \oplus B \oplus C$$

$$C' = (A \oplus B)C + A \cdot B$$

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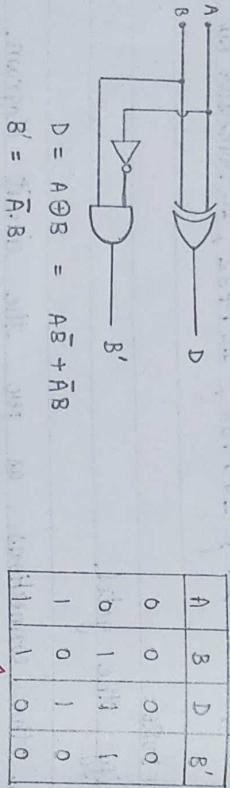
AIM: To study and realize half and full subtraction using KOR

and basic gates. — or T_{C7432} , T_{C7434} IC Trainer Kit

APPARATUS REQUIRED: IC 1486, IC 1470, IC 100, Patch Leads.

CIRCUIT DIAGRAM:

Half Subtractor using basic gates



A	B	D	B'
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0
0	0	0	0

Full subtractor using basic gates

$$D = A \oplus B = A\bar{B} + \bar{A}B$$

$$D = A \oplus B \oplus C$$

A	B	C	D	B'
-	-	-	-	0
-	0	0	-1	0
1	0	0	-1	1
1	0	0	0	1
1	0	0	0	1

APPARATUS REQUIRED:

IC 7486 (x-0R), IC 7408 (AND), IC 7404 (NOT), IC 7432 (OR),
IC Trainer kit, Patch cords.

PROCEDURE:

2. Make the connections as per the circuit diagram.

3. Switch on the Vcc and apply various combination of input according to the truth table.

4. Note down the output readings for half / full subtraction difference and the borrow bit for different combination of inputs.

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EXPERIMENT -5

EXPERIMENT -5

Teacher's Signature :

EXPERIMENT - 6

AIM: To study and realize the working of logic gates using NOR and NAND gate respectively.

APPARATUS REQUIRED: IC 7402 (NOR gate), IC 7400(NAND gate), IC Trainer kit, Patch cords

CIRCUIT DIAGRAMS:

Logic Gates using NAND gate (IC 7400)

• AND

$$Y = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A} + \overline{B}} = A \cdot B$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

• OR

$$Y = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A} + \overline{B}} = A + B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

• NOT

$$Y = \overline{A} = \bar{A}$$

A	Y
0	1
1	0

• NAND

$$Y = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A} + \overline{B}} = A \cdot B$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

• NOR

$$Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A} \cdot \overline{B}} = A + B$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

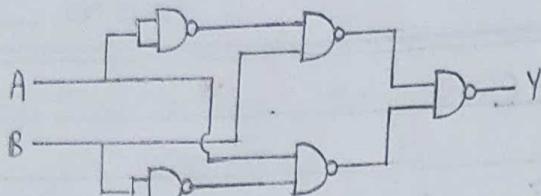
2. Make the connections as per circuit diagram.

3. Switch on Vcc power supply and apply various combination of input according to the truth table.

4. Note down and verify the output readings for all the logic gates circuit made using universal NOR & NAND gate for different combinations of inputs.

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• XOR

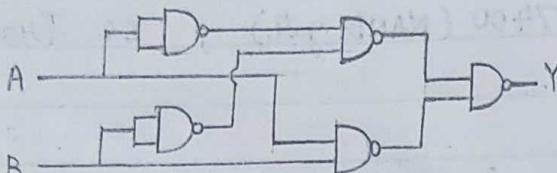


$$Y = \overline{\overline{A}B \cdot A\overline{B}} = \overline{\overline{A}B} + \overline{A\overline{B}}$$

$$= \overline{\overline{A}B} + A\overline{B} = A \oplus B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

• XNOR



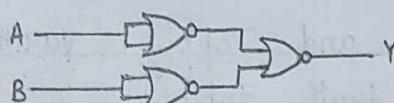
$$Y = \overline{\overline{A}\overline{B} \cdot \overline{A}\overline{B}} = \overline{\overline{A}\overline{B}} + \overline{A\overline{B}}$$

$$= \overline{\overline{A}\overline{B}} + A\overline{B} = A \odot B$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Logic gates using NOR gate (IC 7402)

• AND

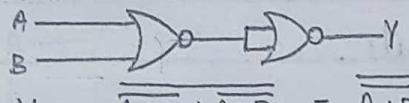


$$Y = \overline{\overline{A}+A + \overline{B}+B} = \overline{\overline{A}+\overline{B}}$$

$$= \overline{\overline{A}\cdot\overline{B}} = A \cdot B$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

• OR



$$Y = \overline{\overline{A}+B + \overline{A}+B} = \overline{\overline{A}+B}$$

$$= A+B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

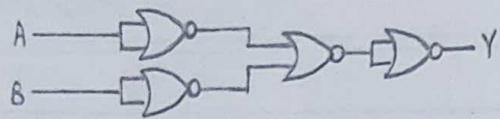
• NOT



$$Y = \overline{A}$$

A	Y
0	1
1	0

• NAND



$$\begin{aligned}
 Y &= \overline{\overline{A+A} + \overline{B+B} + \overline{\overline{A+A} + \overline{B+B}}} \\
 &= (\overline{\overline{A}} + \overline{B})(\overline{\overline{A}} + \overline{B}) = (\overline{A} + \overline{B})(\overline{A} + \overline{B}) \\
 &= \overline{A} + \overline{B} = \overline{A \cdot B}
 \end{aligned}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

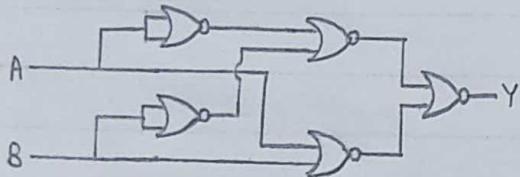
• NOR



$$Y = \overline{A+B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

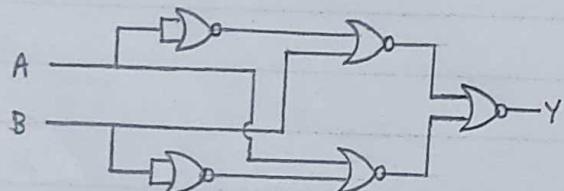
• XOR



$$\begin{aligned}
 Y &= \overline{\overline{A+A} + \overline{B+B}} + \overline{A+B} \\
 &= (\overline{\overline{A}} + \overline{B})(\overline{\overline{A}} + \overline{B}) = (\overline{A} + \overline{B})(A+B) \\
 &= \overline{A}\overline{B} + \overline{B}A = A \oplus B
 \end{aligned}$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

• XNOR



$$\begin{aligned}
 Y &= \overline{\overline{A+A} + B} + \overline{A+\overline{B+B}} \\
 &= (\overline{\overline{A}} + \overline{B})(\overline{\overline{A}} + \overline{B}) = (\overline{A} + \overline{B})(A+B) \\
 &= \overline{A}\overline{B} + AB = A \odot B
 \end{aligned}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

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AIM: To design and implement multiplexer using logic gates.

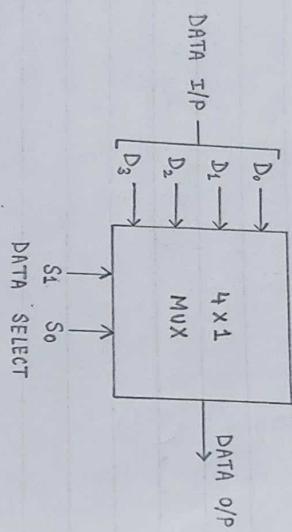
EXPERIMENT - 7

DESIGN, IMPLEMENTATION AND STUDY OF MULTIPLEXER

APPARATUS REQUIRED:

S.No.	Component Specification	Qty.
1.	3 I/P AND GATE IC 7411	1
2.	OR GATE IC 7432	1
3.	NOT GATE IC 7404	1
4.	IC TRAINER KIT	—
5.	PATCH CORDS	—

BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:



THEORY:

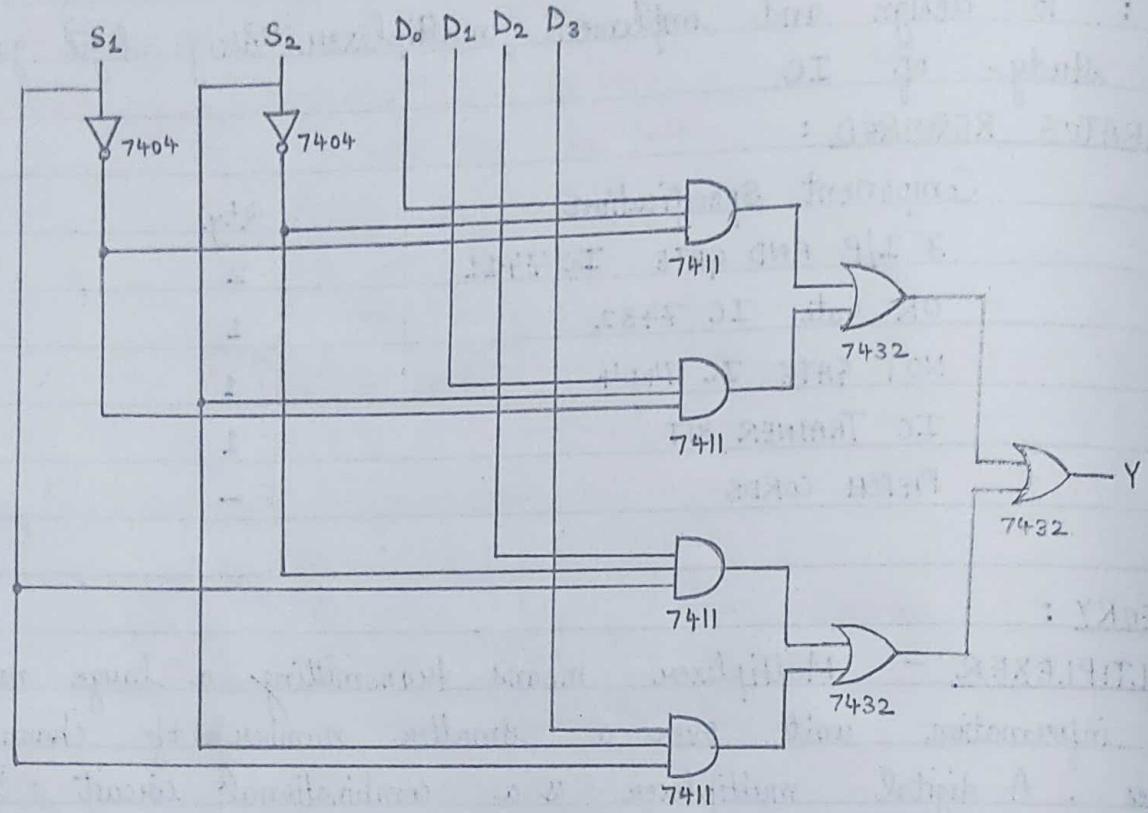
MULTIPLEXER — Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input lines and n selection lines whose bit combination determine which input is selected.

PROCEDURE:

- Connections are given as per circuit diagram.
- Logical inputs are given as per circuit diagram.
- Observe the output and verify the truth table.

$$Y = D_0\bar{S}_1\bar{S}_0 + D_1\bar{S}_1S_0 + D_2S_1\bar{S}_0 + D_3S_1S_0$$

CIRCUIT DIAGRAM FOR MULTIPLEXER:



TRUTH TABLE:

S_1	S_0	$Y = \text{OUTPUT}$
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

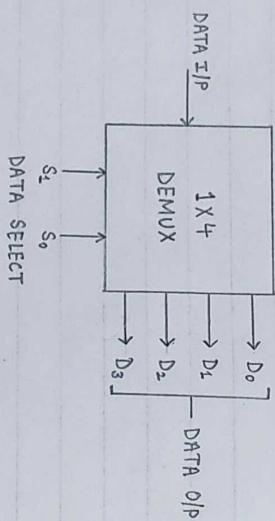
✓ No. 110

AIM: To design and implement demultiplexer using logic gates.

APPARATUS REQUIRED :

S.N.	Component Specification	Qty.
1.	3 I/P AND GATE IC 7411	2
2.	NOT GATE IC 7404	1
3.	IC TRAINER KIT	1
4.	PATCH CORDS	—

Block Diagram For 1:4 DEMULTIPLEXER :



FUNCTION TABLE :

S ₁	S ₀	INPUT
0	0	X → D ₀ = X̄S ₁ S ₀
0	1	X → D ₁ = X̄S ₁ S ₀
1	0	X → D ₂ = XS ₁ S ₀
1	1	X → D ₃ = XS ₁ S ₀

$$Y = X\bar{S}_1\bar{S}_0 + X\bar{S}_1S_0 + XS_1\bar{S}_0 + XS_1S_0$$

THEORY :

DEMULITPLEXER — The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as data distributor. Decoder can also be used as demultiplexer.

In the 1:4 demultiplexer circuit, the data input line goes to all the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

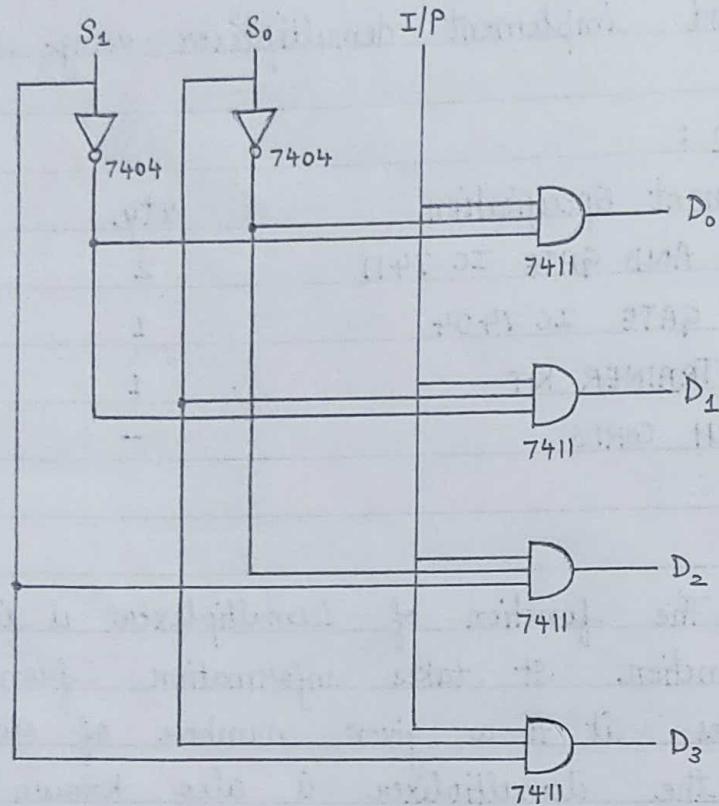
PROCEDURE :

- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table.

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CIRCUIT DIAGRAM FOR DEMULTIPLEXER:



TRUTH TABLE:

INPUT			OUTPUT			
S_1	S_0	I/P	D_0	D_1	D_2	D_3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

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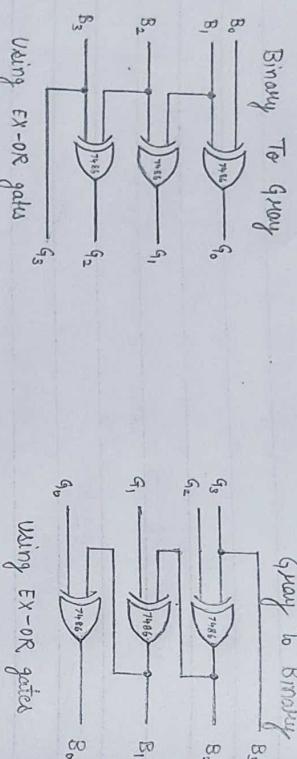
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AIM: To convert given binary numbers to gray codes.

APPARATUS REQUIRED: IC 7486, IC Trainer Kit, Patch Cords

CIRCUIT DIAGRAM:



Using EX-OR gates

Using EX-OR gates

TRUTH TABLE:

(Same for Both)

B_3	B_2	B_1	B_0	$g_3(V)$	$g_2(V)$	$g_1(V)$	$g_0(V)$
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	1	0	1
1	1	1	1	0	1	1	0

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EXPERIMENT-9

BINARY TO GRAY CODE AND GRAY TO BINARY CODE CONVERSION

AIM: To convert given binary numbers to gray codes and vice versa.

APPARATUS REQUIRED: IC 7486, IC Trainer Kit, Patch Cords

PROCEDURE:

1. The circuit connections are made as shown in figure.
2. Pin (14) is connected to +Vcc and Pin(7) to ground.
3. In the case of binary to gray conversion, the inputs B_0, B_1, B_2 and B_3 are given at respective pins and outputs g_0, g_1, g_2, g_3 are taken from all the 16 combinations of the input.
4. In the case of gray to binary conversion, the inputs g_0, g_1, g_2 and g_3 are given at respective pins and outputs B_0, B_1, B_2 and B_3 are taken from all the 16 combinations of inputs.
5. The values of the outputs are tabulated.

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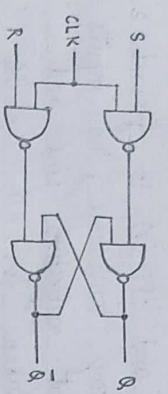
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AIM : Truth Table verification of Flip-Flops: (i) SR - Type
(ii) D - Type

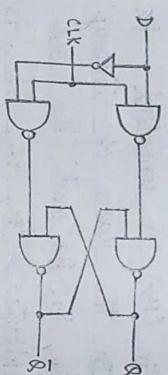
APPARATUS REQUIRED: IC 7400, IC 7404, IC Trainer Kit, Patch cords

CIRCUIT DIAGRAM & TRUTH TABLE:

(i) SR FLIP-FLOP



(ii) D FLIP-FLOP



CLK	S	R	Q_n	Q_{n+1}	o/p
\uparrow	0	0	0	0	
\uparrow	0	0	1	1	Hold
\uparrow	0	1	0	0	
\uparrow	0	1	0	0	
\uparrow	1	0	1	1	
\uparrow	1	0	1	1	
\uparrow	1	1	X	X	Invalid

- SR FLIP-FLOP: The SR flip-flop is the simplest memory element. It is constructed by feeding the outputs of the two NOR/NAND gate back to the other NOR/NAND gate input. The inputs 'S' and 'R' are referred to as Set & Reset input respectively.

- D FLIP-FLOP: The D flip-flop tracks the input, making transitions with those of D. The 'D' stands for "Data Delay". This flip-flop stores the value that is on the data line. It is constructed using SR flip-flop and NOT gate.

CLK	S	R	Q_n	Q_{n+1}	o/p
\downarrow	X	X			
\uparrow	0	0			
\uparrow	1	1			
\uparrow	1	1			

- SR FLIP-FLOP: The SR flip-flop is the simplest memory element. It is constructed by feeding the outputs of the two NOR/NAND gate back to the other NOR/NAND gate input. The inputs 'S' and 'R' are referred to as Set & Reset input respectively.
- D FLIP-FLOP: The D flip-flop tracks the input, making transitions with those of D. The 'D' stands for "Data Delay". This flip-flop stores the value that is on the data line. It is constructed using SR flip-flop and NOT gate.

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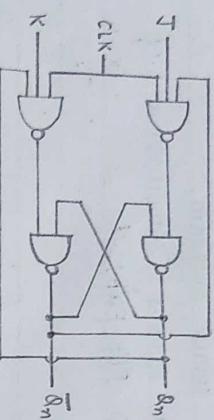
AIM: Truth Table verification of Flip-Flops : (i) JK-Type
(ii) T - Type

(iii) T - Type

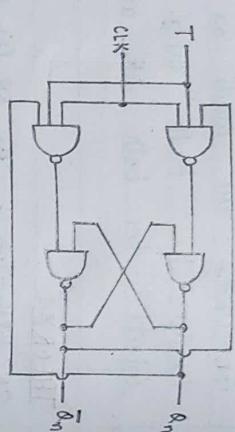
APPARATUS REQUIRED: IC 7400, IC 7410, IC Trainer Kit, Patch Cords

CIRCUIT DIAGRAM & TRUTH TABLE:

(i) JK FLIP-FLOP



(ii) T FLIP-FLOP



PROCEDURE :

1. Connections are made as per circuit diagram.
2. Verify the truth table for various combination of inputs for both JK and T Flip-Flop.

THEORY:

• JK FLIP-FLOP: JK flip-flop is the most used memory element.

It has four states, namely: memory, preset, clear & toggle.

The flip-flop is constructed using two 3-IP NAND gates and two 2-IP NAND gates. The inputs J and K are the set and reset inputs respectively.

- T FLIP-FLOP: T flip-flop also termed as toggle flip-flop is used to toggle the memory state at a constant rate. It is fabricated by shorting the J & K inputs of JK flip-flop.

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CLK	J	K	Q _n	Q _{n+1}	O/P
↑	0	0	0	0	
↑	0	0	1	1	Hold
↑	0	1	0	0	
↑	0	1	0	0	0
↑	1	0	0	1	1
↑	1	0	1	1	1
↑	1	0	1	0	0
↑	1	1	0	1	0
↑	1	1	0	0	Toggle