S.S. JAIN SUBODH COLLEGE OF GLOBAL EXCELLENCE

Pre University Examination 2022

BCA Part – I

Paper I - Elementary Physics

Maximum Marks - 100 TIME: 3Hrs

All questions are compulsory.

PART I Each question is of 2-marks. Word limit for the answers is 40 words

Q.1 a. Define Electric dipole?
b. What Superposition principle?
c. Define Electric field?
d. What do you mean by NAND gate?
e. State De Morgan's theorem?
f. What is a Multiplexer?
g. What is a D Flip-Flop?
h. What do you mean by edge triggered?
i. Define Shift register?
j. What is meant by Electrical potential?

Part-II Each question is of 4 marks word limit for the answer is 80 words.

Q2. State and prove Gauss theorem.

Q3. Differentiate between conductor, inductor and semiconductor?

Q4. Find the reduced form of

$AB + A(B+C) + B(B+C)$

Q5. What is Demultiplexer & explain IC – 74154 Demultiplexer?

Q6. What is clocked J-K Flip-Flop write truth table with circuit diagram?

Part-III Each question is of 12 marks.

Q7. State Kirchhoff's law and Ohm's law?

OR

Write properties of electric line of force?

Q8. Write the difference between Diamagnetic, Paramagnetic and Ferromagnetic substances?

OR

Explain series and parallel combination in resistances?

Q9. Minimize the following function and realize (logic circuit) using minimum number of gates

$$Y_1(A,B,C,D) = \sum m(1,3,4,5,7,9,11,13)$$

OR

Show the NAND and NOR gates are universal gate & also Realize the circuit of EX-OR gate with the help of either NAND or NOR gate

Q10. Sketch the segments of a seven segment indicator and explain the function of a seven segment decoder drive

OR

(i) Explain the construction and working of 16:1 multiplexer
(ii) Draw the truth table. For IC74180 Parity checker.

Q11. Give a Schematic of a 4-Bit Serial in parallel out shift resister and show the status of 4 stages for the data 0110

OR

Describe a 3-bit synchronous counter with its wave form and counting sequence? How it is different to an asynchronous counter with same moduli?

This question paper contains 2 printed pages.

Roll No. 324(7)1

101/131

B.C.A. (Part-I) EXAMINATION - 2022

101729

[Also Common for (Hons.) Part-I]

(Three-Year Scheme of 10+2+3 Pattern)

ELEMENTARY PHYSICS

Time Allowed : Three Hours

Maximum Marks : 100

No supplementary answer-book will be given to any candidate. Hence the candidates should write their answer precisely in the main answer-book only.

All the parts of one question should be answered at one place in the answer-book. One complete question should not be answered at different places in the answer-book.

Write your roll number on question paper before start writing answers of questions.

PART - I

10x2=20

1. (a) Write two examples of good electrical conductor and insulator.
   (b) Sketch the electric field of lines from a positive test charge and negative test charge.
   (c) Draw the magnetic field of lines for a current carrying circular loop.
   (d) State the Faraday's first law of electromagnetic induction.
   (e) Draw the logic symbol for two input AND and EX-OR gate.
   (f) Solve the Y= A.(1+A).
   (g) What do you mean by combinational circuit ?
   (h) Name the IC which is used for Parity checker.
   (i) Classify the sequential logic circuits.
   (j) What do you mean by edge trigger D flip- flop.

PART - II

5x4=20

2. Define the concept of electric flux. What will be maximum and minimum value of it ?

3. Explain the magnetic properties of materials and classify it.

4. Design AND gate using NAND gate and explain it with truth table.

5. Draw the block diagram and truth table for 4:1 multiplexer.

6. Draw the block diagram, circuit diagram and truth table for R-S flip flop.

PART - III

7. (a) Derive an expression for effective capacitance for series and parallel connected of capacitors in a suitable circuit. 3+3=6

(b) Two point charges of 1 μC and 2 μC are placed 10 cm apart. Determine the position on line at which Electric field will be zero. 6

OR

(a) Derive an expression for effective Resistance for series and parallel connected of resistors in a suitable circuit. 3+3=6

(b) Three capacitors have capacities 5 μF, 3 μF and 2 μF respectively. How you will connect to get

(i) Maximum capacitance and

(ii) Minimum capacitance. Calculate their values also. 3+3=6

8. Derive an expression for magnetic field due to bar magnet on (i) a point on the axis of magnet and (ii) point on the equatorial line. 6+6=12

OR

(a) Derive an expression for magnetic field at axial distance x due to circular coil carrying current I ampere in it. 6

(b) Derive an expression for magnetic force per unit length for a current carrying parallel wires; current in each wire is 1A; separated by distance 2 m. What will be the maximum and minimum force per unit length ? 3+3=6

9. Draw the R-D logic diagram for AND and OR gate. Explain the working mechanism with truth table. 6+6=12

OR

(a) State the Boolean algebra rules for digital electronics. Prove it using truth table. 6

(b) State the De Morgan's theorems. And reduce below expression by using it. 6

$$Y = \overline{\overline{(A+B)} + \overline{(A+B)}}$$

10. Discuss the 16:1 Multiplexer with giving pin out diagram, truth table and logic diagram. 12

OR

Discuss the BCD to seven segment decoder with giving pin out diagram, truth table and Boolean expressions for desired outputs. 12

11. What do you mean by sequential circuits ? Discuss in details the asynchronous and clocked R-S flip flop with suitable logic diagram and truth table. How does it differ from D flip-flop ? 2+4+4+2=12

OR

Using three (03) J-K flip flops, design down counter. Describe the working mechanism using time diagram and truth table. 3+3+3+3=12

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