[Total No. of Questions - 9] [Total No. of Printed Pages - 3]

Dec-24-0320 (NEP)

MCA-6103 (Computer Organization and Architecture)

MCA-1st CBCS/NEP

Time : 3 Hours **Max. Marks : 60**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note: Attempt five questions in all, select one question each from section A, B, C, D. Section E (Question-9) is compulsory.

SECTION A

1. A 36-bit floating-point binary number has eight bits plus sign for the exponent and 26 bits plus sign for the mantissa. The mantissa is a normalized fraction. Numbers in the mantissa and exponent are in signed-magnitude representation. What are the largest and smallest positive quantities that can be represented, excluding zero? (6)

   B. Draw and explain the circuit for error detection with even parity bit. (6)

2 A. Explain, in detail, about booth multiplication algorithm with an example. (6)

   B. Explain the process for signed magnitude addition and subtraction with flow chart. (6)

SECTION B

3. A. Design and implement 4-bit Arithmetic unit which performs ADD, ADD with carry, SUB, Sub with borrow, Increment and decrement operations. (6)

   B. Identify the crucial features to design the instruction set architecture for a specific purpose processor. (6)

4. A. What is RTL (Register Transfer Language)? What is its significance? Explain with suitable examples. (6)

   B. Design a 4-bit combinational circuit decrementer using four full-adder circuits. (6)

SECTION C

5. A. Explain the difference between hardwired control and micro-programmed control. Is it possible to have a hardwired control associated with a control memory? (6)

   B. Explain about address sequencing in control memory with neat diagrams. (6)

6. A. Convert the following arithmetic expressions from infix to reverse Polish notation.

   a) A * B + C * D + E * F

   b) A * B + A * (B * D + C * E) (6)

   B. Explain hardware organization of micro programmed control unit. (6)

SECTION D

7. A. What is virtual memory? Explain the relation between address space and memory space in a virtual memory system along with its memory table for mapping. (6)

   B. What is Cache memory? And explain different types of mapping procedures for cache memory with examples. (6)

[P.T.O.]

8. A. With a neat schematic, explain about DMA controller and its mode of data transfer. (6)

   B. Classify and describe the possible modes of data transfer to and from peripherals with examples. (6)

SECTION E (Compulsory)

9. a) What is Locality of Reference?

   b) List out the Register transfer notations for Arithmetic Micro Operations.

   c) Why is Hard disk preferred as secondary storage device rather than SRAM?

   d) Explain Associative Memory.

   e) What do you understand by register transfer language?

   f) Differentiate between computer architecture and computer organisation. (6×2=12)