[Total No. of Questions - 9] [Total No. of Printed Pages - 3]

Dec.-23-1241

MCA-6103 (Computer Organization and Architecture)

MCA 1st (CBCS/NEP)

Time : 3 Hours **Max. Marks : 60**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : The candidates are required to attempt one question each from Section A, B, C, D and all questions from section E.

SECTION - A

1. A 36-bit floating-point binary number has eight bits plus sign for the exponent and 26 bits plus sign for the mantissa. The mantissa is a normalized fraction. Numbers in the mantissa and exponent are in signed-magnitude representation. What are the largest and smallest positive quantities that can be represented, excluding zero? (12)

OR

2. Perform the following arithmetic operations with the decimal numbers using signed-10's complement representation for negative numbers.

   a. (–638) + (+785).

   b. (–638) – (+185). (2×6=12)

SECTION - B

3. Show that a JK flip-flop can be converted to a D flip-flop with an inverter between the J and K inputs. (12)

OR

4. An 8-bit register contains the binary value 10011100. What is the register value after an arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow. (12)

SECTION - C

5. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

   a. How many bits are there in the operation code, the register code part, and the address part?

   b. Draw the instruction word format and indicate the number of bits in each part.

   c. How many bits are there in the data and address inputs of the memory? (3×4=12)

OR

6. The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word. (12)

SECTION - D

7. (a) What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each? (6)

(b) Design a parallel priority interrupt hardware for a system with eight interrupt sources. (6)

OR

8. A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped 1/0 configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

   a. How many RAM and ROM chips are needed?

   b. Draw a memory-address map for the system.

   c. Give the address range in hexadecimal for RAM, ROM, and interface. (3×4=12)

SECTION - E (Compulsory)

9. a. Convert the following binary numbers to decimal: 101110 and 1110101?

   b. Draw the truth table of 2-input Ex-OR gate.

   c. What are the addressing modes used by 8086 microprocessor?

   d. What are the different types of filed in instruction?

   e. What are the modes of modes of I/O data transfer?

   f. What is the role of virtual memory? (6×2=12)