SNC7320 Series

32-bit Dual-Core SoC

1 Introduction

1.1 Features

CPU

- Two ARM® Cortex®-M3 Processors (Core 0 and Core 1), each up to 162 MHz
- One serial wire debug (SWD) port
- Built-in Memory Protect Unit (MPU)
- Built-in Nested Vectored Interrupt Controller (NVIC)
- One interrupt signal for the interaction between the two cores
- System clocks
  - High: 12 MHz XTAL and IHRC at 1.2V
  - Low: 32 kHz XTAL and ILRC at 1.2V
- Supports fast Fourier transform (FFT)/finite impulse response (FIR) accelerator (Core 1)

Memory

- Internal memory
  - ROM size for Core 0: 64 KB
  - PRAM size for Core 0: 64 KB
  - ROM size for Core 1: 128 KB
  - Shared AHB SRAM: 256 KB
  - Shared Mailbox RAM: 4 KB
- SPI NOR flash controller
  - Clock frequency: Up to 40.5 MHz
  - Size: Up to 256 MB
  - Supports 1/2/4-bit mode
  - Supports execute in place (XIP)
- DRAM controller
  - 4 channels with burst transfer
  - Supports DDR1 DRAM or OPI PSRAM
- Supports one 16 KB I-cache
- DMA engine with 19 channels
- Storage
  - SD card controller (SD0)
  - NAND flash controller with 8-bit ECC

System Control (Core 0)

- Operation modes
  - Normal/sleep/deep sleep/deep power-down (DPD)
- Deep power-down with opional wakeup pin
- Low Voltage Detect (LVD)/Low Voltage Reset (LVR)
  - LVR: 0.7V for core; 2.1V for I/O (normal mode); 1.8V for I/O (power on/power off)
  - LVD12: 1.0V for core
  - LVD33: 2.4V/2.6V/2.8V/3.0V for I/O flag detect
- ROM/RAM remap

Peripherals

- Up to 80 general-purpose input/output (GPIO) pins
- Up to three master/slave Inter-Integrated Circuit (I^2C) buses
- Serial Peripheral Interface (SPI) controller
- Up to two Universal Asynchronous Receivers/Transmitters (UART)
- Up to eight 32-bit general-purpose timers providing up to 24 PWM outputs
- Two 8-bit Watchdog timers (WDT)
- 10-bit SAR ADC with up to six input channels
- SD/SDIO controller (SD1)
- SPI controllers with DMA
  - Supports one-byte FIFO
  - Supports 1/2/4-bit DMA mode
  - With 8-bit Error Correcting Code (ECC)
- USB 2.0 high speed host
  - Supports MSC/HUB/UVC class
  - Supports accelerator for ISO transfer
- USB 2.0 high speed host/device
  - Supports MSC/HID/UAC/UVC class
  - Host/device option

Multimedia

- Picture Processing Unit (PPU)
- TFT-LCD interface
  - 8-bit serial and 18-bit parallel RGB
  - UPS051 (serial RGB)/UPS052 (serial dummy RGB)
  - RGB565 format only
- 8080 MCU interface
- CMOS Image Sensor (CIS) interface
  - Supports resolution in VGA/CIF/ QVGA/QCIF/QQVGA
  - Supports scaling and windowing
  - Supports Line to block (L2B) mode
  - Connects to CIS/JPEG/CSC in script mode
- JPEG 422/420 codec
- Color Space Converter (CSC)
- Up to five I^2S interfaces
  - Communicates in master or slave mode
  - Connects to audio codecs in slave mode only
  - Left/right justified format
  - Supports microphone array

Voltage

- Core: 1.2V typically
- I/O: 3.3V typically
- DRAM: 1.8V typically

1.2 Application

The SNC7320 Series is suitable for a wide range of applications such as:

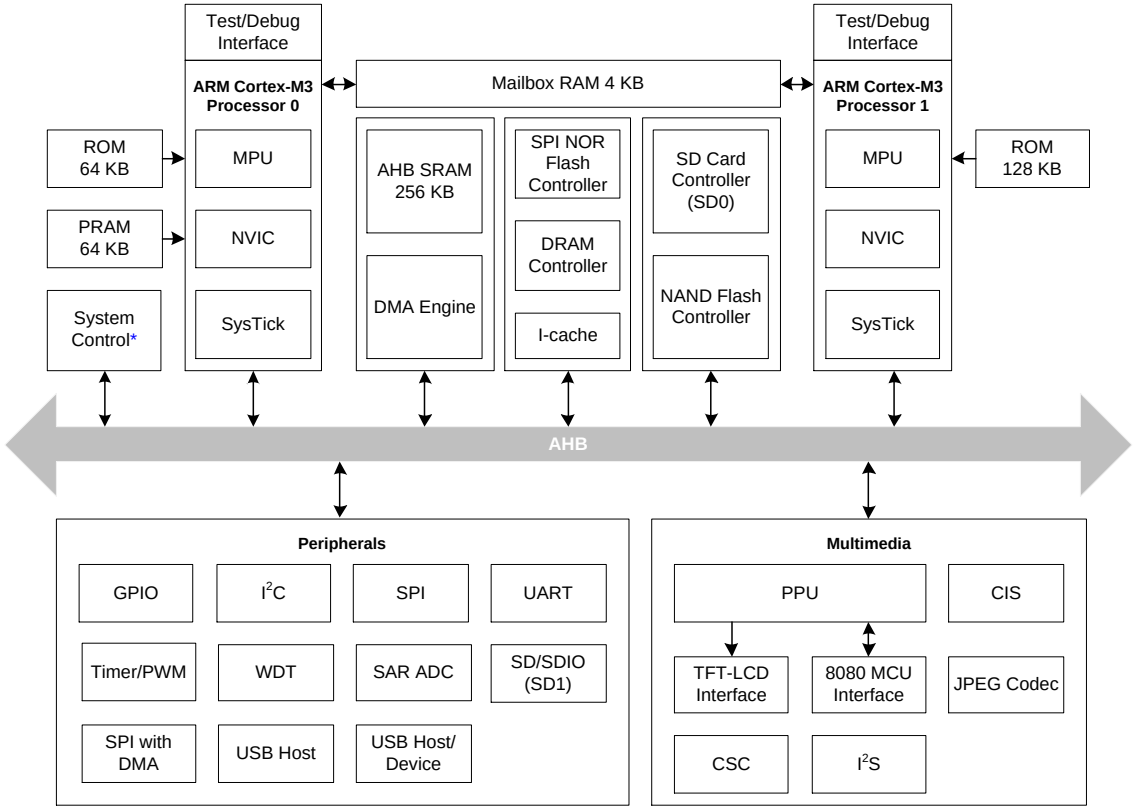
- Game controllers
- Gaming headsets
- Portable cameras
- Touch LCD
- Home automation

1.3 Description

The SNC7320 Series has two 32-bit ARM® Cortex®-M3 processors in symmetric dual-core architecture. Each of the two cores controls respective designated peripherals, cooperates with the other, and can be independently programmed. The two processors of the SNC7320 Series operate at a frequency of up to 162 MHz individually. Supporting RAM array with data bandwidth of up to 5 GB/sec and deep power-down mode consuming less than 1 µA, the SNC7320 Series is designed for high performance and low power consumption embedded applications.

The SNC7320 Series offers a wide range of peripherals including I^2C, SPI, WDT, SAR ADC, SD/SDIO, SPI NOR flash controller, NAND flash controller, USB host and device, and up to five I^2S controllers. With the software development kit (SDK) that includes various sample codes complying with the Keil® MDK-ARM® compiler, development, programming, and debugging can be implemented efficiently for various applications.

1.4 Functional Block Diagram



* For ARM Cortex-M3 Processor 0 only

Figure 1–1 Functional Block Diagram

1.5 Support

Sonix offers an extensive line of tools available for the SNC7320 Series including a software development kit (SDK) and other useful development tools such as:

- RTOS based development environments
- Mass production test tool
- Firmware download tool

For information on pricing and availability, please contact the nearest Sonix sales office or an authorized distributor.

Revision History

Date	Revision	Description
18-Sep-2019	1.0	Official release
01-Nov-2019	1.1	Updated part numbers in Selection Table, Pin Information Updated Recommended Operating Conditions \ Device supply voltage, V_{DDC} Updated Nomenclature and Marking Added QFN48L (6 x 6 x 0.8 mm/Pitch: 0.4) related information in Package Dimensions and Packing Quantity
21-Nov-2019	1.2	Updated Selection Table Updated Pin Assignment and Pin Description
13-Jan-2020	1.3	Updated Pin Description \ P0.6 Updated Table 2–2 \ Mode 2 of P4.12–P4.15 Updated Absolute Maximum Ratings \ Ambient temperature Updated Recommended Operating Conditions \ Device supply voltage, I/O, V_{DDIO33}, and Ambient temperature Updated Thermal Data
09-Mar-2020	1.4	Updated Pin Description Updated footnotes of Table 2–2 Updated Figure 8–1 and Figure 8–2 in Power Sequence
18-Feb-2021	1.5	Added LQFP80L, LQFP48L and related information in Features, Selection Table, Pin Information, Section 9.2 and 9.3 Updated Functional Block Diagram Updated System Reset \ Low Voltage Reset Updated Electrical Characteristics \ Deep sleep current and Internal pull-up/pull-down resistance Updated Figure 8–1 in Section 8.4
29-Apr-2021	1.6	Updated Selection Table \ Replaced 73230 with 73231
11-Jun-2021	1.7	Updated Selection Table \ Deleted 73289 and all related information; added 73290
08-Feb-2022	2.0	Updated for clarifications
01-Jun-2022	2.1	Removed RTC and all related information Updated Timer with PWM related information in Table 3–2, section 3.3 and 7.5 Updated Figure 5–1 Updated for clarifications Removed register summaries

Convention

⓵ WARNING	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
🛠 TIP	Indicates a tip that may help you solve a problem or save time.
🕮 NOTE	Provides additional information to emphasize or supplement important points of the main text.

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2 Device Comparison

Device No.	Package	SiP Audio Codec	SiP Memory	USB Host	USB Device/ Host	I/O	I²C	UART (Tx/Rx)	PWM	SAR ADC	SD/ SDIO	SPI DMA	SD Card	NAND	I²S	CIS	TFT LCD
SNC73200 M0NLFG-000	LQFP128L	–[1]	–	✓	✓	80	3	2	24	6-CH	✓	2	✓[2]	✓	5	✓	8/16-bit 8080/RGB
SNC73200 M1NLFG-000			8 MB OPI PSRAM														
SNC73231 M0NGFG-000	LQFP80L	–[1]	–	–	✓	58	2	1	17	4-CH	✓	2	✓[2]	–	3	✓	8-bit 8080/RGB
SNC73231 M1NGFG-000			8 MB OPI PSRAM														
SNC73240 M1VHJG-000	QFN88L	MIC x1 SPK x1	8 MB OPI PSRAM	–	✓	56	1	1	18	4-CH	✓	2	✓[2]	–	3	✓	8-bit 8080/RGB
SNC73252 M0NEJG-000	QFN68L	–[1]	–	–	✓	40	2	2	12	2-CH	✓	1	✓[2]	–	2	✓	8-bit 8080/RGB
SNC73252 M3NEJG-000			2 MB DDR1 DRAM														
SNC73282 M0UTJG-000	QFN48L (7 x 7 mm)	MIC x2 SPK x1	–	–	✓	18	2	1	7	2-CH	–	1	–	–	1	–	–
SNC73283 M0UTJG-000	QFN48L (7 x 7 mm)	MIC x2 HP x1	–	–	✓	18	1	1	8	2-CH	–	1	✓	–	–	–	–
SNC73285 M4NTJG-000	QFN48L (6 x 6 mm)	–[1]	512 KB Flash	–	✓	29	2	1	14	2-CH	–	–	–	–	5	–	–
SNC73290 M0NTFG-000	LQFP48L	–[1]	–	–	✓	28	2	1	12	4-CH	–	1	✓	–	2	–	–

[1] Supports external stereo/mono audio codec, SNAUD01 or SNAUD02.
[2] Shares the same pins with CIS.

3 Pin Information

3.1 Pin Assignment

Figure 3–1 to Figure 3–8 are pin assignments available for the SNC7320 Series. M*x* is a variable representing SiP memory options. For details, refer to the Device Comparison or the Nomenclature.

3.1.1 SNC73200M*x*NLFG-000

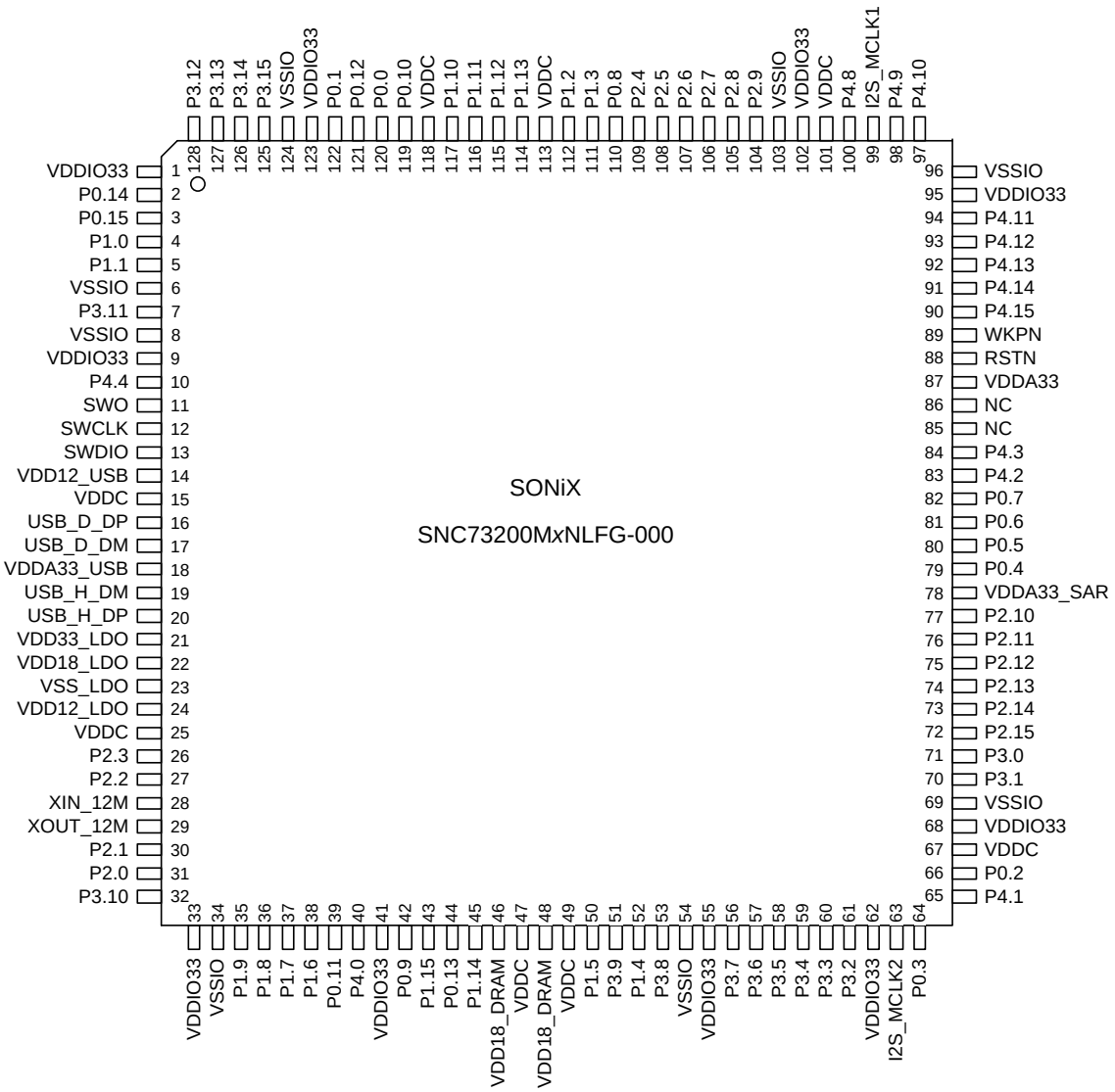


Figure 3–1 SNC73200M*x*NLFG-000 Pin Assignment

3.1.2 SNC73231MxNGFG-000

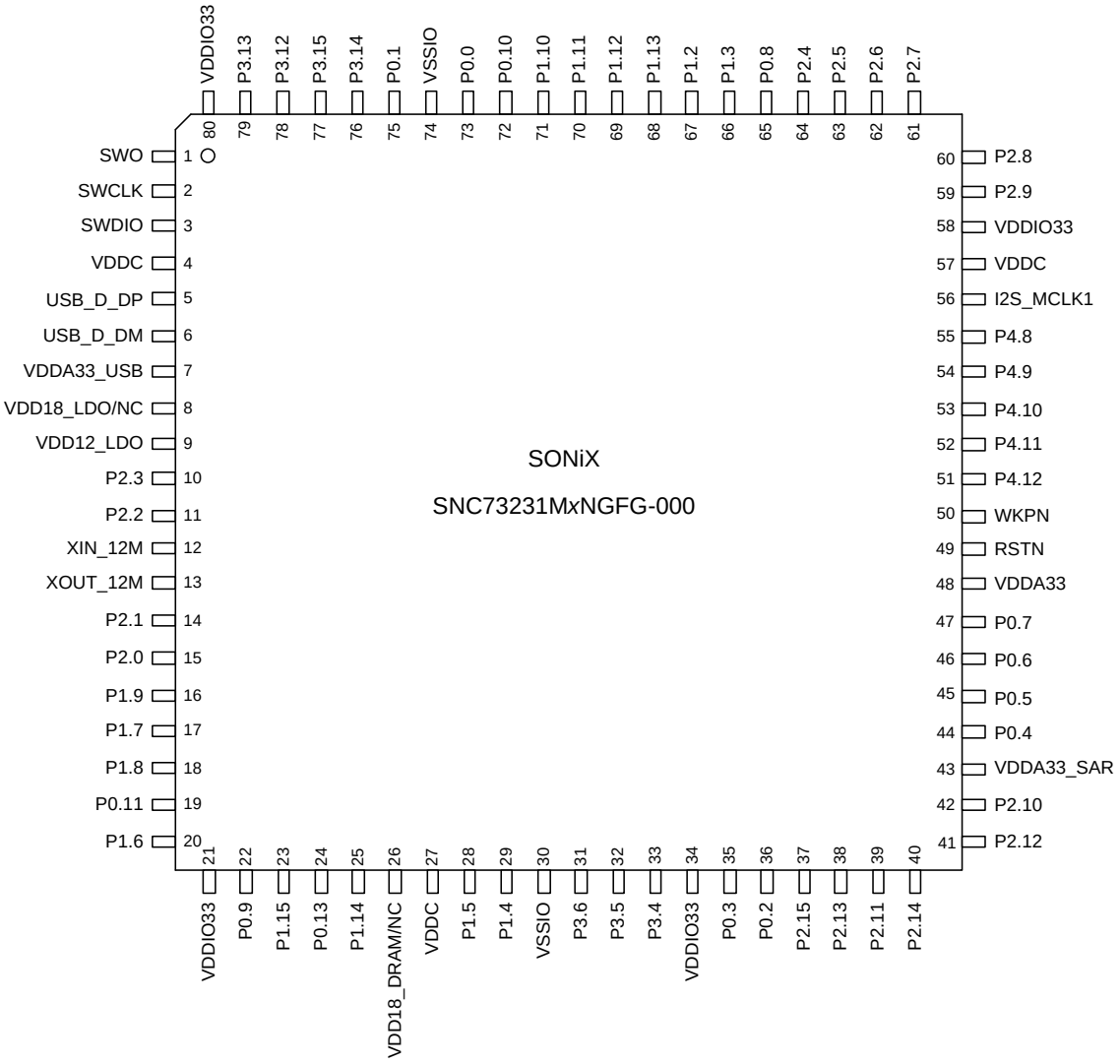


Figure 3–2 SNC73231MxNGFG-000 Pin Assignment[3]

[3] Pin 8 and pin 26 are NC for SNC73231M0NGFG-000.

3.1.3 SNC73240M*x*VHJG-000

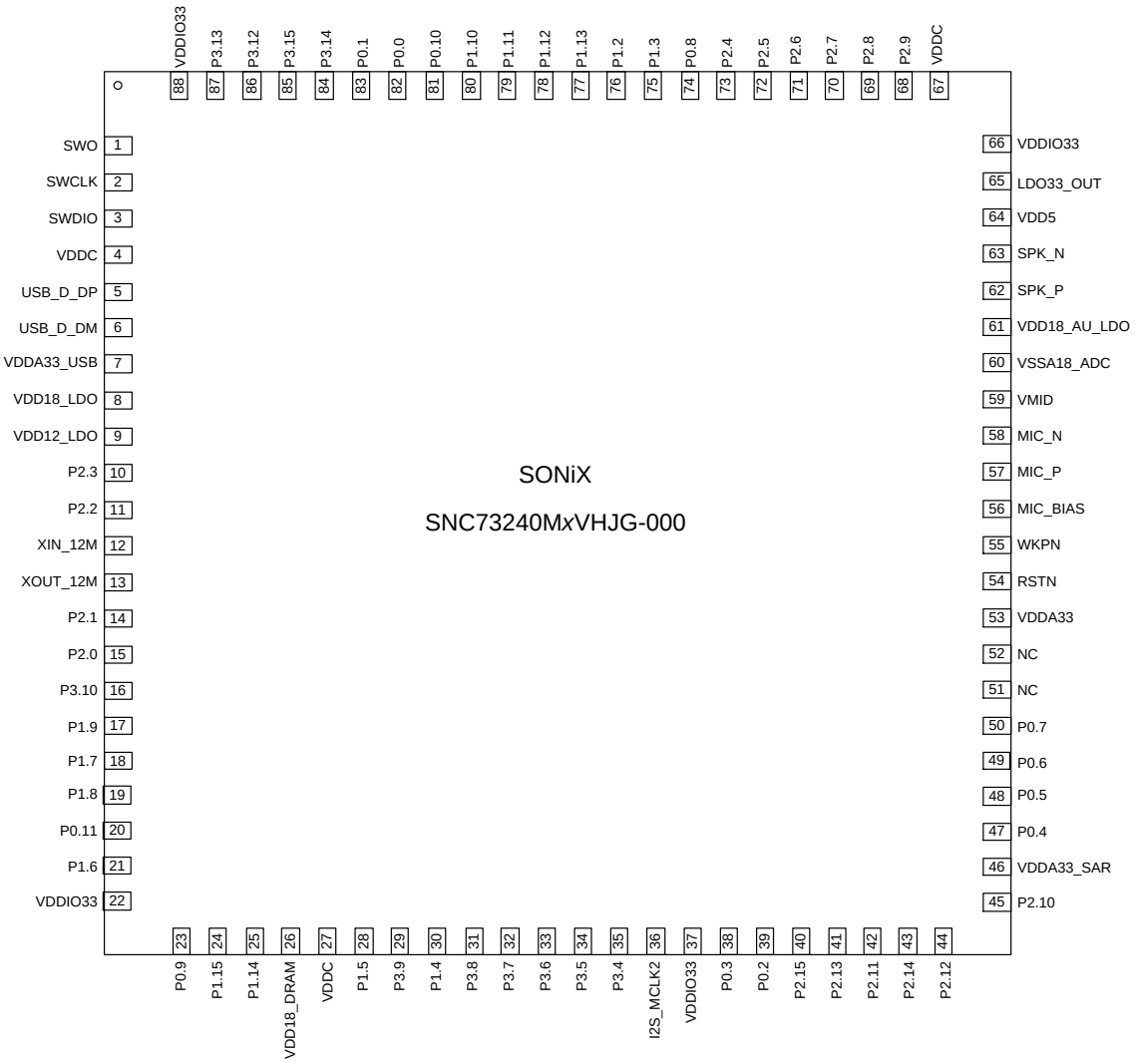


Figure 3–3 SNC73240M*x*VHJG-000 Pin Assignment

3.1.4 SNC73252M*x*NEJG-000

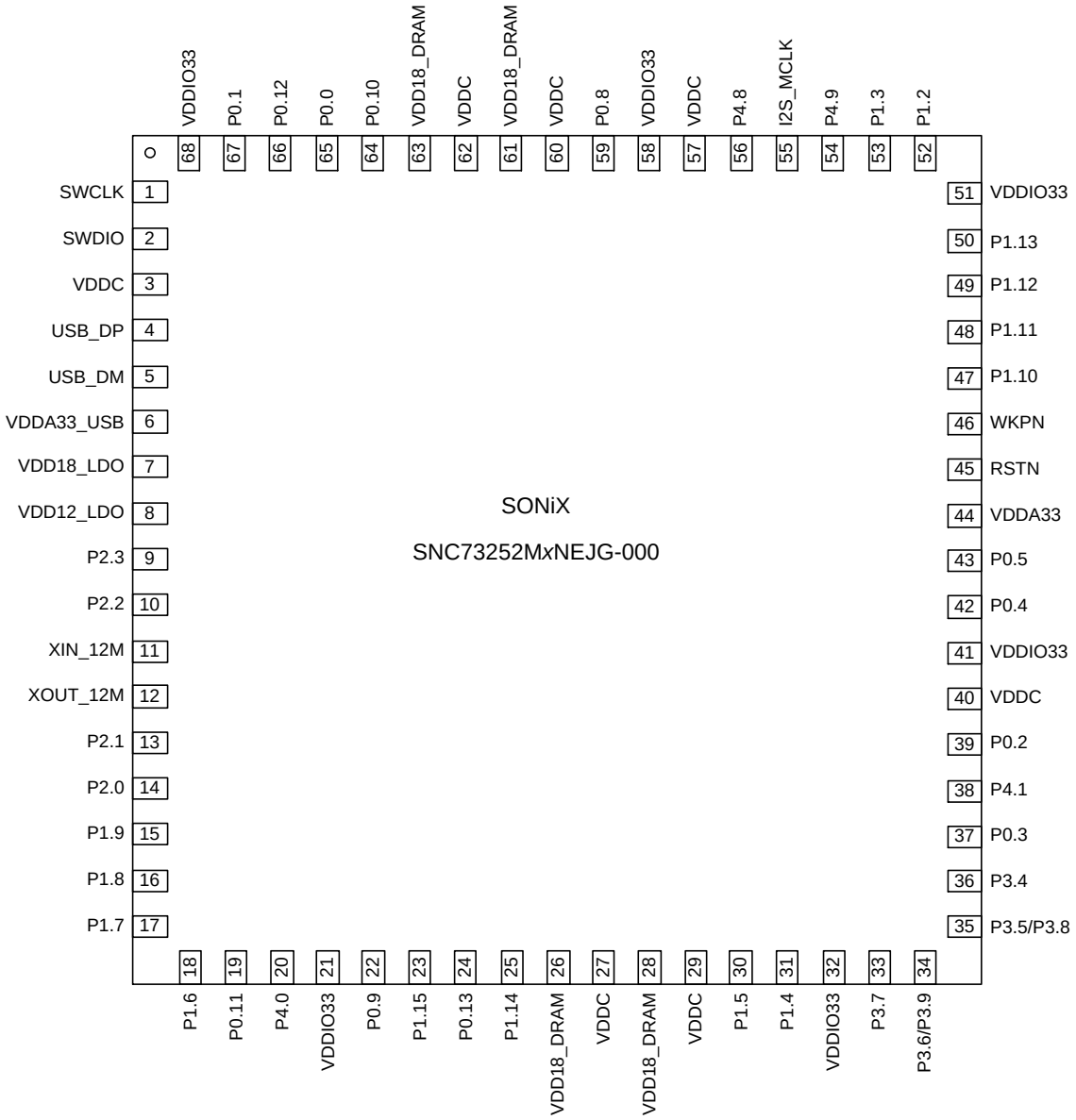


Figure 3–4 SNC73252M*x*NEJG-000 Pin Assignment

3.1.5 SNC73282M*x*UTJG-000

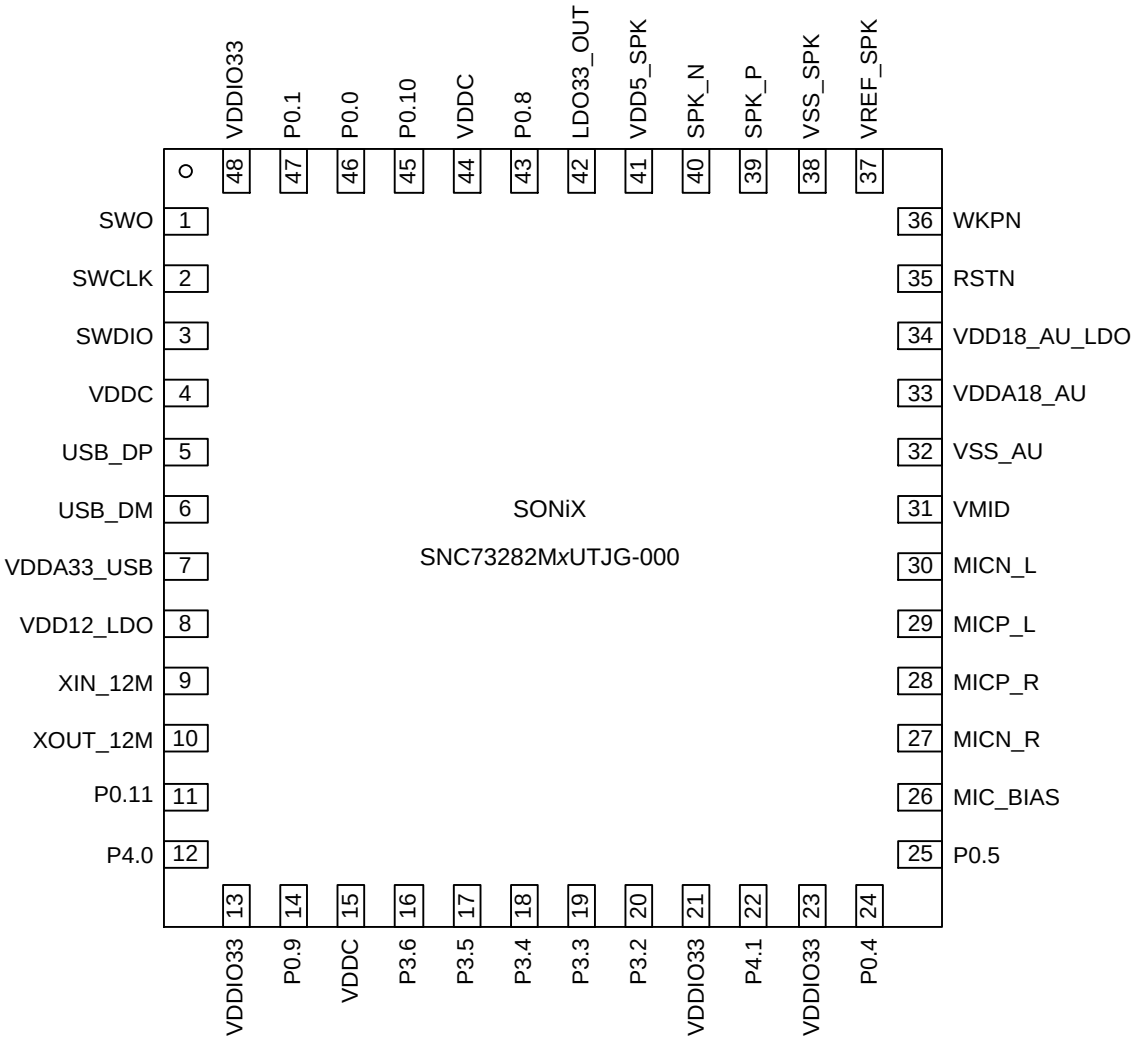


Figure 3–5 SNC73282M*x*UTJG-000 Pin Assignment

3.1.6 SNC73283M*x*UTJG-000

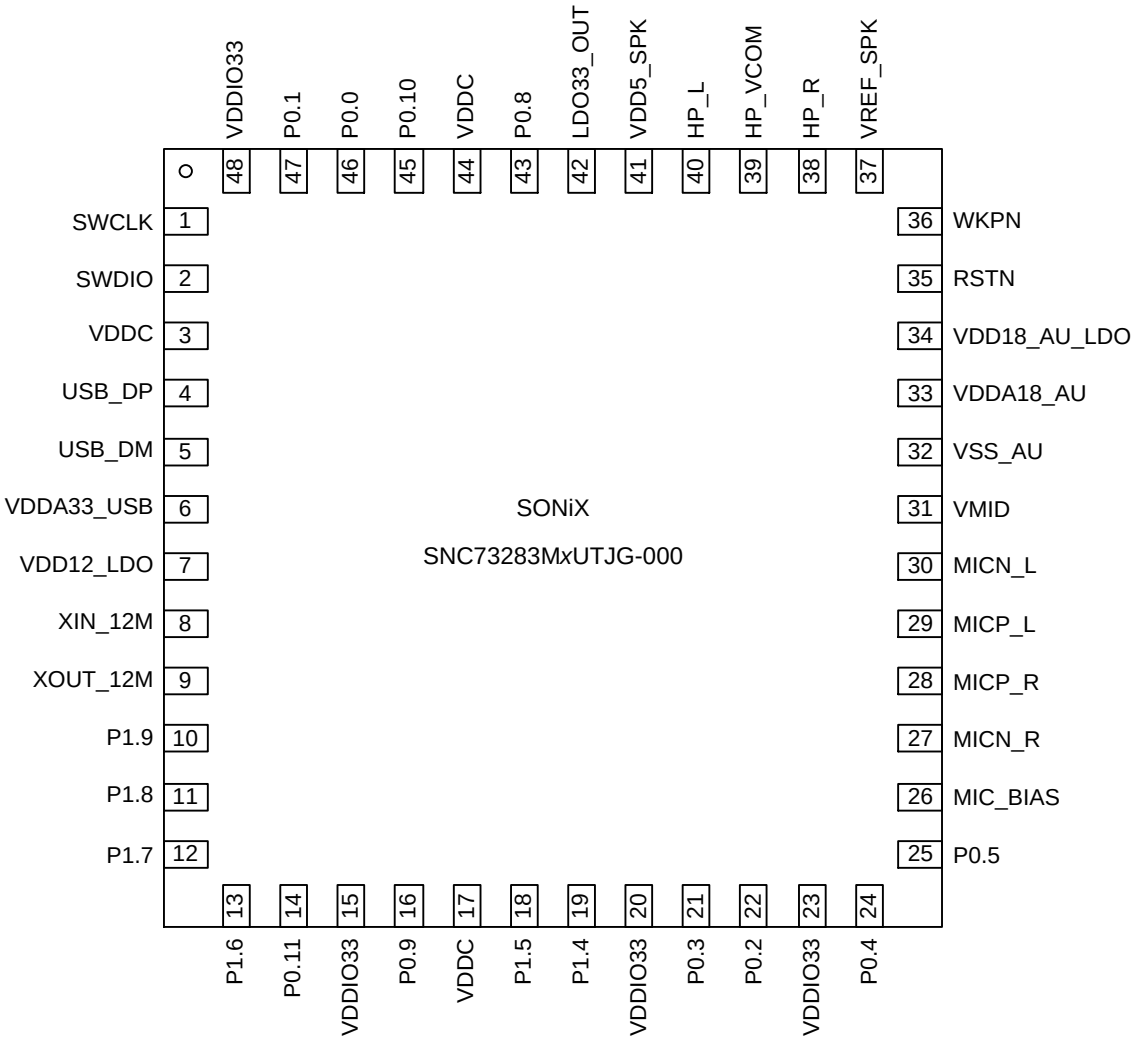


Figure 3–6 SNC73283M*x*UTJG-000 Pin Assignment

3.1.7 SNC73285MxNTJG-000

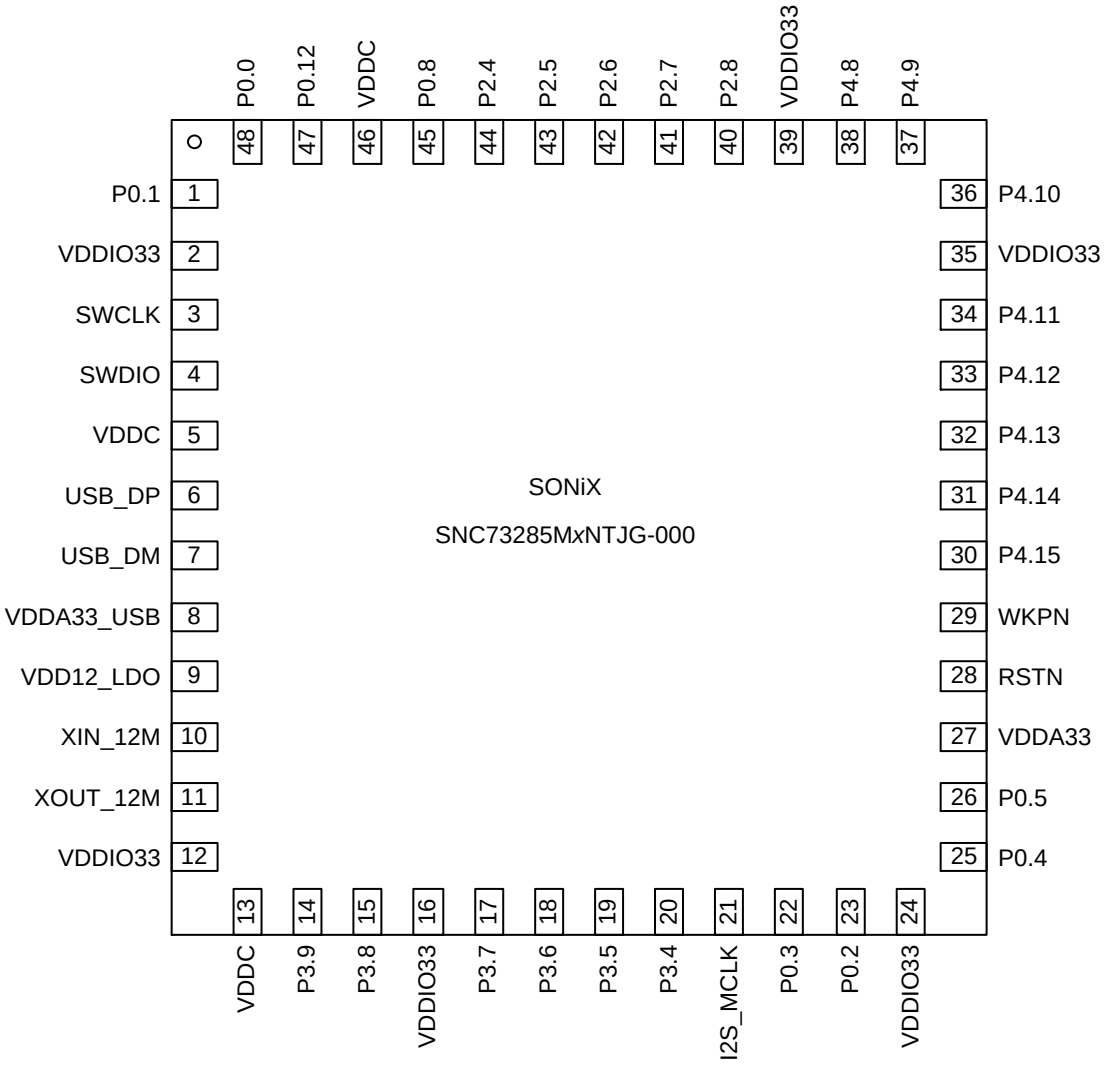


Figure 3–7 SNC73285MxNTJG-000 Pin Assignment

3.1.8 SNC73290MxNTFG-000

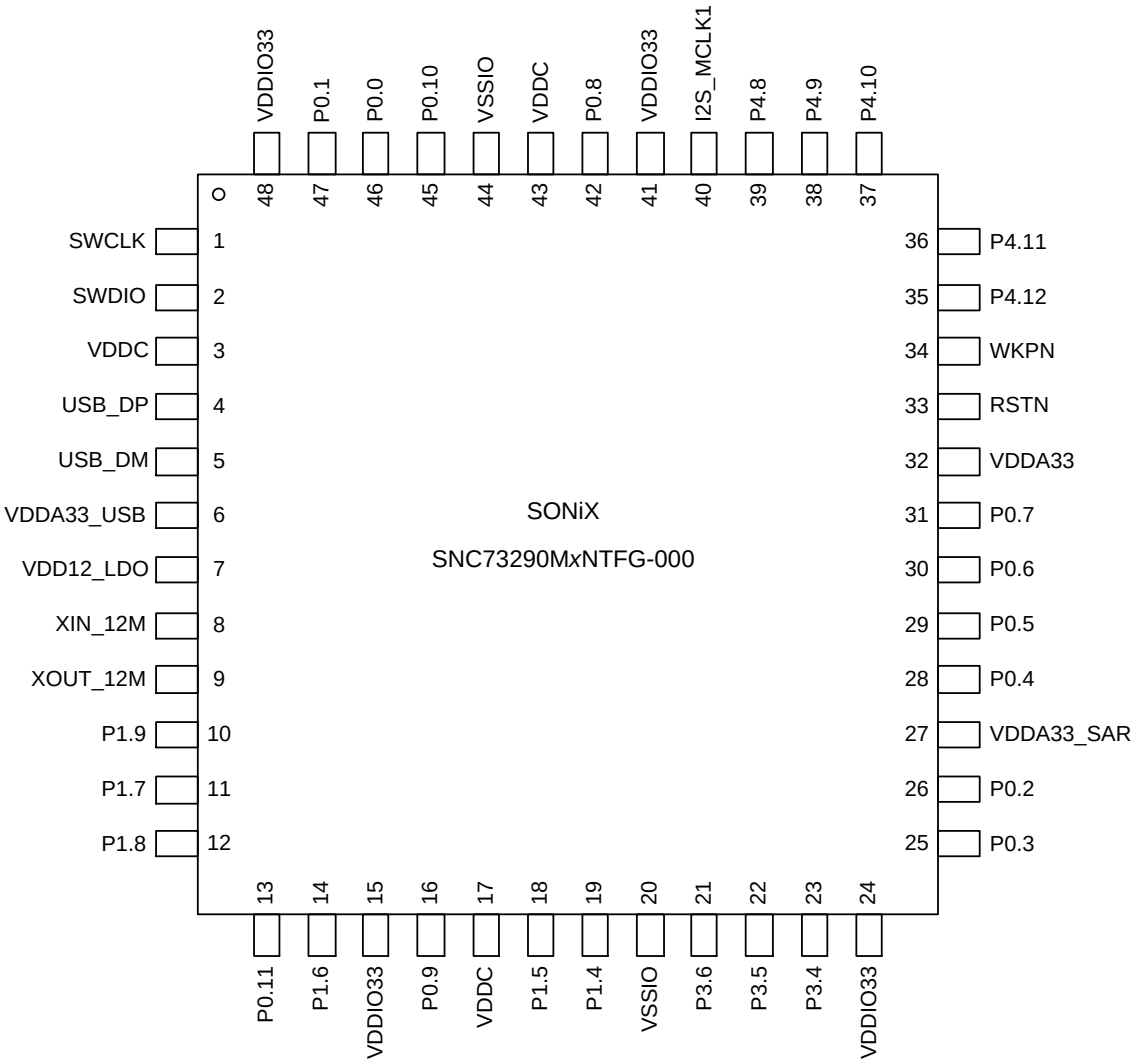


Figure 3–8 SNC73290MxNTFG-000 Pin Assignment

3.2 Pin Description

Table 3–1 Pin Description

Pin Number								Name	Type[4]	Description
SNC73200 MxNLFG-000	SNC73231 MxNGFG-000	SNC73240 MxVHJG-000	SNC73252 MxNEJG-000	SNC73282 MxUTJG-000	SNC73283 MxUTJG-000	SNC73285 MxNTJG-000	SNC73290 MxNTFG-000			
1	–	–	–	–	–	–	–	VDDIO33	P	3.3V I/O power
2	–	–	–	–	–	–	–	P0.14	I/O	GPIO0 pin 14
3	–	–	–	–	–	–	–	P0.15	I/O	GPIO0 pin 15
4	–	–	–	–	–	–	–	P1.0	I/O	GPIO1 pin 0
5	–	–	–	–	–	–	–	P1.1	I/O	GPIO1 pin 1
6	–	–	–	–	–	–	–	VSSIO	GND	I/O ground
7	–	–	–	–	–	–	–	P3.11	I/O	GPIO3 pin 11
8	–	–	–	–	–	–	–	VSSIO	GND	I/O ground
9	–	–	–	–	–	–	–	VDDIO33	P	3.3V I/O power
10	–	–	–	–	–	–	–	P4.4	I/O	GPIO4 pin 4
11	1	1	–	1	–	–	–	SWO	O	Serial wire output trace port/ GPIO4 pin 5
12	2	2	1	2	1	3	1	SWCLK	O	Serial wire clock/ GPIO4 pin 6
13	3	3	2	3	2	4	2	SWDIO	I/O	Serial wire debug bi-directional data. A pull-up resistor, 100 kΩ recommended by ARM, is required./ GPIO4 pin 7
14	–	–	–	–	–	–	–	VDD12_USB	P	1.2V USB power
15	4	4	3	4	3	5	3	VDDC	P	1.2V core power
16	5	5	4	5	4	6	4	USB_D_DP (USB_DP)	A I/O	USB D+ signal; carries USB data to and from the USB 2.0 PHY
17	6	6	5	6	5	7	5	USB_D_DM (USB_DM)	A I/O	USB D- signal; carries USB data to and from the USB 2.0 PHY
18	7	7	6	7	6	8	6	VDDA33_USB	P	3.3V USB analog power
19	–	–	–	–	–	–	–	USB_H_DM	A I/O	USB D- signal; carries USB data to and from the USB 2.0 PHY
20	–	–	–	–	–	–	–	USB_H_DP	A I/O	USB D+ signal; carries USB data to and from the USB 2.0 PHY
21	–	–	–	–	–	–	–	VDD33_LDO	P	3.3V analog/digital power; powered from low dropout regulator (LDO)
22	8	8	7	–	–	–	–	VDD18_LDO/ NC	P –	1.8V analog/digital power; powered from low dropout regulator (LDO)/ No connection (for SNC73231M0NGFG-000 only)

[4] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

Pin Number								Name	Type[4]	Description
SNC73200 MxNLFG-000	SNC73231 MxNGFG-000	SNC73240 MxVHJG-000	SNC73252 MxNEJG-000	SNC73282 MxUTJG-000	SNC73283 MxUTJG-000	SNC73285 MxNTJG-000	SNC73290 MxNTFG-000			
23	–	–	–	–	–	–	–	VSS_LDO	GND	Ground for power pins powered from low dropout regulator (LDO)
24	9	9	8	8	7	9	7	VDD12_LDO	P	1.2V analog/digital power; powered from low dropout regulator (LDO)
25	–	–	–	–	–	–	–	VDDC	P	1.2V core power
26	10	10	9	–	–	–	–	P2.3	I/O	GPIO2 pin 3
27	11	11	10	–	–	–	–	P2.2	I/O	GPIO2 pin 2
28	12	12	11	9	8	10	8	XIN_12M	I	External 12 MHz crystal input
29	13	13	12	10	9	11	9	XOUT_12M	O	External 12 MHz crystal output
30	14	14	13	–	–	–	–	P2.1	I/O	GPIO2 pin 1
31	15	15	14	–	–	–	–	P2.0	I/O	GPIO2 pin 0
32	–	16	–	–	–	–	–	P3.10	I/O	GPIO3 pin 10
33	–	–	–	–	–	–	–	VDDIO33	P	3.3V I/O power
34	–	–	–	–	–	–	–	VSSIO	GND	I/O ground
35	16	17	15	–	10	–	10	P1.9	I/O	GPIO1 pin 9
36	18	19	16	–	11	–	12	P1.8	I/O	GPIO1 pin 8
37	17	18	17	–	12	–	11	P1.7	I/O	GPIO1 pin 7
38	20	21	18	–	13	–	14	P1.6	I/O	GPIO1 pin 6
39	19	20	19	11	14	–	13	P0.11	I/O	GPIO0 pin 11
40	–	–	20	12	–	–	–	P4.0	I/O	GPIO4 pin 0
41	21	22	21	13	15	12	15	VDDIO33	P	3.3V I/O power
42	22	23	22	14	16	–	16	P0.9	I/O	GPIO0 pin 9
43	23	24	23	–	–	–	–	P1.15	I/O	GPIO1 pin 15
44	24	–	24	–	–	–	–	P0.13	I/O	GPIO0 pin 13
45	25	25	25	–	–	–	–	P1.14	I/O	GPIO1 pin 14
46	26	26	26	–	–	–	–	VDD18_DRAM/ NC	P –	1.8V DRAM I/O power/ No connection (for SNC73231M0NGFG-000 only)
47	–	–	27	–	17	–	17	VDDC	P	1.2V core power
48	–	–	28	–	–	–	–	VDD18_DRAM	P	1.8V DRAM I/O power
49	27	27	29	15	–	13	–	VDDC	P	1.2V core power
50	28	28	30	–	18	–	18	P1.5	I/O	GPIO1 pin 5
51	–	29	–	–	–	14	–	P3.9	I/O	GPIO3 pin 9
52	29	30	31	–	19	–	19	P1.4	I/O	GPIO1 pin 4
53	–	31	–	–	–	15	–	P3.8	I/O	GPIO3 pin 8
54	30	–	–	–	–	–	20	VSSIO	GND	I/O ground
55	–	–	32	–	20	16	–	VDDIO33	P	3.3V I/O power
56	–	32	33	–	–	17	–	P3.7	I/O	GPIO3 pin 7
57	31	33	–	16	–	18	21	P3.6	I/O	GPIO3 pin 6
–	–	–	34				–	P3.6/P3.9[5]	I/O	GPIO3 pin 6 or GPIO3 pin 9
58	32	34	–	17	–	19	22	P3.5	I/O	GPIO3 pin 5
–	–	–	35	–	–	–	–	P3.5/P3.8	I/O	GPIO3 pin 5 or GPIO3 pin 8
59	33	35	36	18	–	20	23	P3.4	I/O	GPIO3 pin 4
60	–	–	–	19	–	–	–	P3.3	I/O	GPIO3 pin 3
61	–	–	–	20	–	–	–	P3.2	I/O	GPIO3 pin 2
62	34	37	–	21	–	–	24	VDDIO33	P	3.3V I/O power

[5] P3.6 must pair with P3.5 when configured as I²S1 and P3.9 must pair with P3.8 when configured as I²S3.

Pin Number								Name	Type[4]	Description
SNC73200 MxNLFG-000	SNC73231 MxNGFG-000	SNC73240 MxVHJG-000	SNC73252 MxNEJG-000	SNC73282 MxUTJG-000	SNC73283 MxUTJG-000	SNC73285 MxNTJG-000	SNC73290 MxNTFG-000			
63	–	36	–	–	–	21	–	I2S_MCLK2 (I2S_MCLK)	O	I^2S master clock output 2 (I^2S master clock output)
64	35	38	37	–	21	22	25	P0.3	I/O	GPIO0 pin 3
65	–	–	38	22	–	–	–	P4.1	I/O	GPIO4 pin 1
66	36	39	39	–	22	23	26	P0.2	I/O	GPIO0 pin 2
67	–	–	40	–	–	–	–	VDDC	P	1.2V core power
68	–	–	41	23	23	24	–	VDDIO33	P	3.3V I/O power For QFN packages, also supplies 3.3V analog power for SAR ADC
69	–	–	–	–	–	–	–	VSSIO	GND	I/O ground
70	–	–	–	–	–	–	–	P3.1	I/O	GPIO3 pin 1
71	–	–	–	–	–	–	–	P3.0	I/O	GPIO3 pin 0
72	37	40	–	–	–	–	–	P2.15	I/O	GPIO2 pin 15
73	40	43	–	–	–	–	–	P2.14	I/O	GPIO2 pin 14
74	38	41	–	–	–	–	–	P2.13	I/O	GPIO2 pin 13
75	41	44	–	–	–	–	–	P2.12	I/O	GPIO2 pin 12
76	39	42	–	–	–	–	–	P2.11	I/O	GPIO2 pin 11
77	42	45	–	–	–	–	–	P2.10	I/O	GPIO2 pin 10
78	43	46	–	–	–	–	27	VDDA33_SAR	P	3.3V SAR ADC analog power
79	44	47	42	24	24	25	28	P0.4	I/O	GPIO0 pin 4
80	45	48	43	25	25	26	29	P0.5	I/O	GPIO0 pin 5
81	46	49	–	–	–	–	30	P0.6	I/O	GPIO0 pin 6; enables SDCARD0 and NAND flash, or SDCARD1
82	47	50	–	–	–	–	31	P0.7	I/O	GPIO0 pin 7
83	–	–	–	–	–	–	–	P4.2	I/O	GPIO4 pin 2
84	–	–	–	–	–	–	–	P4.3	I/O	GPIO4 pin 3
85	–	51	–	–	–	–	–	NC	–	No connection
86	–	52	–	–	–	–	–	NC	–	No connection
87	48	53	44	–	–	27	32	VDDA33	P	3.3V analog power
–	–	56	–	26	26	–	–	MIC_BIAS	I/O	Microphone bias circuit power supply
–	–	–	–	27	27	–	–	MICN_R	I/O	Microphone right channel negative input
–	–	–	–	28	28	–	–	MICP_R	I/O	Microphone right channel positive input.
–	–	–	–	29	29	–	–	MICP_L	I/O	Microphone left channel positive input.
–	–	–	–	30	30	–	–	MICN_L	I/O	Microphone left channel negative input.
–	–	57	–	–	–	–	–	MIC_P	I	Microphone positive input
–	–	58	–	–	–	–	–	MIC_N	I	Microphone negative input
–	–	59	–	31	31	–	–	VMID	I/O	SD-ADC VMID pin
–	–	–	–	32	32	–	–	VSS_AU	GND	Ground for audio codec
–	–	60	–	–	–	–	–	VSSA18_ADC	GND	Audio ADC ground
–	–	–	–	33	33	–	–	VDDA18_AU	P	1.8V analog power input for audio codec
–	–	61	–	34	34	–	–	VDD18_AU_LDO	P	1.8V power for audio codec; powered from low dropout regulator (LDO)
88	49	54	45	35	35	28	33	RSTN	I	Reset pin
89	50	55	46	36	36	29	34	WKPN	I	Wakeup pin

Pin Number								Name	Type[4]	Description
SNC73200 MxNLFG-000	SNC73231 MxNGFG-000	SNC73240 MxVHJG-000	SNC73252 MxNEJG-000	SNC73282 MxUTJG-000	SNC73283 MxUTJG-000	SNC73285 MxNTJG-000	SNC73290 MxNTFG-000			
–	–	–	–	37	37	–	–	VREF_SPK	I/O	Reference voltage for speaker driver
–	–	–	–	–	38	–	–	HP_R	O	Headphone right channel output
–	–	–	–	–	39	–	–	HP_VCOM	O	Headphone VCOM output
–	–	–	–	–	40	–	–	HP_L	O	Headphone left channel output
–	–	–	–	38	–	–	–	VSS_SPK	GND	Ground for speaker driver
–	–	62	–	39	–	–	–	SPK_P	O	Speaker positive output
–	–	63	–	40	–	–	–	SPK_N	O	Speaker negative output
–	–	–	–	41	41	–	–	VDD5_SPK	P	5V speaker power
–	–	64	–	–	–	–	–	VDD5	P	5V PWM driver power
–	–	65	–	42	42	–	–	LDO33_OUT	P	3.3V LDO power output
90	–	–	–	–	–	30	–	P4.15	I/O	GPIO4 pin 15
91	–	–	–	–	–	31	–	P4.14	I/O	GPIO4 pin 14
92	–	–	–	–	–	32	–	P4.13	I/O	GPIO4 pin 13
93	51	–	–	–	–	33	35	P4.12	I/O	GPIO4 pin 12
94	52	–	–	–	–	34	36	P4.11	I/O	GPIO4 pin 11
95	–	–	51	–	–	35	–	VDDIO33	P	3.3V I/O power
96	–	–	–	–	–	–	–	VSSIO	GND	I/O ground
97	53	–	–	–	–	36	37	P4.10	I/O	GPIO4 pin 10
98	54	–	54	–	–	37	38	P4.9	I/O	GPIO4 pin 9
99	56	–	55	–	–	–	40	I2S_MCLK1 (I2S_MCLK)	O	I^2S master clock output 1 (I^2S master clock output)
100	55	–	56	–	–	38	39	P4.8	I/O	GPIO4 pin 8
101	57	67	57	–	–	–	–	VDDC	P	1.2V core power
102	58	66	58	–	–	39	41	VDDIO33	P	3.3V I/O power
103	–	–	–	–	–	–	–	VSSIO	GND	I/O ground
104	59	68	–	–	–	–	–	P2.9	I/O	GPIO2 pin 9
105	60	69	–	–	–	40	–	P2.8	I/O	GPIO2 pin 8
106	61	70	–	–	–	41	–	P2.7	I/O	GPIO2 pin 7
107	62	71	–	–	–	42	–	P2.6	I/O	GPIO2 pin 6
108	63	72	–	–	–	43	–	P2.5	I/O	GPIO2 pin 5
109	64	73	–	–	–	44	–	P2.4	I/O	GPIO2 pin 4
110	65	74	59	43	43	45	42	P0.8	I/O	GPIO0 pin 8
111	66	75	53	–	–	–	–	P1.3	I/O	GPIO1 pin 3
112	67	76	52	–	–	–	–	P1.2	I/O	GPIO1 pin 2
113	–	–	60	44	44	46	–	VDDC	P	1.2V core power
114	68	77	50	–	–	–	–	P1.13	I/O	GPIO1 pin 13
115	69	78	49	–	–	–	–	P1.12	I/O	GPIO1 pin 12
116	70	79	48	–	–	–	–	P1.11	I/O	GPIO1 pin 11
–	–	–	61	–	–	–	–	VDD18_DRAM	P	1.8V DRAM power
117	71	80	47	–	–	–	–	P1.10	I/O	GPIO1 pin 10
–	–	–	62	–	–	–	–	VDDC	P	1.2V core power
118	–	–	–	–	–	–	43	VDDC	P	1.2V core power
–	–	–	63	–	–	–	–	VDD18_DRAM	P	1.8V DRAM power
119	72	81	64	45	45	–	45	P0.10	I/O	GPIO0 pin 10
120	73	82	65	46	46	48	46	P0.0	I/O	GPIO0 pin 0
121	–	–	66	–	–	47	–	P0.12	I/O	GPIO0 pin 12
122	75	83	67	47	47	1	47	P0.1	I/O	GPIO0 pin 1
123	80	88	68	48	48	2	48	VDDIO33	P	3.3V I/O power
124	74	–	–	–	–	–	44	VSSIO	GND	I/O ground
125	77	85	–	–	–	–	–	P3.15	I/O	GPIO3 pin 15
126	76	84	–	–	–	–	–	P3.14	I/O	GPIO3 pin 14

Pin Number								Name	Type[4]	Description
SNC73200 MxNLFG-000	SNC73231 MxNGFG-000	SNC73240 MxVHJG-000	SNC73252 MxNEJG-000	SNC73282 MxUTJG-000	SNC73283 MxUTJG-000	SNC73285 MxNTJG-000	SNC73290 MxNTFG-000			
127	79	87	–	–	–	–	–	P3.13	I/O	GPIO3 pin 13
128	78	86	–	–	–	–	–	P3.12	I/O	GPIO3 pin 12
–	–	89	69	49	49	49	–	EPAD	GND	The ePad on the bottom of the package must be soldered to the ground plane of the PCB.

NOTE All pins are pull-up (PU). To pull-up a signal to the opposite supply rail, a 1 kΩ resistor is required.

3.3 Pin Multiplexing

Extensive use of pin multiplexing (pinmux) allows reusing the same pin for different purposes. Pinmux is controlled by a combination of hardware configuration at device reset and software programmable register settings.
Interrupt mode is supported in the pinmux GPIO. When the pinmux GPIO mode is selected, there is an IRQ connected between the IP and INTC. Modes and data must all be programmed and then poll for the status of each upper level pinmux GPIO pin when a pin is set to the GPIO input mode.

3.3.1 Pinmux Table

Pin multiplexing allows I/O pins to be set as a pin of another function. Table 3–2 lists all pins with pinmux options, and Table 3–3 provides descriptions of the pins when being multiplexed.

Table 3–2 Pinmux Overview[6] [7]

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P0.0	I2C0_SCL	–	–	–	–	–	–
P0.1	I2C0_SDA	–	–	–	–	–	–
P0.2	UART0_TXD	–	–	–	–	–	CT32B7_PWM2[8]
P0.3	UART0_RXD	–	–	–	–	–	CT32B7_PWM1[8]
P0.4	AIN0	–	–	–	–	–	CT32B7_PWM0[8]
P0.5	AIN1	–	–	–	–	–	CT32B6_PWM2[8]
P0.6	AIN2	–	–	–	–	–	CT32B6_PWM1[8]
P0.7	AIN3	–	–	–	–	–	CT32B6_PWM0[8]
P0.8	SPIFC_CS	–	SPI0DMA_CS	–	–	–	–
P0.9	SPIFC_CLK	–	SPI0DMA_SCLK	–	–	–	–
P0.10	SPIFC_MISO	–	SPI0DMA_MISO	–	–	–	–
P0.11	SPIFC_MOSI	–	SPI0DMA_MOSI	–	–	–	–
P0.12	SPIFC_D2/WP	–	SPI0DMA_MISO2	–	–	–	CT32B0_PWM1[8]
P0.13	SPIFC_D3	–	SPI0DMA_MISO3	–	–	–	CT32B0_PWM0[8]
P0.14	–	CLKOUT	–	SPI0_CS	–	–	–
P0.15	–	–	NAND_CS	SPI0_SCLK	–	–	–
P1.0	–	–	NAND_RB	SPI0_MISO	–	–	–
P1.1	–	–	NAND_ALE	SPI0_MOSI	–	–	–
P1.2	–	CIS_VSYNC	NAND_WE	LCD_HSYNC/ 8080_RE[9]	–	–	–
P1.3	–	CIS_HSYNC	NAND_RE	LCD_VSYNC/ 8080_WE[9]	–	–	–
P1.4	SD0_CLK	CIS_MCLK	NAND_WP	LCD_DE/ 8080_CS[9]	SPI0DMA_CS[10]	–	CT32B7_PWM2
P1.5	SD0_CMD	CIS_PCLK	NAND_CLE	LCD_DCLK/ 8080_A0[9]	SPI0DMA_SCLK[10]	–	CT32B7_PWM1
P1.6	SD0_D0	CIS_D0	NAND_D0	LCD_D0/ 8080_D0[9]	SPI0DMA_MISO[10]	–	CT32B7_PWM0
P1.7	SD0_D1	CIS_D1	NAND_D1	LCD_D1/ 8080_D1[9]	SPI0DMA_MOSI[10]	–	CT32B6_PWM2
P1.8	SD0_D2	CIS_D2	NAND_D2	LCD_D2/ 8080_D2[9]	SPI0DMA_MISO2[10]	–	CT32B6_PWM1

6 "–" represents reserved pinmux options.
7 If multiple functions of a pin are enabled, the pin will function in the mode of the lowest number.
8 To configure the pins for this I/O function, refer to Pin Control Register (SYS0_PINCTRL) in *SNC7320_reg_vx.xx* for detailed settings.
9 Refer to The Control Register (SYS0_PINCTRL[1]) in *SNC7320_reg_vx.xx* for detailed settings.
10 Refer to The Control Register (SYS0_PINCTRL[8]) in *SNC7320_reg_vx.xx* for detailed settings.

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P1.9	SD0_D3	CIS_D3	NAND_D3	LCD_D3/ 8080_D3[9]	SPI0DMA_MISO3[10]	–	CT32B6_PWM0
P1.10	–	CIS_D4	NAND_D4	LCD_D4/ 8080_D4[9]	–	–	–
P1.11	–	CIS_D5	NAND_D5	LCD_D5/ 8080_D5[9]	–	–	–
P1.12	–	CIS_D6	NAND_D6	LCD_D6/ 8080_D6[9]	–	–	–
P1.13	–	CIS_D7	NAND_D7	LCD_D7/ 8080_D7[9]	–	–	–
P1.14	SDIO_CLK	–	–	–	I2S4_MCLK	–	–
P1.15	SDIO_CMD	–	–	–	I2S4_DI	–	–
P2.0	SDIO_D0	–	–	–	I2S4_DO	–	–
P2.1	SDIO_D1	–	–	–	I2S4_BCLK	–	–
P2.2	SDIO_D2	–	–	–	I2S4_WS	–	–
P2.3	SDIO_D3	–	–	–	–	–	–
P2.4	LCD_HSYNC	8080_RD	–	–	I2S4_MCLK[8]	–	CT32B5_PWM2
P2.5	LCD_VSYNC	8080_WR	–	–	I2S4_DI[8]	–	CT32B5_PWM1
P2.6	LCD_DE	8080_CS	–	–	I2S4_DO[8]	–	CT32B5_PWM0
P2.7	LCD_DCLK	8080_A0	–	–	I2S4_BCLK[8]	–	CT32B4_PWM2
P2.8	LCD_D0	8080_D0	–	–	I2S4_WS[8]	–	–
P2.9	LCD_D1	8080_D1	–	–	–	–	–
P2.10	LCD_D2	8080_D2	–	–	–	–	–
P2.11	LCD_D3	8080_D3	–	–	–	–	–
P2.12	LCD_D4	8080_D4	–	–	–	–	–
P2.13	LCD_D5	8080_D5	–	–	–	–	–
P2.14	LCD_D6	8080_D6	–	–	–	–	–
P2.15	LCD_D7	8080_D7	–	–	–	–	–
P3.0	LCD_D8	8080_D8	NAND_CE[11]	–	–	–	–
P3.1	LCD_D9	8080_D9	NAND_RB[11]	–	–	–	–
P3.2	LCD_D10	8080_D10	NAND_ALE[11]	–	I2S4_MCLK[8]	I2C2_SCL	–
P3.3	LCD_D11	8080_D11	NAND_WE[11]	–	I2S4_DI[8]	I2C2_SDA	–
P3.4	LCD_D12	8080_D12	NAND_RE[11]	–	I2S4_DO[8]	I2S1_DI	–
P3.5	LCD_D13	8080_D13	NAND_WP[11]	SD0_CLK[8]	I2S4_BCLK[8]	I2S1_BCLK	–
P3.6	LCD_D14	8080_D14	NAND_CLE[11]	SD0_CMD[8]	I2S4_WS[8]	I2S1_WS	–
P3.7	LCD_D15	8080_D15	NAND_D0[11]	SD0_D0[8]	–	I2S3_DO	–
P3.8	LCD_D16	–	NAND_D1[11]	SD0_D1[8]	–	I2S3_BCLK	–
P3.9	LCD_D17	–	NAND_D2[11]	SD0_D2[8]	–	I2S3_WS	–

[11] Refer to The Control Register (SYS0_PINCTRL[0]) in *SNC7320_reg_vx.xx* for detailed settings.

Default	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
P3.10	–	–	NAND_D3[11]	SD0_D3[8]	–	–	CT32B4_PWM1
P3.11	–	–	NAND_D4[11]	–	–	–	CT32B4_PWM0
P3.12	SPI1_CS	–	NAND_D5[11]	SPI1DMA_CS	–	CT32B0_CAP0	CT32B3_PWM2
P3.13	SPI1_CLK	–	NAND_D6[11]	SPI1DMA_SCLK	–	CT32B1_CAP0	CT32B3_PWM1
P3.14	SPI1_MISO	–	NAND_D7[11]	SPI1DMA_MISO	–	CT32B2_CAP0	CT32B3_PWM0
P3.15	SPI1_MOSI	–	–	SPI1DMA_MOSI	–	CT32B3_CAP0	CT32B2_PWM2
P4.0	UART1_TXD	–	–	SPI1DMA_MISO2	–	CT32B4_CAP0	CT32B2_PWM1
P4.1	UART1_RXD	–	–	SPI1DMA_MISO3	–	CT32B5_CAP0	CT32B2_PWM0
P4.2	AIN4	–	–	–	–	CT32B6_CAP0	CT32B1_PWM2
P4.3	AIN5	–	–	–	–	CT32B7_CAP0	CT32B1_PWM1
P4.4	–	–	–	–	–	–	CT32B1_PWM0
SWO	P4.5	–	–	–	–	–	CT32B0_PWM2
SWCLK	P4.6	–	–	–	–	–	CT32B0_PWM1
SWDIO	P4.7	–	–	–	–	–	CT32B0_PWM0
P4.8	I2C1_SCL	–	–	–	–	–	CT32B3_PWM2[8]
P4.9	I2C1_SDA	–	–	–	–	–	CT32B3_PWM1[8]
P4.10	I2S0_DI	–	–	–	–	–	CT32B3_PWM0[8]
P4.11	I2S0_BCLK	–	–	–	–	–	CT32B2_PWM2[8]
P4.12	I2S0_WS	CIS_D4[8]	–	–	–	–	–
P4.13	I2S2_DO	CIS_D5[8]	–	–	–	–	–
P4.14	I2S2_BCLK	CIS_D6[8]	–	–	–	–	–
P4.15	I2S2_WS	CIS_D7[8]	–	–	–	–	–

Table 3–3 Function Description of Pinmux

Function	Name	Type[12]	Description
GPIO	P*x.x*[13]	I/O	General purpose input output
I²C	I2C*n*_SCL	O	I²C serial clock or GPIO Output with open-drain; input depends on GPIO*n*_CFG.
	I2C*n*_SDA	I/O	I²C serial data or GPIO Output with open-drain; input depends on GPIO*n*_CFG.
UART	UART*n*_TXD	O	UART serial transmit data or GPIO
	UART*n*_RXD	I	UART serial receive data; GPIO configuration depends on GPIO*n*_CFG or GPIO
SAR ADC	AIN*n*	I	ADC input channel
SPI	SPI*n*_CLK	I/O[14]	SPI serial clock GPIO configuration in slave mode depends on GPIO*n*_CFG or GPIO
	SPI*n*_CS	I/O[14]	SPI slave select/SSI frame sync in master mode/SPI slave select in slave mode; GPIO configuration in slave mode depends on GPIO*x*_CFG or GPIO
	SPI*n*_MOSI	I/O[14]	SPI master out slave in; GPIO configuration in slave mode depends on GPIO*n*_CFG or GPIO
	SPI*n*_MISO	I/O[15]	SPI master in slave out; GPIO configuration in master mode depends on GPIO*n*_CFG or GPIO
	SPI*n*DMA_CS	O	SPI chip select
	SPI*n*DMA_SCLK	O	SPI clock
	SPI*n*DMA_MISO*x*	I	SPI master in slave out
	SPI*n*DMA_MOSI	O	SPI master out slave in
SD0/ SD1/SDIO	SD0_CLK	O	SD0 clock output or GPIO
	SD0_CMD	O	SD0 command or GPIO
	SD0_D*x*	I/O	SD0 data or GPIO
	SD0_WP	I	SD0 write protection, active low or GPIO
	SD0_CD	I	SD0 card detect, active high or GPIO
	SDIO_CLK	O	SD/SDIO (SD1) clock output
	SDIO_CMD	O	SD/SDIO (SD1) command
	SDIO_D*x*	I/O	SD/SDIO (SD1) data
I²S	I2S*x*_DI	I	I²S data input or GPIO
	I2S*x*_DO	O	I²S data output or GPIO
	I2S*x*_BCLK	I/O	I²S bit clock or GPIO. Bit clock can be programmed as a master or a slave.
	I2S*x*_MCLK	I/O	I²S master clock or GPIO. Master clock can be generated from an external clock source or be an internal generated clock.
	I2S*x*_WS	I/O	I²S word select or GPIO.
Timer	CT32B*n*_CAP0	I	32-bit timer/counter capture channel
PWM	CT32B*n*_PWM*x*	O	Pulse width modulation data output
TFT-RGB/ 8080 MCU Interface	LCD_Dx/ 8080_Dx	O	TFT-LCD data bus/ 8080 CPU data bus or GPIO
	LCD_HSYNC/ 8080_RD	O	TFT-LCD horizontal/line synchronization/ 8080 CPU read; active low
	LCD_VSYNC/ 8080_WR	O	TFT-LCD vertical/frame synchronization/ 8080 CPU write; active low
	LCD_DE/ 8080_CS	O	TFT-LCD data enable/ 8080 CPU chip select; active low
	LCD_DCLK/ 8080_A0	O	TFT-LCD clock/ 8080 CPU address 0
	SPIFC_CS	O	SPI NOR flash chip select

[12] The types listed below represent pin type of the primary function. For pins with GPIO as pinmux option, the pin type is I/O when being used as GPIO.
[13] *x* = a variable number
[14] Output in master mode; input in slave mode
[15] Input in master mode; output in slave mode

Function	Name	Type[1][2]	Description
SPI NOR Flash Controller	SPIFC_CLK	O	SPI NOR flash clock output
	SPIFC_MISO	I	SPI NOR flash master in slave out
	SPIFC_MOSI	O	SPI NOR flash master out slave in
	SPIFC_D2/WP	I/O	SPI NOR flash 4 x I/O mode, data pin or write protection
	SPIFC_D3	I/O	SPI NOR flash 4 x I/O mode, data pin
NAND Flash Controller	NAND_CS	O	NAND flash
	NAND_RB	O	NAND flash ready/busy output
	NAND_ALE	O	NAND flash address latch enable
	NAND_WE	O	NAND flash write enable
	NAND_RE	O	NAND flash read enable
	NAND_WP	O	NAND flash write protect
	NAND_CLE	O	NAND flash command latch enable
	NAND_Dx	I/O	NAND flash data input/output
CMOS Image Sensor Interface	CIS_VSYNC	I	CMOS image sensor output vertical sync
	CIS_HSYNC	I	CMOS image sensor output horizontal sync
	CIS_MCLK	O	CMOS image sensor master clock
	CIS_PCLK	I	CMOS image sensor pixel clock
	CIS_D*x*	I	CMOS image sensor output data

4 Central Processing Unit (CPU)

4.1 Dual-core Architecture

The SNC7320 Series integrates two ARM Cortex-M3 processors, Core 0 and Core 1. Both cores can access the 256 KB shared AHB RAM, 4 KB mailbox RAM and all peripherals. The Core 0 takes the role of a master core which controls the operation mode of the system and boots the code of Core 1. The Core 1 acts as a slave core, and is an independent subsystem. Two cores interact by the inter-process communication (IPC) protocol. The most important function of the two cores is to separate two subsystems of the SNC7320 Series, not only to increase the performance of the system, but also to reduce the code complexity of each core.

4.1.1 ARM Cortex-M3 Processor

The ARM Cortex-M3 is a low-power processor that features low gate count, low interrupt latency, and low-cost debugging. It is intended for embedded applications requiring fast interrupt response features. The processor implements the ARM architecture v7-M. The processor incorporates:

- Memory Protect Unit (MPU)
- Nested Vectored Interrupt Controller (NVIC)
- Serial wire debug (SWD) port with Trace Port Interface Unit (TPIU) and Data Watchpoint and Trace (DWT) debug protocol

For complete details on the ARM Cortex-M3, please refer to the technical reference manual available at https://www.arm.com/products/silicon-ip-cpu/cortex-m/cortex-m3.

4.1.2 Inter-processor Communication (IPC)

The communication between the two cores is achieved with IPC which is implemented with a ring buffer of software framework. Messages are passed through queues using a cyclic share buffer as message box RAM (0x2000_0000 to 0x2000_1000). A queue is filled with MsgBoxs from start to end addresses. Two cores use these share RAM to inter-change data and commands.

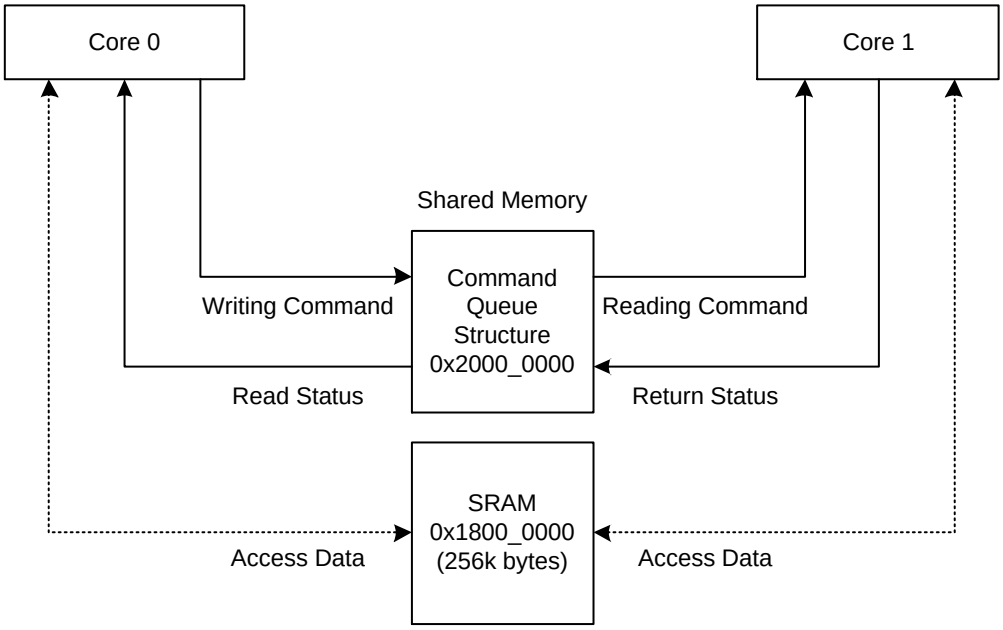


Figure 4–1 Inter-processor Communication Block Diagram

4.2 Memory Protect Unit (MPU)

The Memory Protect Unit (MPU) is a component for memory protection of the SNC7320 Series. The processors support the standard ARMv7 Protected Memory System Architecture model.
Features of the MPU include:

- Protection regions
- Overlapping protection regions with ascending region priority
  - 7 = Highest priority
  - 0 = Lowest priority
- Access permissions
- Exporting memory attributes to the system

The MPU mismatches and permission violations invoke the programmable-priority MemManage fault handler. For more information, see the ARMv7-M Architecture Reference Manual.
Major functions of the MPU include:

- Enforce privilege rules
- Separate processes
- Enforce access rules

Please refer to the official website of ARM for more details:
https://developer.arm.com/documentation/dui0552/a/cortex-m3-peripherals/optional-memory-protection-unit?lang=en

4.3 Nested Vectored Interrupt Controller (NVIC)

The nested vectored interrupt controller (NVIC) provides a software interface to the interrupt system. Based on the ARM subsystem, the SNC7320 Series has one level of interrupts: Interrupt Request (IRQ) for general interrupts.

The sequence of events for the interrupts is:

1. INTC collects interrupt signals from various modules
2. INTC generates the IRQ interrupt signals to the ARM

The properties of all interrupt signals can be configured by the INTC registers which are mapped to the AHB peripherals. The INTC supports up to 57 interrupt sources listed in Table 4–1. The software initializes edge or level sensitivity and checks the source of the interrupt when it receives IRQ events from the ARM. The registers of INTC are at base address 0xE000_E000.

Features of the NVIC are:

- Up to 64 vectored interrupts
- Programmable priority levels of 0–7 for each interrupt. Higher levels correspond to a lower priority. Thus, level 0 is the highest interrupt priority with low-latency exception for interrupt handling.
- Level and pulse detection of interrupt signals
- Dynamic reprioritization of interrupts
- Grouping of priority values into group priority and sub-priority fields
- Interrupt tail-chaining
- External non-maskable interrupt (NMI)

Table 4–1 is a list of interrupt and exception vectors including the 56 interrupt sources (IRQ) with IRQ numbers.

Table 4–1 Interrupt and Exception Vectors

Execution No.	Priority	Function	Description	Address Offset[16]
0	–	–	Reserved	–
1	-3	Reset	Reset	0x0000 0004
2	-2	NMI handler	Non-maskable interrupt; shared with WDT	0x0000 0008
3	-1	HardFault handler	All class of fault	0x0000 000C
4	Settable	MemManage handler	MPU fault	0x0000 0010
5	Settable	BusFault handler	Bus fault	0x0000 0014
6	Settable	UsageFault handler	Usage fault	0x0000 0018
7–10	–	–	Reserved	–
11	Settable	SVCCall	Supervisor call	0x0000 0018
12	Settable	DebugMon handler	Debug fault	0x0000 0030
13	–	–	Reserved	–
14	Settable	PendSV	Pendable service call	0x0000 0038
15	Settable	SysTick	System tick	0x0000 003C
16	Settable	IRQ0	Dual core interrupt from Core 0	0x0000 0040
17	Settable	IRQ1	Dual core interrupt from Core 1	0x0000 0044
18	–	–	Reserved	–
19	Settable	IRQ3	Wakeup33	0x0000 004C
20	Settable	IRQ4	PPU vertical blanking	0x0000 0050
21	Settable	IRQ5	PPU horizontal blanking	0x0000 0054
22	Settable	IRQ6	USB device	0x0000 0058
23	Settable	IRQ7	USB host 0	0x0000 005C
24	Settable	IRQ8	USB host 1	0x0000 0060
25	Settable	IRQ9	SAR ADC	0x0000 0064
26	Settable	IRQ10	CIS Vsync	0x0000 0068
27	Settable	IRQ11	CIS DMA	0x0000 006C
28	Settable	IRQ12	JPEG encoder end	0x0000 0070
29	Settable	IRQ13	JPEG decoder DMA in	0x0000 0074
30	Settable	IRQ14	JPEG decoder DMA out	0x0000 0078
31	Settable	IRQ15	SDIO interrupt	0x0000 007C
32	Settable	IRQ16	SDIO DMA	0x0000 0080
33	Settable	IRQ17	SD/NAND ECC	0x0000 0084

[16] "–" = Unknown

Execution No.	Priority	Function	Description	Address Offset[16]
34	Settable	IRQ18	SD/NAND DMA	0x0000 0088
35	Settable	IRQ19	IDMA0	0x0000 008C
36	Settable	IRQ20	IDMA1	0x0000 0090
37	Settable	IRQ21	I²S0 DMA	0x0000 0094
38	Settable	IRQ22	I2S1 DMA	0x0000 0098
39	Settable	IRQ23	I²S2 DMA	0x0000 009C
40	Settable	IRQ24	I2S3 DMA	0x0000 00A0
41	Settable	IRQ25	I²S4	0x0000 00A4
42	Settable	IRQ26	GPIO0	0x0000 00A8
43	Settable	IRQ27	GPIO1	0x0000 00AC
44	Settable	IRQ28	GPIO2	0x0000 00B0
45	Settable	IRQ29	GPIO3	0x0000 00B4
46	Settable	IRQ30	GPIO4	0x0000 00B8
47	Settable	IRQ31	I²C0	0x0000 00BC
48	Settable	IRQ32	I²C1	0x0000 00C0
49	Settable	IRQ33	I2C2	0x0000 00C4
50	Settable	IRQ34	SPI0	0x0000 00C8
51	Settable	IRQ35	SPI1	0x0000 00CC
52	Settable	IRQ36	UART0	0x0000 00D0
53	Settable	IRQ37	UART1	0x0000 00D4
54	Settable	IRQ38	CT32B0 timer	0x0000 00D8
55	Settable	IRQ39	CT32B1 timer	0x0000 00DC
56	Settable	IRQ40	CT32B2 timer	0x0000 00E0
57	Settable	IRQ41	CT32B3 timer	0x0000 00E4
58	Settable	IRQ42	CT32B4 timer	0x0000 00E8
59	Settable	IRQ43	CT32B5 timer	0x0000 00EC
60	Settable	IRQ44	CT32B6 timer	0x0000 00F0
61	Settable	IRQ45	CT32B7 timer	0x0000 00F4
62	Settable	IRQ46	SPI0 DMA	0x0000 00F8
63	Settable	IRQ47	SPI0 ECC	0x0000 00FC
64	Settable	IRQ48	SPI1 DMA	0x0000 0100
65	Settable	IRQ49	SPI1 ECC	0x0000 0104
66	Settable	IRQ50	CSC DMA in	0x0000 0108
67	Settable	IRQ51	CSC DMA out	0x0000 010C
68	Settable	IRQ52	Script interrupt	0x0000 0110
69	Settable	IRQ53	CRC16 interrupt	0x0000 0114
70	Settable	IRQ54	USB device suspend/resume INT	0x0000 0118
71	Settable	IRQ55	JPEG encoder in for DMA	0x0000 011C
72	Settable	IRQ56	JPEG encoder out for DMA	0x0000 0120

Please refer to the official website of ARM for more details:
https://developer.arm.com/documentation/100166/0001/Nested-Vectored-Interrupt-Controller?lang=en

4.4 System Clock

The system clock is the major clock domain except for the USB and the WDT. A divider is used to lower the operating clock for all IPs in the system clock domain. During boot up, the CPU uses the 12 MHz IHRC (Internal High-speed RC) as the default system source clock. It can be switched to other clock sources for better performance or power saving. The system clock block diagram is as shown in Figure 4–2, and Table 4–2 lists the sources of the system clock.

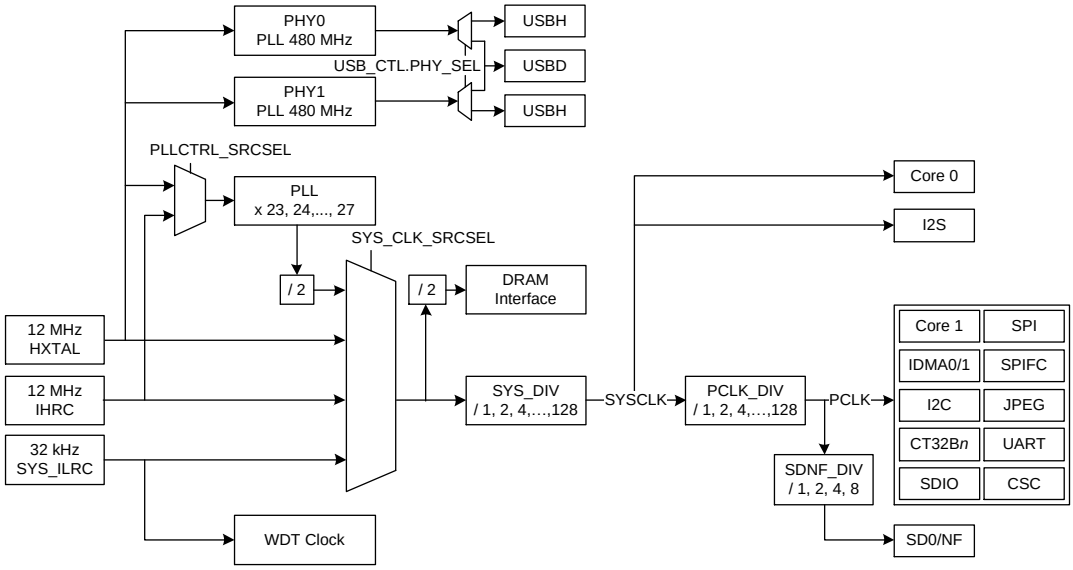


Figure 4–2 System Clock Block Diagram

Table 4–2 Sources of System Clock

Source	Frequency	Interface	Default	Note
IHRC	12 MHz	Internal	On	Power on default (±1.5% tolerance)
HXTAL	12 MHz	External: HXIN/HXOUT	Off	–
SYS_ILRC	32 kHz	–	On	Always on
PLL	276–324 MHz	Internal	Off	System Clock = PLL / 2

4.4.1 Phase-Locked Loops (PLL)

Features of the PLL are:

- Provides primary system clock
- Programmable PLL divider value
- Programmable PLL multiplier value
- Accepts IHRC input or HXTAL input

The PLL module requires one primary reference clock. The reference 12 MHz clock frequency may be generated either by the IHRC or the HXTAL. The SNC7320 Series has two sets of PLL for the system and the USB.

Table 4–3 PLL Clock Frequency

Module	Output Frequency	Description
System PLL	276–324 MHz	For main system clocks (12 MHz HXTAL/IHRC x 23, 24,…, 27)
USB_PLL	480 MHz	For USB host and device

Table 4–4 PLL List

Name	Used by	Maximum Frequency
System Clock	CPU0/CPU1	162 MHz
	AHB	162 MHz for the ROM, the SRAM, and the IP blocks on AHB including the peripherals.
System Clock / 2	DRAM	81 MHz

Name	Used by	Maximum Frequency
PLL	USB device	480 MHz
	USB host	480 MHz
ILRC (1.2V)	WDT	32 kHz

4.5 Hardware Accelerators

Comparing to processing with pure software, fast Fourier transform (FFT) and finite impulse response (FIR), the hardware accelerators of Core 1 require less instruction cycles when handling audio and image related algorithms.

Features of the FIR accelerator are:
- 16-bit input and 32-bit output data width
- Data overflow handling
- Programmable FIR tap (max. 2048)
- Suitable for algorithms including but not limited to acoustic echo cancellation, equalizer, 3D audio speech codec, and image enhancement

Features of the FFT accelerator are:
- 16-bit input and 32-bit output data width
- Data overflow handling
- Programmable FFT tap (max. 1024)
- Suitable for algorithms including but not limited to voice recognition, sound effect, and fingerprint identification

5 Memory

5.1 Physical Memory Map

The SNC7320 Series includes private libraries such as the USB library and FAT system to save memory size. There are 64 KB in the internal ROM, and there is a 64 KB PRAM dedicated for CPU programs for Core 0. Furthermore, a 256 KB internal memory is equipped to be shared by the CPU and peripherals. A ROM is dedicated for digital signal processing programs of Core 1. With its high compression algorithm, the SNC7320 Series is capable of performing audio applications such as MP3.

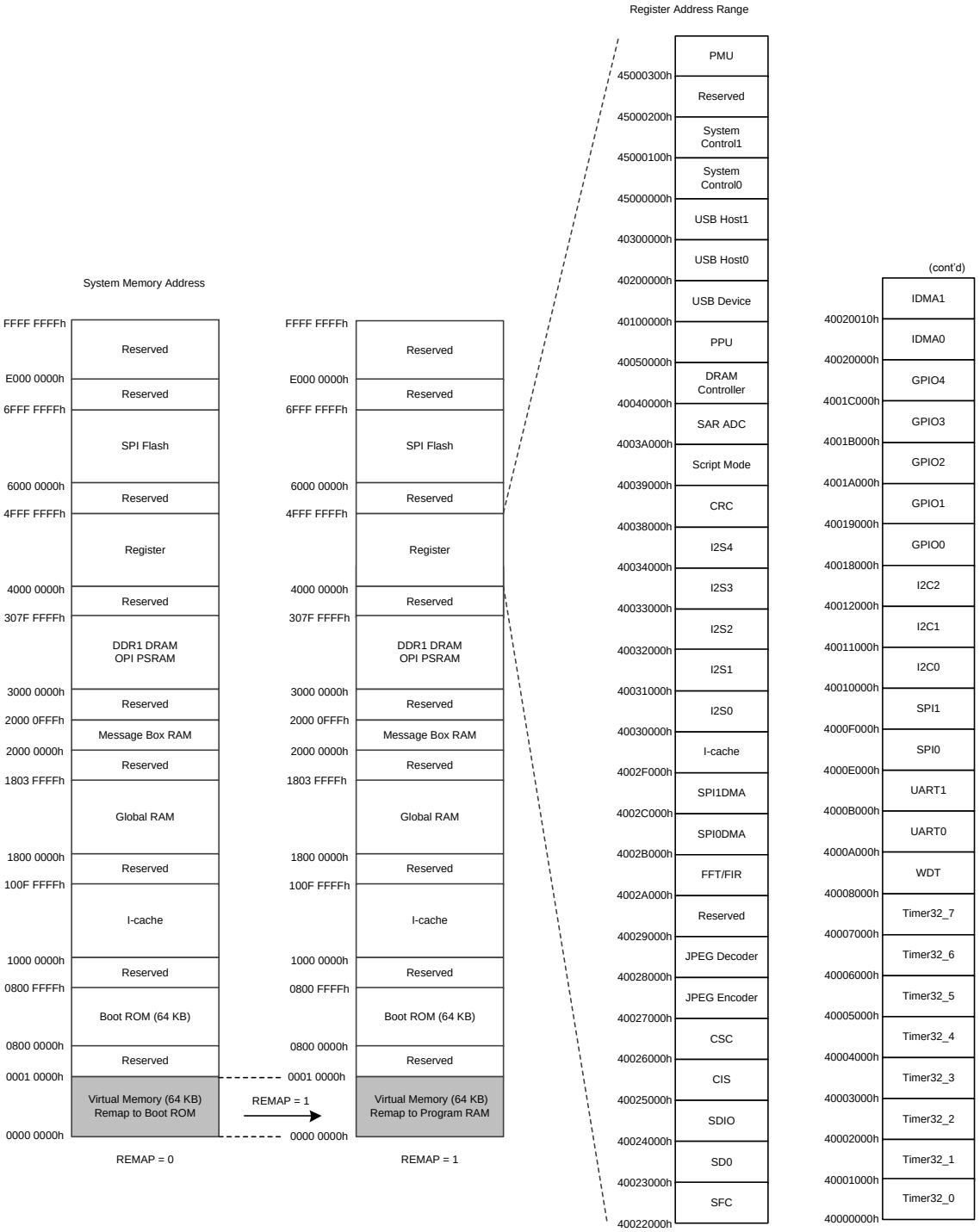


Figure 5–1 Memory Map

Table 5–1 Internal Memory

Region	Internal RAM Address Range	Size	Access			
			Core 0	Core 1	PPU	Peripheral DMAs
ROM (Core 0)	0x0800_0000–0x0800_FFFF	64 KB	R	–	–	–
Program RAM	0x0000_0000–0x0000_FFFF (After remap)	64 KB	R	–	–	–
ROM (Core 1)	0x0000_0000–0x0001_FFFF	128 KB	–	R	–	–
I-cache	0x1000_0000–0x100F_FFFF	1 MB	R	R	–	–
Shared AHB RAM	0x1800_0000–0x1803_FFFF	256 KB	R/W	R/W	R/W	R/W
Shared Mailbox RAM	0x2000_0000–0x2000_0FFF	4 KB	R/W	R/W	–	–

Table 5–2 External Memory

Region	External Memory Address Range	Size	Access			
			Core 0	Core 1	PPU	Peripheral DMAs
DDR1 DRAM/ OPI PSRAM	0x3000_0000–0x3FFF_FFFF	2/2/2/8 MB	R/W	R/W	R	R/W[17]
SPI NOR flash	0x6000_0000–0x6FFF_FFFF	256 MB	R	R	–	R/W[17]

5.2 DMA Engine

The DMA engine controls data transfer between the modules as listed in Table 5–3, along with SRAM access. There are a total of 19 sets of DMA channels where each channel functions independently. 17 sets function for a designated IP, and the last two are for general purpose.

Table 5–3 DMA Channels

Module	Base Address	Access to DRAM Controller (DDR1 DRAM or OPI PSRAM)
DMA0	0x4002_0000	Yes
DMA1	0x4002_0010	Yes
DMA-SPIFC	0x4002_2100	No
DMA-SD0/NF	0x4002_3100	No
DMA-SDIO	0x4002_4100	No
DMA-CIS	0x4002_5100	Yes
DMA-CSC-IN	0x4002_6100	No
DMA-CSC-OUT	0x4002_6110	No
DMA-JPEG_ENC-IN	0x4002_7100	No
DMA-JPEG_ENC-OUT	0x4002_7110	Yes
DMA-JPEG_DEC-IN	0x4002_8100	Yes
DMA-JPEG_DEC-OUT	0x4002_8110	No
DMA-SPI0	0x4002_B100	No
DMA-SPI1	0x4002_C100	No
DMA-I2S0	0x4003_0100	No
DMA-I2S1	0x4003_1100	No
DMA-I2S2	0x4003_2100	No
DMA-I2S3	0x4003_3100	No

[17] For certain DMAs

5.3 SPI NOR Flash Controller

Features of the SPI NOR flash controller include:

- Built-in SPI interface
- DMA for large data transfers
- 1/2/4-bit read mode and 1/4 bits write mode
- SPI NOR flash controller stops when LVD is triggered
- Supports direct addressing for CPU
- Supports MXIC/SST/GD command series serial flash

The SPI NOR flash controller block diagram is as shown in Figure 5–2.

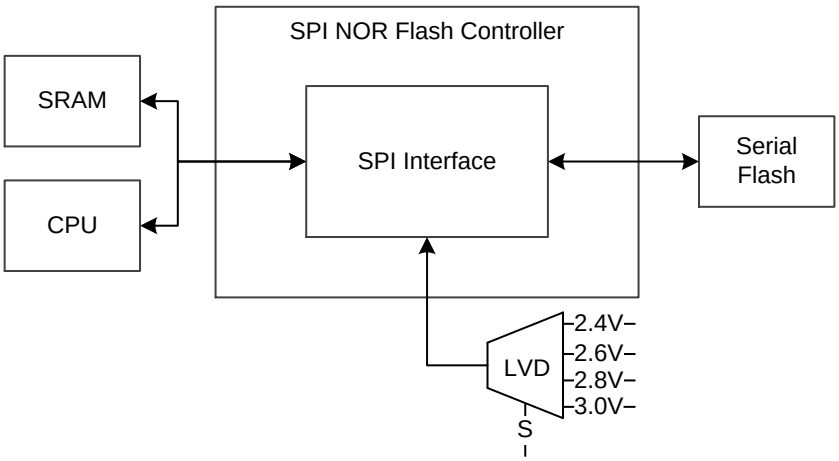


Figure 5–2 SPI NOR FLASH Controller Block Diagram

5.3.1 Timing

Table 5–4 lists the switching characteristics over the condition that SPI NOR flash clock = 162 / *n* MHz where *n* = 4.

Table 5–4 Switching Characteristics for SPI NOR Flash Controller

No.	Parameter		Device			Unit
			MIN.	TYP.	MAX.	
1	$t_{c(CLK)}$	Cycle time, SPI NOR flash clock	25	–	200	ns
2	$t_{w(CLKH)}$	Pulse width, SPI NOR flash clock high	9	–	0.45P[18]	
3	$t_{w(CLKL)}$	Pulse width, SPI NOR flash clock low	9	–	0.45P[18]	
4	$t_{d(CLK-SDX)}$	Delay time, SPI NOR flash clock transmit falling edge to SF_MO data output	3	–	–	
5	$t_{oh(CLK-SDX)}$	Output hold time, SF_MO data valid after receive rising edge of clock	11	–	–	
6	$t_{d(CSN-CLK)}$	Delay time, SPI NOR flash chip select asserting to the first SPI NOR flash clock rising edge	10	–	–	

[18] P = SF clock period

No.	Parameter		Device			Unit
			MIN.	TYP.	MAX.	
7	$t_{d(CLK-CSN)}$	Delay time, the final SPI NOR flash clock falling edge to SPI NOR flash chip select de-asserting	4	–	–	

Table 5–5 Input Timing Requirements of Controller in Master Mode

No.	Parameter		Device			Unit
			MIN.	TYP.	MAX.	
8	$t_{su(SDR-CLK)}$	Setup time, SF_MI data valid before receive rising edge of SPI NOR Flash clock	4	–	–	ns
9	$t_{h(CLK-SDR)}$	Hold time, SF_MI data valid after receive rising edge of SPI NOR flash clock	11	–	–	

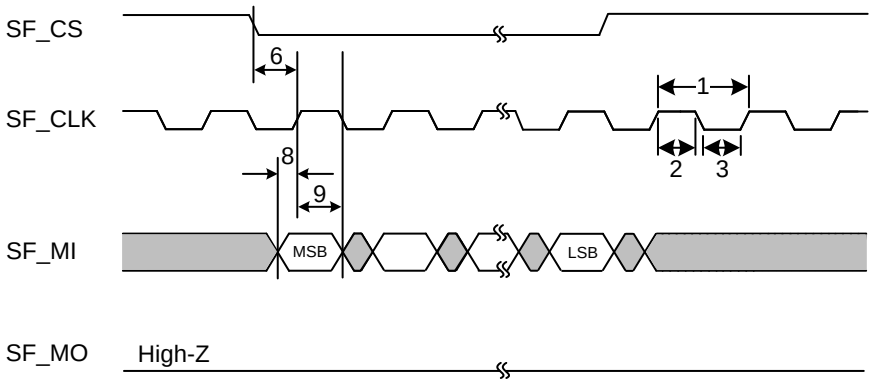


Figure 5–3 SPI NOR Flash Master Mode Input Timing

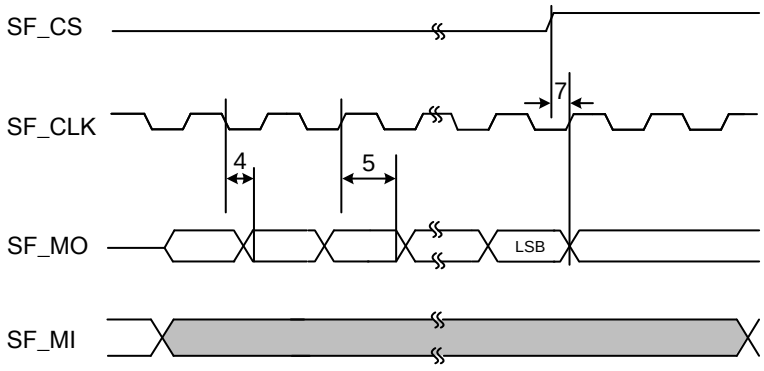


Figure 5–4 SPI NOR Flash Master Mode Output Timing

5.4 DRAM Controller

The DRAM controller has four channels for DMA or CPU access to extend the memory buffer. This controller supports DDR1 and OPI interfaces, and there are 16-bit DDR and 8-bit OPI data widths for different memory sizes.

Features of the DRAM controller are:

- Supports WRAP transfer
- AHB 32-bit data width
- Three configurable channels (0–2)
- Group round-robin arbitration scheme
- Low-power bitrate control (BRC) mode for address mapping
- Sequential DRAM burst type
- Supports auto refresh and self refresh
- Supports dynamic frequency change
- Supports DDR1 and OPI interfacesDDR1 and

The figure below shows DMA controller channels.

- Channel0 to Channel2: PPU, JPEG_E, JPEG_D, IDMA0/IDMA1, CIS, USB Device, USB Host0, USB Host1
- Channel3: Core 0, Core 1

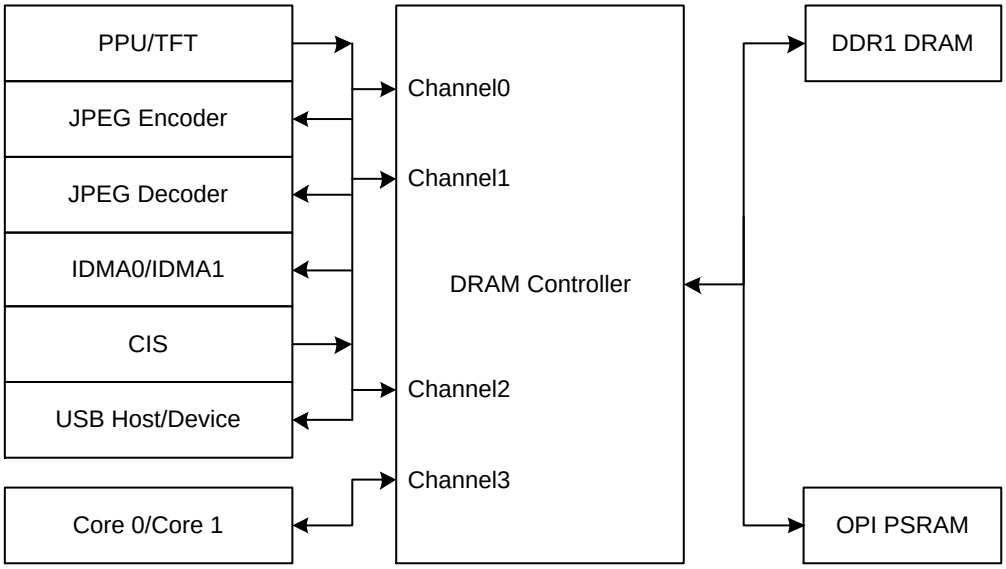


Figure 5–5 DMA Controller Channels

5.5 I-cache Controller

The SNC7320 Series supports I-cache with 16 KB SRAM to correspond to 1 MB program size running at maximum clock frequency.

Features of the I-cache are:

- 64-way set-associative cache with 16 KB SRAM, 32 bytes per line
- 1 MB address mapping
- Supports DDR1 DRAM, OPI PSRAM, or SPI flash at one time
- Supports one of the Core 0 and Core 1 at a time
- Read DDR1 DRAM/OPI PSRAM with burst eight transfer (32 bytes)

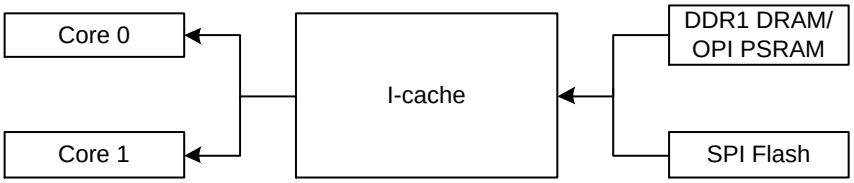


Figure 5–6 I-cache Block Diagram

5.5.1 Steps to Enable the I-cache

STEP 1: Enable the I-cache clock ROM in the system control register 1 (SYS1_PERICLKEN)

STEP 2: Reset I-cache from the System Control Register 1 (SYS1_CLKRST)

STEP 3: Set the cache offset register

STEP 4: Enable I-cache by writing the Cache_Mode_Selection register

Table 5–6 Throughput of DRAM Controller

DRAM Type Operating in 80 MHz	Access Unit		Read (MB/s)	Write (MB/s)
	Burst Type	Byte Per Transfer		
OPI PSRAM	Single access	4	16.4	149
	Burst4	16	49.5	149
	Burst8	32	74.9	149
	Burst16	64	100.9	149
DDR1 DRAM	Single access	4	22.7	149
	Burst4	16	76.3	289
	Burst8	32	121.2	291
	Burst16	64	172.1	289

5.6 Storage

5.6.1 SD Card Controller (SD0)

Features of the SD card controller (SD0) include:

- Built-in SD controller in 4-bit mode
- Compliant with SD 2.0 specification
- Programmable clock frequency
- Auto multiple block read/write command
- CRC-16 for the SD data
- CRC-7 for the SD command

Refer to 7.8.1 Timing of SD/SDIO Controller (SD1).

5.6.2 NAND Flash Controller

Features of the NAND flash controller include:

- SLC NAND flash
- 1/4/8-bit ECC
- 512 bytes/2 KB/4 KB page size
- DMA access

I. Timing

Table 5–7 Timing Requirements for NAND Flash Controller

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	t_{CLS}	CLE set up time	50	–	ns
2	t_{CLH}	CLE hold time	17	–	
3	t_{CS}	CE set up time	50	–	
4	t_{ALS}	ALE set up time	58	–	
5	t_{ALH}	ALE hold time	48	–	
6	t_{DS}	Data set up time	45	–	
7	t_{DH}	Data hold time	45	–	

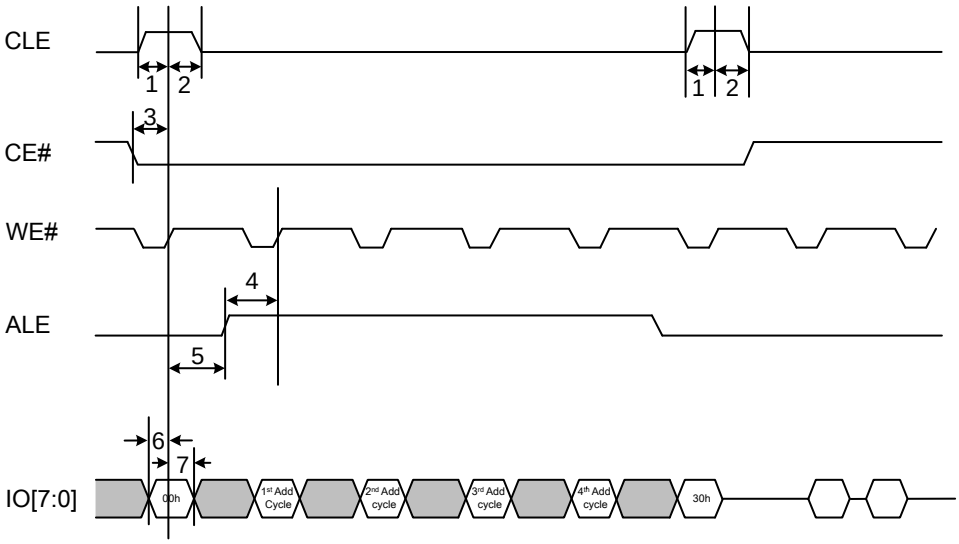


Figure 5–7 NAND Flash Controller Timing

6 System Control

6.1 System Controller (SYS0/SYS1)

The system controller enables the device to provide a customized solution by enabling/disabling each IP. It is easy to find a balance between high performance and low power consumption through different settings.

Features of the system controller are:

- Operation modes and wakeup selection
- Change settings of the PLL and clock rate control for operation in different clock frequencies
- Disable the peripheral clocks by the clock gating registers
- Select pinmux functions and setting pull-up/down

6.2 System Operation Mode

The SNC7320 Series operates in four modes for different clock rates and power saving conditions.

- Normal mode
- Sleep mode
- Deep sleep mode
- Deep power-down (DPD) mode

These modes control oscillators, the op-code operation, and the operation of analog peripheral devices. All of the GPIOs are switched into input-floating in deep power-down mode.

6.3 System Reset

A system reset is generated when one of the following events occurs.

- Power-on reset
  – 0.7V core power LVR trigger
  – Reset pin trigger
  – Restart program from ROM after the reset signal releases
- LVR/LVD reset
  – 0.7V core power LVR trigger
  – 1.0V core power LVD trigger
  – 2.1V I/O power (normal mode) LVR trigger; 1.8V I/O power (power on/power off) LVR trigger
  – Restart program from ROM after the reset signal releases
- RST pin (external reset)
  – One or two I/O power trigger
  – Restart program from ROM after the reset signal releases
- DPDWAKEUP reset
  – When waking up from DPD mode, the system resets and restarts from ROM
- WDT reset
  – Reset and restart program from ROM
- Software reset
  – Reset and restart from PRAM

6.4 Boot

The SNC7320 Series supports several storage devices to boot up from:

- SPI NOR flash
- SD card 0
- SD card 1
- SLC NAND flash
- SPI NAND flash

After power on, the CPU searches each device for an identifying data mark and enters USB-ISP mode if the identifying data mark is not found.

In normal conditions, the CPU reads data out from the SPI NOR flash (or other storage devices). After parsing a specific data structure called the load table, the CPU places the user code to the internal-memory-address zero, which is also called PRAM, and issues a software system reset to reboot itself to the user code.

7 Peripherals

7.1 General Purpose Input/Output (GPIO)

The general-purpose input/output (GPIO) is used to transmit signals between systems and devices. GPIO pins can be configured as input, output, or interrupt input. As an output, the state driven on the output pin is controlled by writing to an internal register. As an input, the state of the input is detected by reading the state of an internal register. The GPIO supports rising edge, falling edge, both-edges, and high level/low level interrupt sense types. The SNC7320 Series provides 80 GPIO pins in a pinmux architecture.

The GPIO mode bits in the GPIO_P*n*CFG (*n* = 0, 1, 2, 3, or 4) register configure the on-chip pull-up resistor for each pin or select the repeater mode. The options of the on-chip resistor configuration are pull-up enabled and inactive (no pull-up/pull-down by default). The repeater mode automatically enables the pull-up resistor if the pin is at logic high and enables the pull-down resistor if the pin is at logic low. Such characteristic causes the pin to retain its last known state if it is configured as an input and is not driven externally. State retention is not applicable in the deep power-down mode. The repeater mode is typically used to prevent a pin from floating and potentially using significant power if it floats to an indeterminate state when it is temporarily not driven.

Features of the GPIO include:

- Each pin triggers the GPIO interrupt independently
- The interrupt generation of each pin is triggered by rising/falling edge, both edges, or high/low level
- Each pin can be inactive, pulled high or pulled down
- A pull-up/pull-down resistor is 38 kΩ
- Output data bits can be set or cleared independently
- All pins are set to input mode at hardware reset
- Voltage input high (VIH) is 2.0V, and voltage input low (VIL) is 0.8V for all pins

The GPIOs generate CPU interrupts in different interrupt/event generation modes while providing generic connections to external devices.

7.1.1 Timing

Table 7–1 and Figure 7–1 are the timing and switching characteristics over recommended operating conditions and under firmware control for GPIO.

Table 7–1 Switching Characteristics for GPIO

No.	Parameter		Device[19]		Unit
			MIN.	MAX.	
1	$t_{w(GPIH)}$	Pulse duration, GPO*n*–15 high	6.1	–	ns
2	$t_{w(GPIL)}$	Pulse duration, GPO*n*–15 low	6.1	–	

NOTE In reality, the speed of the firmware control is not fast enough to toggle GPIO in every PCLK cycle[20], and the performance of the GPIO may be affected by the PCB layout and the circuit signal length.

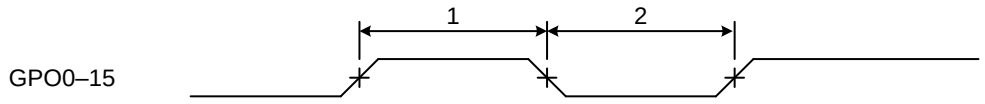


Figure 7–1 GPIO Port Timing under Firmware Control

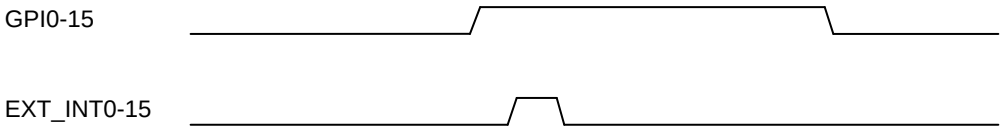


Figure 7–2 GPIO External Interrupt in Rising Edge Trigger Mode

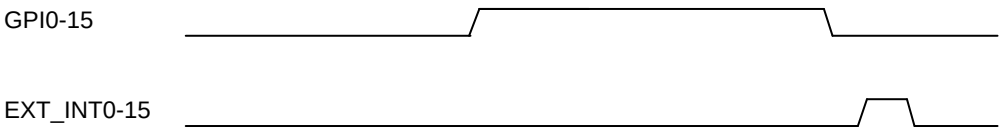


Figure 7–3 GPIO External Interrupt in Falling Edge Trigger Mode

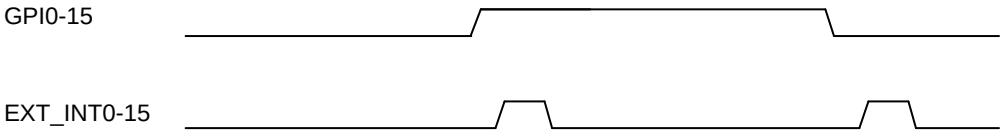


Figure 7–4 GPIO External Interrupt in Both Edges Trigger Mode

[19] The parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
[20] Peripheral clock (PCLK) cycle = AHB peripherals clock period

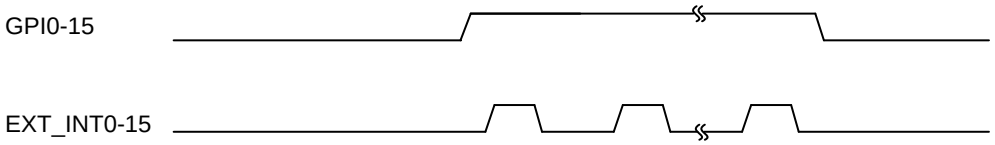


Figure 7–5 GPIO External Interrupt in High Level Trigger Mode

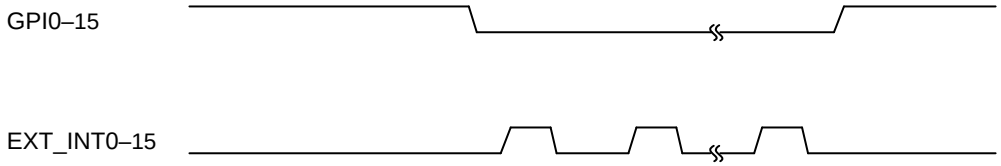


Figure 7–6 GPIO External Interrupt in Low Level Trigger Mode

7.2 Inter-integrated Circuit (I²C)

The inter-integrated circuit (I²C) interface implements the standard I²C master/slave functions and complies with the Philips I²C bus protocol. It serves as a standard master I²C device to receive/transmit data from/to a slave device over the I²C bus. On the contrary, it can also serve as a slave to respond to requests. The I²C is a two-wire bi-directional serial bus that provides a simple and efficient method of data exchange while minimizing the interconnection requirements between devices. The I²C interface is mainly used for controlling external I²C devices.

The SNC7320 Series I²C is allowed to communicate with external I²C devices. The interface has two pins, serial clock (SCL) and serial data (SDA). It supports bit rates of up to 400 kbps. The SNC7320 Series I²C has up to three sets of I²C controllers, I²C0, I²C1, and I²C2. Each has two I²C pins and is at base address 0x4001_0000, 0x4001_1000, and 0x4001_2000.

Features of the I²C include:

- I²C master
  - Standard speed up to 100 kHz
  - Fast speed up to 400 kHz
  - Start and stop generation
  - Fast mode plus up to 1 MHz
- I²C slave
  - Transmit and receive
  - Programmable I²C address detection
  - Optional recognition of up to four distinct slave addresses
  - Supports FIFO mode
  - Stop bit detection
- Arbitration handled between simultaneously transmitting masters without corruption of serial data on the bus
- Programmable clock allowing adjustment of I²C transfer rates
- Bidirectional data transfer between masters and slaves
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization as a handshake mechanism to suspend and resume serial transfer
- Generation and detection of 7/10-bit addressing and general call

7.2.1 Clock Ratios and Timing

According to the standard I²C protocol, the start signal, Start, is a special signal sent by the master on the bus to wake up all the slaves and indicates the start of a data transfer. The slave address transmit (slave address + W/R) refers to the first data packet sent by the master after a start condition. It has seven slave address bits and one read/write bit. The equation for clock ratios is:

SCL High Period Time = (SCLH+1) * I2C0_PCLK cycle
SCL Low Period Time = (SCLL+1) * I2C0_PCLK cycle

Two data packets need to be transmitted only when it is a 10-bit slave address. Otherwise, other bits (except the 10 bits address) are reserved according to the protocol. Each slave is used to transmit or receive data based on the address information. After receiving the slave address successfully, the corresponding slave pulls down the SDA at the ninth SCL cycle and returns an acknowledgement signal (ACK) to the master. Then, a subsequent data transfer can start. The data transfer "DATA" refers to data receive/transmit according to read/write commands after the master receives the slave address ACK signal successfully. During the data transfer, the SDA changes its state only when the SCL is low. The SDA holds when the SCL is high. Each time the receiver gets one byte, it must send an ACK signal to the transmitter. The transmitter stops or restarts the data transfer when it does not receive the ACK signal.
The stop signal, Stop, is a special signal sent by the master to indicate the end of the data transfer according to the I²C protocol. It occurs when the transfer is complete and there are no subsequent transfers required. Once the master sends the stop signal, the slave must release the bus.

Table 7–2 Timing Requirements for I²C

No.	Parameter		Device				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
1	$t_{c(SCL)}$	Cycle time, SCL	10	–	2.5	–	µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7	–	0.6	–	
3	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4	–	0.6	–	
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7	–	1.3	–	
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4	–	0.6	–	
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250	–	100	–	
7	$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low	0	3.45	0	0.9	
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7	–	1.3	–	
9	$t_{r(SDA)}$	Rise time, SDA	–	1000	20 + $0.1C_b$[21]	300	ns
10	$t_{r(SCL)}$	Rise time, SCL	–	1000	20 + $0.1C_b$	300	
11	$t_{f(SDA)}$	Fall time, SDA	–	300	20 + $0.1C_b$	300	
12	$t_{f(SCL)}$	Fall time, SCL	–	300	20 + $0.1C_b$	300	
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4	–	0.6	–	µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	–	–	–	50	
15	C_b	Capacitive load for each bus line	–	400	–	400	pF

[21] Cb = total capacitance of one bus line in pF. Faster fall-times are allowed when mixing with HS-mode devices.

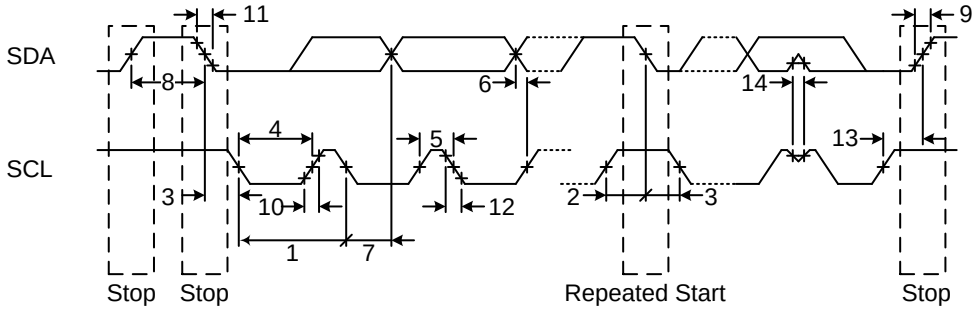


Figure 7–7 I²C Receive Timings

Table 7–3 Switching Characteristics for I²C

No.	Parameter		Device				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
16	$t_{c(SCL)}$	Cycle time, SCL	10	–	2.5	–	µs
17	$t_{d(SCLH-SDAL)}$	Delay time, SCL high to SDA low (for a repeated START condition)	4.7	–	0.6	–	
18	$t_{d(SDAL-SCLL)}$	Delay time, SDA low to SCL low (for a START and a repeated START condition)	4	–	0.6	–	
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7	–	1.3	–	
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4	–	0.6	–	
21	$t_{d(SDAV-SCLH)}$	Delay time, SDA valid to SCL high	250	–	100	–	
22	$t_{v(SCLL-SDAV)}$	Valid time, SDA valid after SCL low (For I²C devices)	0	–	0	0.9	
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7	–	1.3	–	
24	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4	–	0.6	–	
25	C_p	Capacitance for each I²C pin	–	10	–	10	

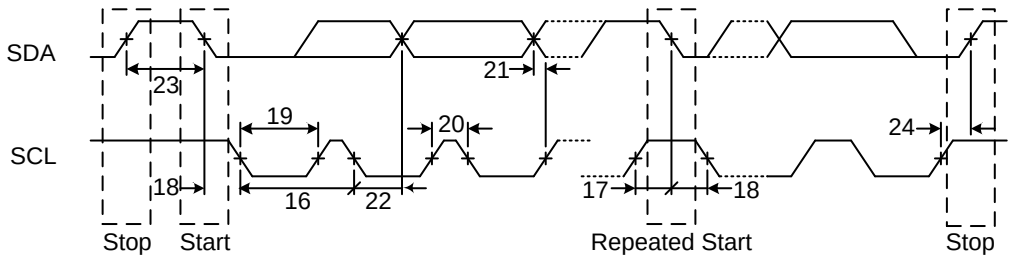


Figure 7–8 I²C Transmit Timings

7.2.2 Arbitration and Synchronization Logic

In the master transmitter mode, the arbitration logic checks that every transmitted logic 1 actually appears as a logic 1 on the I^2C bus. If another device on the bus overrules a logic 1 and pulls the SDA line low, the arbitration is lost, and the I^2C block immediately changes from master transmitter to slave receiver. The I^2C block will continue to output clock pulses on SCL until transmission of the current serial byte is complete.

Arbitration may also be lost in the master receiver mode. Loss of arbitration in this mode only occurs when the I^2C block returns a "not acknowledge" message to the bus. Arbitration is lost when another device on the bus pulls this signal low. Since this occurs only at the end of a serial byte, the I^2C block generates no further clock pulses.

7.3 Serial Peripheral Interface (SPI)

The SPI interface is a 4-wire interface where the SSEL signal behaves as a slave select. The main feature of the SPI format is that the inactive state and phase of the SCK signal are programmable through the CPOL and CPHA bits in SPI*n*_CTRL1 register. When the "CPOL" clock polarity control bit is LOW, it produces a steady state low value on the SCK pin.
If the CPOL clock polarity control bit is HIGH, a steady state high value is placed on the CLK pin when data is not being transferred. The CPHA clock phase bit controls the phase of the clock on which data is sampled. When CPHA = 1, the first edge of SCK is for data transition, and receive and transmit data is at the second edge of the SCK. When CPHA = 0, the first bit is fixed already, and the first edge of the SCK is to receive and transmit data. When the SPI is in master mode, it has to connect with one slave device as shown in Figure 7–9.

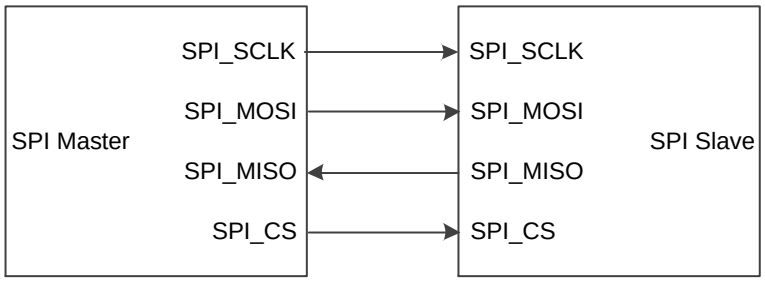


Figure 7–9 SPI Connection Diagram

The SPI controller interacts with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice it is often the case that only one of these data flows carries meaningful data.

Features of the SPI include:

- Compatible with Motorola SPI, and 4-wire TI SSI bus.
- Synchronous Serial Communication.
- Supports master or slave operation.
- 8-frame FIFO for both transmitter and receiver.
- 4-bit to 16-bit frame.
- Maximum SPI speed of 40.5 MHz in master mode or 40.5 MHz in slave mode
- Data transfer format is from MSB or LSB controlled by register
- The start phase of data sampling location selection is first phase or second phase controlled register

7.3.1 Clock Ratios and Timing

When the SPI controller is in master mode, the frequency of SCLK_OUT is derived from the following equation:

$$F_{SCLK} = F_{SPICLK}^{22} / (2 \times (SCLKDIV + 1))$$

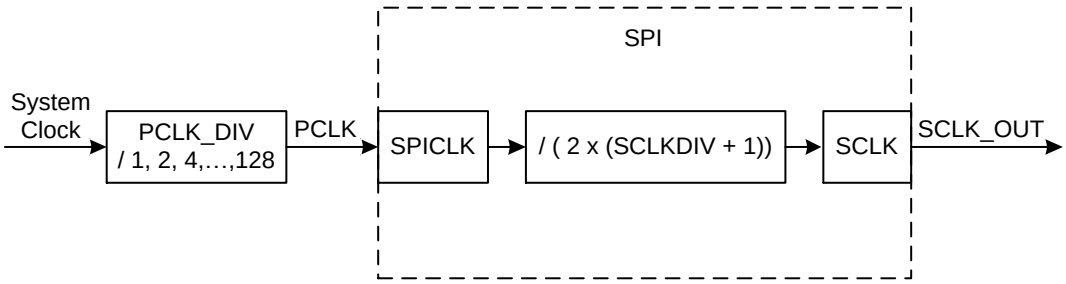


Figure 7–10 SPI Clock Block Diagram

The bit rate of the SPI is the frequency of the SCLK_OUT which is controlled by SPI_SCLKDIV in the clock divide register. When the SPI controller is in slave mode, SCLKDIV is ignored, and the SPI transfer bitrate is decided on the master side. Due to clocks synchronization, the bit clock from the master side has to be slower than SPICLK by at least six times.

SCLK stops toggling when it is idling. The frame/sync is used as the chip-select signal. Through the SPI interface, data is transmitted and received simultaneously to and from an external device. The data lines are synchronized by a serial clock.

In master mode, when the SPI controller is enabled and TX FIFO contains data, the transmit logic reads the data in TX FIFO and shifts it out at every transmit edge (depending on SCLKPO and SCLKPH) from MSB to LSB. Synchronously, the receive logic receives data. After the LSB is transmitted or received, frame/sync holds low for half or one SCLK cycle, depending on SCLKPH, and then pulled high if TX FIFO is empty. Received data is written into RX FIFO. When TX FIFO is not empty, the transmit logic restarts to transmit data.

In slave mode, when frame/sync is activated and SCLK is enabled, the transmit logic tries to shift the data into the TX FIFO even if the TX FIFO is empty. The transmit FIFO under-run interrupt is issued when TX FIFO is enabled. The receive logic receives data at the same time, and the data is written into RX FIFO.

Table 7–4 Input Timing Requirements for SPI in Master Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{su(RX-CLK)}$	Setup time, SPI_MOSI valid before receive rising or falling edge of SPI_SCLK	10	–	ns
2	$t_{h(CLK-RX)}$	Hold time, SPI_MOSI valid after receive rising or falling edge of SPI_SCLK	15	–	

[22] $F_{SPICLK} = F_{PCLK}$

Table 7–5 Switching Characteristics for SPI in Master Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
3	$t_{c(CLK)}$	Cycle time, SPI_SCLK	25	–	ns
4	$t_{w(CLKH)}$	Pulse width, SPI_SCLK high	0.45 ($t_{c(CLK)}$)	–	
5	$t_{w(CLKL)}$	Pulse width, SPI_SCLK low	0.45 ($t_{c(CLK)}$)	–	
6	$t_{osu(TX-CLK)}$	Ouput setup time, SPI_MISO valid before initial SPI_SCLK rising or falling edge.	0.5 ($t_{c(CLK)}$) - 4	–	
7	$t_{d(CLK-TX)}$	Delay time, SPI_SCLK transmit rising or falling edge to SPI_MISO output	4	–	
8	$t_{oh(CLK-TX)}$	Output hold time, SPI_MISO valid after receive rising or falling edge of SPI_SCLK	0.5 ($t_{c(CLK)}$) - 4	–	

The SPI data transfer timings are as below:

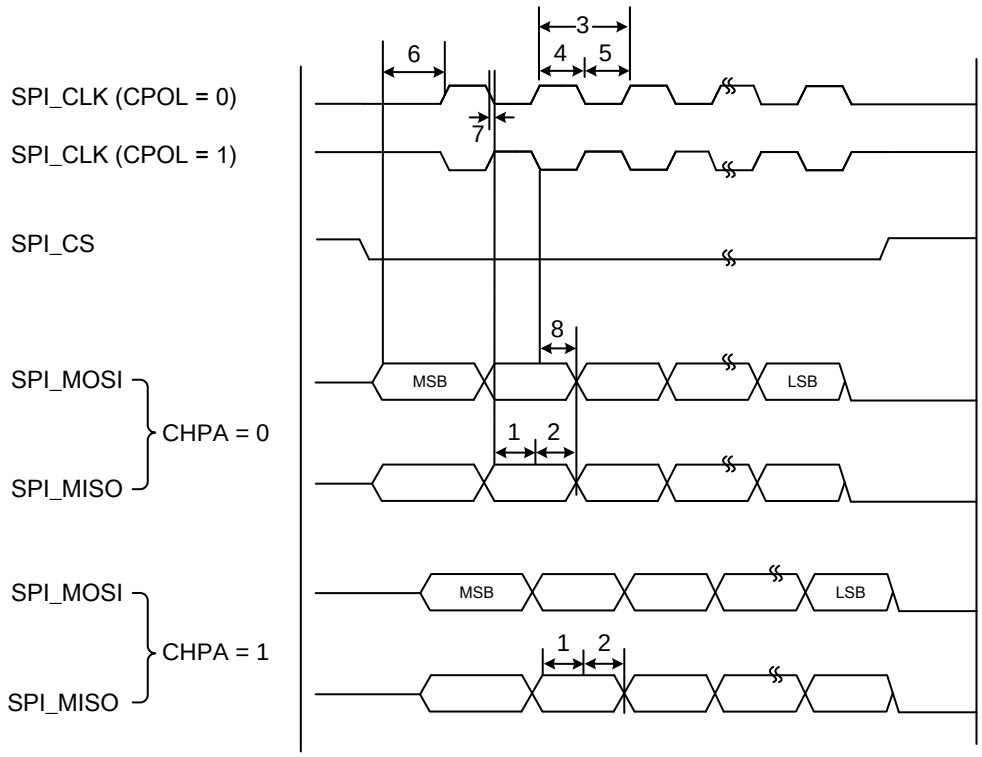


Figure 7–11 SPI Timings

7.4 Universal Asynchronous Receiver Transmitter (UART)

The SNC7320 Series UART controller uses serial communication for data transmission. The UART offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The SNC7320 Series provides two sets of UART. Each UART includes a programmable baud rate generator capable of dividing the module's reference clock by divisors to generate the correct UART baud rate.

Features of the UART controller include:

- Baud rates of up to 921600 bps
- One start bit, 8-bit data, and one or two stop bit format
- 16 bytes TX and 16 bytes RX FIFO buffer
- Register locations conform to 16650 industry standard
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes
- Built-in baud rate generator
- Software or hardware flow control

Figure 7–12 is the UART connection diagram with flow control.

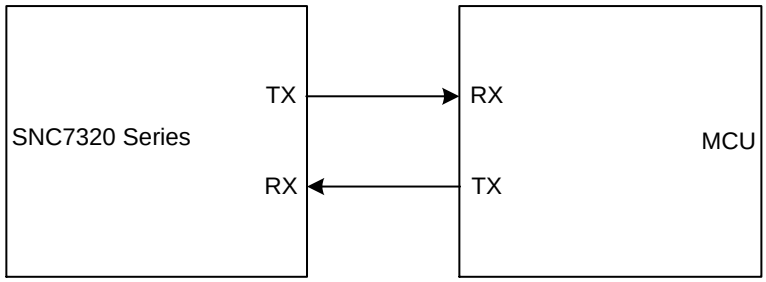


Figure 7–12 UART Connection Diagram

7.4.1 Baud Rate, Timing, and Transfer Format

It is required to set the proper baud rate for UART transmission initiation. The minimum and maximum baud rates supported by UART are a function of UART*n*_PCLK as well as the number of data bits, stop bits and parity bits.

$$UART_{baudrate} = PCLK / (Oversampling \times (256 \times DLM + DLL) \times (1 + DIVADDVAL / MULVAL))$$

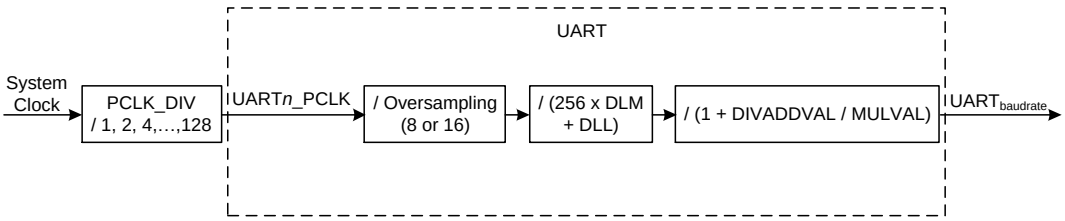


Figure 7–13 UART Clock Block Diagram

Where UART*n*_PCLK is the peripheral clock, UART*n*_DLM and UART*n*_DLL are the standard UART baud rate divider registers, and DIVADDVAL and MULVAL are UART fractional baud rate generator specific parameters in UART*n*_FD register.

Table 7–6 Timing Requirements for UART Receiver

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{w(URXDB)}$	Pulse duration, receive data bit	0.96U[23]	1.05U[23]	ns
2	$t_{w(URXSB)}$	Pulse duration, receive start bit	0.96U[23]	1.05U[23]	

The table below lists switching characteristics over recommended operating conditions for the UART transmitter.

Table 7–7 Switching Characteristics for UART Transmitter

No.	Parameter		Device		Unit
			MIN.	MAX.	
3	$t_{w(URXDB)}$	Pulse duration, transmit data bit	U[23] - 2	U[23] + 2	ns
4	$t_{w(URXSB)}$	Pulse duration, transmit start bit	U[23] - 2	U[23] + 2	
5	$f_{(baud)}$	UART1 maximum programmable baud rate1	110	921600	bps
		UART2 maximum programmable baud rate	110	921600	

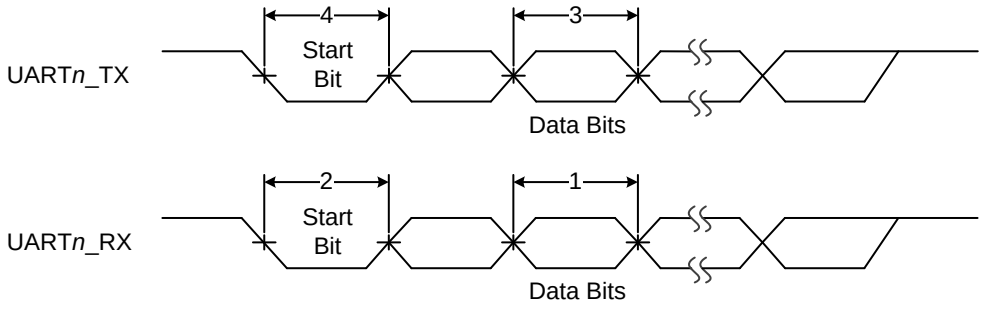


Figure 7–14 UART Transmit/Receive Timing

The SNC7320 Series UART includes TX and RX pins for transmitting, receiving, and flow control. It has one start bit, 8-bit data, and one/two stop bits for each communication.

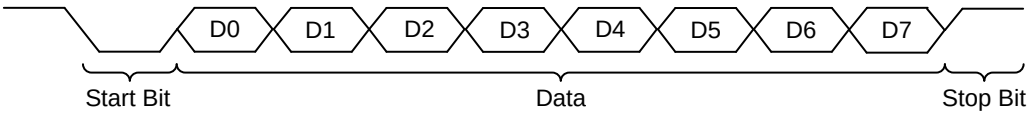


Figure 7–15 UART Transfer Format

7.5 Timer with Pulse Width Modulator (PWM)

The SNC7320 Series provides up to eight sets of timers. Each timer is designed to count cycles of the peripheral clock (PCLK) or an external clock and can optionally generate interrupts or perform other actions at specified timer values based on four match registers. Each timer also includes one capture input to trap the timer value during input signal transitions, optionally generating an interrupt. In PWM mode, up to three match registers can be used to provide a single-edge controlled PWM output on match output pins.

[23] U = UART baud time = 1 / programmed baud rate.

Features of the timers include:

- Up to 24 PWM outputs
- Up to eight 32-bit timers with a programmable 32-bit prescalar
- Timer operation
- Eight 32-bit capture channels that can take a snapshot of the timer value during input signal transitions. Each capture event may also optionally generate an interrupt.
- The timer and prescalar may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Each set of timers has four 32-bit match registers with the following capabilities:
  Set PWM output LOW on match (CT32B*n*_MR0–2).
  Set PWM output HIGH on match (CT32B*n*_MR0–2).
  Toggle PWM output on match (CT32B*n*_MR0–2).
  Reset or stop timer on match (CT32B*n*_MR0–3).
  Generate an interrupt on match (CT32B*n*_MR0–3).
  Do nothing on match (CT32B*n*_MR0–3).

The following figure shows a timer configured to reset a count and generate an interrupt on match. The CT32B*n*_PRE register is set to 2, and the CT32B*n*_MR*x* register is set to 6. At the end of the timer cycle where the match occurs, the timer count resets and gives a full length cycle to the match value. The interrupt indicating a match occurred is generated in the next clock, after the timer has reached the match value.

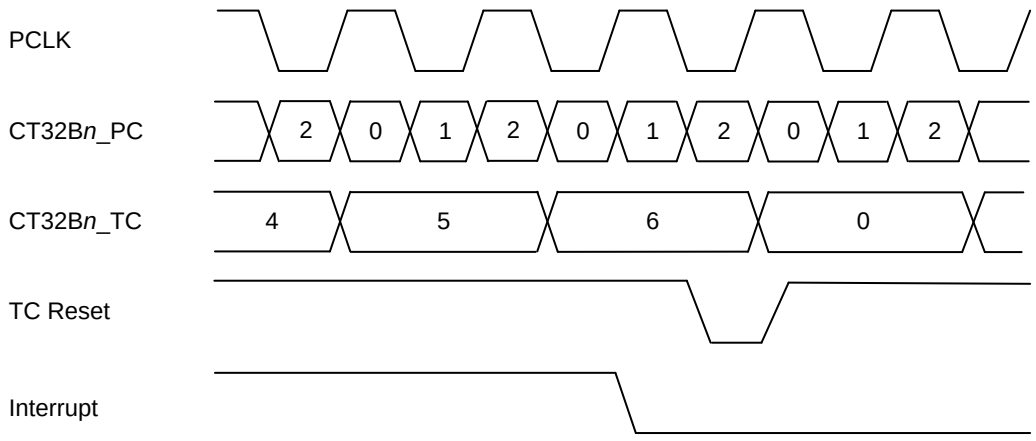


Figure 7–16 Timer Reset Timing

The following figure shows a timer configured to stop the count and generate an interrupt on match. The CT32B*n*_PRE register is set to 2, and the CT32B*n*_MR*x* register is set to 6. In the next clock after the timer reaches the match value, the CEN bit in CT32B*n*_TMRCTRL register is cleared, and the interrupt is generated indicating a match occurred.

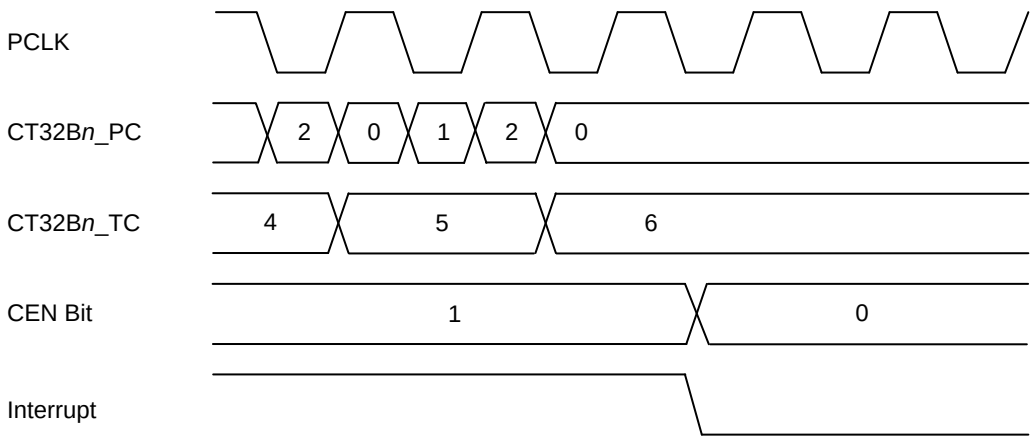


Figure 7–17 Timer Stop Timing

7.5.1 PWM Timing

All single edge controlled PWM outputs go LOW at the beginning of each PWM cycle when the timer is set to zero unless their match value in CT32B*n*_MR0–3 registers is equal to zero. Each PWM output goes HIGH when its match value is reached. If no matching occurs, the PWM output remains continuously LOW. If a match value larger than the PWM cycle length is written to CT32B*n*_MR0–3 registers, and the PWM signal is already HIGH, the PWM signal is cleared on the start of the next PWM cycle. If a match register contains the same value as the timer reset value (the PWM cycle length), the PWM output is reset to LOW on the next clock tick. Therefore, the PWM output always consists of one clock tick wide positive pulse with a period determined by the PWM cycle length. If a match register is set to zero, the PWM output goes HIGH the first time the timer goes back to zero and continues to stay HIGH.

The table below lists switching characteristics over recommended operating conditions for PWM.

Table 7–8 Switching Characteristics for PWM

No.	Parameter		Device	
			MIN.	MAX.
1	t_{all}	PWM periodic timing	624.6 ns	26.51 sec
2	$t_{w(PWML)}$	Pulse duration PWM low	6.246 ns	26.51 sec
3	$t_{w(PWMH)}$	Pulse duration PWM high	6.246 ns	26.51 sec
4	$t_{t(PWM)}$	PWM transition time	–	6 ns

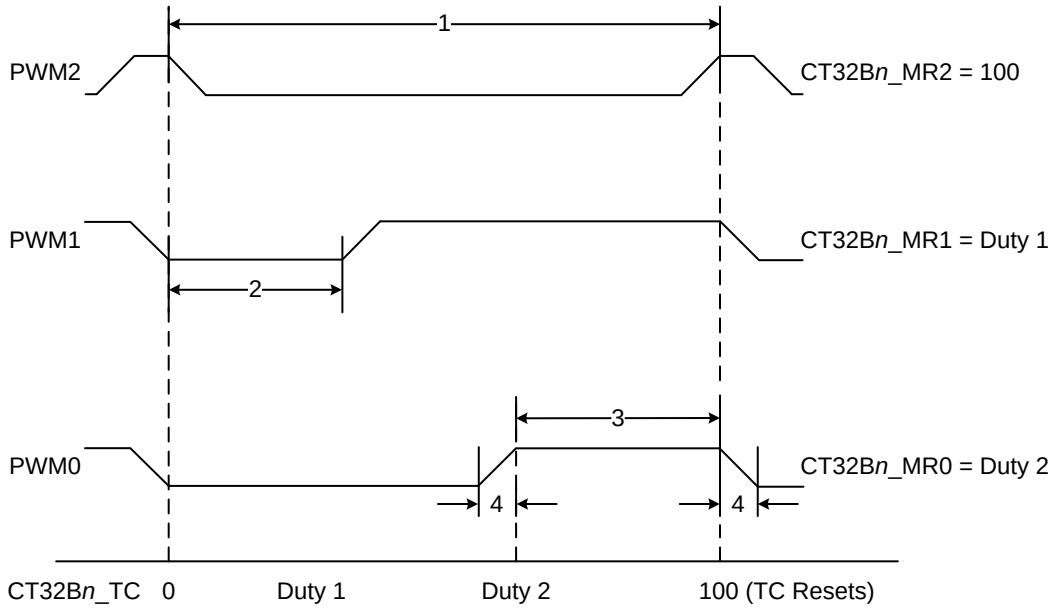


Figure 7–18 PWM Duty Cycle Timings

7.6 Watchdog Timer (WDT)

The purpose of the WDT is to reset the MCU within a reasonable amount of time if it enters an erroneous state. When enabled, the WDT generates a system reset or interrupt if the user program fails to "feed" (or reload) the WDT within a predetermined amount of time. The WDT consists of a fixed pre-scalar that is divided by 128 and an 8-bit counter. The clock is fed to the timer via a pre-scalar. The timer decreases when clocked. The minimum value from the counter decrements is 0x01. Hence the minimum WDT interval is *(TWDT_PCLK × 128 × 1)* and the maximum WDT interval is *(TWDT_PCLK × 128 × 256)*. When the WDT is started by setting the WDTEN in WDT_CFG register, the time constant value is loaded in the watchdog counter and the counter starts counting down. When the WDT is in the reset mode and the counter underflows, the CPU will be reset, loading the stack pointer and program counter from the vector table as in the case of external reset. Whenever the value 0x55AA is written in WDT_FEED register, the WDT_TC value is reloaded in the watchdog counter and the watchdog reset or interrupt is prevented. WDT reset or interrupt will occur any time the watchdog is running and has an operating clock source.

Features of the WDT include:

- 8-bit watchdog counter
- Counter restart
- Generate reset signals
- Watchdog timer clock from 32.768 kHz ILRC
- Programmable assert duration of WD_RST and WD_INTR
- Generate interrupts to the system

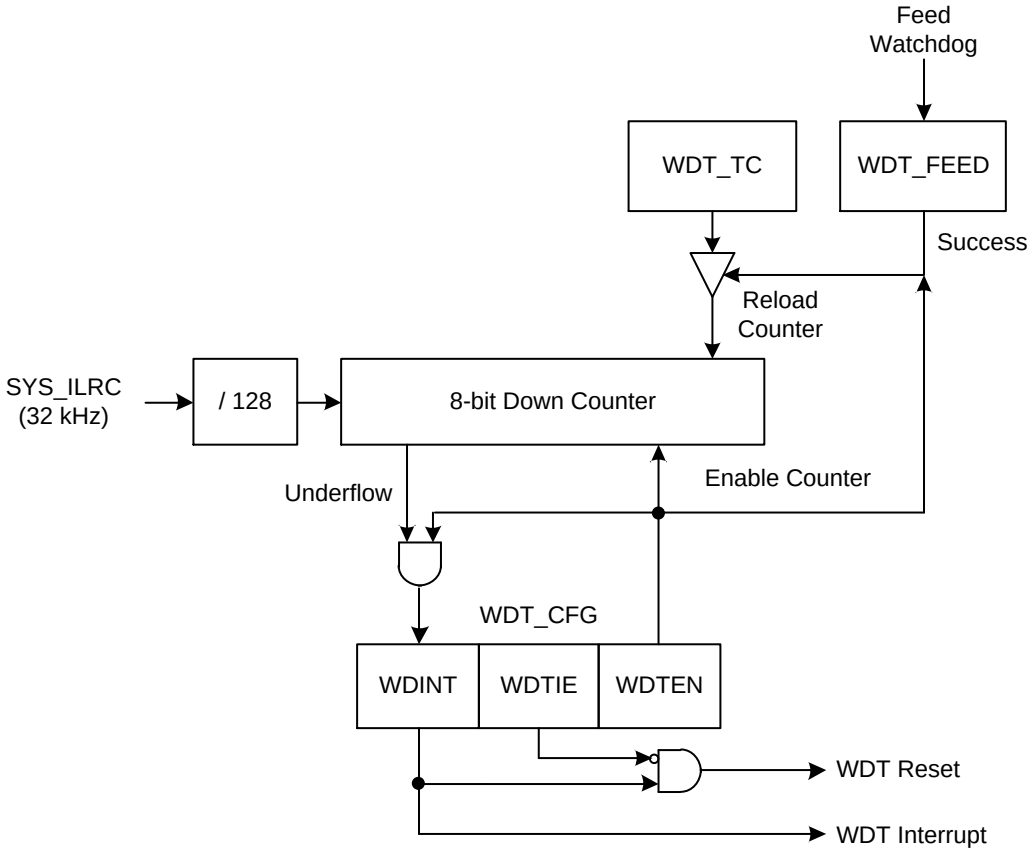


Figure 7–19 WDT Block Diagram

7.7 Successive Approximation Register Analog-to-Digital Converter (SAR ADC)

The 10-bit SAR ADC converter has six input sources with up to 1024-step resolution to convert analog signals into 10-bits digital data. In the SNC7320 Series provides an interrupt to indicate the ADC result is ready. However, the interrupt event is optional.

Features of the SAR ADC include:

- Input 0V to 3.3V full swing
- Conversion rate up to 1M SPS
- Low latency-time
- Supports 10-bit resource
- Supports 128/64/32/16/8/4/2/1 kHz audio conversion rate (system frequency = 162 MHz)
- Supports single mode and normal mode

7.7.1 Timing

Table 7–9 Switching Characteristics for SAR ADC

No.	Parameter		Device		Unit
			MIN.	MAX.	
Digital Interface					
1	t_p	ADC clock period	61.7	–	ns
2	t_{HOLD}	ADC data hold time	956.79	–	µs
3	t_S	Sampling period	925.926	–	
–	F_S	Conversion rate	–	1.08	
Internal Clock					

No.	Parameter		Device		Unit
			MIN.	MAX.	
4	t_1[24]	ADC setup time per conversion	246.8		ns
5	t_2[25]	ADC sampling time per conversion	185.1		
6	t_3[26]	ADC OS time per conversion	61.7		

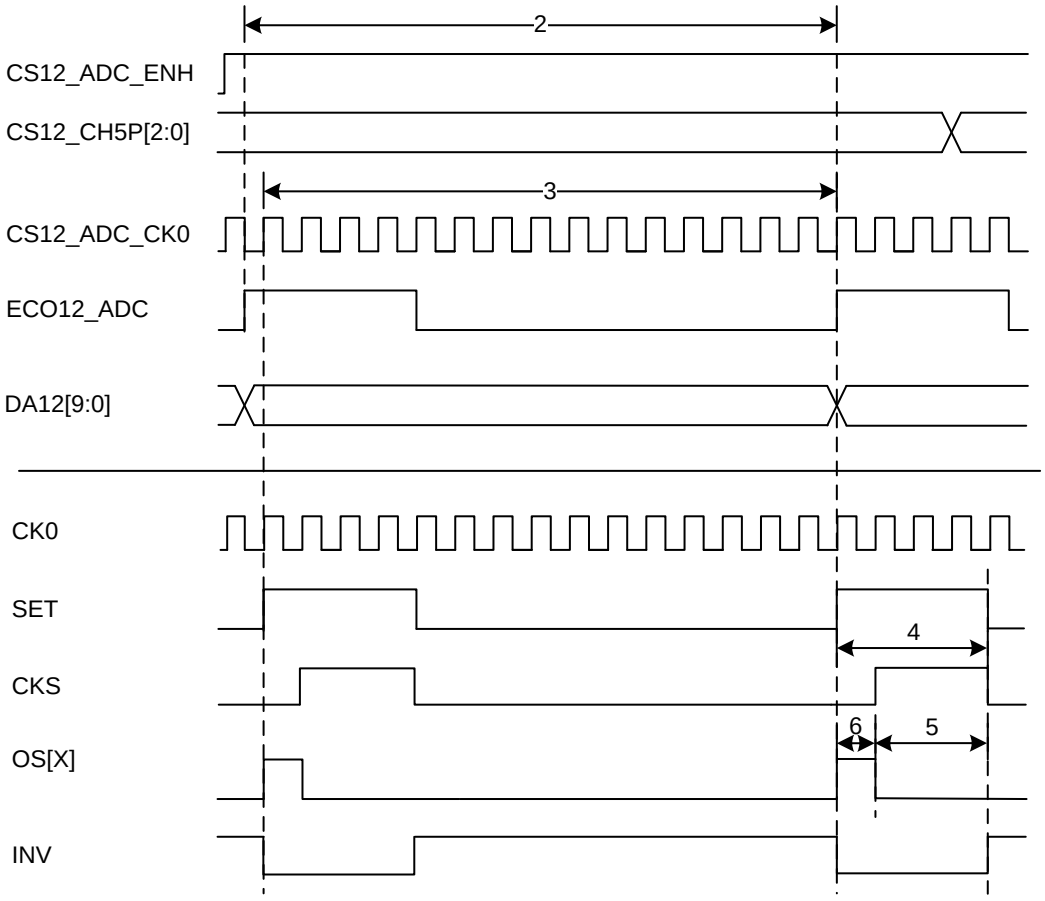


Figure 7–20 SAR ADC Timing

The figures below illustrate SAR ADC timings in single and normal modes respectively. The sample data of both modes can be selected by setting the CHS register as disclosed in the SNC7320 Series Register Table subsection 32.1 [15:13]. In normal mode, the start bit is set through the register before the conversion of the first sample data. When the first sample data conversion is completed, the hardware automatically sets the start bit for conversion of the next sample data to begin.

[24] t_1 = 4 Tp
[25] t_2 = 3 Tp
[26] t_3 = Tp

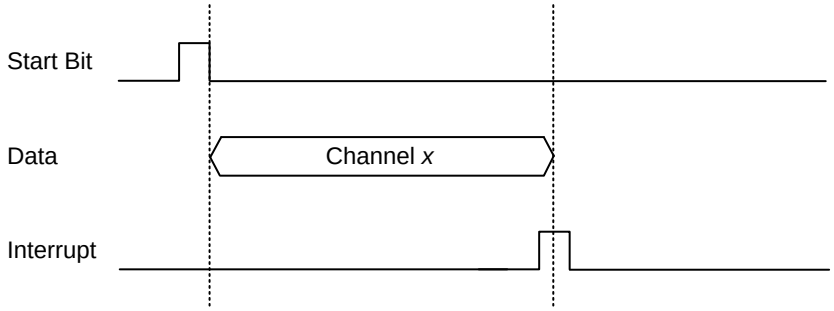


Figure 7–21 SAR ADC Single Mode Timing

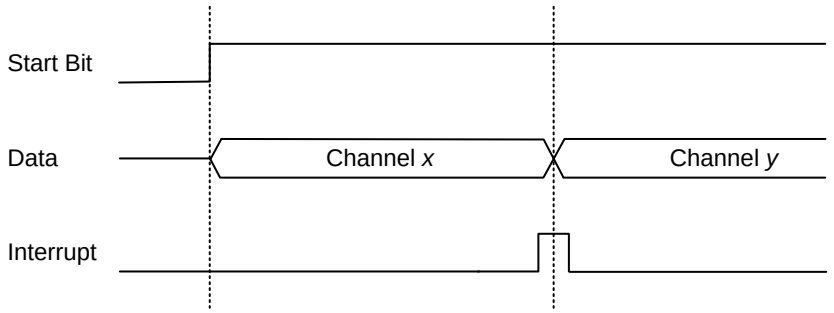


Figure 7–22 SAR ADC Normal Mode Timing

7.8 SD/SDIO Controller (SD1)

Features of the SD/SDIO controller include:

- Built-in SD/SDIO controller
- Compliant with SD 2.0 specification
- Compliant with SDIO 2.0 specification
- Programmable clock frequency
- Auto multiple block read/write command
- DMA for large data transfers
- CRC-16 for the SD data
- Write-protect for the SD cards
- Card-detect for the SD cards

7.8.1 Timing

The table below lists timing requirements over the condition of SD clock = 162 / 2 / (*n* + 2) MHz, *n* = 0 for SD module.

Table 7–10 Timing Requirements for SD Module

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{su(CMDV–CLKH)}$	Setup time, SD_CMD valid before SD_CLK high	9	–	ns
2	$t_{h(CLKH–CMDV)}$	Hold time, SD_CMD valid after SD_CLK high	12	–	

No.	Parameter		Device		Unit
			MIN.	MAX.	
3	$t_{SU(DATV–CLKH)}$	Setup time, SD_D[3:0] valid before SD_CLK high	6	–	
4	$t_{h(CLKH–DATV)}$	Hold time, SD_D[3:0] valid after SD_CLK high	7	–	

The table below lists switching characteristics over recommended operating conditions for SD module.

Table 7–11 Switching Characteristics for SD Module[27]

No.	Parameter		Device		Unit
			MIN.	MAX.	
5	$f_{(CLK)}$	Operating frequency	–	32[28]	MHz
6	$t_{W(CLKL)}$	Pulse width, SD_CLK low	0.5P[29]	–	ns
7	$t_{W(CLKH)}$	Pulse width, SD_CLK high	0.5P[29]	–	
8	$t_{r(CLK)}$	Rise time, SD_CLK	–	6	
9	$t_{f(CLK)}$	Fall time, SD_CLK	–	6	
10	$t_{d(CLKL-CMD)}$	Delay time, SD_CLK low to SD_CMD transition	17	–	
11	$t_{d(CLKL-DAT)}$	Delay time, SD_CLK low to SD_D[3:0] transition	17	–	

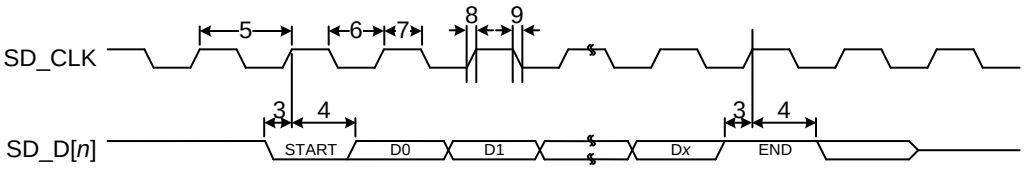


Figure 7–23 SD Host Read and Card CRC Status Timing

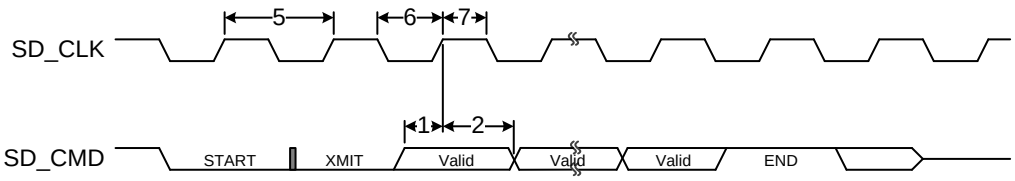


Figure 7–24 SD Card Response Timing

[27] When initializing, the clock of the SD card should be less than 400 kHz.
[28] The SD clock delay is 1 idle clock (1/80 MHz) per byte transmission.
[29] P = SD_CLK period

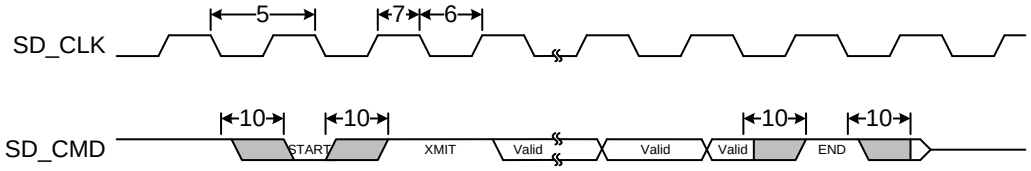


Figure 7–25 SD Host Command Timing

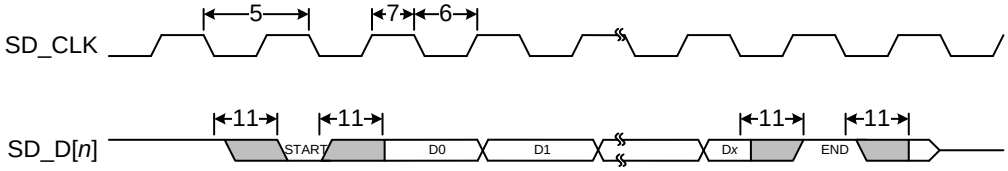


Figure 7–26 SD Host Write Timing

7.9 SPI Controller with DMA

The SNC7320 Series has two SPI controllers with DMA to connect to a wide variety of SPI devices. The DMA data transmission avoids interruptions and increases CPU computing bandwidth. An ECC is built-in for the SPI NAND for error-bit detection and to correction.

Features of the SPI controller with DMA are:
- Master mode only
- 4 or 3-wire protocol
- 1-byte FIFO
- 1/2/4-bit TX/RX DMA mode
- 5, 10, 20, and 40 MHz clock frequencies
- Supports 1/4/8-bit ECC
- DMA access

7.9.1 Timing

Refer to 7.3 Serial Peripheral Interface (SPI). The hardware delays one idle clock (110 ns) in every 4 bytes.

7.10 Universal Serial Bus 2.0 (USB 2.0)

The SNC7320 Series has two USB 2.0 controllers. One is a high speed host, and the other with host/device option. The functions of the controllers when being used as a host or a device are elaborated in subsections 7.10.1 and 7.10.2 respectively.

Features of the USB 2.0 host include:
- Two USB 2.0 hosts, each supporting an individual USB system
- USB 2.0 all transfer modes (control, bulk, isochronous, and interrupt)
- One port for root hub function
  - The companion host controller for full-speed (FS) and low-speed (LS) functionalities are fully supported, but it is not implemented based on the OHCI or UHCI standard.
    - Port router is not required-Companion port route description for OHCI/UHCI
  - Bus topology
    - Only high-speed (HS) hub plugged into tier one layer
    - Device with HS control transfer/ HS bulk transfer/ HS isochronous transfer/ HS interrupt

transfer/ FS control transfer/ FS bulk transfer/ FS interrupt transfer plugged into the root hub

The USB 2.0 host **does NOT** support

- FS ISO
- Transaction isochronous transfer descriptor (siTD)
- Frame span traversal node (FSTN)
- USB On-The-Go (OTG) and embedded host supplement

Features of the USB 2.0 device include:

- Compliant to USB 2.0 specification
- Compliant to AMBA 2.0 specification
- HS and FS supported
- Control transfer supported by endpoint #0
- One BULK-IN, one BULK-OUT, and one INT-IN endpoints
- Scatter-gather DMA
- 2.5k bytes (KB) FIFO RAM shared by all endpoints
- USB video class (UVC) bulk mode
- Mass storage class (MSC)
- Human interface device (HID)

The USB 2.0 device **does NOT** support isochronous transfer type.

7.10.1 USB 2.0 Host

The USB host function contains a universal serial bus (USB) 2.0 host controller and a built-in USB 2.0 host PHY. Without software intervention, the host controller can deal with a transaction-based data structure to offload the CPU and automatically transmit/receive data on the USB bus. The transceiver interface is UTMI+ level 3, which supports HS transfer with a HS hub. Without supporting siTD, FS with isochronous transfer device cannot be applied to USB 2.0 host via a HS hub or root hub.

I. AHB Interface

The EHCI host controller (HC) is connected to the system by the AHB. The design requires both master and slave bus operations. As a master, the host controller is responsible for running cycles on the AHB to access transfer descriptors as well as transferring data between memory and the local data buffer. As a slave, the host controller monitors the cycles on the AHB and determines when to respond to these cycles. Configuration and non-real-time control access to the host controller operational registers are through the AHB slave interface.

II. EHCI Controller

The EHCI supports two transfer types: asynchronous and periodic. The periodic transfer type includes isochronous and interrupt, and the asynchronous transfer type includes control and bulk.

III. Interrupt Processing

HC-initiated communication with the host controller driver by interrupts. There are several events that may trigger an interrupt from the host controller. Each specific event sets a specific bit in the interrupt status register.

IV. DMA

The DMA is the central block in the data path. The DMA coordinates all access to the AHB master interface. There are two sources of bus mastering within a host controller: the link list processor and the data buffer engine.

V. Data Buffer

The data buffer serves as the data interface between the AHB master and the USB protocol engine. It is a Ping-Pong FIFO RAM with 1024 bytes x 2 size.

VI. USB 1.1 Host Controller Interface

A new structure is created to substitute the OHCI/UHCI USB 1.1 control unit. The port routing logic was disregarded as there is only one port in root hub.

VII. Timing

Table 7–12 Switching Characteristics for USB 2.0 Host

Parameter		Device						Unit
		Low-Speed		Full-Speed		High-Speed		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{r(D)}$	Rise time, USB_DP and USB_DM signals[30]	75	300	4	20	0.5	20	ns
$t_{f(D)}$	Fall time, USB_DP and USB_DM signals[30]	75	300	4	20	0.5	20	
t_{rfm}	Rise/fall time, matching[31]	80	125	90	111.11	–	–	%
V_{CRS}	Output signal cross-over voltage[30]	1.3	2	1.3	2	–	–	V
$t_{jr(source)NT}$	Source (host) driver jitter, next transition	–	2	–	2	–	–	ns
$t_{jr(FUNC)NT}$	Function driver jitter, next transition	–	25	–	2	–	–	
$t_{jr(source)PT}$	Source (host) driver jitter, paired transition[32]	–	1	–	1	–	–	
$t_{jr(FUNC)PT}$	Function driver jitter, paired transition	–	10	–	1	–	–	
$t_{w(EOPT)}$	Pulse duration, EOP transmitter	1250	1500	160	175	–	–	
$t_{w(EOPR)}$	Pulse duration, EOP receiver	670	–	82	–	–	–	
$t_{(DRATE)}$	Data rate	–	1.5	–	12	–	480	Mb/s
Z_{DRV}	Driver output resistance	–	–	28	49.5	40.5	49.5	Ω

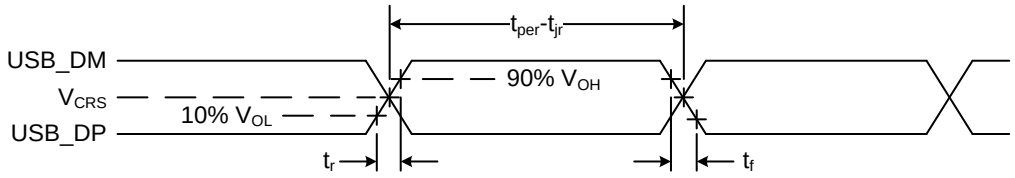


Figure 7–27 USB 2.0 Host Integrated Transceiver Interface Timing

[30] Low Speed: CL = 200 pF, Full Speed: CL = 50 pF; High Speed: CL = 50 pF
[31] $t_{rfm} = (t_r / t_f) \times 100$; excluding the first transaction from the idle state
[32] $t_{jr} = t_{px(1)} - t_{px(0)}$

7.10.2 USB 2.0 Device

Other than a USB host, the SNC7320 Series has a USB 2.0 high speed device interface, forward compatible with full speed mode. That enables the SNC7320 Series to be a USB device supporting bulk, isochronous, interrupt, and control transfers that are compliant to the USB 2.0 specification.

The USB controller transfers data through the AHB and the USB. The AHB includes the AHB master interface and AHB slave interface. The CPU programs the USB controller through the AHB slave interface. For IN or OUT transfer, the USB controller writes data to system memory or reads data from system memory through the AHB master interface. The USB controller also includes a USB transceiver as the interface of the USB.

USB endpoints: includes nine endpoints, designated EP0, EP1, EP3, EP4, EP5, EP7, EP12, EP13, EP14, and EP15. Each is intended for a particular use as below:

- EP0: the default endpoint uses control transfer (in/out) to handle configuration and control functions required by the USB specification.
- EP1: Interrupt in endpoint
- EP3: Isochronous in endpoint
- EP4: Isochronous out endpoint
- EP5: Interrupt in endpoint
- EP7: Isochronous in endpoint
- EP12: Bulk in endpoint
- EP13: Bulk out endpoint
- EP14: Bulk in endpoint
- EP15: Bulk out endpoint

I. Timing

Table 7–13 Switching Characteristics for USB 2.0 Device

Parameter		Full Speed		High Speed		Unit
		MIN.	MAX.	MIN.	MAX.	
$t_{r(D)}$	Rise time, USB_DP and USB_DM signals[30]	4	20	0.5	20	ns
$t_{f(D)}$	Fall time, USB_DP and USB_DM signals[30]	4	20	0.5	20	
t_{rfm}	Rise/fall time, matching[31]	90	111.11	–	–	%
V_{CRS}	Output signal cross-over voltage[30]	1.3	2	–	–	V
$t_{jr(source)NT}$	Source (host) driver jitter, next transition	–	2	–	–	ns
$t_{jr(FUNC)NT}$	Function driver jitter, next transition	–	2	–	–	
$t_{jr(source)PT}$	Source (host) driver jitter, paired transition[32]	–	1	–	–	
$t_{jr(FUNC)PT}$	Function driver jitter, paired transition	–	1	–	–	
$t_{w(EOPT)}$	Pulse duration, EOP transmitter	160	175	–	–	
$t_{w(EOPR)}$	Pulse duration, EOP receiver	82	–	–	–	
$t_{(DRATE)}$	Data rate	–	12	–	480	Mb/s
Z_{DRV}	Driver output resistance	28	49.5	40.5	49.5	Ω

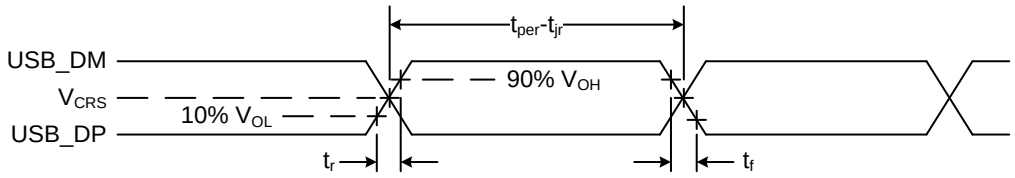


Figure 7–28 USB 2.0 Device Integrated Transceiver Interface Timing

8 Multimedia

8.1 Picture Processing Unit (PPU)

The PPU activates graphic processing and turns on the TFT/8080 controller for display. It supports up to two layers of texts and 256 sprites in one screen. The text and sprites can be configured independently when displaying. The Text 3 of the PPU provides two buffer addresses for setting, and it will be exchanged when it is enabled. To avoid display error, the content must be filled before switching the buffer addresses.

Features of the PPU are:

- Picture resolution: Up to VGA (640 x 480)
- Sprite RAM: 2 KB
- Palette RAM: 1 KB for Text 1, 1 KB for Text 2, and 8 KB for sprites
- 2-layer text screen (background) and 256 sprites available
- Text 1 and Text 2
  - 4/16/256 colors
  - 65536 colors (RGB565)
  - Horizontal/vertical scrolling function
  - Vertical compression/extension function
  - 640 x 480 (H x V) pixels for normal display
  - Pixel bitmap
- Text 3
  - Text 3 cannot be used with Text 1 and Text 2
  - 65536 colors (RGB565)
  - 640 x 480 (H x V) pixels for normal display
- Sprite
  - 4/16/256 colors
  - Each sprite consists of one character
  - Locatable anywhere on the screen
  - Up to 63 sprites (8 x 8 pixels) per line
  - Scaling and rotation
  - Size (H&V): 8/16/32/64/128/256 pixels
  - Horizontal/vertical flip function for normal and scaling display
- Special effect: 16-level brightness adjustment (Text 1 and Text 2 only)

The data path of PPU is shown in the figure below.

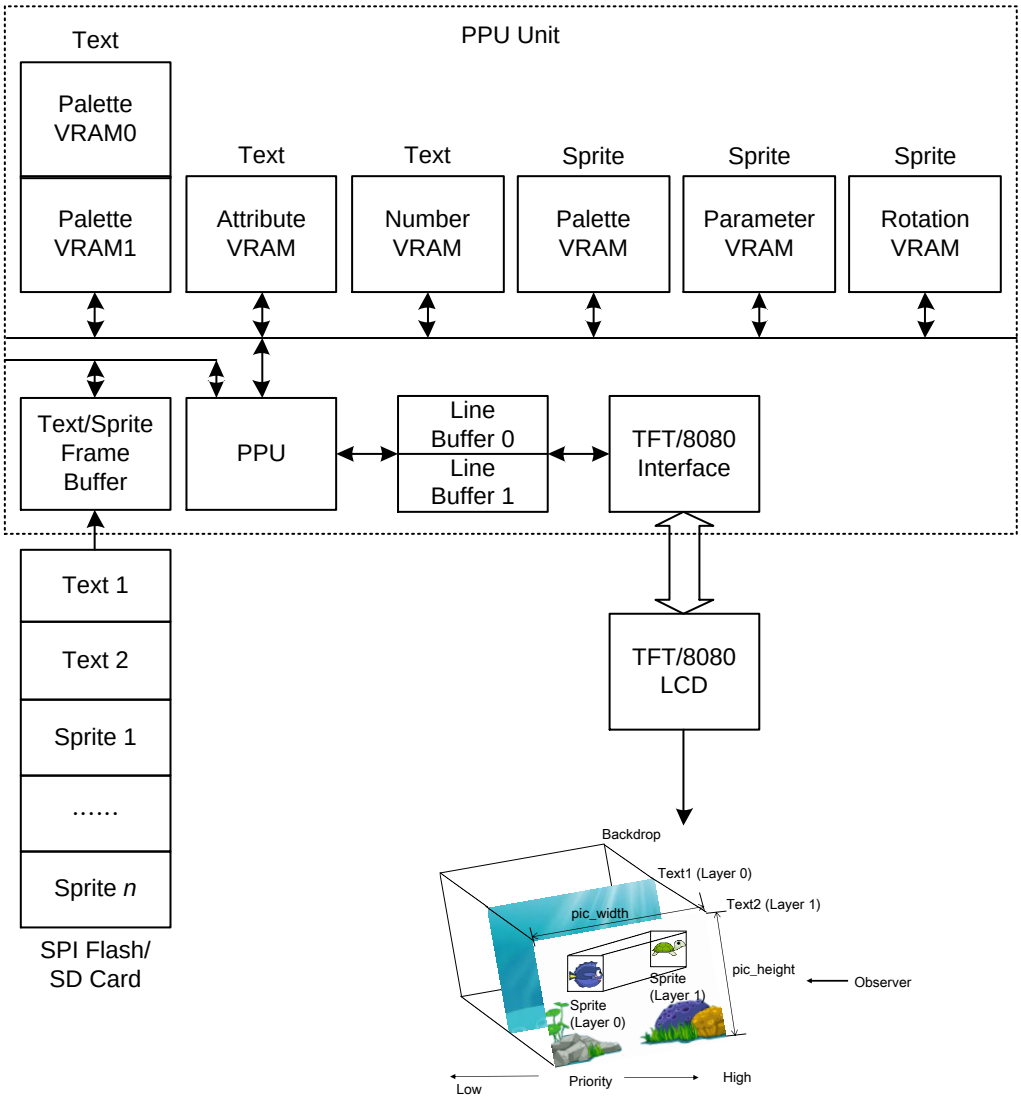


Figure 8–1 PPU Data Path

8.2 TFT-LCD Interface

The built-in TFT-LCD interface supports serial and parallel RGB modes (UPS051/UPS052) in RGB565 format only with resolution up to VGA (640 x 480).

8.2.1 Timing

Table 8–1 Switching Characteristics for TFT-LCD

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	t_H	Horizontal line	0	4 x (2^{15} - 1)	
2	t_{hsw}	Horizontal sync pulse width	0	2^{15} - 1	

No.	Parameter		Device		Unit
			MIN.	MAX.	
3	t_{hblk}	Horizontal sync blanking	0	2 x (2^{15} - 1)	DCLK[33]
4	t_{hdisp}	Horizontal display area	0	2^{15} - 1	
5	t_{hfp}	Horizontal sync front porch	0	2^{15} - 1	
6	t_V	Vertical sync period time	0	4 x (2^{15} - 1)	t_H
7	t_{vsw}	Vertical sync pulse width	0	2^{15} - 1	
8	t_{vblk}	Vertical sync blanking	0	2 x (2^{15} - 1)	
9	t_{vdisp}	Vertical display area	0	2^{15} - 1	
10	t_{vfp}	Vertical sync front porch	0	2^{15} - 1	

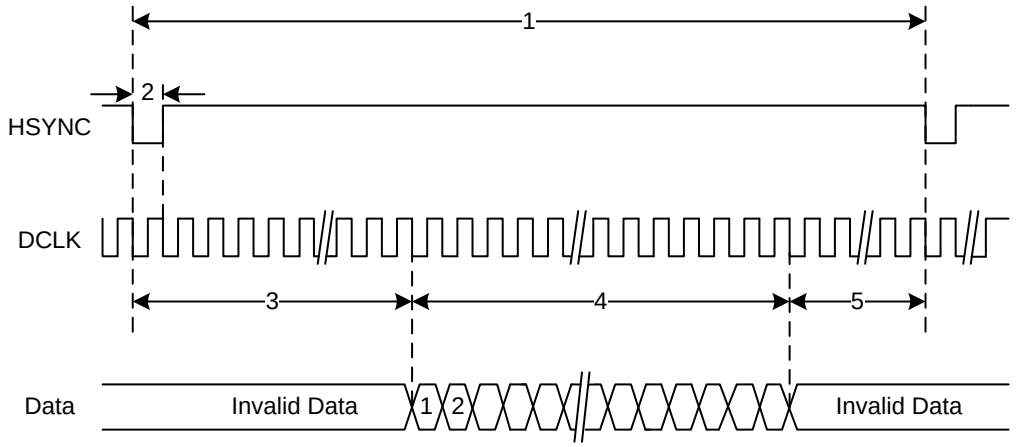


Figure 8–2 TFT-LCD Horizontal Timing

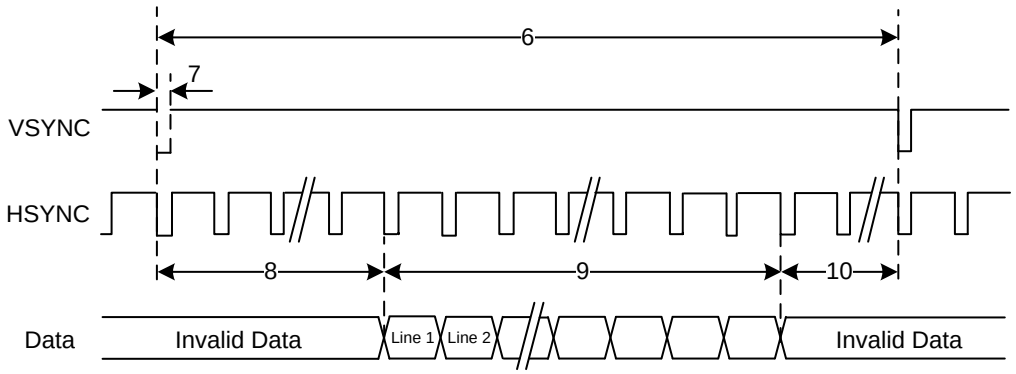


Figure 8–3 TFT-LCD Vertical Timing

8.3 8080 MCU Interface

The 8080 MCU interface for communication between the MCU controller and a LCD driver chip includes 8 or 16 bi-directional data lines, one chip-select line (CS), one writing-latch line (WE)/one reading-latch line (RE), and one data/command select line (A0).

[33] DCLK = 162 MHz / (CLK_PreScaler + 1); CLK_PreScaler = 0–65535

Features of the 8080 MCU interface are:
- 8/16-bit data space
- Auto access word data for the lower 8-bit data bus (high byte first or low byte first)
- Adjustable access signal pulse

8.3.1 Timing

The clock delay of 8080 MCU interface is 1 idle clock (1 / 162 MHz) per 16-bit transmission.

Table 8–2 Switching Characteristics for 8080 MCU Interface

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	t_{PWLW}	Write low time	1 / 162 MHz x (0 + 1)	1 / 162 MHz x (255 + 1)	ns
2	t_{PWHW}	Write high time	1 / 162 MHz x (0 + 1)	1 / 162 MHz x (255 + 1)	
3	t_F	Fall time	6		
4	t_R	Rise time	6		

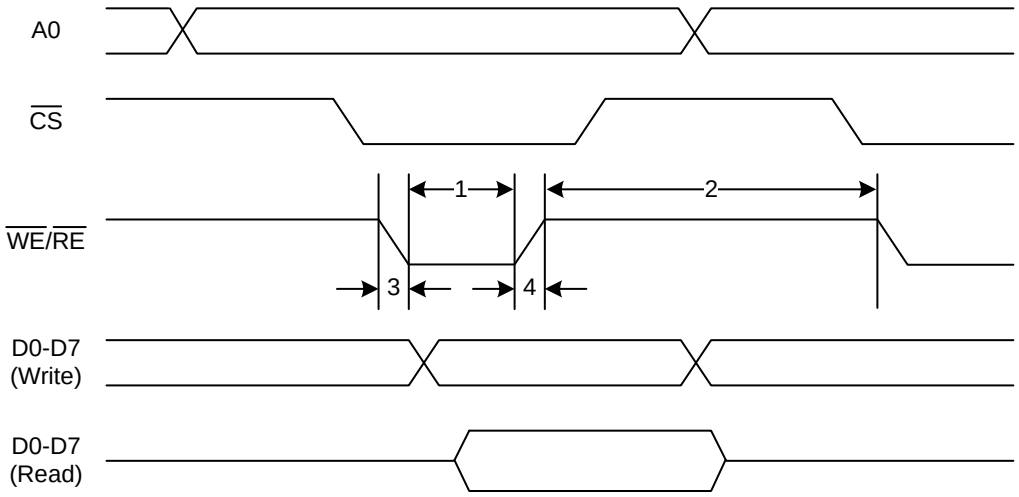


Figure 8–4 8080 MCU Interface Timings

8.4 CMOS Image Sensor (CIS) Interface

The CIS interface is an advanced 12-pin interface consisting of a CIS clock, VSYNC, HREF, pixel clock and eight data lines. The frequency of the CIS clock which outputs to the CIS module can be configured as MCLK / 2, MCLK / 4 or MCLK / 8. VSYNC, HSYNC and the pixel clock signals from the CIS module can be configured for active timing as rising or falling edge. An interrupt flag will be issued after a line of data is transmitted to RAM, which informs the system to access data that is stored at Window Random Access Memory (WRAM).

Features of the CIS interface are:
- Supports image resolution in VGA (640 x 480), CIF (352 x 288), QVGA (320 x 240), QCIF (176 x 144), and QQVGA (160 x 120)
- Supports image data formats in YUV422 and 8-bit RGB
- Adjustable VSYNC, HREF and pixel clock edge trigger selection
- Adjustable clock output, system clock divided by 2, 4, or 8
- Output image cropping and scaling
- Supports Line to block (L2B) mode for CSC and JPEG encoder

- Supports three line buffers, Line 0, Line 1, and Line 2[34]
- RGB and YUV data mode to DRAM or SRAM by DMA, but L2B mode to DRAM is not available.

WARNING The system crushes when using cropping and scaling functions at the same time.

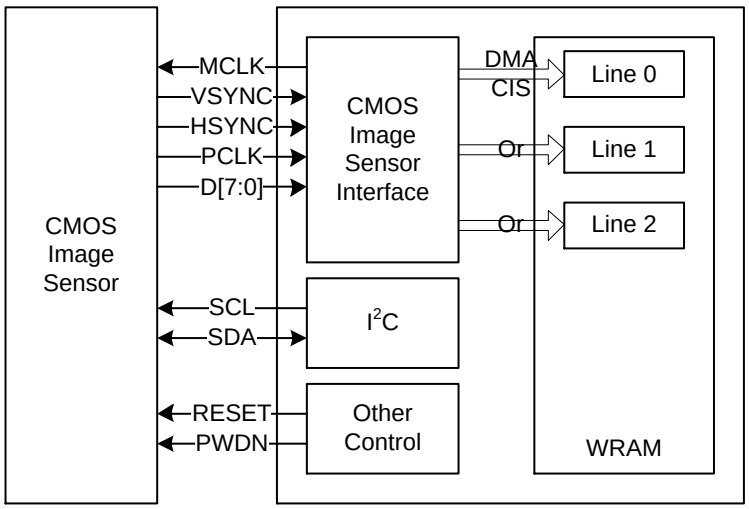


Figure 8–5 CIS Interface Block Diagram

8.4.1 Timing

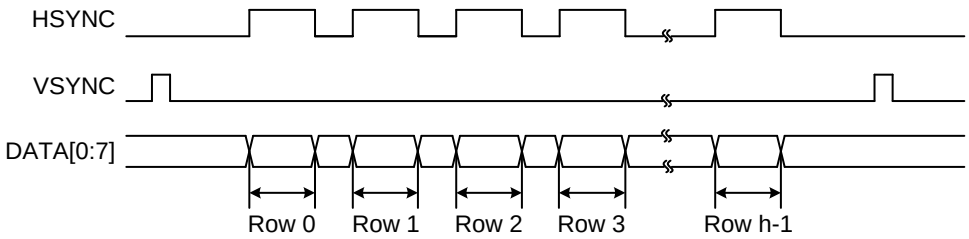


Figure 8–6 CIS Interface Timing

[34] When L2B mode is enabled, set the size of the line buffer = frame width x 8. Refer to The DMA CIS Register (CH_LEN) in *SNC7320_reg_vx.xx* for detailed settings.

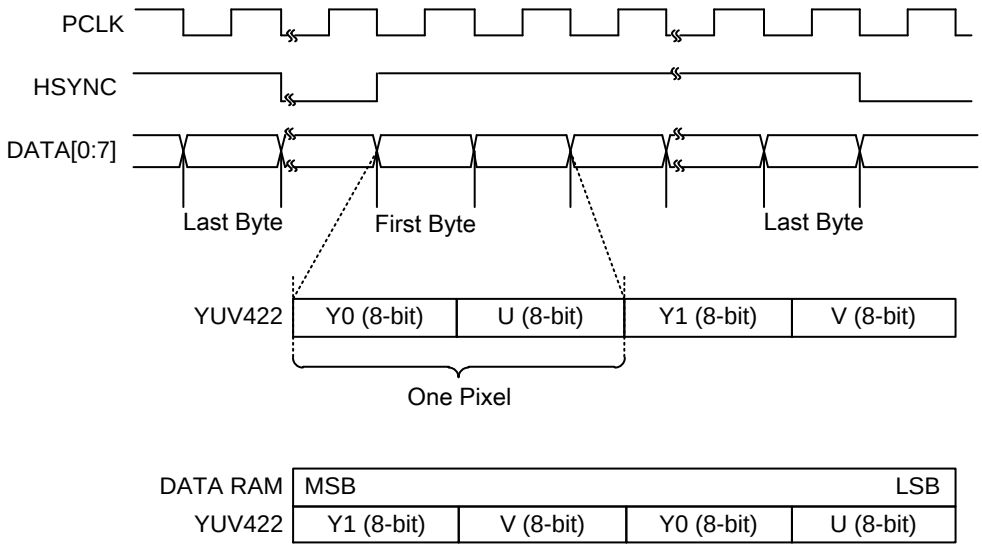


Figure 8–7 CIS Data Format

8.5 JPEG Codec

The JPEG codec of the SNC7320 Series supports JFIF format and functions either in encoder or decoder mode at the same time.

Features of the JPEG codec are:

- Video rate JPEG encode and decode
- Baseline DCT, fixed quantization table (two AC and two DC typical Huffman tables at ISO/IEC10918-1)
- Supports scaling quantization table ranging from 000.00001(B)–111.11111(B)
- JPEG File Interchange Format (JFIF)
- Format: YCbCr422 and 420 (depending on the external block function)
- Sharing DCT, zig-zag, quantizer and FIFO for encoder and decoder
- Encoder format:
  Block input: YCbCr422: 16 x 8 pixels; YCbCr420: 16 x 16 pixels, 8-bit data input
  Output: JPEG bit-stream, 8-bit data output
- Decoder format:
  Input: JPEG bit-stream in 8-bit data input
  Block output: YCbCr422: 16 x 8 pixels; YCbCr420: 16 x 16 pixels, 8-bit data output

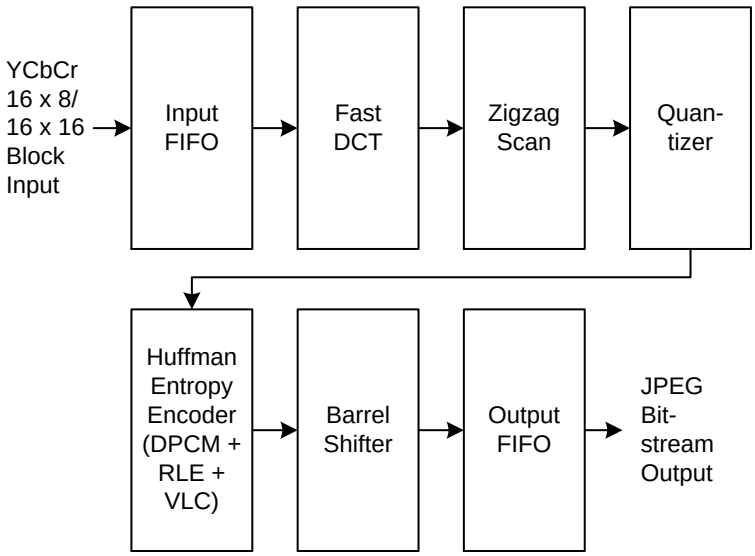


Figure 8–8 Encoder Hardware Block Diagram

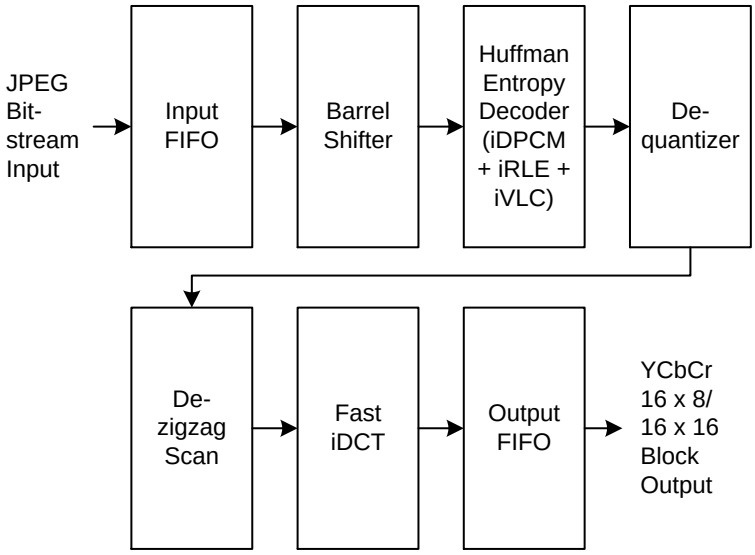


Figure 8–9 Decoder Hardware Block Diagram

8.6 Color Space Converter (CSC)

The CSC converts pixel data from YCbCr422 or 420 to RGB565 format.

Features of the CSC are:

- Direct raw data to line buffer movement
- RGB output sequence: R0, G0, B0; R1, G1, B1
- YCbCr422 input sequence:
  Y1, Y0; Y3, Y2; Cb23, Cb01; Cr23, Cr01
  Y5, Y4; Y7, Y6; Cb67, Cb34; Cr67, Cr34
- YCbCr420 input sequence:
  Y1, Y0; Y3, Y2; Cb4567, Cb0123; Cb4567, Cr0123

Y5, Y4; Y7, Y6; Cb4567, Cb0123; Cr4567, Cb0123

- Dithering and scaling mode
  Supports nine-tap FIR filters to avoid aliasing and false color when scaling down. The value should be:

Filter0 + (Filter1 + Filter2 + Filter3 + Filter4) x 2 = 256

8.7 Audio-I²S

The audio system of the SNC7320 Series has five sets of I²S. I²S0 to I²S3 support slave mode with DMA and connect to multiple audio codecs such as SNAUD01. I²S4 supports slave and mater mode and is dedicated to communicate with other master chips. To maximize the utilities, the SNC7320 Series supports eight Microphone arrays or six Microphone arrays and a stereo DAC.

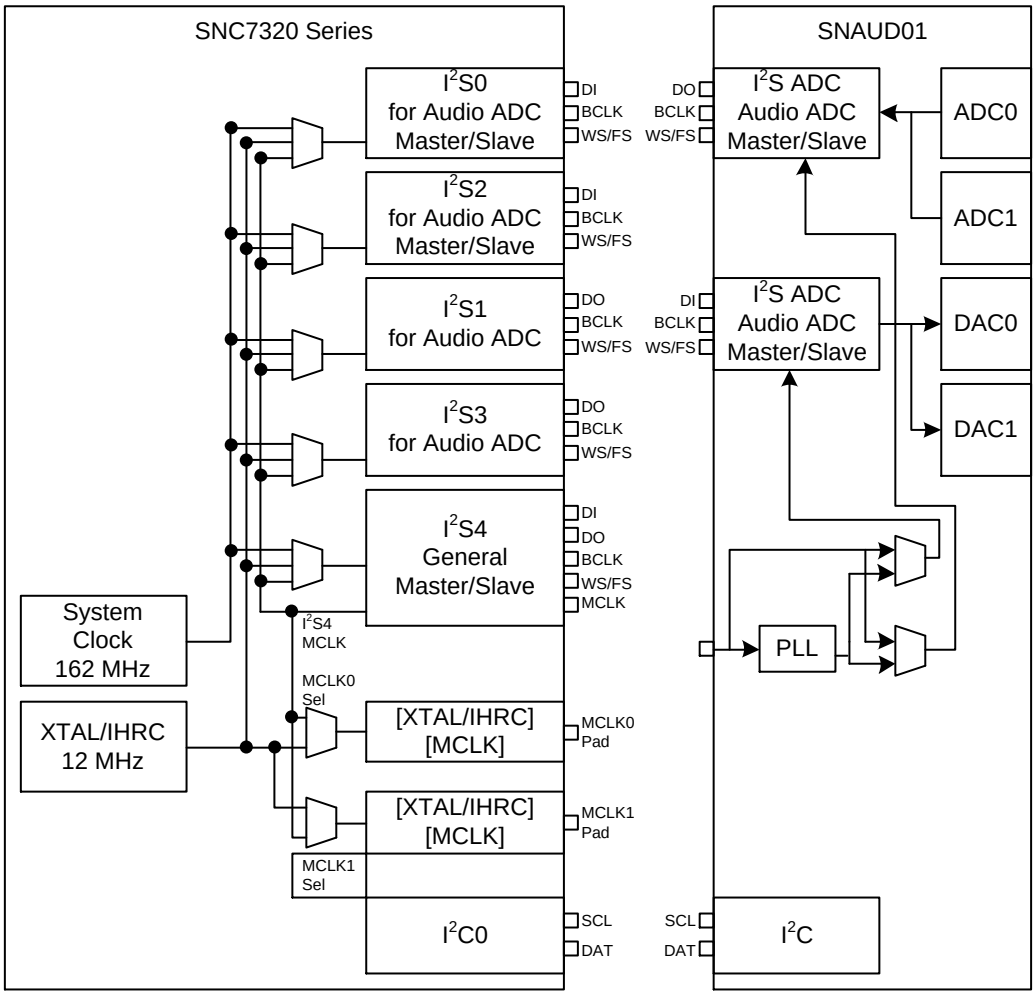


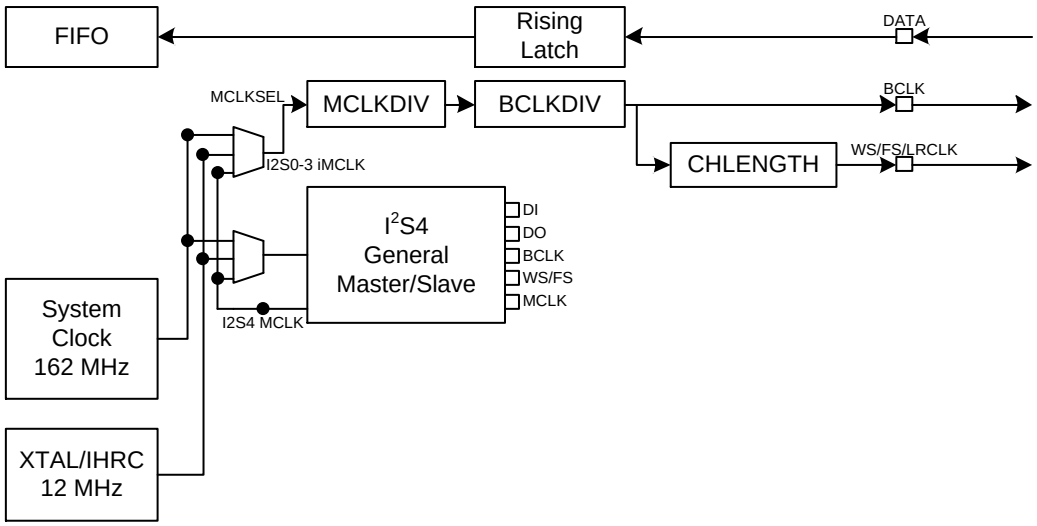
Figure 8–10 Audio Block Diagram

Features of the I²S include:

- Master or slave mode
- 8/16/24/32-bit data length
- Mono and stereo audio data
- I²S and MSB justified data format

- Provides 8-word (32-bit) FIFO data buffers
- Generate interrupt requests when buffer levels cross a programmable boundary
- Independent reset, stop, and mute control options for I²S input and output

Master Mode Rx



Master Mode Tx

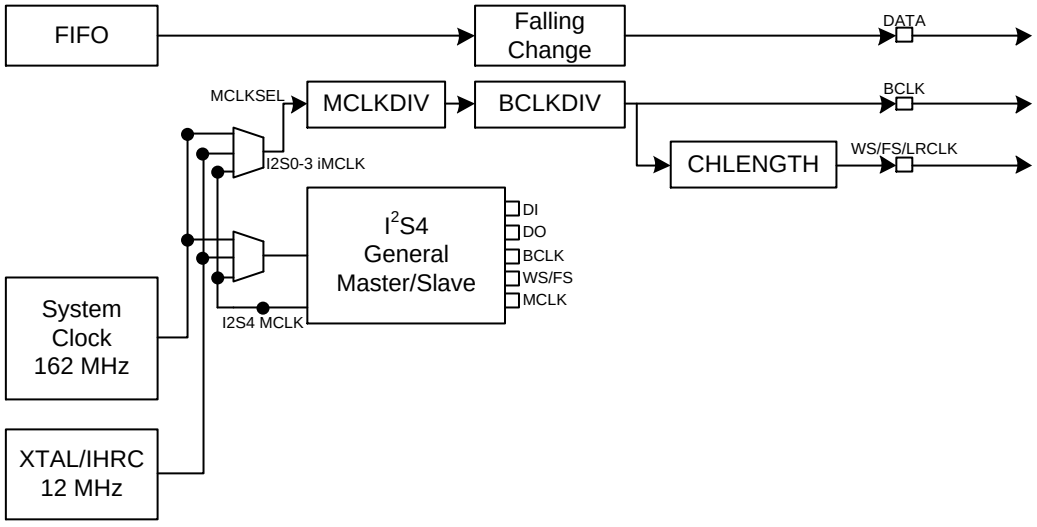
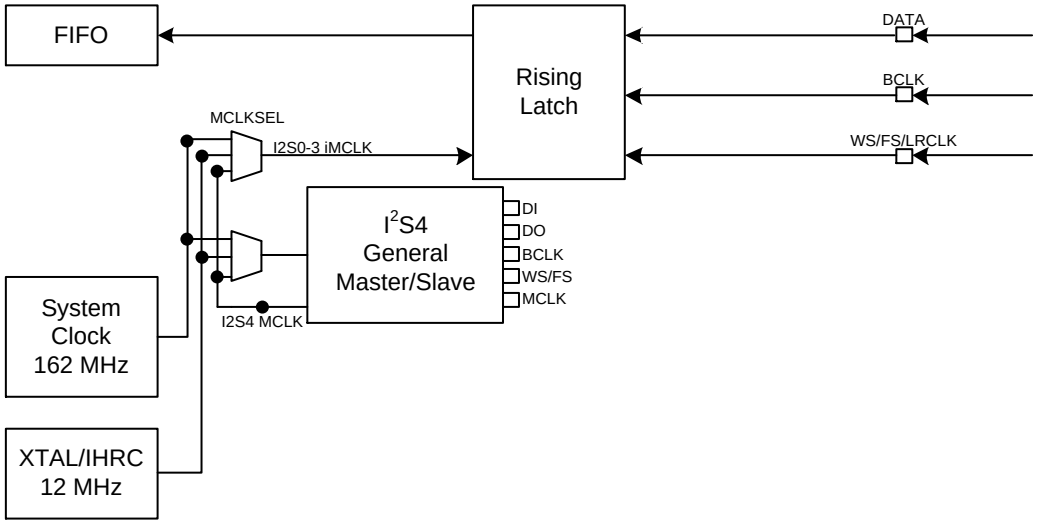


Figure 8–11 I²S Master Mode Block Diagram

Slave Mode Rx



Slave Mode Tx

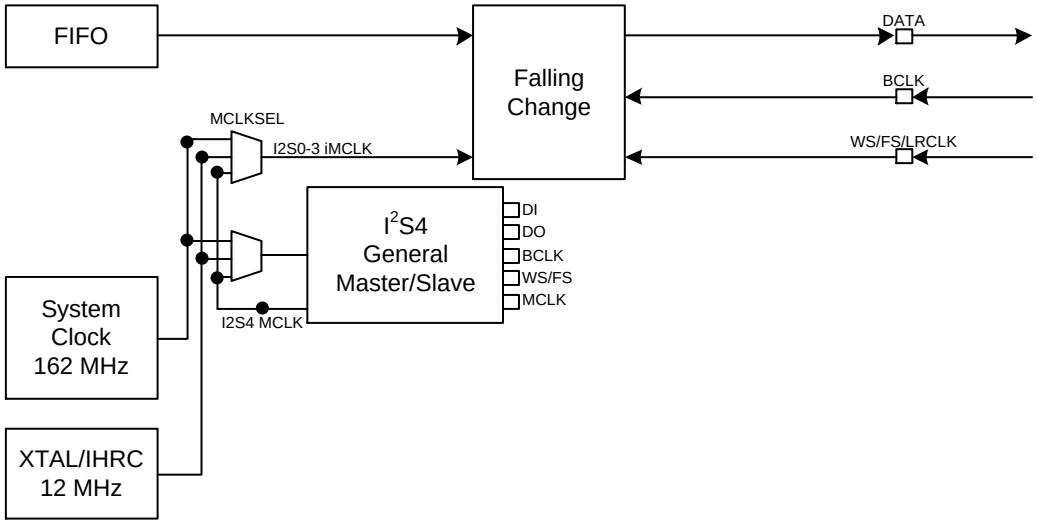


Figure 8–12 I²S Slave Mode Block Diagram

8.7.1 Timing

Table 8–3 Input Timing Requirements for I²S Master Receiver

Parameter		Device		Unit
		MIN.	MAX.	
$t_{su(SDR-BCK)}$	Setup time, I2S_DATA_IN valid before I2S_BCLK rising edge	0.2 ($t_{c(BCK)}$)	–	ns
$t_{h(BCK-SDR)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	2	–	

Table 8–4 Input Timing Requirements for I²S Slave Receiver

Parameter		Device		Unit
		MIN.	MAX.	
$t_{c(BCK)}$	Cycle time, I2S_BCLK	80	10200	ns
$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.35 ($t_{c(BCK)}$)	–	
$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.35 ($t_{c(BCK)}$)	–	
$t_{su(SDR-BCK)}$	Setup time, I2S_DATA_IN valid before receive rising edge of I2S_BCLK	0.2 ($t_{c(BCK)}$)	–	
$t_{h(BCK-SDR)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	2	–	

Table 8–5 Input Timing Requirements for I²S Slave Transmitter

Parameter		Device		Unit
		MIN.	MAX.	
$t_{c(BCK)}$	Cycle time, I2S_BCLK	80	10200	ns
$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.35 ($t_{c(BCK)}$)	–	
$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.35 ($t_{c(BCK)}$)	–	
$t_{r(BCK)}$	Rise time, I2S_BCLK	–	0.15 ($t_{c(BCK)}$)	

Table 8–6 Switching Characteristics for I²S Master Receiver

Parameter		Device		Unit
		MIN.	MAX.	
$t_{c(BCK)}$	Cycle time, I2S_BCLK	200[35]	10200	ns
$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.4 ($t_{c(BCK)}$)	–	
$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.4 ($t_{c(BCK)}$)	–	

Table 8–7 Switching Characteristics for I²S Master Transmitter

Parameter		Device		Unit
		MIN.	MAX.	
$t_{c(BCK)}$	Cycle time, I2S_BCLK	200[35]	10200	ns
$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.4 ($t_{c(BCK)}$)	–	
$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.4 ($t_{c(BCK)}$)	–	
$t_{d(BCK-LRCK\_SDX)}$	Delay time, I2S_BCLK rising edge to I2S_DATA_OUT output	–	0.5 ($t_{c(BCK)}$) + 5	
$t_{h(BCK-LRCK\_SDX)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	0.5 ($t_{c(BCK)}$) - 5	–	
$t_{r(BCK)}$	Rise time, I2S_BCLK	–	20	

Table 8–8 Switching Characteristics for I²S Slave Transmitter

Parameter		Device		Unit
		MIN.	MAX.	
$t_{d(BCK-LRCK\_SDX)}$	Delay time, I2S_BCLK rising edge to I2S_DATA_OUT output	–	0.5 ($t_{c(BCK)}$) + 15	ns
$t_{h(BCK-LRCK\_SDX)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	0.35 ($t_{c(BCK)}$)	–	

[35] The minimum period of the master clock is 40 ns and the minimum period of BCK is two master clock cycles. But considering the period of BCK is three master clock cycles, the minimum pulse width (high or low) of BCK is 0.33 ($t_{c(BCK)}$) which violates the I²S input timing requirement. To meet the input timing requirement, the minimum period of BCK is five master clock cycles.

The I²S is a standard interface for general use. Since the audio controller supports mono and stereo, the data is valid in first 8/16/24/32-bit from MSB in left channel of its timing diagram.

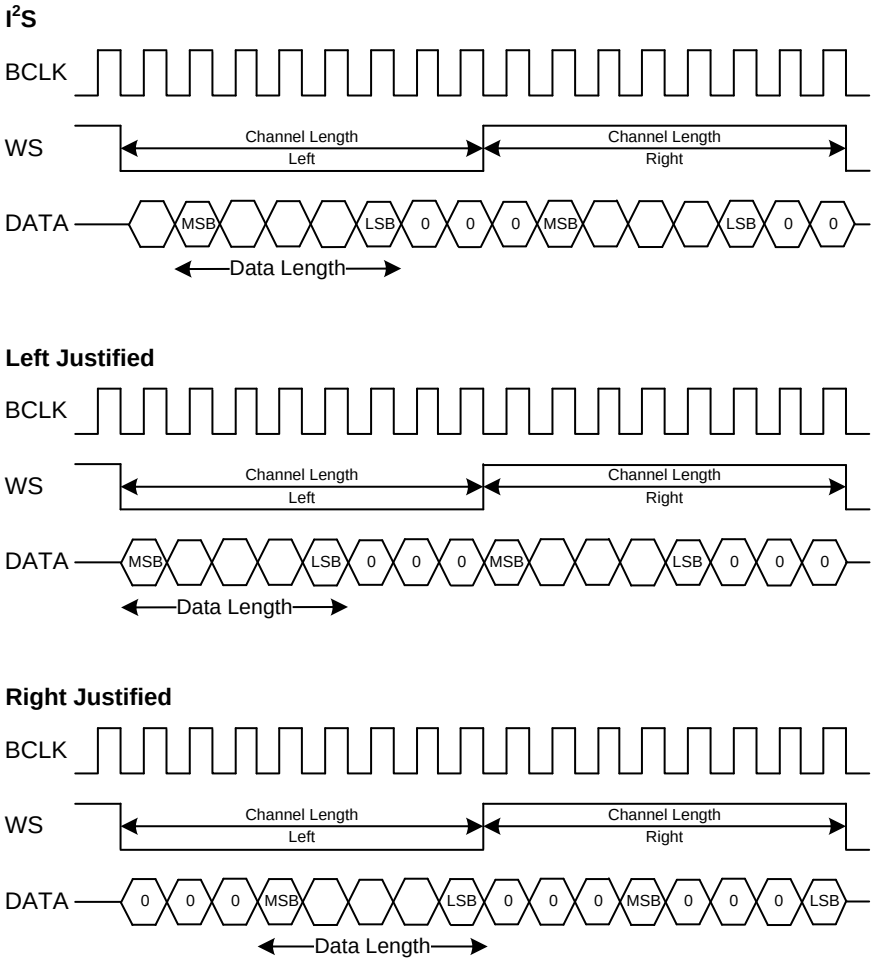


Figure 8–13 I²S Timings when Channel Length > Data Length

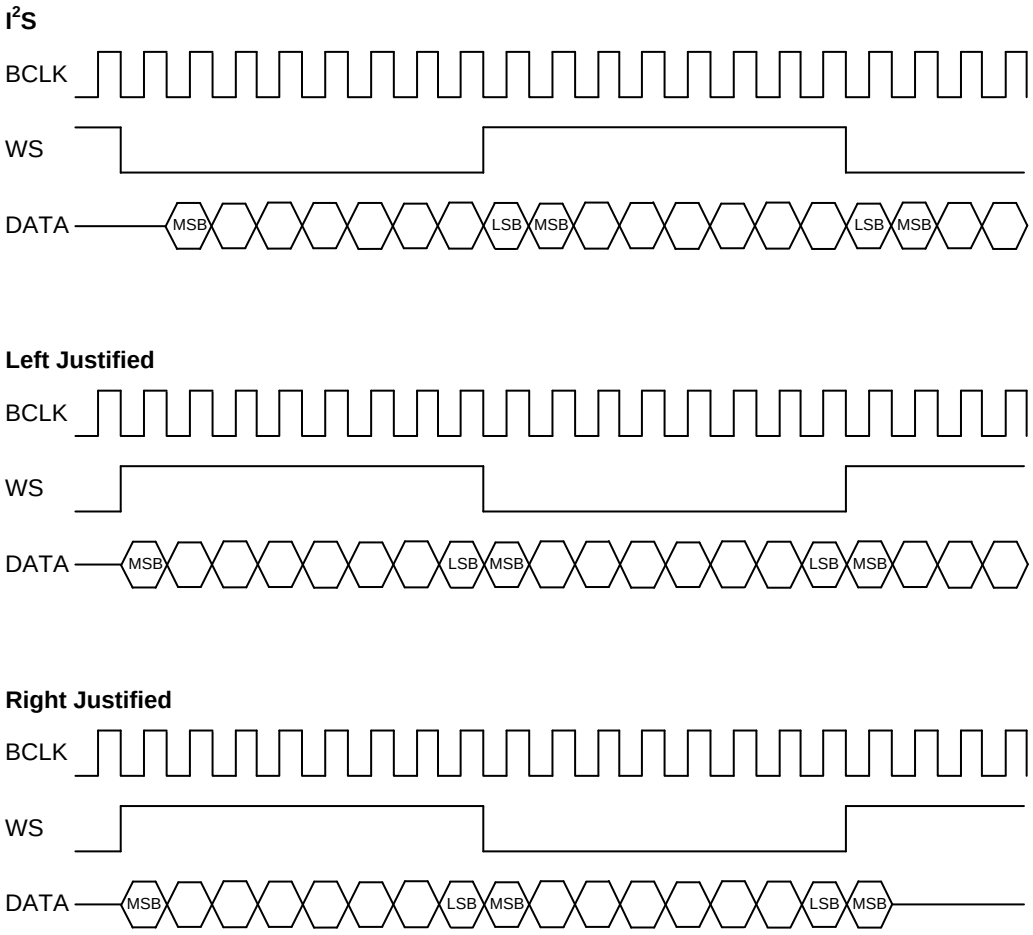


Figure 8–14 I²S Timings when Channel Length = Data Length

9 Device Operating Conditions

9.1 Absolute Maximum Ratings

Table 9–1 Absolute Maximum Ratings[36] [37]

Parameter		MIN.	MAX.	Unit
Supply voltage	V_{DDC}/V_{DD12} with respect to V_{ss}	-0.3	1.22	V
	V_{DD18} with respect to V_{ss}	-0.3	1.90	
	V_{DDIO33} with respect to V_{ss}	-0.3	3.60	
Analog voltage	V_{DDA18}	-0.3	1.90	
	V_{DDA33}	-0.3	3.60	
Input voltage	V_{IN} (1.8V)	-0.3	1.90	
	V_{IN} (3.3V)	-0.3	3.60	
Ambient temperature	T_A	0	85	°C
Junction temperature	T_J	-40	125	
Storage temperature	T_{STG}	-40	125	

9.2 Recommended Operating Conditions

Table 9–2 Recommended Operating Conditions

Parameter	MIN.	TYP.	MAX.	Unit
Device supply voltage, I/O, V_{DDIO33}	2.93	3.30	3.63	V
Device supply voltage, V_{DD18}	1.75	1.82	1.90	
Device supply voltage, V_{DDC}/V_{DD12} (normal mode)	1.19	1.22	1.26	
Device supply voltage, V_{DDC}/V_{DD12} (suspend mode)	0.95	0.99	1.04	
Supply ground, V_{SS}		0		
Analog supply voltage, V_{DDA33}	2.70	3.30	3.60	
Analog supply voltage, V_{DDA18}	1.75	1.82	1.90	
Analog supply ground, V_{SSA}		0		
Ambient temperature, T_A	0	–	85	°C
Junction temperature, T_J	-40	–	125	

[36] Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if the operation exceeds the maximum ratings.
[37] All voltage values are with respect to VSS.

9.3 Electrical Characteristics

Table 9–3 Electrical Characteristics over Recommended Ranges

Parameter		Conditions (T_A = 25 °C)	MIN.	TYP.	MAX.	Unit
Normal current 40.5 MHz	$I_{NOR40.5}$	Dual core program run; no I/O toggle	–	20	–	mA
Normal current 81 MHz	I_{NOR81}	Dual core program run; no I/O toggle	–	30	–	
Normal current 162 MHz	I_{NOR162}	Dual core program run; no I/O toggle	–	50	–	
Deep power-down current	I_{DPD}	V_{DD} = 3.3V; internal LDO 1.1/1.8V off, all clock off	–	1	5	µA
Deep sleep current	I_{DSLP}	All clock off	–	2.3	12	mA
IHRC	F_{IHRC}	Accuracy to ±1.5%	11.82	12	12.18	MHz
ILRC	F_{ILRC}	For WDT frequency	–	32	–	kHz
SAR ADC ENOB	ENOB	–	–	9	–	bit(s)
SAR ADC DNL	DNL	–	-2	–	2	LSB
SAR ADC INL	INL	–	-2	–	2	
Internal pull-up/pull-down resistance	R_{PU}/R_{PD}	–	30k	40k	66k	Ω
Internal pull-down resistance	R_{PD}	–	30k	40k	66k	
IO driving CFG0[38]	IO_{CFG0}	All GPIOs except SAR I/O	2	4.2	6	mA
IO driving CFG1 (default)	IO_{CFG1}		4	8.2	12	
IO driving CFG2	IO_{CFG2}		6	12.2	18	
IO driving CFG3	IO_{CFG3}		8	15.7	24	
IO sink CFG0	IO_{CFG0}		2	3.8	6	
IO sink CFG1 (default)	IO_{CFG1}		4	7.4	12	
IO sink CFG2	IO_{CFG2}		6	11	18	
IO sink CFG3	IO_{CFG3}		8	14.3	24	
SAR I/O driving CFG0	AIO_{CFG0}	P0.4–P0.7/P4.2–P4.3	5	10	17	
SAR I/O driving CFG1 (default)	AIO_{CFG1}		10	21.8	35	
SAR I/O driving CFG2	AIO_{CFG2}		15	25.2	51	
SAR I/O driving CFG3	AIO_{CFG3}		20	27.4	68	
SAR I/O sink CFG0	AIO_{CFG0}		5	10	17	
SAR I/O sink CFG1 (default)	AIO_{CFG1}		10	21.0	35	
SAR I/O sink CFG2	AIO_{CFG2}		15	23.9	51	
SAR I/O sink CFG3	AIO_{CFG3}		20	26.5	68	

[38] CFG*n* represents the configurations of GPIO driving control register (*n* = 0–3).

9.4 Power Sequence

9.4.1 Power-up Sequence

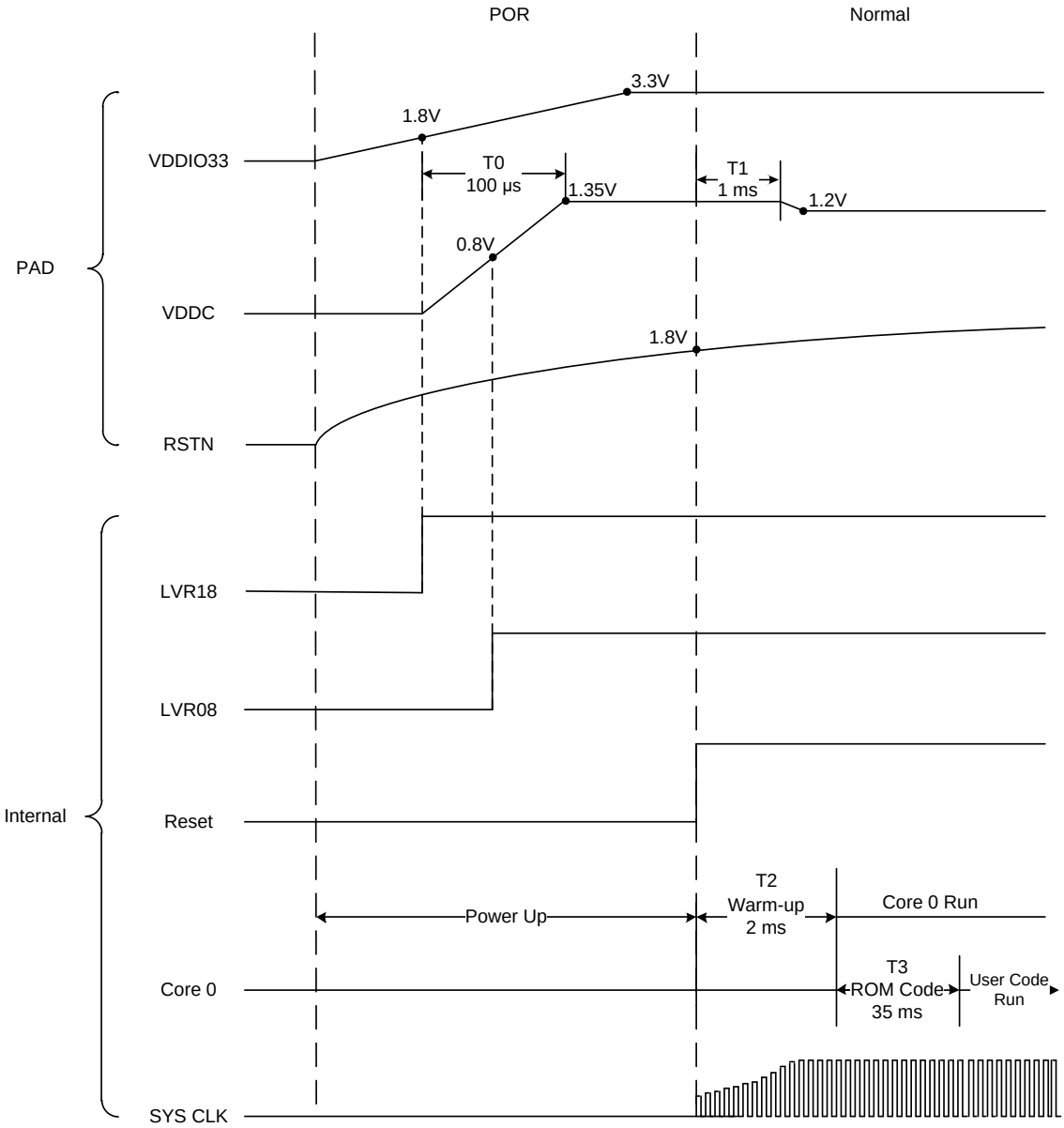


Figure 9–1 Power-up Sequence

Designs of the SNC7320 Series must comply with the power-up sequence guidelines below to ensure reliable operation of the device.

Requirements:
1. VDDC must be over 1.2V before M3 enters T1 state.
2. VDDIO33 must be over 1.8V before RSTN reaches 1.8V.

9.4.2 Deep Power-down (DPD) and Wakeup (WKP) Sequence

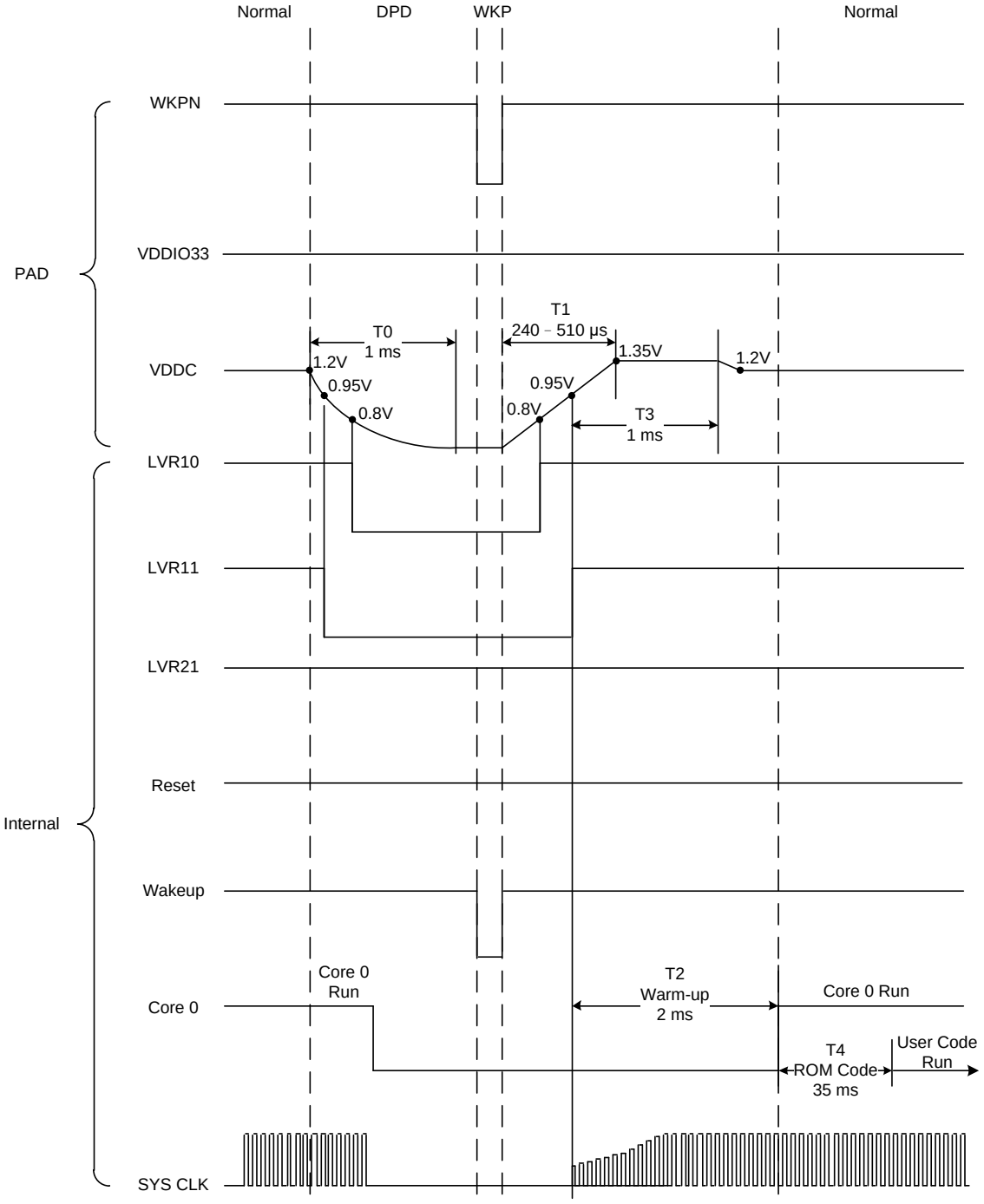


Figure 9–2 Deep Power-down and Wakeup Sequence

Requirement: The WKPN signal must return to high before VDDC enters T1 state.

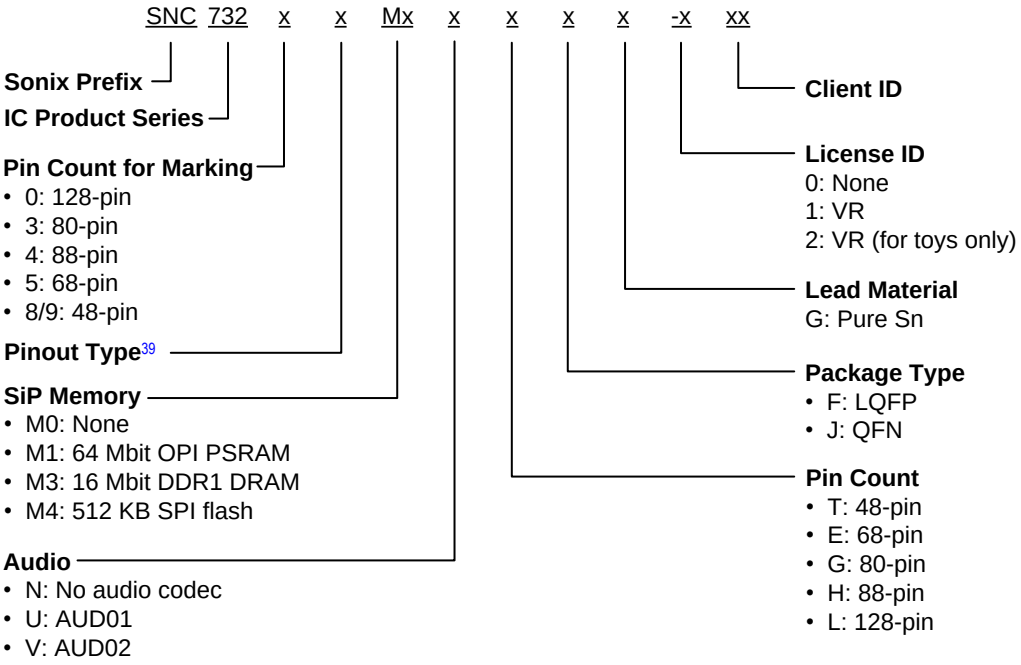
10 Mechanical Data

10.1 Thermal Data

The permissible operating temperature range for the bearing is 0 °C to 85 °C.

10.2 Package Information

10.2.1 Nomenclature



[39] This code represents different pinout of the same package.

10.2.2 Marking

The product ID and symbols shown in the figure below represents an example and may vary according to different packages.

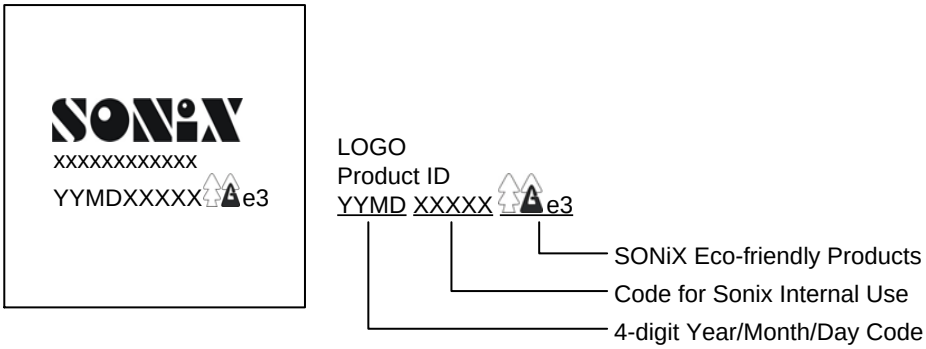
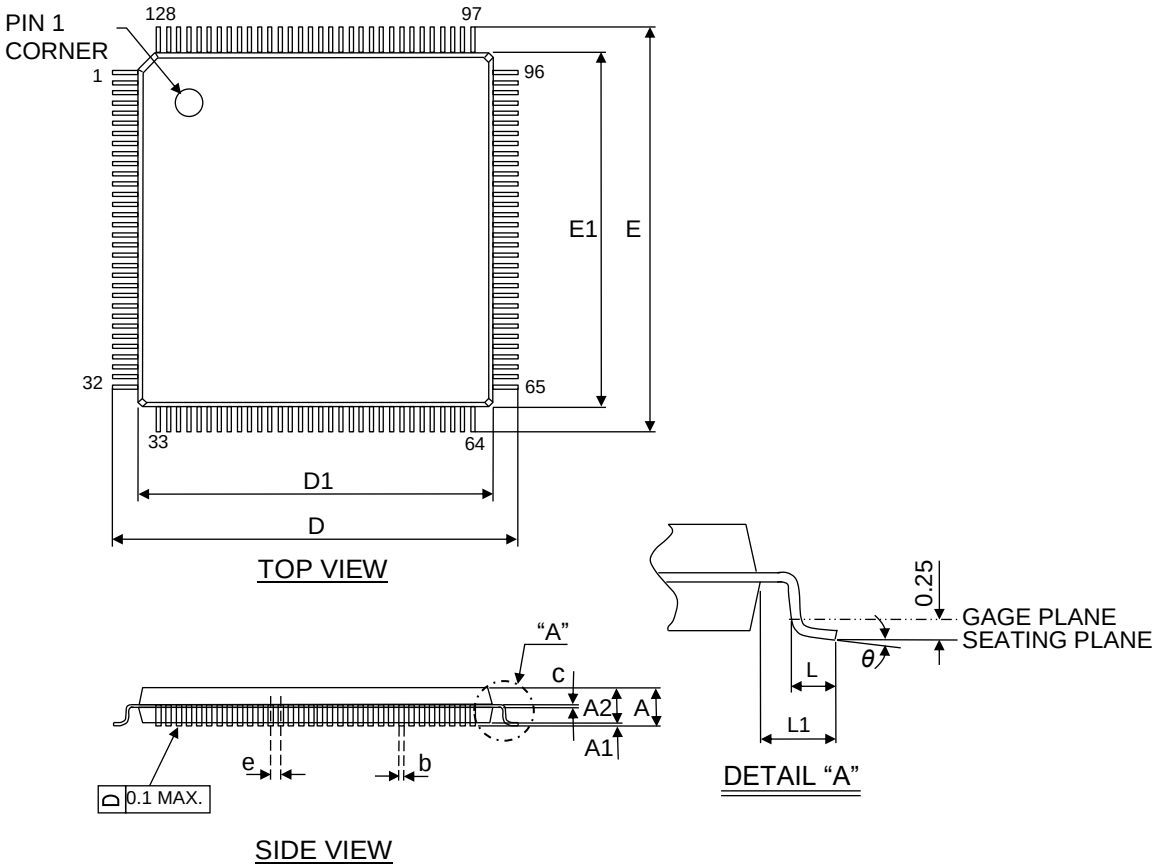


Figure 10–1 Example of Device Marking

10.2.3 Package Dimensions

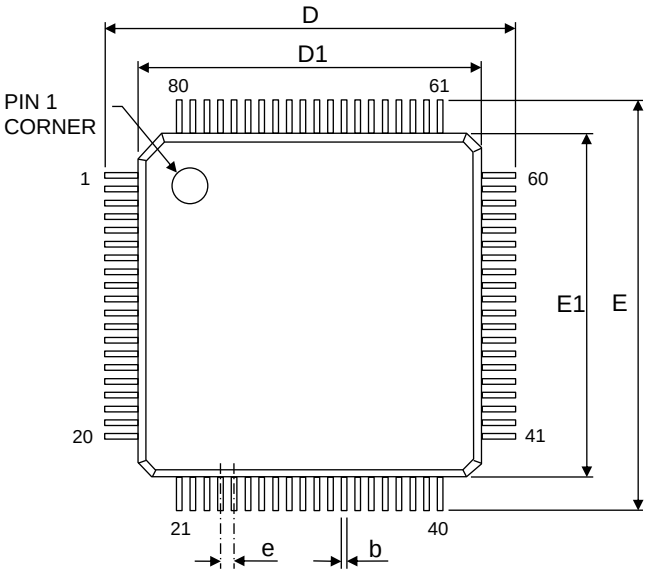
I. LQFP128L (14 x 14 x 1.4 mm/Pitch: 0.4)



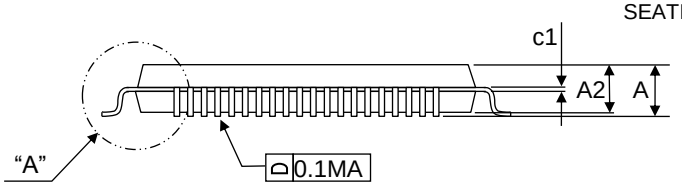
Symbols	Dimension in mm[40]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b[41]	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09	–	0.20	0.004	–	0.008
D	16.00 BSC			0.630 BSC		
D1[42]	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1[42]	14.00 BSC			0.551 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0˚	3.5˚	7˚	0˚	3.5˚	7˚

[40] Controlling dimension: millimeter (mm)
[41] Dimension "b" does not include dambar protrusion.
[42] Dimensions "D1" and "E1" do not include mold protrusion.

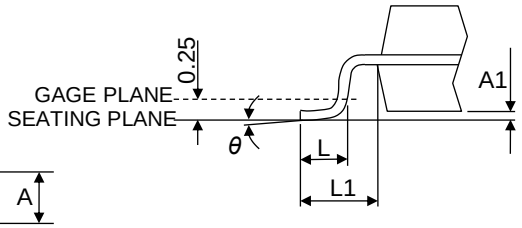
II. LQFP80L (10 x 10 x 1.4 mm/Pitch: 0.4)



TOP VIEW



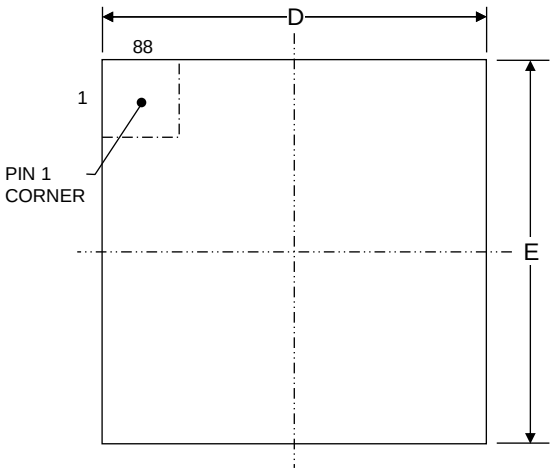
SIDE VIEW



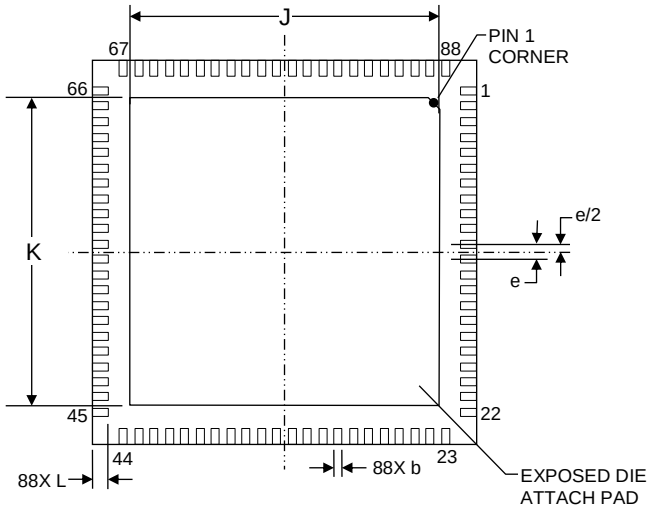
DETAIL "A"

Symbols	Dimension in mm[40]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.2	0.002	–	0.008
A2	1.35	1.40	1.45	0.053	0.055	0.057
b[41]	0.13	0.18	0.23	0.005	0.007	0.009
c1	0.09	–	0.18	0.004	–	0.007
D	12 BSC			0.472 BSC		
D1[42]	10 BSC			0.394 BSC		
e	0.4 BSC			0.016 BSC		
E	12 BSC			0.472 BSC		
E1[42]	10 BSC			0.394 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.0 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

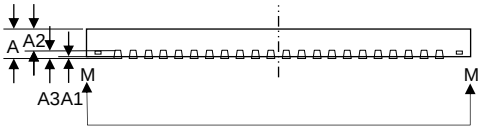
III. QFN88L (10 x 10 x 0.8 mm/Pitch: 0.4)



TOP VIEW



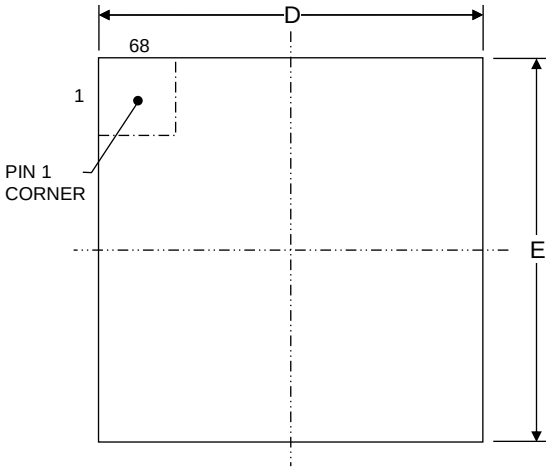
BOTTOM VIEW
VIEW M－M



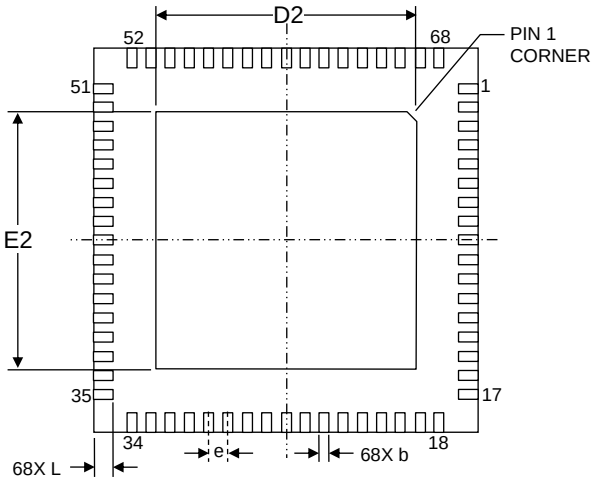
SIDE VIEW

Symbols	Dimension in mm[40]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.035	0.05	0.000	0.001	0.002
A2	–	0.55	0.57	–	0.022	0.022
A3	0.203 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	10.00 BSC			0.394 BSC		
E	10.00 BSC			0.394 BSC		
e	0.40 BSC			0.016 BSC		
J	6.50	7.50	8.50	0.256	0.295	0.335
K	6.50	7.50	8.50	0.256	0.295	0.335
L	0.30	0.40	0.50	0.012	0.016	0.020

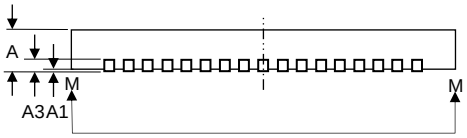
IV. QFN68L (8 x 8 x 0.8 mm/Pitch: 0.4)



TOP VIEW



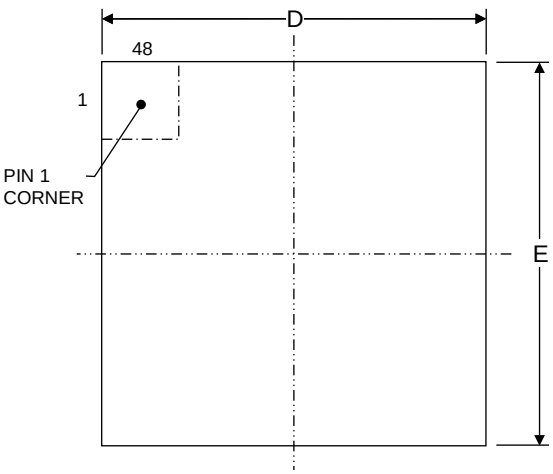
BOTTOM VIEW
VIEW M－M



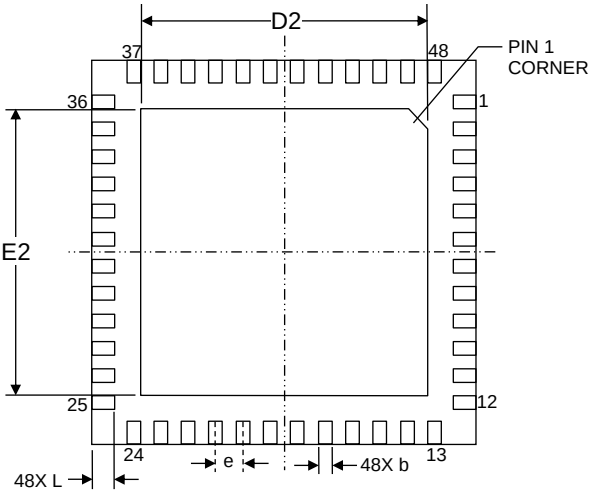
SIDE VIEW

Symbols	Dimension in mm[40]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.035	0.05	0.000	0.001	0.002
A3		0.203 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D		8.00 BSC			0.315 BSC	
E		8.00 BSC			0.315 BSC	
e		0.40 BSC			0.016 BSC	
D2	4.20	5.25	6.30	0.165	0.207	0.248
E2	4.20	5.25	6.30	0.165	0.207	0.248
L	0.30	0.40	0.50	0.012	0.016	0.020

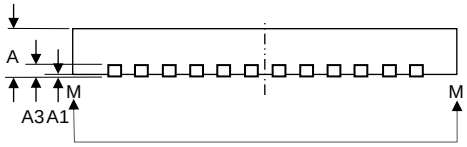
V. QFN48L (7 x 7 x 0.8 mm/Pitch: 0.5)



TOP VIEW



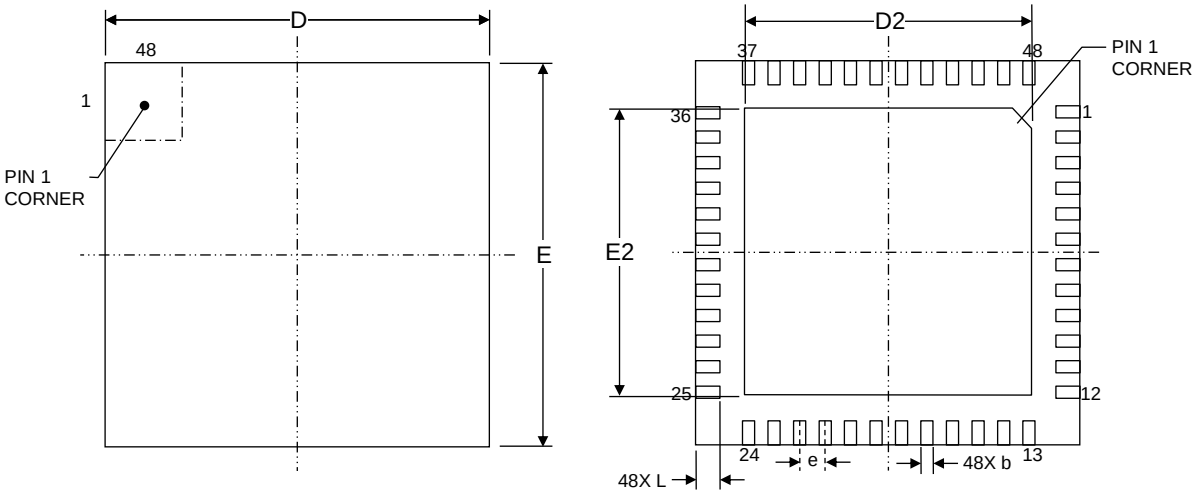
BOTTOM VIEW
VIEW M－M



SIDE VIEW

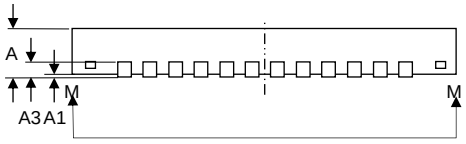
Symbols	Dimension in mm[40]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.20	0.25	0.30	0.008	0.010	0.012
D		7.00 BSC			0.267 BSC	
E		7.00 BSC			0.267 BSC	
e		0.50 BSC			0.020 BSC	
D2	4.40	5.00	5.60	0.173	0.197	0.220
D3	4.40	5.00	5.60	0.173	0.197	0.220
L	0.30	0.40	0.50	0.012	0.016	0.020

VI. QFN48L (6 x 6 x 0.8 mm/Pitch: 0.4)



TOP VIEW

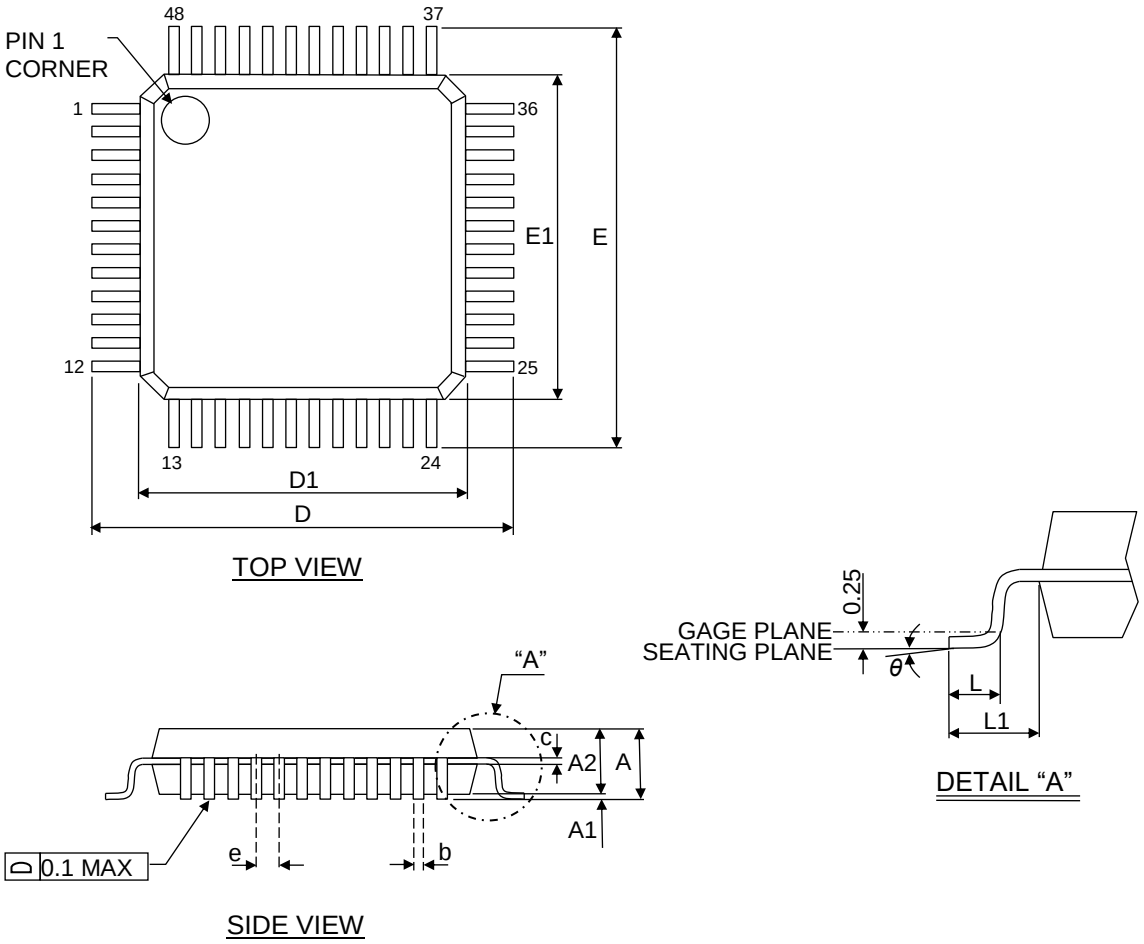
BOTTOM VIEW
VIEW M－M



SIDE VIEW

Symbols	Dimension in mm[40]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 BSC			0.236 BSC		
E	6.00 BSC			0.236 BSC		
e	0.4 BSC			0.016 BSC		
D2	3.70	4.20	4.70	0.146	0.165	0.185
E2	3.70	4.20	4.70	0.146	0.165	0.185
L	0.30	0.40	0.50	0.012	0.016	0.020

VII. LQFP48L (7 x 7 x 1.4 mm/Pitch: 0.5)



Symbols	Dimension in mm[40]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b[41]	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09	–	0.20	0.004	–	0.008
D	9.00 BSC			0.354 BSC		
D1[42]	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1[42]	7.00 BSC			0.276 BSC		
E	0.50 BSC			0.020 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

10.3 Packing Appearance and Storage Information

10.3.1 Packing Quantity

Table 10–1 Packing Quantity Information

Type	Pin Count	Carry Type	Package Size	IC Q'ty per Tube or Tray or Reel	Tube or Tray or Reel Q'ty per Inner Box	Total Q'ty in One Inner Box	Inner Box Q'ty per Carton	IC Q'ty per Carton
LQFP	128	Tray	14 x 14	90	10	900	6	5400
LQFP	80	Tray	10 x 10	160	10	1600	6	9600
LQFP	48	Tray	7 x 7	250	10	2500	6	15000
QFN	88	Tray	10x10	168	10	1680	6	10080
QFN	68	Tray	8 x 8	348	10	3480	6	20880
QFN	48	Tray	7 x 7	260	10	2600	6	15600
QFN	48	Tray	6 x 6	260	10	2600	6	15600

10.3.2 Packing Dimension

Table 10–2 Inner Box/Carton Dimension for LQFP128/LQFP80/LQFP48

Inner Box/Carton	Dimension in mm
Inner box	360 x 152 x 90
Carton	470 x 370 x 210
Carton (optional)	380 x 340 x 300

Table 10–3 Inner Box/Carton Dimension for QFN88/QFN68/QFN48

Inner Box/Carton	Dimension in mm
Inner box	358 x 159 x 88
Carton	555 x 435 x 280

10.3.3 Temperature and Humidity Environmental Control Requirements in Storage

Table 10–4 Store Condition

Control Requirement	Specification
Temperature (°C)	24 ± 6
Humidity (% RH)	60 ± 20

10.3.4 Shelf-life

1. The shelf life for unopened vacuum pack products is four years after the date on the label.
2. Once the packing is opened the product should be conducted SMT process within 168 hours and environmental control is under ≤ 30°C / 60% RH.
3. If the product has been exposed to the room environment for more than 168 hours, it should be baked in an oven at 125°C for 10 hours and vacuum packed.

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