CE252 : Digital Electronics

20DCS103

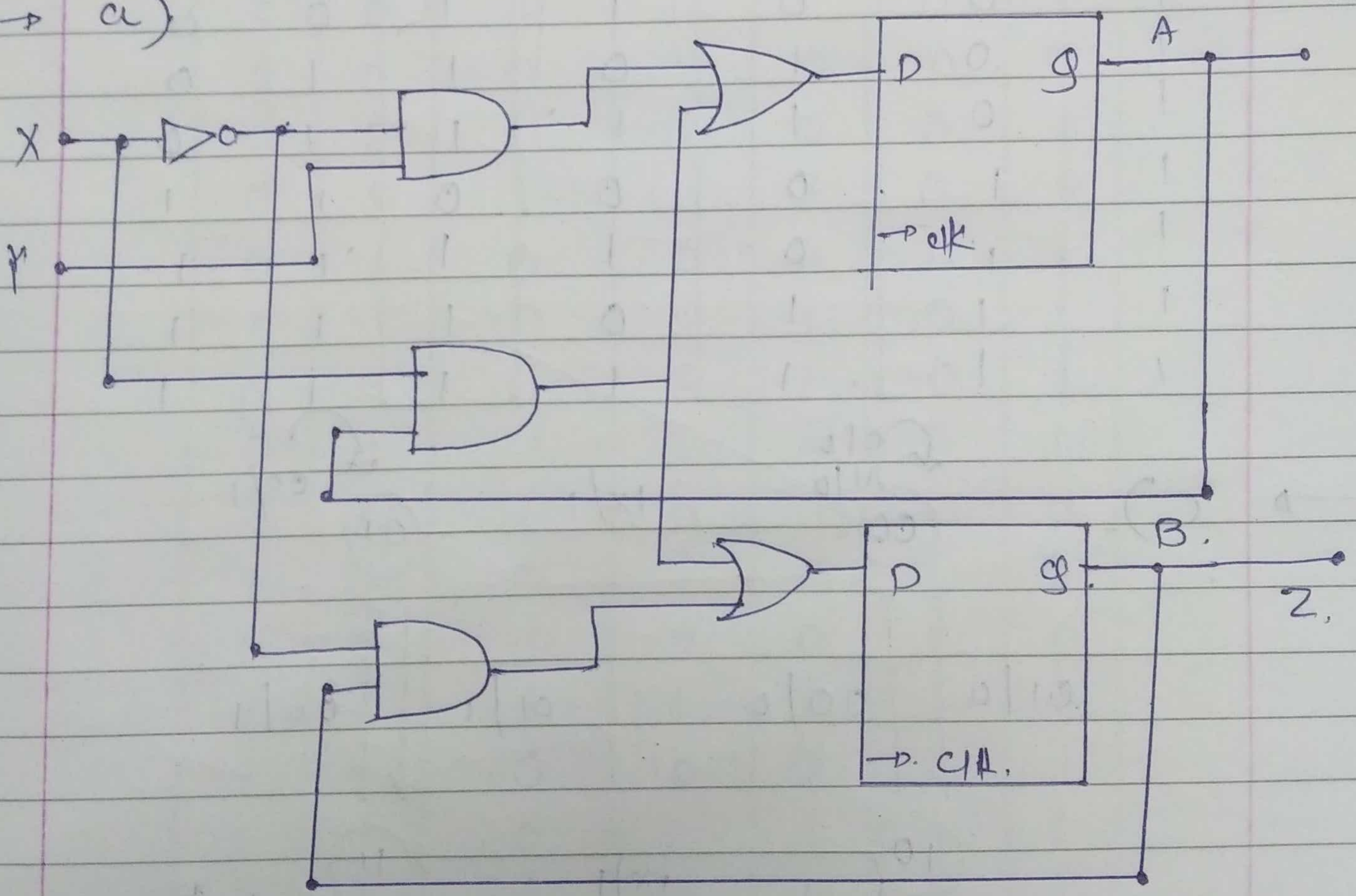
Assignment : Ch : 06

1. A sequential circuit with Two D - flip-flops, A and B ; Two inputs x and y and One output z specified by the following next state and output equations :

$A(t+1) = x'y + xA = DA$
$B(t+1) = x'B + xA = DB$
$z = B.$

a. Draw the logic diagram of the circuit
b. Derive the state table.
c. Derive the state diagram.

→ a)

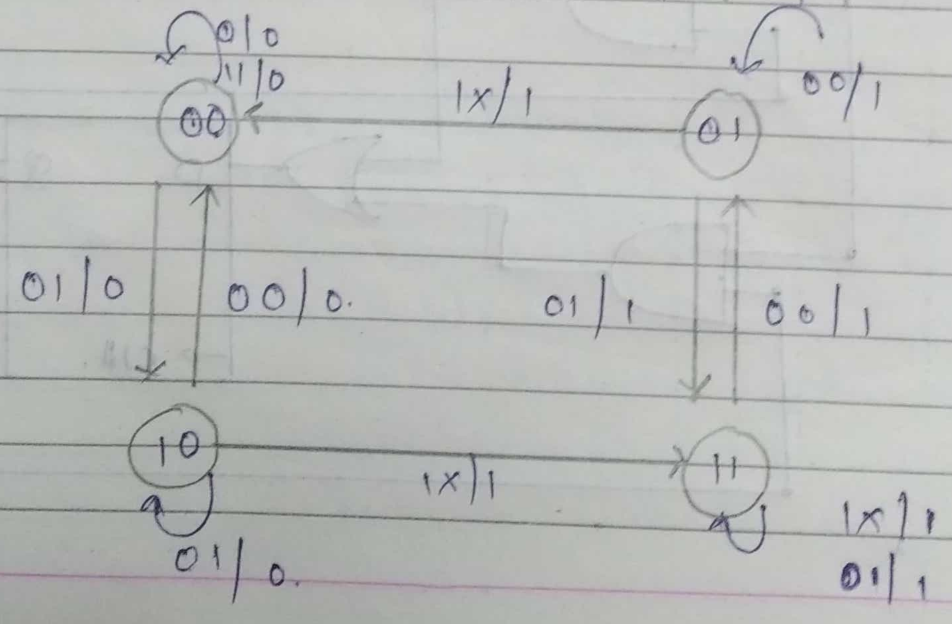


20DCS103

b).

Present state		Input		Next state		Output
A	B	x	y	A	B	
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

c).



20DCS103

2. A sequential circuit has three D-flip-flops, A, B & C. and one input x. It is described by the following flip-flop input functions :

$$D_A = (BC' + B'C)x + (BC + B'C')x$$

$$D_B = A$$

$$D_C = B.$$

a. Derive the state table for the circuit.

b. Derive the state diagram.

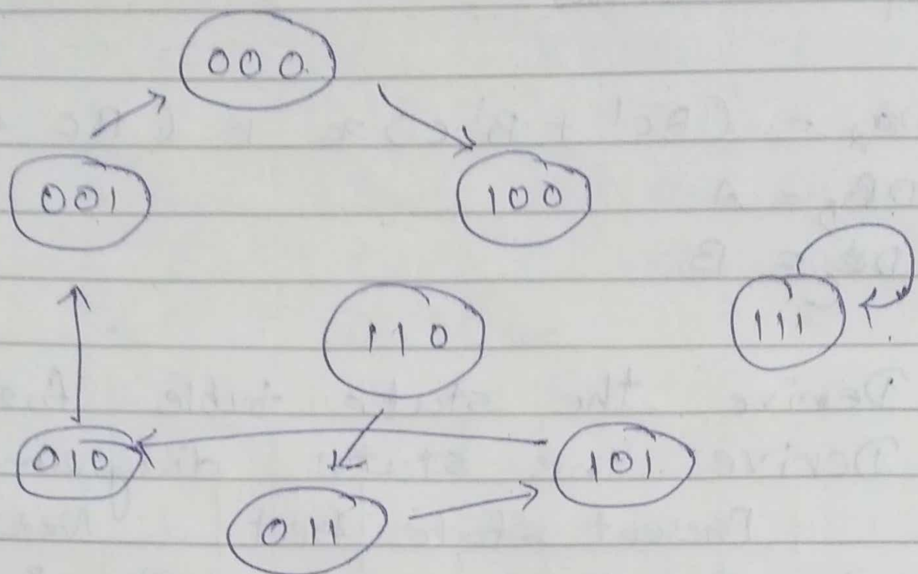
a).

Present state			Input	Next state		
A	B	C	x	A	B	C.
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	0	0	1
1	0	0	0	1	1	0
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	0	1	1

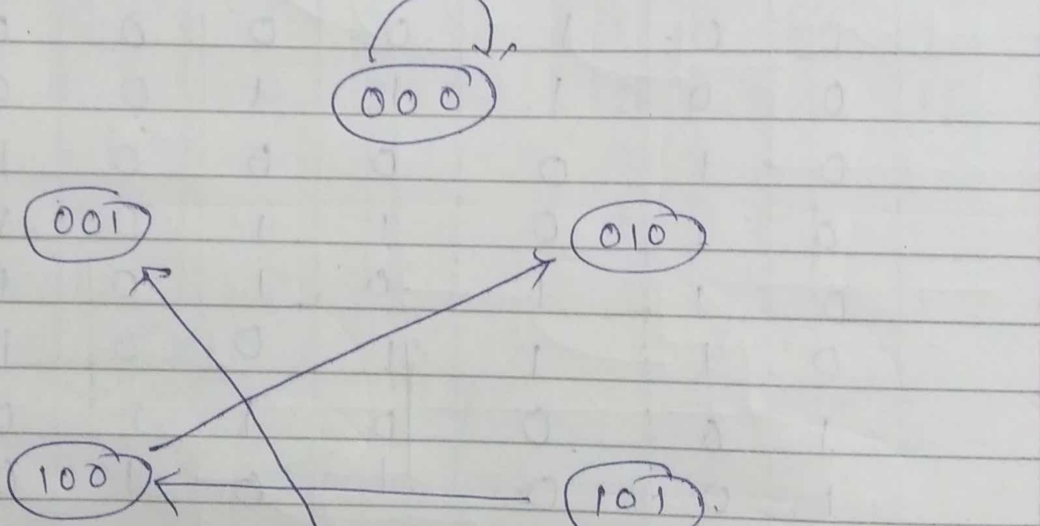
20DCS103

b) State diagram :-

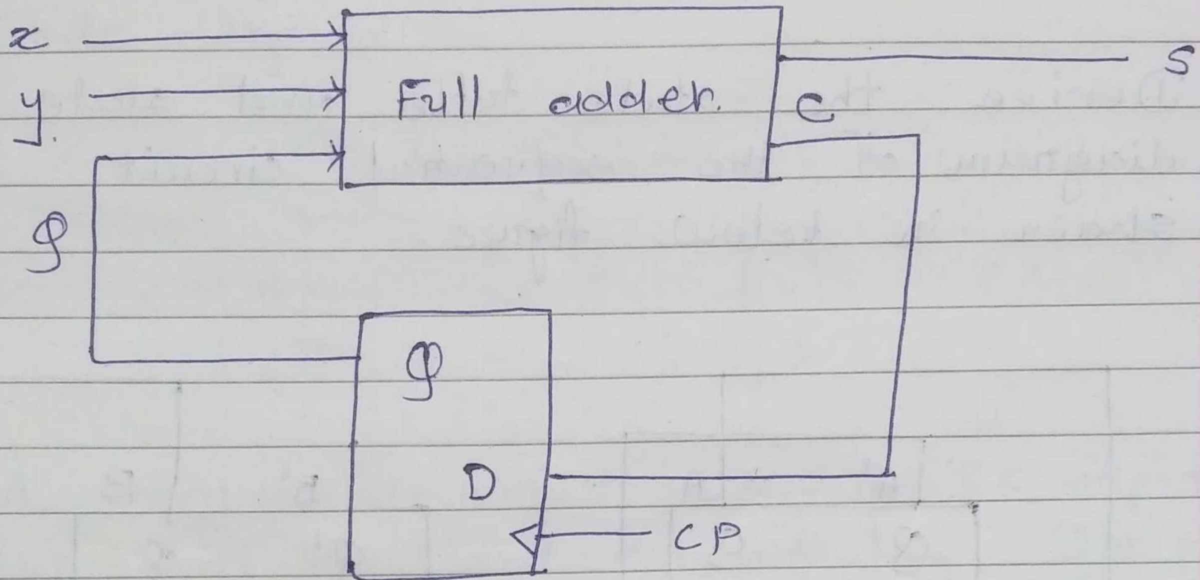
for x = 0.



for x = 1.



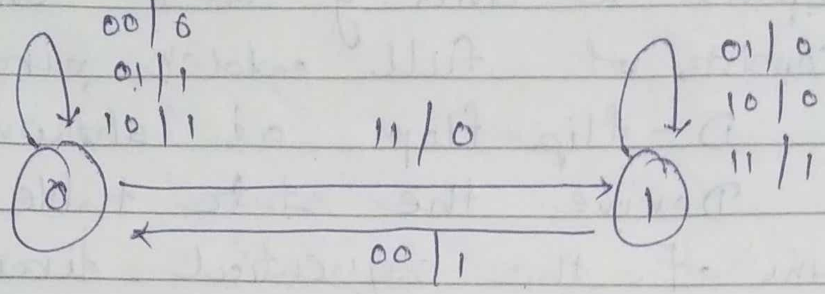
3. A sequential circuit has one flip-flop, Q; two inputs x and y and one output s. It consists of full adder circuit connected to a D-flip-flop as shown in below figure. Derive the state table and state diagram of the sequential circuit.



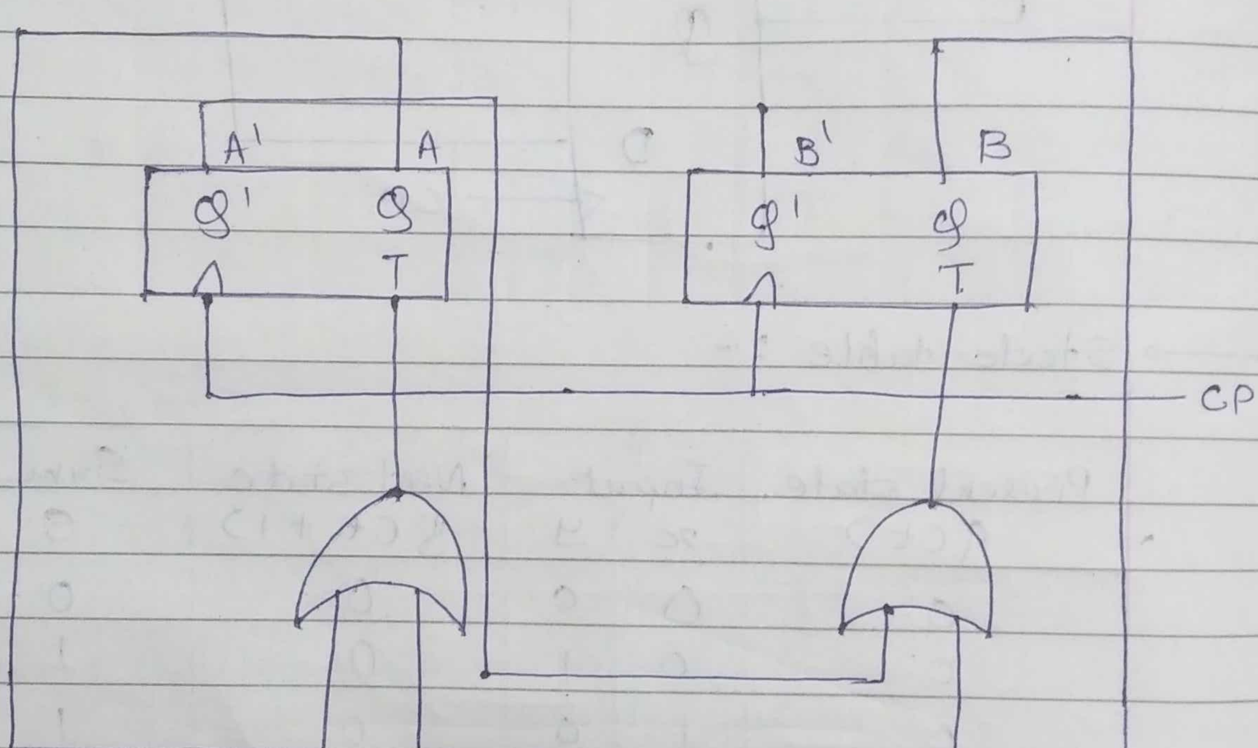
→ State table :-

Present state	Input		Next state	Sum
Q(t)	x	y	Q(t+1)	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

→ State diagram :-



4. Derive the state table and state diagram of the sequential circuit shown in below figure.

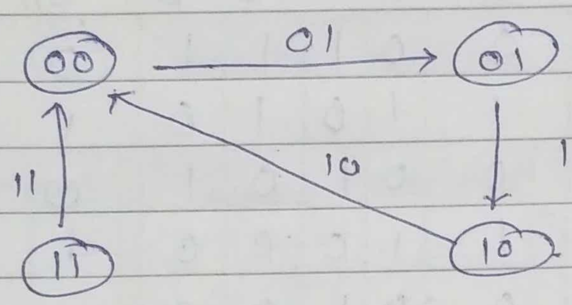


→ $T_A = A + B$

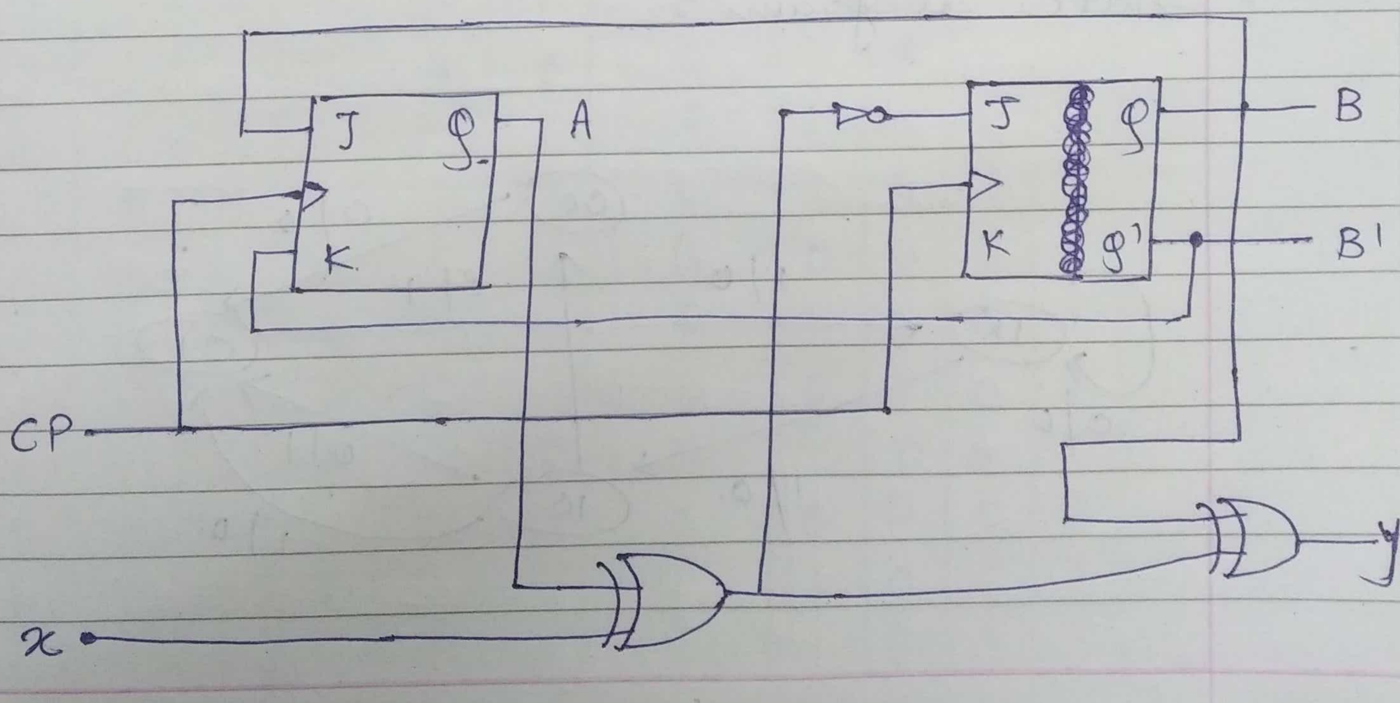
$T_B = A' + B$

Present state		Next state		Inputs	
A(t)	B(t)	A(t+1)	B(t+1)	TA	T_B
0	0	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1

→ State diagram :



5. A sequential circuit has two JK flip-flops; One input x : and one output y. Derive the state table and state diagram of the sequential circuit shown in below figure.



20DCS103

→ $J_A = B = Q_B \qquad J_B = \overline{A \oplus X} = A \odot X = Q_A$

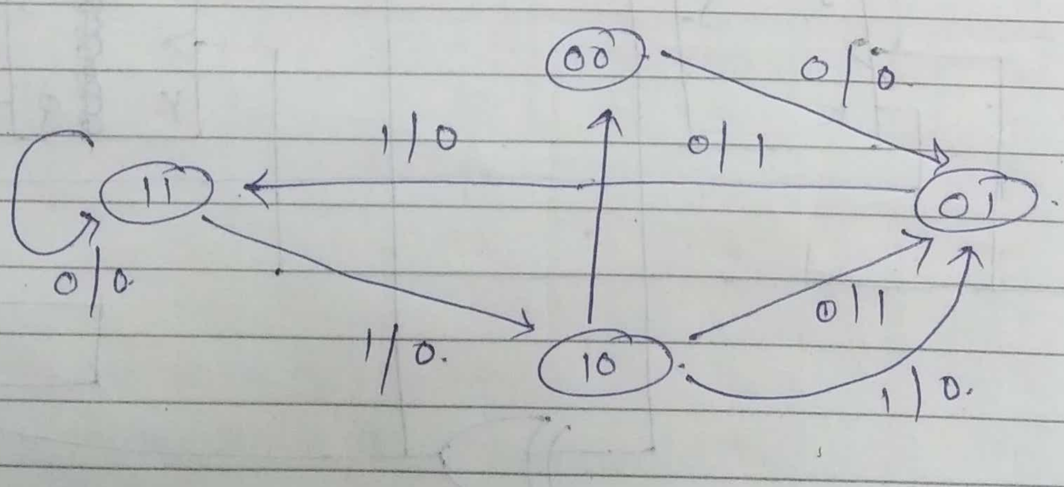
$K_A = \bar{B} = Q_B \qquad K_B = \overline{A \oplus x} = A \odot X = Q_A.$

$y = B \oplus (A \oplus X)$

→ State table :-

Input	Present state		FF Input				Next state		Output
X	A	B	J_A	K_A	J_B	K_B	Q_A	Q_B	y
0	0	0	0	1	1	1	0	1	0
0	0	1	1	0	1	0	1	0	1
0	1	0	0	1	0	1	0	0	1
0	1	1	1	0	0	0	1	1	0
1	0	0	0	1	0	0	0	0	1
1	0	1	1	0	0	0.	1	1	0
1	1	0	0	1	1	1	0	1	0
1	1	1	1	0	1	1	1	0.	1

→ State diagram :-



20DCS103

6. A sequential circuit has two JK flip-flops A and B ; two inputs x and y and one output z. It is described by the following flip-flop ~~output~~ input functions :

$J_A = (Bx + B'y')$ $\quad K_A = B'xy'$

$J_B = (A'x)$ $\quad K_B = A + (xy')$

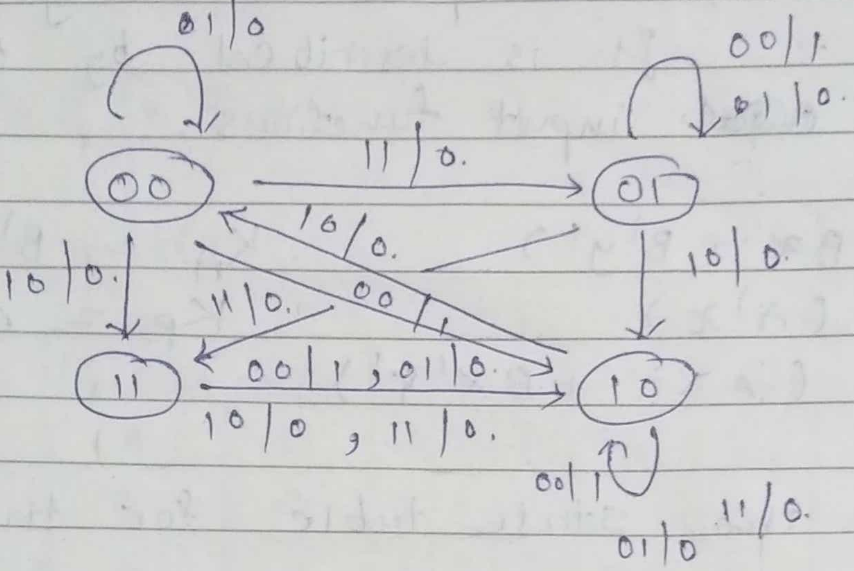
$Z = (AXY + BX'Y')$

a) Derive the state table for the circuit.

Present state		Input		Next state		Output	FF Input			
A	B	x	y	A(t+1)	B(t+1)	Z	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1
0	0	1	1	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	0	1	0	1	1
0	1	1	1	1	1	0	1	0	1	0
1	0	0	0	1	0	1	1	0	0	1
1	0	0	1	1	0	0	0	0	0	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0	0	0	1
1	1	0	1	1	0	0	0	0	0	1
1	1	1	0	1	0	0	1	0	0	1
1	1	1	1	1	0	0	1	0	0	1

20DCS103

→ b) State diagram :-



7. Draw the state diagram for the following state table. Also reduce the numbers of states of the state table. Tabulate reduced state table and draw the reduced state diagram of it.

Present State	Next State $x=0$	Next State $x=1$	Output $x=0$	Output $x=1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0.

$x = (d = h)$

Present State	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	h	c	0	0
c	f	e	0	0
d	g	a	1	0
e	h	c	0	0
f	g	h	1	1
g	g	a	0	1

x (b=e)

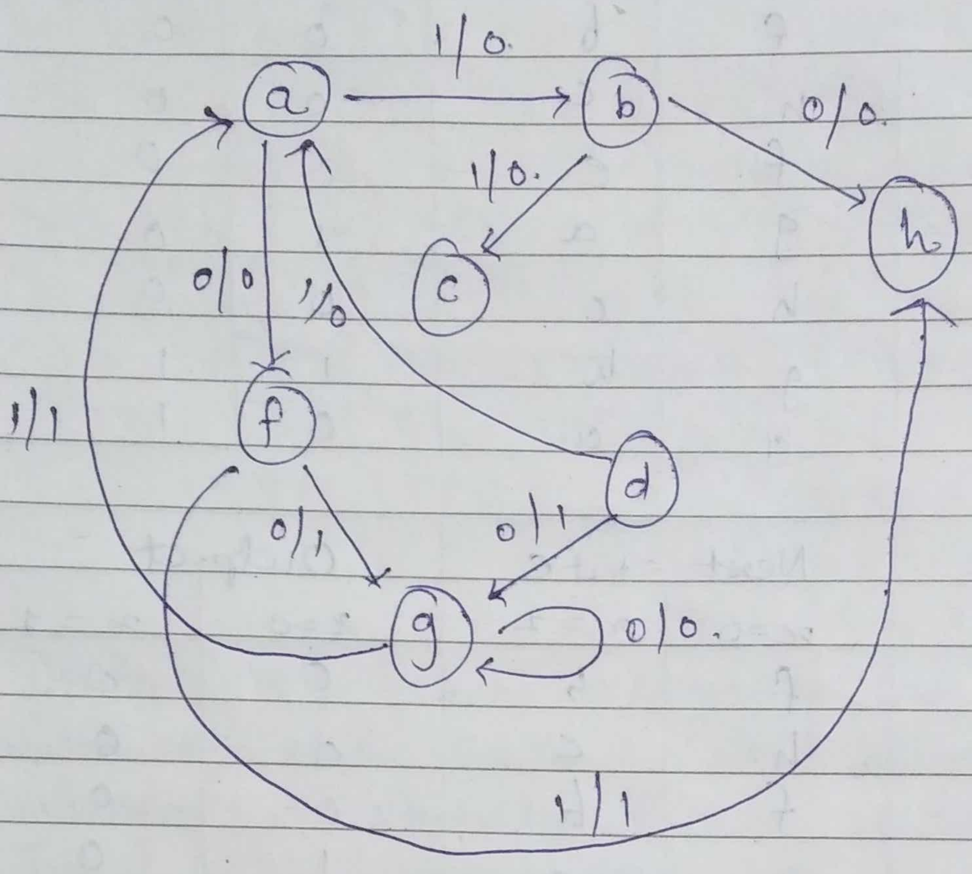
Present State	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	h	c	0	0
c	f	b	0	0
d	g	a	1	0
f	g	h	1	1
g	g	a	0	1

x (c=a)

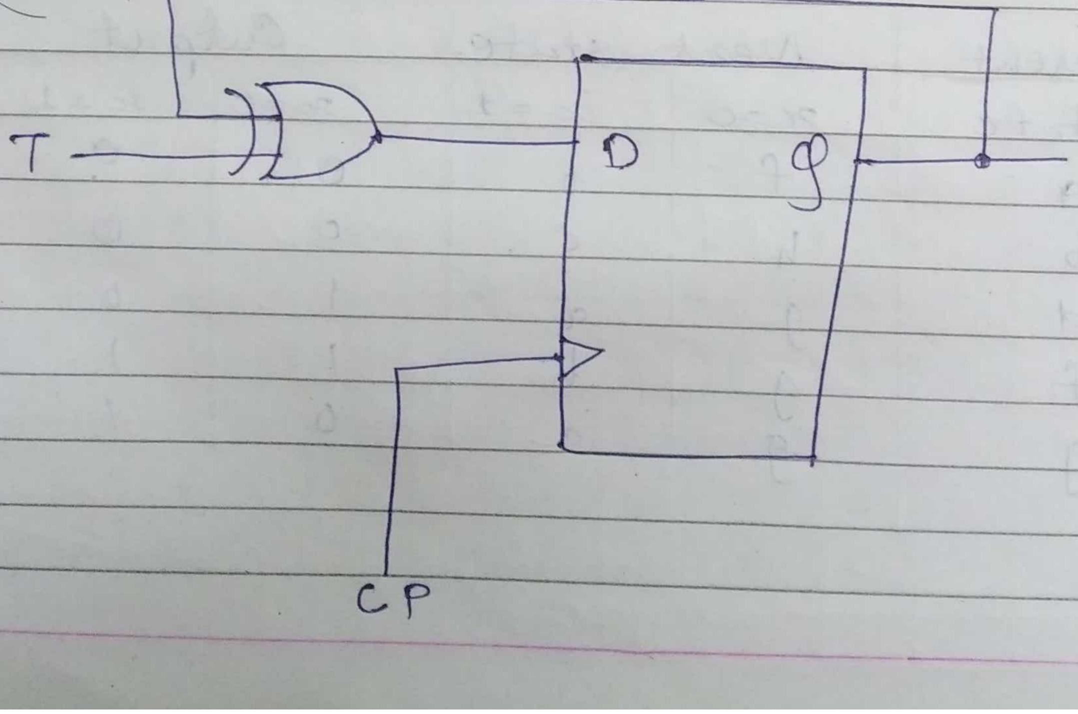
Present State	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	h	c	0	0
d	g	a	1	0
f	g	h	1	1
g	g	a	0	1

20DCS103

→ State diagram :-



8. Analyze the circuit shown below and prove that it is equivalent to a T-flip flop



→ From the circuit, we can write that,

$D = T \oplus Q$

D	Q_{n+1}
0	0
1	1

Suppose, initially Q_n is set to 0 and $T = 0$.

$$\therefore D = Q \oplus T$$
$$= 0 \oplus 0$$
$$= 0$$

Thus, $Q_{n+1} = 0$
$= Q_n$.

Suppose $Q_n = 0$ and $T = 1$.

$$\therefore D = Q \oplus T$$
$$= 0 \oplus 1$$
$$= 1$$

Thus, $Q_{n+1} = \overline{Q_n}$

when $T = 0$, $Q_{n+1} = Q_n$
and $T = 1$, $Q_{n+1} = \overline{Q_n}$

$\therefore$

T	Q_{n+1}
0	Q_n.
1	$\overline{Q_n}$

, $Q_{n+1} = T \oplus Q_n$

Hence, it proved as T- flip flop.

20DCS103

9. Design a sequential circuit with two JK flip-flops A and B and two inputs E and X. If E = 0, the circuits remain in the same state regardless of input X. When E = 1 and X = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00 and repeats. When E = 1 & X = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and repeats.

→ When E = 0, Next state = Present state

when E = 1 & X = 1

Transtitions : 00 → 01
01 → 10
10 → 11
11 → 00.

when E = 1 & X = 0.

Transtitions : 00 → 11
11 → 10
10 → 01
01 → 00.

Present state		Inputs		Next state		FF Inputs			
A	B	E	X	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	0	0	X	0	X
0	0	1	0	1	1	1	X	1	X
0	0	1	1	0	1	0	X	1	X
0	1	0	0	0	1	0	X	X	0
0	1	0	1	0	1	0	X	X	0
0	1	1	0	0	0	0	X	X	1
0	1	1	1	1	0	1	X	X	1
1	0	0	0	1	0	X	0	0	X
1	0	0	1	1	0	X	0	0	X
1	0	1	0	0	1	X	1	1	X
1	0	1	1	1	1	X	0	1	X
1	1	0	0	1	1	X	0	X	0
1	1	0	1	1	1	X	0	X	0
1	1	1	0	1	0	X	0	X	1
1	1	1	1	0	0	X	1	X	1

→ K-map for J_A :

AB \ EX	00	01	11	10
00	0	0	0	1
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

$$J_A = BEX + B'EX'$$

$\therefore J_A = E\ (Bx + B'x')$

$= E\ (B \odot x)$

→ K-map for K_A :

AB \ EX	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	1

$\therefore K_A = E\ (B \odot x)$

→ K-map for J_B :

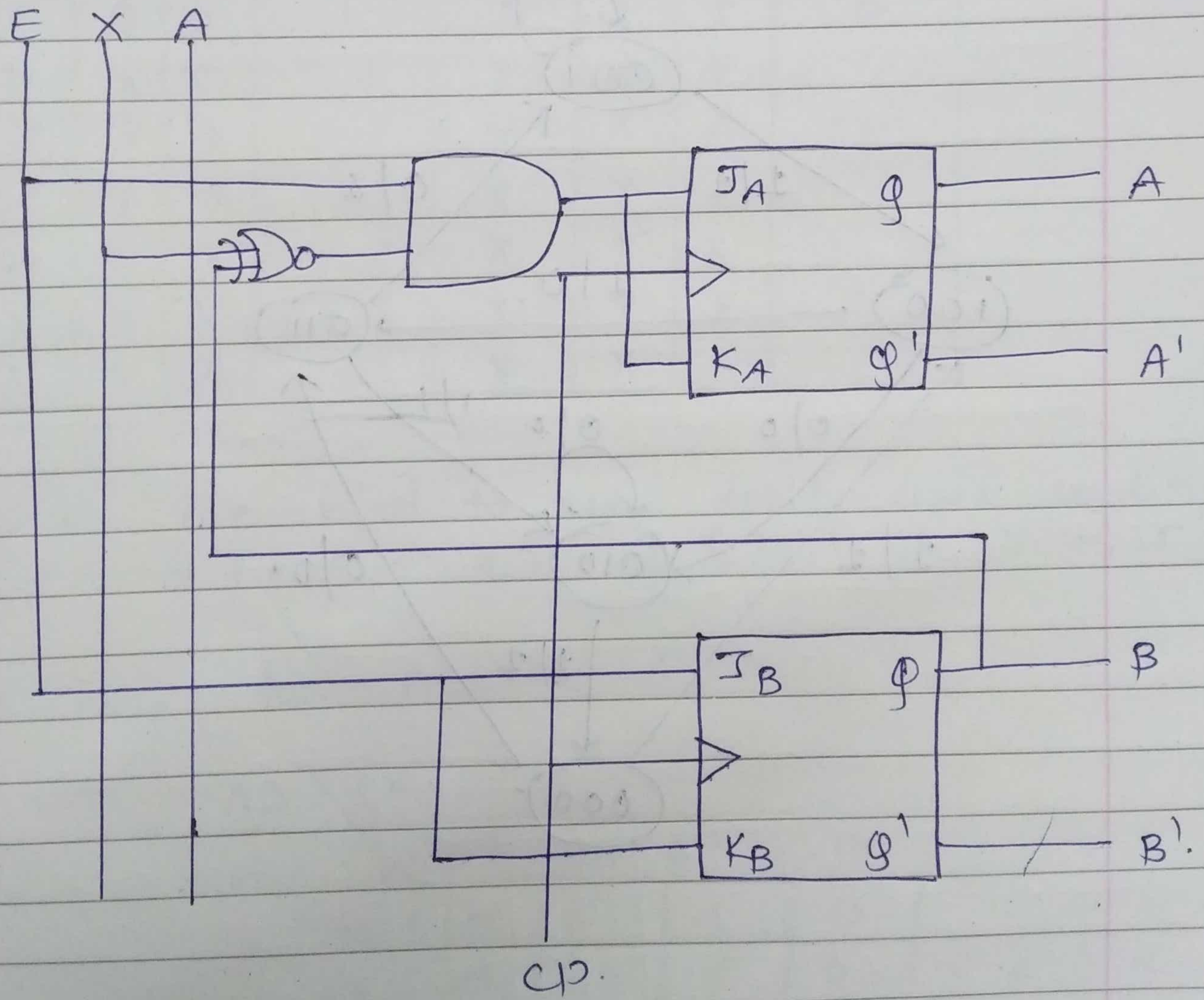
AB \ EX	00	01	11	10
00	0	0	1	1
01	X	X	X	X
11	X	X	X	X
10	0	0	1	1

$\therefore J_B = E$

→ K-map fo K_B :

AB \ EX	00	01	11	10
00	X	X	X	X
01	0	0	1	1
11	0	0	1	1
10	X	X	X	X

$\therefore K_B = E.$

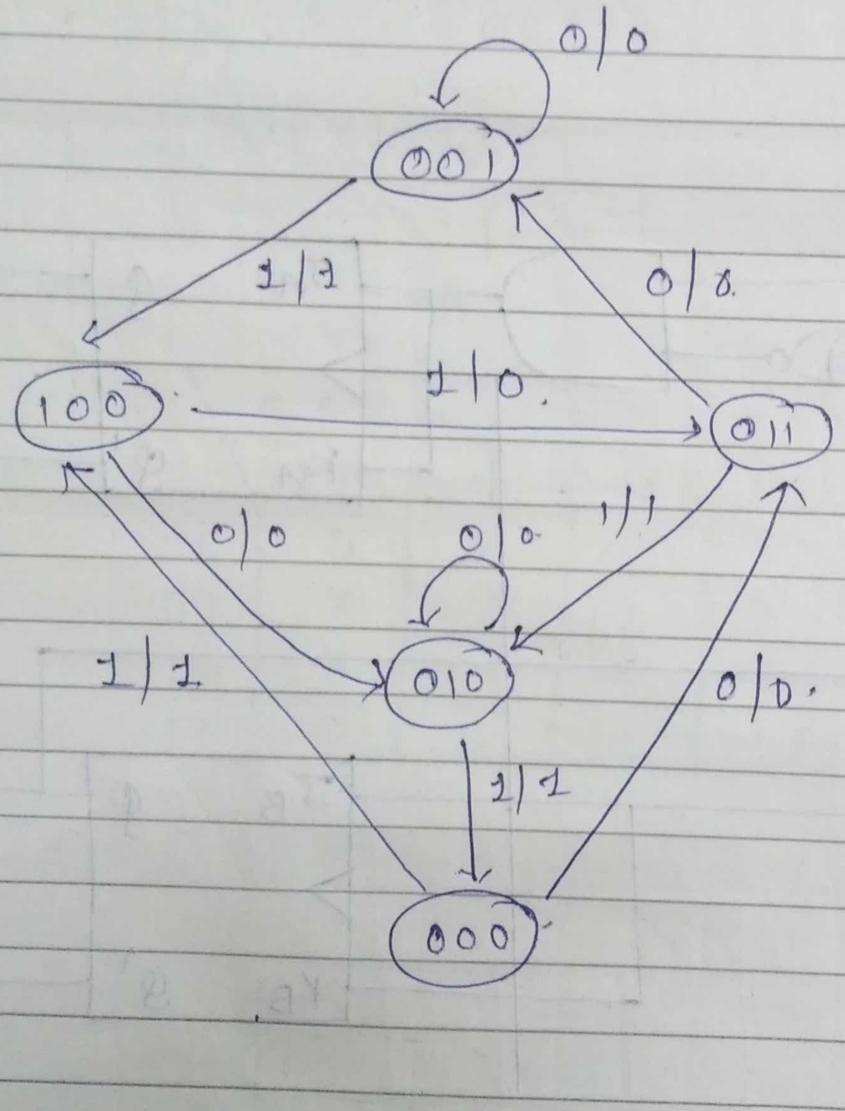


20DCS103

10. A sequencial circuit has three flip-flops A, B and C. One input X and one Output Y. The state diagram is as shown below.

a). Design the sequential circuit using D flip-flops.
b) Design the sequential circuit using JK-flip-flops.

Consider unused state as don't c



20DCS103

Present State			Input	Next State			Output
A	B	C	X	A(t+1)	B(t+1)	C(t+1)	Y
0	0	0	0	0	1	1	0
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	1
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	1	0	1
1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	0
X	X	X		X	X	X	
X	X	X		X	X	X	
X	X	X		X	X	X	
X	X	X		X	X	X	
X	X	X		X	X	X	
X	X	X		X	X	X	

→ Now, we need to use don't care condition
i.e. $d(A, B, C, x) = \Sigma(10, 11, 12, 13, 14, 15)$.

→ K-map for A(t+1) :

AB \ CX	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	X	x	X	X
10	0	0	X	X

$= A'B'X = DA$

20DCS103

→ K-map for B(t+1) :

AB \ CX	00	01	11	10
00	1	0	0	0
01	1	0	1	0
11	X	X	X	X
10	1	1	X	X

$= A + C'X' + BCX$

$= DB.$

→ K-map for C(t+1) :

AB \ CX	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	X	X	X	X
10	0	1	X	X

$= AX + CX' + A'B'X'$

$= DC.$

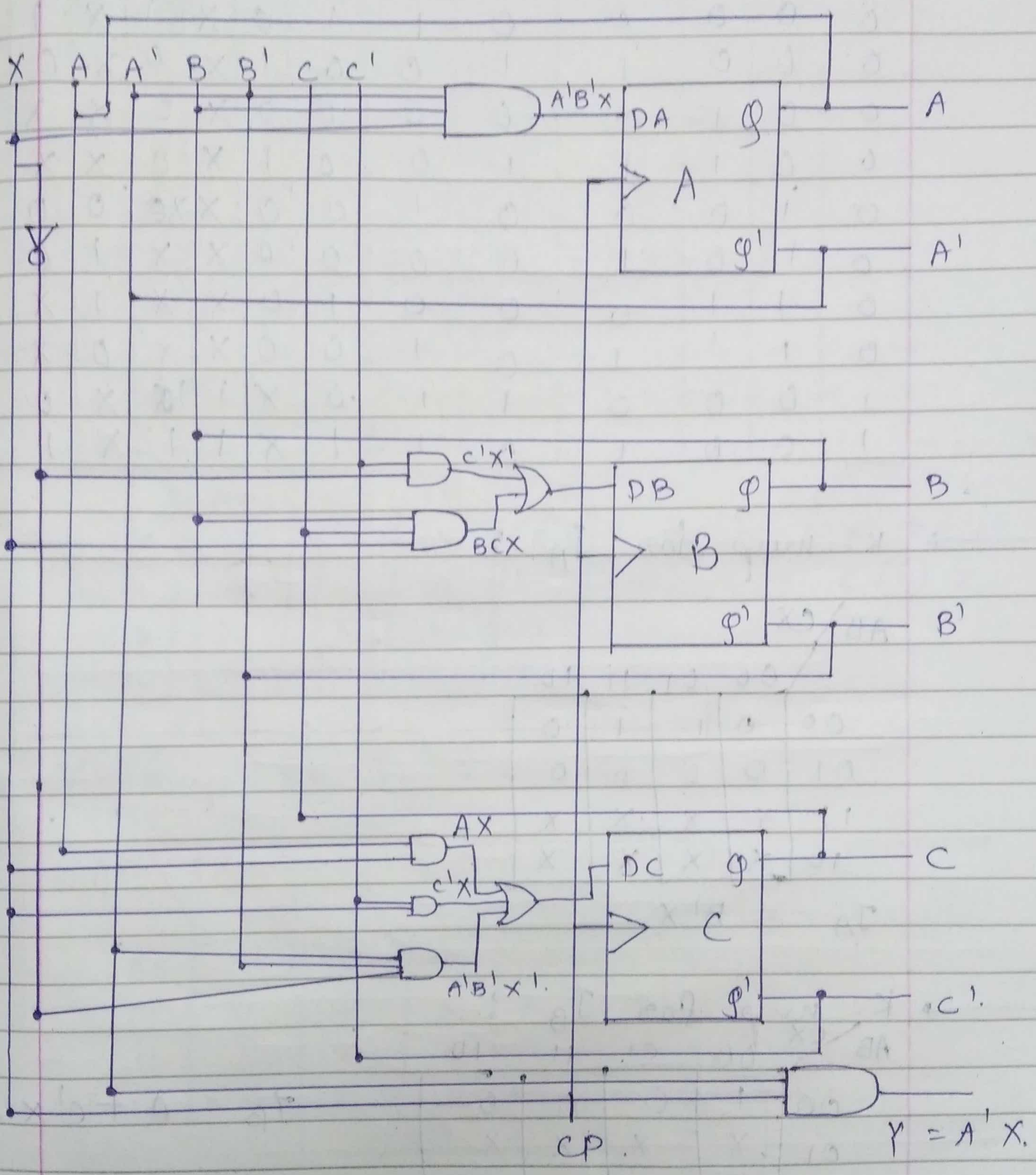
→ K-map for Y :

AB \ CX	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	X	X	X	X
10	0	0	X	X

$= A'x = DD!$

20DCS103

- Sequential circuit using D-flip-flop :-



Present state			Input	Next state			FF. Input					
A	B	C	X	A(t+1)	B(t+1)	C(t+1)	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	1	0	X	1	X	1	X
0	0	0	1	1	0	0	1	X	0	X	0	X
0	0	1	0	0	0	1	0	X	0	X	X	0
0	0	1	1	1	0	0	1	X	0	X	X	1
0	1	0	0	0	1	0	0	X	X	0	0	X
0	1	0	1	0	0	0	0	X	X	1	0	X
0	1	1	0	0	0	1	0	X	X	1	X	0
0	1	1	1	0	1	0	0	X	X	0	X	1
1	0	0	0	1	1	0	X	1	1	X	0	X
1	0	0	1	0	1	1	X	1	1	X	1	X

→ K-map for J_A :

AB \ CX	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	X	X	X	X
10	X	X	X	X

$J_A = B'X$

→ K-map for J_B :

AB \ CX	00	01	11	10
00	1	0	0	0
01	X	X	X	X
11	X	X	X	X
10	1	1	X	X

$J_B = A + C'X'$

20DCS103

→ K-map for K_A :

AB \ CX	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	1	1	X	X

$K_A = 1$

→ K-map for K_B :

AB \ CX	00	01	11	10
00	X	X	X	X
01	0	1	0	1
11	X	X	X	X
10	X	X	X	X

$K_B = C'X + CX'$
$= C \oplus X$

→ K-map for J_C :

AB \ CX	00	01	11	10
00	1	0	X	X
01	0	0	X	X
11	X	X	X	X
10	0	1	X	X

$J_C = AX + A'B'X$

20DCS103

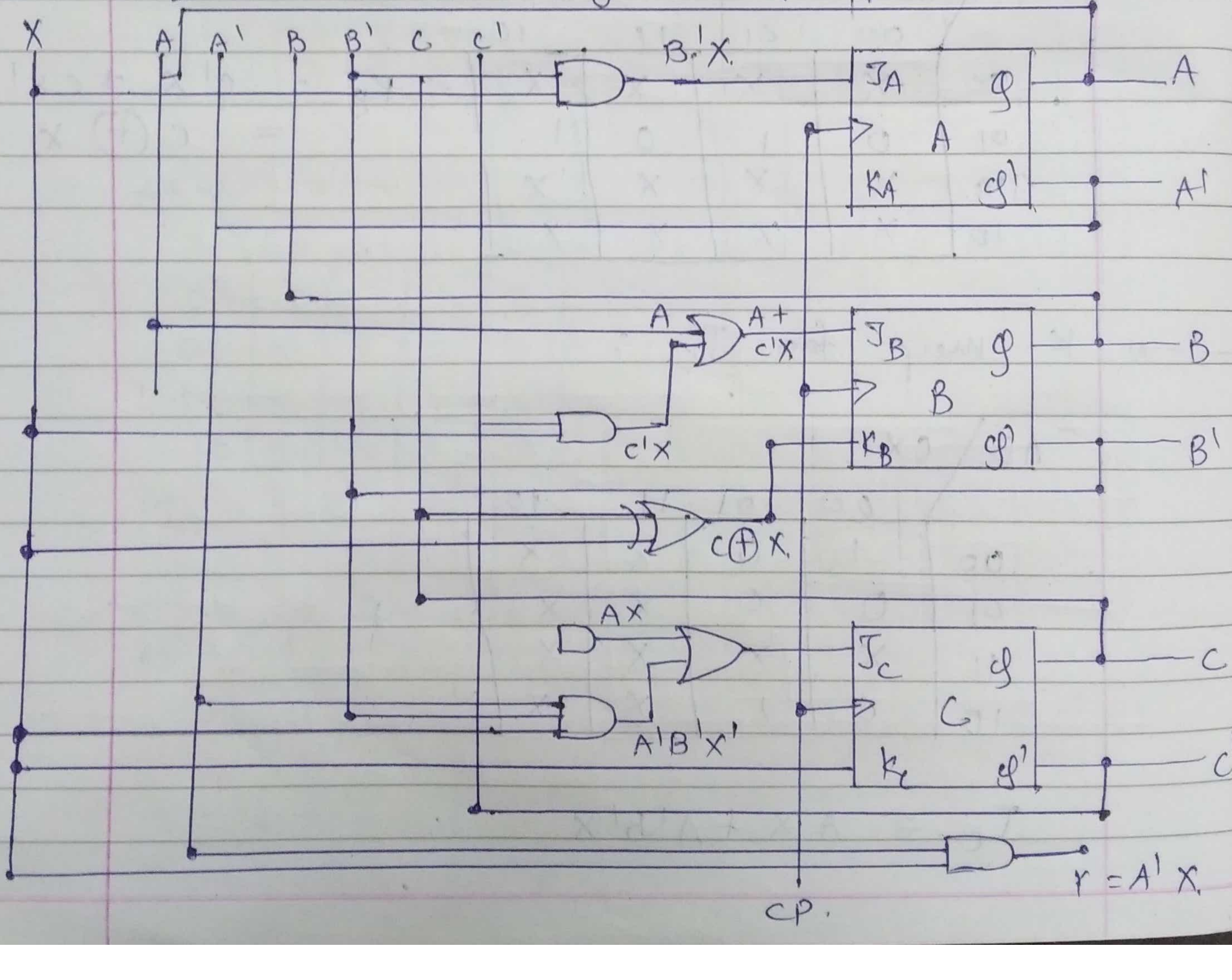
→ K-map for K_C :

AB \ CX	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	X	X
10	X	X	X	X

$K_C = X$.

$Y = A'X$.

→ Sequential circuit using JK flipflop :-



20DCS103

11. Design 4-bit binary counter using JK flip flop.

→ Number of digits = N = 4.
Number of FF CN = 2.

Present state				Next state				FF Inputs							
A	B	C	D	A (t+1)	B (t+1)	C (t+1)	D (t+1)	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1
1	0	1	0	0	0	0	0	X	1	0	X	X	1	0	X
1	0	1	1	0	0	0	0	X	1	0	X	X	1	X	1
1	1	0	0	0	0	0	0	X	1	X	1	0	X	0	X
1	1	0	1	0	0	0	0	X	1	X	1	0	X	X	1
1	1	1	0	0	0	0	0	X	1	X	1	X	1	0	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

→ K map for J_A :

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

$J_A = BCD$

20DCS103

→ K map for K_A :

AB \ CD	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	1	1	1
10	0	1	1	1

$K_A = B + D + C$

→ K map for J_B and for K_B

AB \ CD	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	0	0

AB \ CD	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	1	1	1	1
10	1	X	X	0

$J_B = \bar{A}CD$.

$K_B = CD + A$.

→ K map for J_C and for K_C.

AB \ CD	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	0	0	X	X
10	0	0	X	X

AB \ CD	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	1	1
10	X	X	1	1

$J_C = \bar{A}D$

$K_C = D + A$.

20DCS103

→ K-map for J_D and for K_D

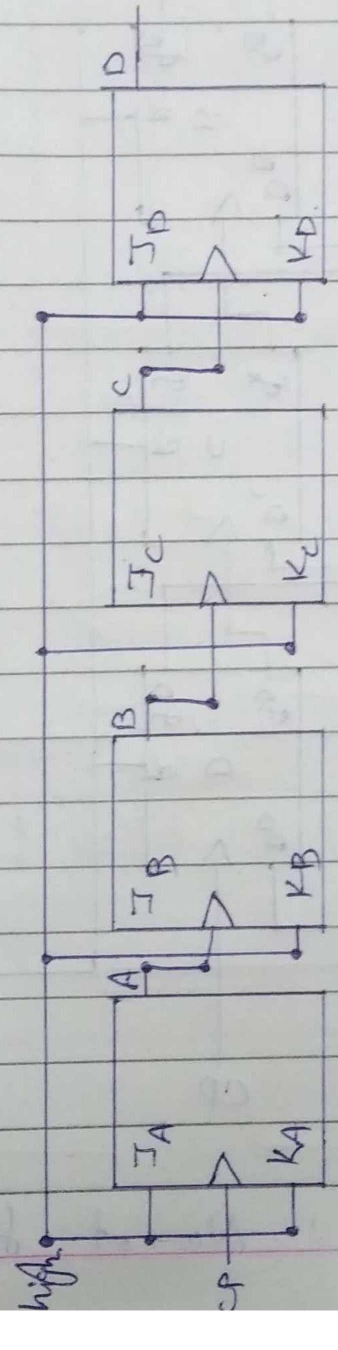
AB \ CD	00	01	11	10
00	1	X	X	1
01	1	X	1	1
11	0	X	X	0
10	1	X	X	0

AB \ CD	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	1
10	X	1	1	1

$J_D = \bar{A} + \bar{B}\bar{C}$

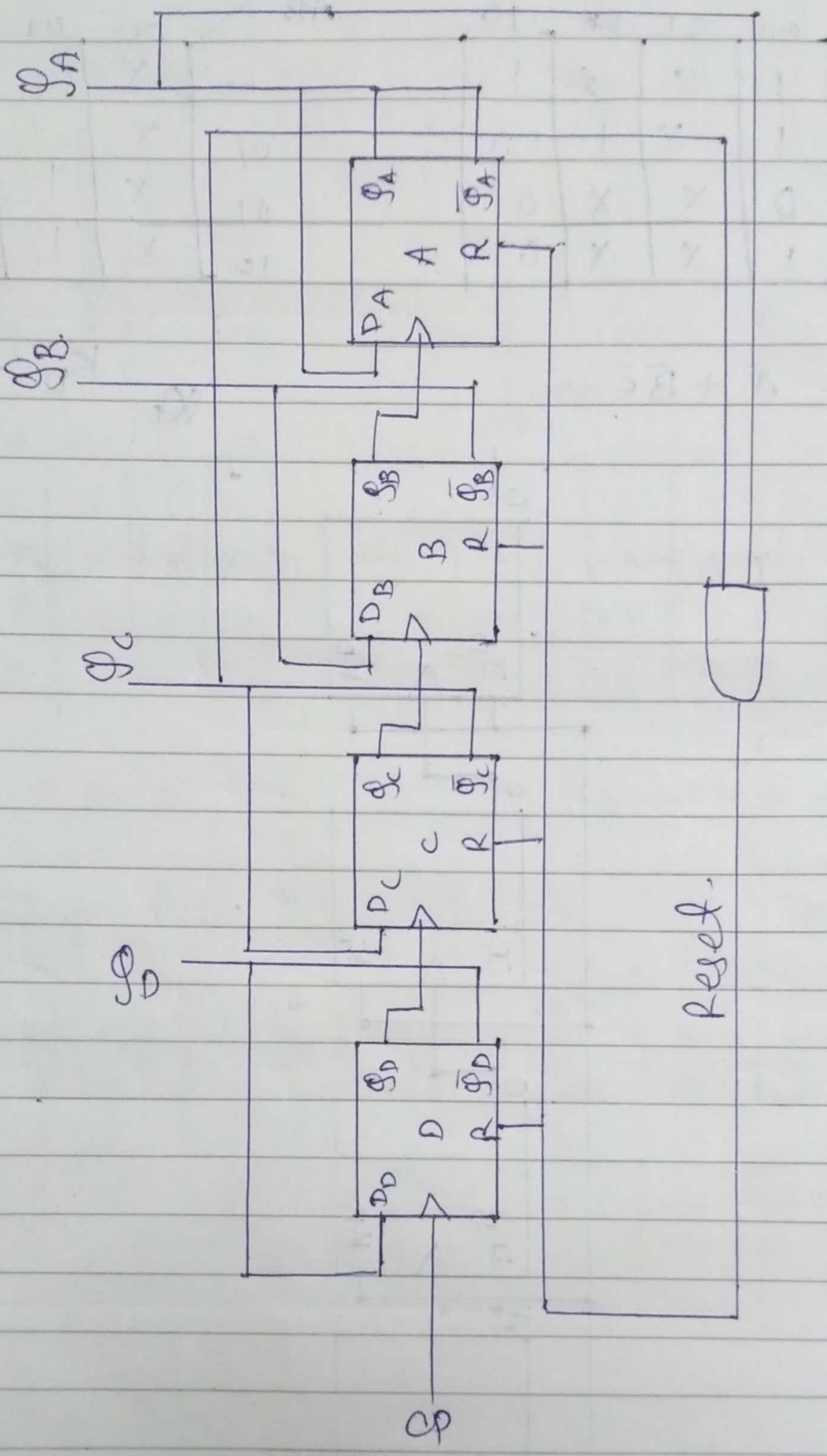
$K_D = 1$.

→



20DCS103

12. Design BCD counter using D-flip-flop.



→ $2^n \geq N = 10$

$2^4 \geq 16 > 10$. ∴ No of flip-flop = 4.

20DCS103

13. Design mod-4 counter using T- flip-flop.

→ Number of flip-flops $= 2^n$
$= 2^1 = 2$.

$N = 0$ (for up) , $N = 1$ (for Sum).

Present state		Next state		FF Outputs	
A	B	A(t+1)	B(t+1)	T_A	T_B
0	0	0	1	0	1
0	1	1	0	1	1
0	1	0	0	0	1
0	0	1	1	1	1
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	0	0	1
1	0	0	1	1	1

→ K-map for T_A :

M \ AB	00	01	11	10
0	0	1	1	0
1	0	1	1	0

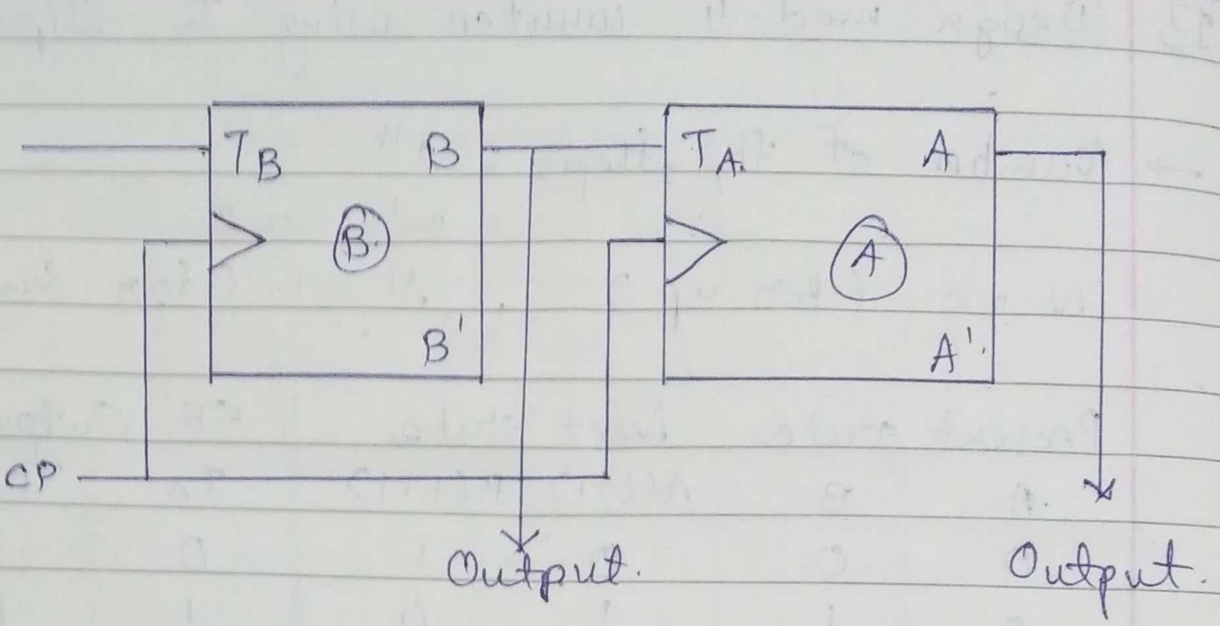
$T_A = B$

→ K-map for T_B :

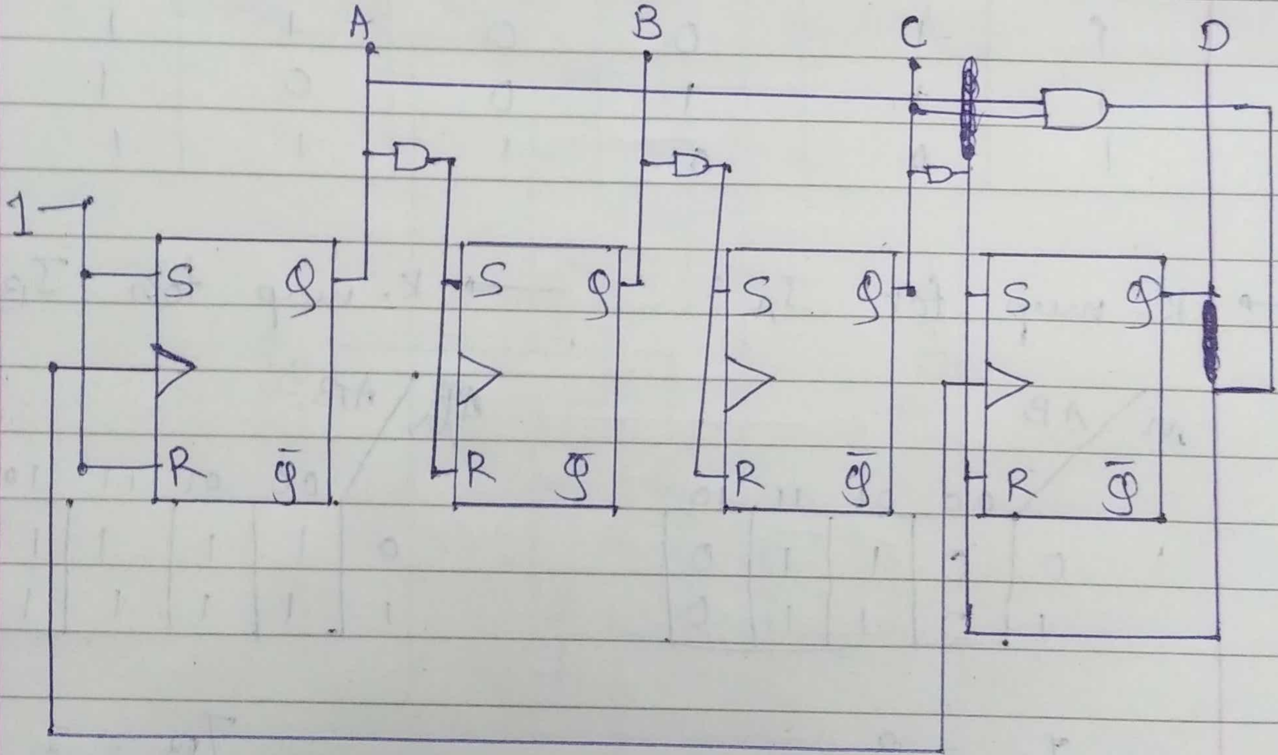
M \ AB	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$T_B = 1$.

20DCS103



14. Design decimal counter using SR flip-flop.



——— X ———