

Machine Dependent Optimisation and Cache Architectures

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Where we are...

- Admin and overview
- Lexical analysis
- Parsing
- Semantic analysis
- Machine-independent optimisation

- Code generation
- Hardware architectures
- Machine-dependent optimisation
- Review



Objectives

- Discuss further compiler optimisations
 - Instruction percolation
 - Loop unrolling
 - Loop fusion
 - etc
- Discuss ways compilers can optimise cache usage



Pipelining and Parallelisation

- Last week we looked at pipelining and parallelisation for different CPU architectures
- Some architectures use dynamic scheduling, others use static
- For static scheduling, code optimisation is essential
- For dynamic scheduling, code optimisation can facilitate further optimisation



Instruction Scheduling

- We would like to reorder the instructions in a way which
 - preserves the dependencies between those instructions (and hence the correctness of the program), and
 - achieves the minimum possible number of pipeline stalls
 - instruction Percolation
- We've seen an example last week



Loop manipulation for Parallelism

- Two common techniques for taking advantage of parallelism
 - Loop unrolling
 - Loop fusion



Loop Unrolling

- Make data independencies explicit through rewriting loop to do more work in each iteration
- Basic principle:

This particular change is useful if we have *four* degrees of parallelism.



Loop Fusion

- Turn two (or more) loops into one
- Basic idea:

This particular change is useful if we have *two* degrees of parallelism.



Branching Decisions

- If we have a choice, can speculatively execute *both* outcomes (assuming they are independent)
- Basic idea:
- Execute

This gives two degrees of parallelism; more can be achieved by discovering opportunities within do a and do b.

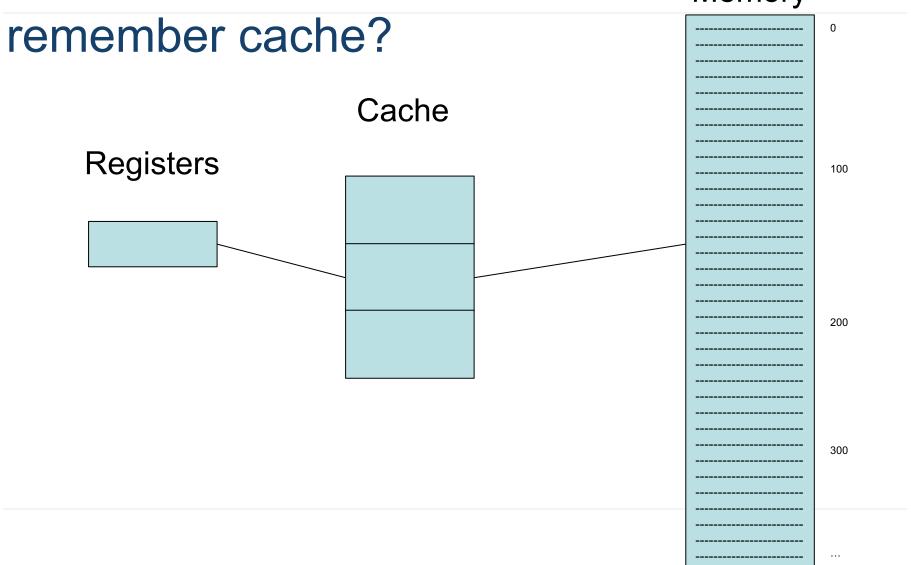


Cache Optimisation

- Try to increase the chances that the needed memory locations are already in cache
- Reorder data accesses to improve data locality
- Cache is divided into cache lines
 - When memory is read into cache, a whole cache line is always read at the same time
 - Good if we have data locality: nearby memory accesses will be fast
 - Typical cache line size: 64-128 bytes (compiler needs to know exactly if it is going to optimise)

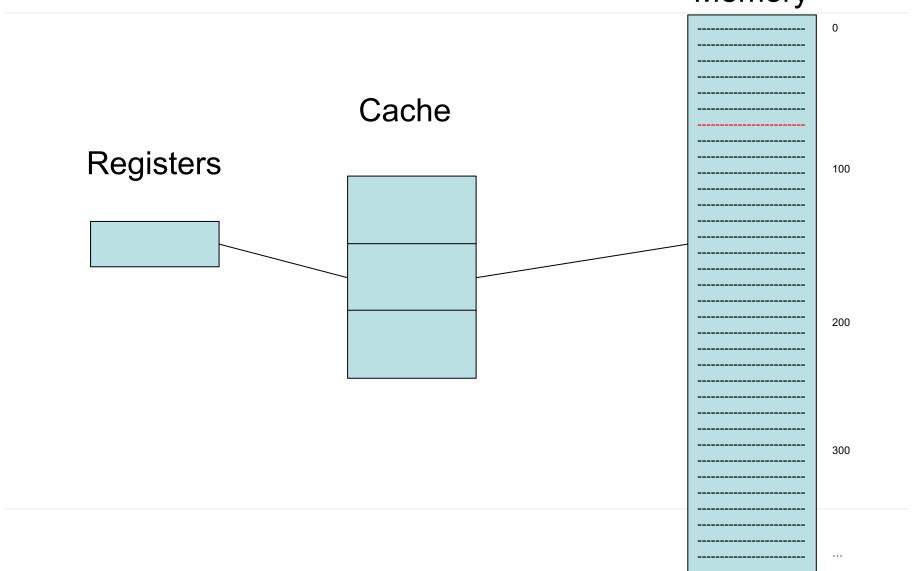
Main Memory





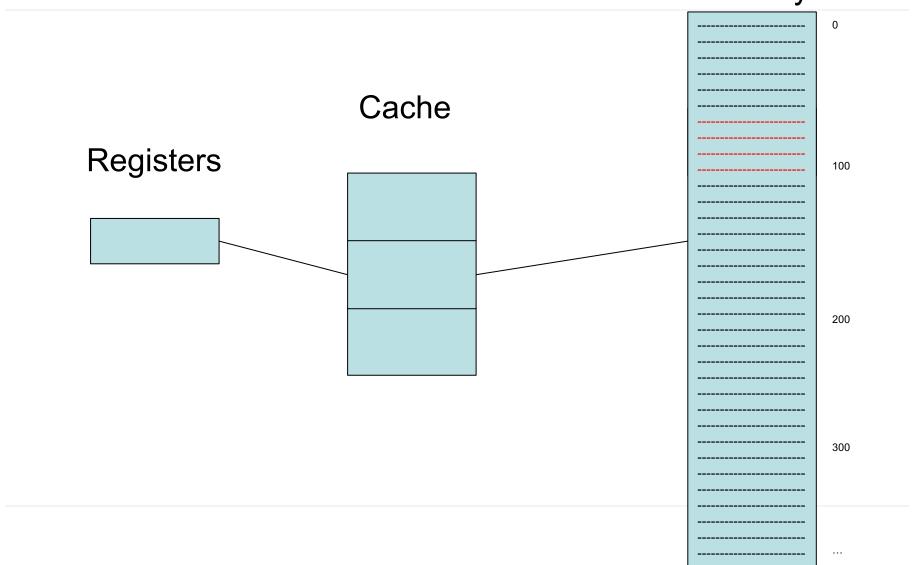
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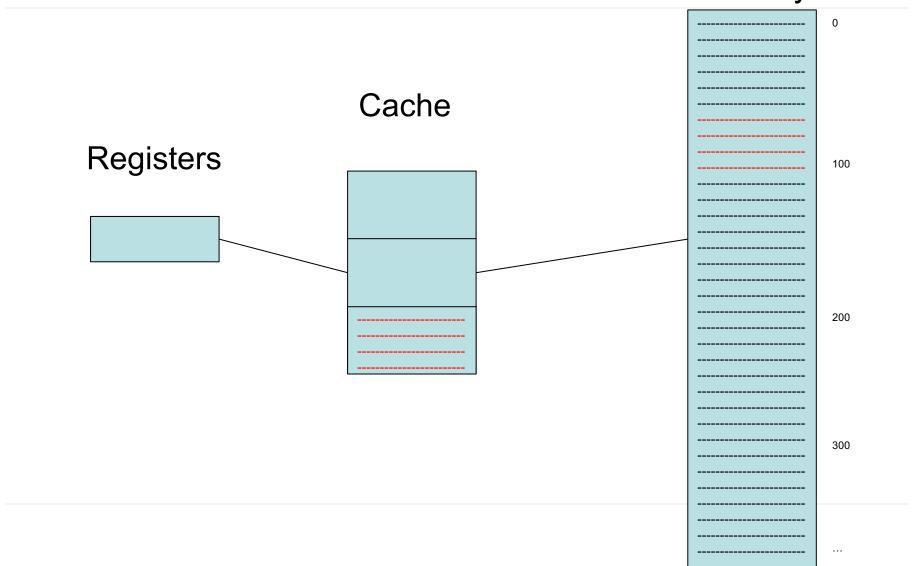
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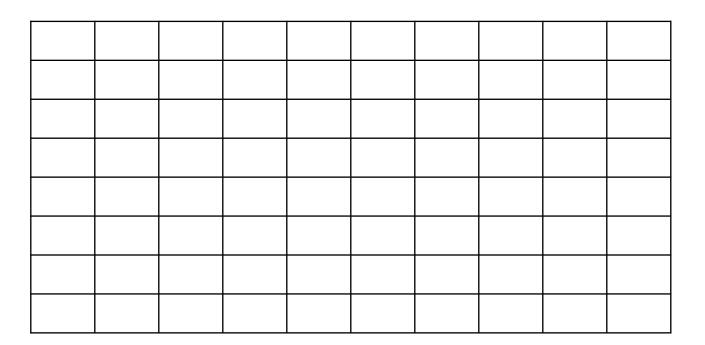




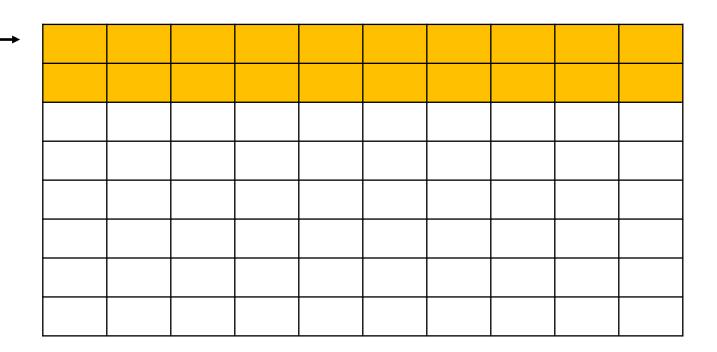


Blocking or Tiling

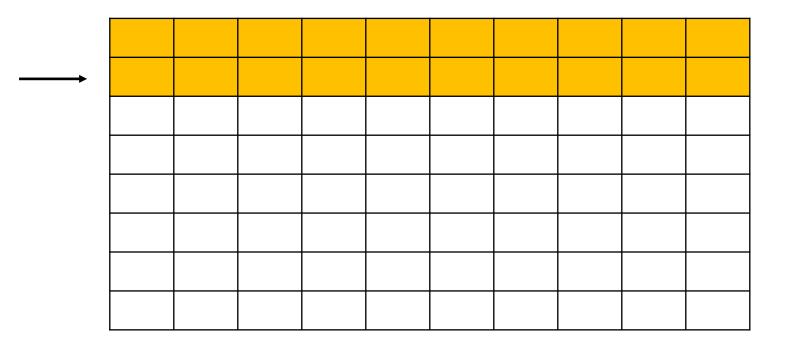




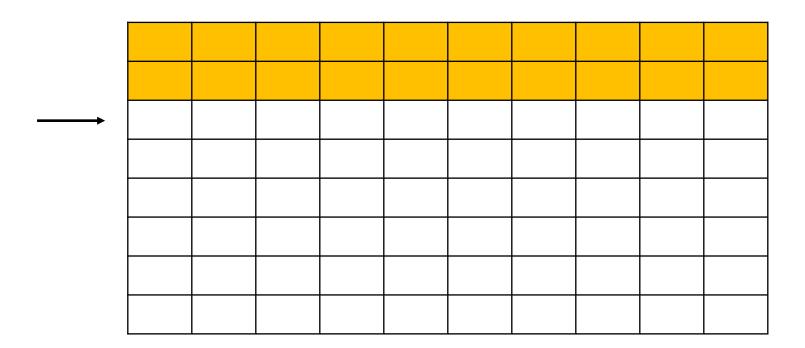




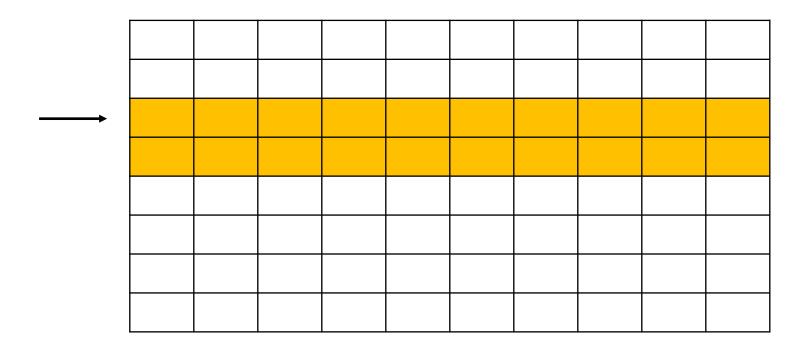




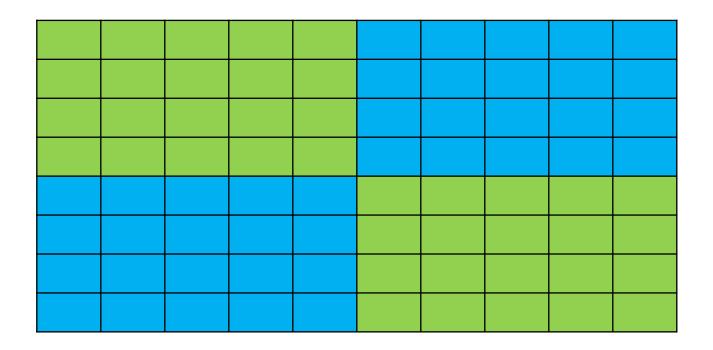














Summary

- Techniques to take advantage of some machinedependent features for optimisation
 - Optimisation for pipelining
 - Instruction percolation
 - Loop unrolling
 - Loop fusion
 - Optimisation for cache
 - Blocking



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