



ST. XAVIER'S COLLEGE
KOLKATA
(AUTONOMOUS)

3rd SEMESTER EXAMINATION
DECEMBER 2021
M. Sc. COMPUTER SCIENCE

CMSM4323

VLSI DESIGN

Monday, December 13, 2021

12:00 NOON to 3:00 PM

3 hours

Full Marks : 80

PLEASE READ THESE INSTRUCTIONS BEFORE YOU START WRITING:

1. Of the questions attempted, the answers to only the first required number of questions (as stipulated in the question paper) will be evaluated. **So please do not attempt extra questions.**
2. Use fountain pen or ball-point pen of **blue or black ink.**
3. Write (**not type**) the answers legibly, in your own words as far as practicable, on A4 size sheets.
4. Save the pages of your answer sheets (hand-written document) to a single PDF file and name the document accurately i.e. **Roll No_Paper Code.PDF** (example: 147_PH36141T).
5. Send the PDF file to the following email address (**in REPLY mode**) **within 30 minutes of the completion of the examination:** [**CMSM43232122@SXCCAL.EDU**](mailto:CMSM43232122@SXCCAL.EDU)
6. The scanned answer scripts should have **enough clarity** to enable evaluation.
7. On top of each page **handwrite** the following information: **Name, Roll Number, Paper Code , Date, and Page Number**
8. No multiple submissions would be allowed.

The marks are given in **brackets []** at the end of each question or part question.

The question paper consists of **2** pages.

Of the questions attempted, the answers to only the first required number of questions (as stipulated in the question paper) will be evaluated.
So, PLEASE DO NOT ATTEMPT EXTRA QUESTIONS.

Answer **QUESTION 1** and **ANY FOUR** from the rest.

1. Answer **ANY FOUR** **[4×5=20]**
 - a) Explain the reasons for the increasing use of VLSI circuits.
 - b) What are different chip design styles available? Compare any two.
 - c) Explain the term Doglegging with an example.
 - d) Explain the procedure of Lithography.
 - e) Write down the working principle of pMOS.
 - f) Write a short note on the following terms: Ad-hoc testing, Built-in-self-test

2.
 - a) Differentiate between Detailed and Global routing. **[5]**
 - b) Write a Line-Probe algorithm for global routing. State the advantages and disadvantages of this algorithm. **[6+4]**

3.
 - a) What do you mean by Corner Stitching data structure used for IC layout editing? Write an algorithm using corner stitching to find a point. **[2+6]**
 - b) Discuss the factors considered for the floorplanning and pin assignment. **[7]**

4. Explain the following terms:
 - i) Slicing Floor-plan and slicing tree with an example,
 - ii) Net and Netlist,
 - iii) Capacity of a channel,
 - iv) rat's nest **[(3+3)+3+3+3]**

5.
 - a) State any group migration algorithm used for circuit partitioning. Discuss in detail. **[5+5]**
 - b) Sketch a schematic of the given function $[(AB)+(CD)]'$ using CMOS. Give explanation. **[5]**

6.
 - a) What is the concept of partitioning? Write down the parameters that are present for increasing the efficiency of partitioning. **[3+4]**
 - b) Discuss the factors considered for the floorplanning and pin assignment. **[8]**

7.
 - a) State the Net-Ordering algorithm for detailed routing. **[5]**
 - b) Write the VHDL implementation of XNOR gate. Comment on each statement. **[10]**
