TASK-1 Answers to Understanding Questions

Q1: Where is the RISC-V program located in the vsd-riscv2 repository?

A: In the Samples directory.

Q2: How is the program compiled and loaded into memory?

A: The program is complied using the RISC-V GNU tool chain linked with a BRAM specific linker script, converted into a HEX file and loaded into on-chip BRAM from which the RISC-V core fetches and executes instructions.

Q3: How does the RISC-V core access memory and memory-mapped IO?

A: The RISC-V core uses load and store instructions to access both memory and IO. Address decoding in the SoC decides whether the access goes to RAM or to a memory-mapped peripheral.

Q4: Where would a new FPGA IP block logically integrate in this system?

A: A new FPGA IP block would be integrated at the SoC level as a memory-mapped peripheral, connected to the RISC-V core via the load/store interface and accessed through address decoding.

Confirmation of environment used:

GitHub Codespace only