INTERNSHIP REPORT

ON

Designing a 32-bit ADC Board

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ABSTRACT

This report presents the design and development of a high-precision data acquisition system using the ADS1263 32-bit ADC integrated with a NCP1117ST33T3G 3.3V LDO regulator. The system is engineered to address the growing need for ultra-low-noise, high-accuracy analog measurement in modern embedded, industrial, and scientific applications. The ADS1263, with its delta-sigma conversion architecture, extremely low RMS noise, programmable gain amplifier (PGA), and multi-channel capability, enables micro-volt level signal detection with exceptional stability and linearity.

• The system incorporates a carefully designed analog front end, filtered power supply, and SPI-based digital communication interface. The NCP1117 regulator provides a clean and stable 3.3V supply to the ADC, minimizing ripples, voltage fluctuations, and power noise that typically degrade measurement accuracy. Together, these components form a reliable platform for capturing precise electrical parameters and sensor outputs. Detailed discussions of circuit architecture, signal conditioning techniques, PCB layout considerations, power regulation strategies, and communication protocols are included to ensure complete understanding of the system's operation.

• By combining theoretical concepts with practical implementation, this work demonstrates a highly scalable, accurate, and cost-effective solution for precision measurement. It highlights the potential of 32-bit ADC technology in applications such as sensor instrumentation, biomedical devices, industrial automation, metrology equipment, and research laboratories. The project contributes to the advancement of high-resolution data acquisition systems and enables reliable monitoring of low-level analog parameters in real-time environments.

1. INTRODUCTION

BACKGROUND

- The demand for high-precision data acquisition has increased significantly across fields such as industrial automation, biomedical instrumentation, metrology, and environmental monitoring. Modern applications often require measurement of extremely small analog signals—sometimes in the microvolt or nanovolt range—with high accuracy, low noise, and long-term stability. Traditional ADCs used in microcontroller-based systems typically offer resolutions of 10- to 16-bit, which are insufficient for capturing such fine variations, especially in the presence of electrical noise or unstable power supplies.

- To overcome these limitations, high-resolution delta-sigma ADCs like the **ADS1263** have become essential in precision measurement systems. The ADS1263, a 32-bit ultra-low-noise ADC from Texas Instruments, provides exceptional accuracy with features such as a programmable gain amplifier (PGA), internal reference, low input bias current, and integrated calibration functions. These characteristics make it highly suitable for applications involving load cells, RTDs, strain gauges, ECG/EEG electrodes, and other sensors producing low-amplitude analog signals.

- However, for any high-resolution ADC to perform optimally, the stability and cleanliness of the power supply are critical. Even small fluctuations or ripple in the supply line can introduce noise that degrades ADC accuracy. To address this, the **NCP1117ST33T3G**, a low-dropout (LDO) voltage regulator, is used to provide a stable, noise-filtered **3.3V supply** to the ADC and associated analog circuitry. Its low dropout voltage, thermal protection, and low ripple output ensure reliable performance even under fluctuating input conditions.

- This project focuses on designing, developing, and validating a **32-bit precision ADC converter board** that brings together the capabilities of the ADS1263 and the stability of the NCP1117. Through careful hardware design, analog filtering, power regulation, and PCB layout practices, the system aims to achieve a high-fidelity data acquisition platform suitable for advanced engineering and industrial tasks.

OBJECTIVES

The primary objectives of this project are:

- **To design and implement a 32-bit high-precision ADC board** using ADS1263 for capturing extremely low-level analog signals.

- **To provide a highly stable and low-noise 3.3V power supply** using the NCP1117ST33T3G LDO regulator.

- **To develop a robust analog front-end** with appropriate filtering, protection, and grounding techniques for accurate signal conditioning.

- **To validate the system** through measurements, calibration, and noise performance analysis, ensuring that the board meets precision standards.

- **To create a scalable architecture** suitable for future expansion, multi-sensor integration, and advanced instrumentation applications.

SCOPE

This report covers a comprehensive analysis of high-precision ADC design involving power, hardware, and signal integrity aspects. The scope includes:

- **Research and Component Study**
- Understanding delta-sigma ADC principles and noise considerations.
- Reviewing ADS1263 datasheet, features, and operating modes.
- Studying LDO regulator characteristics and their role in precision systems.
- **Design and Simulation**
- Power regulation design using NCP1117, including capacitor selection.
- Analog input filtering, reference voltage stability, and grounding.
- Simulation of signal conditioning and SPI communication.
- **Hardware Development**
- Designing the full converter board schematic.
- PCB layout emphasizing low noise, short trace lengths, and analog/digital isolation.
- Integrating analog and digital subsystems with proper shielding.
- **Testing and Validation**
- Measuring noise performance, linearity, stability, and resolution.
- Validating SPI communication and data accuracy.
- **Real-World Applications**
- Exploring industrial, scientific, and sensor-based use cases.
- Scalability options for multi-channel measurement systems.

2. PROBLEM STATEMENTS

NEED FOR HIGH-PRECISION ANALOG-TO-DIGITAL CONVERSION

Today's embedded systems, scientific instruments, industrial control units, and sensor-based platforms require the ability to measure extremely small analog signals with high resolution and very low noise. Traditional ADCs (10-bit, 12-bit, or even 16-bit) are insufficient for detecting micro-volt or nano-volt level variations due to limitations in resolution, sampling accuracy, power noise interference, and input stability.

Applications such as biomedical instrumentation, strain gauge/load cell measurement, seismic sensing, vibration monitoring, and precision laboratory experiments demand an ADC system capable of providing:

- **Ultra-high resolution (up to 32-bit)**
- **Low input noise and high linearity**
- **Stable and low-noise power supply**
- **Reliable digital interface for microcontrollers**

However, most commercially available ADC modules introduce noise from the power supply, lack proper analog front-end conditioning, and do not maintain accuracy under fluctuating environmental or electrical conditions.

DATA PROCESSING AND OUTPUT SYSTEM

- **SIGNAL ACQUISITION**
- The system collects analog inputs from sensors or test sources connected to the ADS1263's differential or single-ended channels.
  The ADS1263 includes:
- Integrated **PGA** for signal amplification
- Digital filters for noise reduction
- High-resolution delta-sigma conversion
- Each input is routed through:
- **Input Protection Circuit**
- **Low-pass RC Filter**
- **PGA Stage (inside ADS1263)**
- This ensures that only clean, conditioned signals enter the ADC.

3. RESEARCH AND LITERATURE REVIEW

PRECISION ADC DESIGN AND HIGH-RESOLUTION MEASUREMENT

• High-performance data acquisition systems rely heavily on precision ADCs capable of detecting micro-volt level signals with minimal noise. Research in instrumentation highlights that **delta-sigma ADCs**, such as the ADS1263, provide superior resolution, linearity, and noise immunity compared to SAR or flash ADCs.

• The ADS1263 offers **32-bit resolution**, extremely low input-referred noise (as low as 5–10 nV), integrated PGA, internal reference, and built-in calibration. Literature confirms that such ADCs are essential for applications like biomedical instrumentation, load-cell measurement, geophysical sensors, and scientific experiments requiring noise-free conversion.

LOW-DROPOUT REGULATORS AND POWER INTEGRITY

• High-resolution ADCs demand a **stable, low-noise power supply**. Studies show that fluctuations in supply voltage directly increase conversion noise. The NCP1117ST33T3G is widely used due to its **low dropout voltage, low output ripple, and fast transient response**.

• Research on power conditioning emphasizes the use of **decoupling capacitors, analog/digital ground separation**, and linear regulators over switching regulators to avoid electromagnetic interference (EMI).

SIGNAL CONDITIONING AND PGA USAGE

• Literature on precision signal acquisition states that analog front-end conditioning—such as **RC low-pass filters, differential measurement, and proper grounding**—is mandatory for reducing external noise.
• The ADS1263's integrated PGA reduces the need for external amplifiers, minimizing design complexity and preserving signal fidelity.

DIGITAL COMMUNICATION AND DATA INTEGRITY

• SPI is the preferred interface for high-resolution ADCs due to its **low latency, simplicity**, and ability to support **high data rates up to several MHz**. Research notes that isolating SPI traces and minimizing their length improves signal integrity.

CHALLENGES IN HIGH-RESOLUTION ADC IMPLEMENTATION

Research identifies several practical challenges:
• **Noise Interference:** High-resolution ADCs can pick up even microvolt noise; PCB layout becomes critical.

• **Ground Loops:** Mixed-signal systems must separate analog and digital ground.

• **Thermal Drift:** ADC accuracy varies with temperature unless compensated.

• **Sensor Impedance:** High source impedance can distort conversion unless buffered.

• **Reference Stability:** Precision measurements require low-drift voltage references.
Studies conclude that accurate 32-bit ADC design is possible only with proper **power isolation, signal conditioning, grounding, and calibration techniques**.

4. METHODOLOGIES

- **COMPONENT SELECTION**
  1. ADS1263 (32-bit ADC)
  Chosen for:
- Extremely high resolution
- Internal PGA for micro-volt signals
- Low RMS noise (as low as 5 nV)
- Multiple differential channels
- Built-in reference and calibration
- Ideal for precise laboratory and industrial sensing.

2. NCP1117ST33T3G (3.3V LDO Regulator)

- Selected because it provides:
- Stable 3.3V output
- Low dropout voltage
- Low noise
- High load regulation
- Essential for the ADC to function without ripple interference.

3. Filtering & Protection Components

- RC low-pass filters
- Decoupling capacitors (0.1µF + 10µF)
- Input protection resistors

4.Bit Calculation

- ADS1263 is a 32-bit Delta-Sigma ADC with theoretical 4.29 billion steps.
- LSB size = Vref / 2^{32} (≈ 0.58 nV for 2.5V reference).
- Effective resolution reduces as data rate increases due to noise.
- Digital output follows: Code = (Vin / Vref) × 2^{31}.

DEVELOPMENT

PCB Layout Design

Special emphasis on:

- Separate AGND and DGND
- Separate layer for the ground plane
- Short, shielded analog traces
- Proper decoupling close to IC pins

5. SYSTEM DESIGNS

This section provides a component-level design with practical values and layout section.

Schematic highlights & component suggestions
Power

- **Input**: 5 V DC.
- **Pre-filter**: RC Low pass filter.
- **LDO**: NCP1117ST33T3G (3.3 V).
- **Capacitors**:
- LDO input: 10 µF + 0.1 µF ceramic.
- LDO output: As per NCP1117 datasheet — 10 recommended and 0.1 µF close to VOUT pin.
- ADS1263 VDD decoupling: 0.1 µF ceramic at each VDD pin, plus 4.7 µF bulk on board.

Input protection:

- Used the Schottky diode as ESD for each analog AIN pins and the power rails.
- **Anti-alias filter**:
- For simple single-pole: R = 1 kΩ, C = 100 nF → fc ≈ 1.6 kHz (adjust to application).

MCU interface

- **SPI**: MOSI, MISO, SCLK, CS; use series resistors (22–100 Ω) on digital lines to damp reflections.
- **DRDY**: attach to MCU interrupt pin for low-latency read.
- **Reset** and **START** lines wired to MCU for full control.
- **Level shifting**: not needed if MCU and ADS1263 share 3.3 V.

Grounding & layout

- **Plane strategy**: continuous ground plane under analog section; keep digital traces on separate area.

Trace routing:

- Keep ADC input traces shortest possible; avoid vias on input traces.
- Place decoupling caps within 1–3 mm of IC pins.

- **Stitching**: multiple vias to ground plane near ADC and reference to reduce loop inductance.
- **Separation**: place switching regulators and high-current traces away from ADC analog inputs.

Mechanical / thermal

- Using more vias (net GND) for the thermal dissipation purpose
- Place heat-sensitive sensing components away from hot parts.

PCB example practical notes

- Using a 4-layer board : Top = signals, Inner1 = ground plane, Inner2 = power plane, Bottom = signals — this dramatically reduces EMI and improves ground return.
- Dedicating one layer as ground pour as recommended in the data sheet.

CIRCUIT OPERATION

The circuit operation of the 32-bit ADC converter board is centered around three main functional blocks: **power regulation**, **analog signal acquisition**, and **digital data conversion & communication**. Each stage ensures stable operation of the ADS1263 ADC and accurate conversion of low-level analog signals.

1. Power Regulation Stage (Using NCP1117ST33T3G)

- The board receives an external input supply ranging from **5V to 12V**.
- This input is fed into the **NCP1117ST33T3G Low Dropout Regulator**, which generates a **stable 3.3V output** required by the ADS1263 ADC and digital logic.
- **Input (10 µF)** and **output (10 µF)** capacitors are placed close to the regulator to reduce voltage ripple and ensure transient stability.
- A **0.1 µF decoupling capacitor** is added near the ADC power pins to suppress high-frequency noise.

- This regulated and filtered supply ensures that analog measurements remain stable and free from power-line-induced fluctuations.

2. ADC Core Operation (ADS1263)

The ADS1263 performs the main analog-to-digital conversion.

a. Reference and Powering

- The ADC is powered from the regulated **3.3V** supply.
- The internal **2.5V reference** or an external precision reference is used for conversion accuracy.
- Proper grounding is ensured using a **star-ground configuration** separating Analog Ground (AGND) and Digital Ground (DGND).

b. Signal Input Handling

- Analog input signals are fed into the **differential or single-ended channels** of the ADS1263.
- Each channel is protected using **RC low-pass filters** to remove high-frequency noise.
- The ADS1263's **programmable gain amplifier (PGA)** adjusts input sensitivity for low-level signals such as sensors, strain gauges, RTDs, or other micro-volt sources.

c. Delta-Sigma Conversion Process

- The ADS1263 uses a **delta-sigma modulator** followed by a digital decimation filter.
- The modulator oversamples the input signal at a very high frequency and converts it into a bitstream.
- The digital filter processes this to produce a stable **32-bit output code** with extremely low noise.

3. Digital Communication Stage (SPI Interface)

- The microcontroller (e.g., ESP32, STM32, Arduino) communicates with the ADS1263 through the **SPI bus**.
- SPI lines include **SCLK, MISO, MOSI, and CS**.
- The **DRDY (Data Ready)** pin signals the microcontroller when a new 32-bit conversion result is available.
- The controller reads the digital output and converts the raw ADC code into voltage using the formula:

$$V_{IN} = \frac{Code}{2^{31} - 1} \times V_{REF}$$

4. Filtering & Stabilization

- Capacitors placed at the AN0–AN7 input pins stabilize high-impedance sensors.
- Ground planes under the analog section reduce EMI.
- Input traces are kept short to prevent noise pickup.

5. Overall Circuit Working Flow

1. External supply enters the board.
2. NCP1117ST33T3G regulates it to 3.3V.
3. ADC receives clean power and reference voltage.
4. Sensor/analog input reaches the ADC through filtering and protection networks.

5. ADS1263 performs 32-bit delta-sigma conversion.
6. DRDY pin notifies the MCU that data is ready.
7. MCU reads the 32-bit output via SPI.
8. Data is processed into voltage or sensor values.

CONCLUSION :

The design and development of the 32-bit ADC converter board using the ADS1263 and NCP1117ST33T3G successfully meet the requirements for high-precision, low-noise, and stable analog-to-digital measurement. The ADS1263, with its ultra-high 32-bit resolution, integrated PGA, extremely low noise characteristics, and multi-channel support, provides a robust platform for capturing micro-level analog signals in scientific and industrial environments. The NCP1117ST33T3G low-dropout regulator ensures a stable and ripple-free 3.3V power supply, which is critical for enhancing ADC accuracy and minimizing noise interference.

Through proper implementation of power filtering, grounding practices, analog front-end conditioning, and SPI-based data acquisition, the board demonstrates excellent measurement stability and reliability. This system produces highly accurate digital output with minimal drift, validating the effectiveness of the overall design. The modular architecture and noise-optimized PCB structure further enhance the system's adaptability for a wide range of applications.

Overall, the project establishes a strong foundation for advanced precision measurement systems. The seamless integration of a 32-bit ADC with a regulated power supply highlights the capability to develop laboratory-grade and industrial-grade sensing platforms. The converter board can be extended for applications involving load cells, biomedical sensors, strain gauges, environmental monitoring, and other domains requiring ultrahigh-resolution signal acquisition. The work demonstrates that with proper component selection and design methodology, high-accuracy data acquisition can be achieved using compact, efficient, and cost-effective hardware**.**

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