HOCHSCHULE
RAVENSBURG-WEINGARTEN
UNIVERSITY
OF APPLIED SCIENCES

CIRCUIT DESIGN 2 PROJECT WS 21/22

Hochschule Ravensburg - Weingarten

The Tea-Brewing-Controller

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Submitted on:	18. January 2022

Acknowledgement

We are glad to express our indebtedness to our guide Prof. Dr. Andreas Siggelkow, Department of Electrical Engineering and Information Technology, Hochschule Ravensburg - Weingarten, for his valuable time, guidance, and constant encouragement at various stages for the execution of the project task.

We are thankful to Mr. Weber, Department of Electrical Engineering and Information Technology, for providing valuable assistance and insight during the experimental process.

Abstract

In this Project, We have designed a Circuitry by using VHDL(Very High Speed Integrated Circuit Hardware Description Language) Programming Language. A system has been developed, which uses a sensor to detect the teabag being dumped into the boiling water, monitors how long it remains there and activates an alarm when brewing should be ended.The Teabag-Sensor-Controller manages the sensor and detects the time of arrival(TOA) of a teabag in the boiling water. Immediately after a detection event, a Three-Wire-Interface (TWI) propagates the time of arrival to the Acoustic-TeaAlarm (ATA).The Acoustic-Tea-Alarm (ATA) reads TOA-data and passes them to the transmitting part of its serial interface, using the ASCII-code. It keeps track of the brewing process and activates the acoustic alarm signal when brewing has ended.

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Section with acronyms

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1 Specification of the project

This chapter consists of the complete top level Block diagram. All the components have been included and connected. The detailed description of individual components has been given in the chapters further.

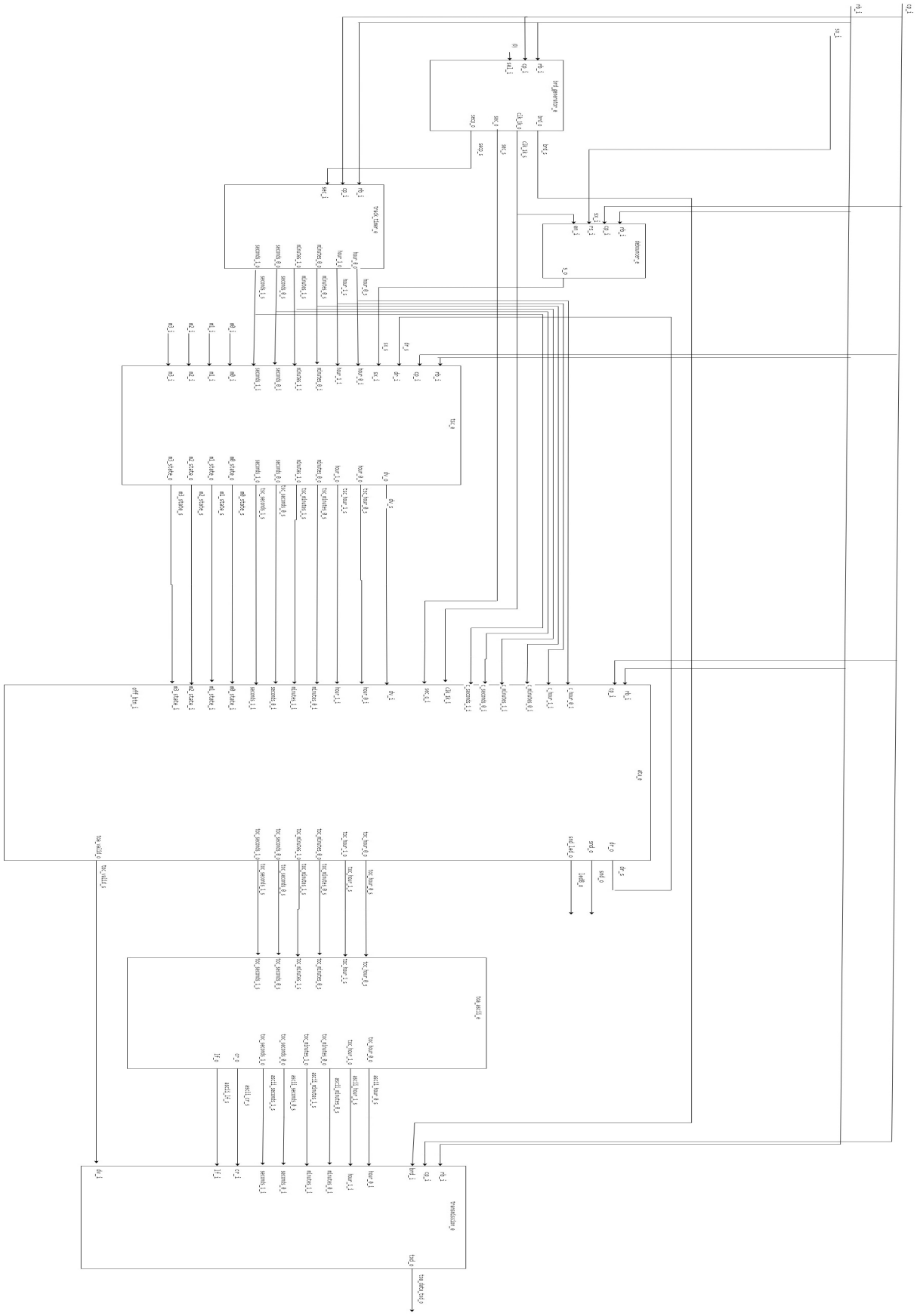

Figure 1: Top Level Architecture

The top level design consists of the following major components :

- Baudrate Generator
- Debouncer
- Time Tracker
- Teabag Controller
- Acoustic Timer Controller
- Transmission

2 Description of Individual Components

This chapter consists of detailed description of the individual components.

2.1 Baudrate Generator

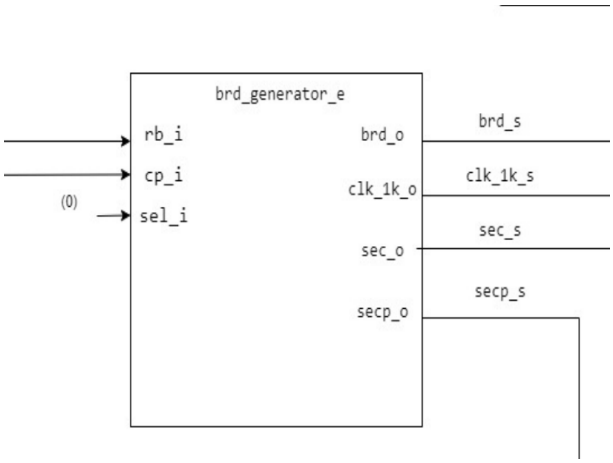

Figure 2: Baudrate Generator

Here rb_i is reset bit and cp_i is clock pulse. sel_i is to select between two frequencies. In this case, we have set it to 0 which means it is set to 20M Hz. brd_o is the baudrate output. clk_1k_o is 1k Hz frequency. sec_o represents the heart beat signal. sec_p gives a clock pulse every second. Figure 3 describes the internal architecture of the Baudrate Generator.

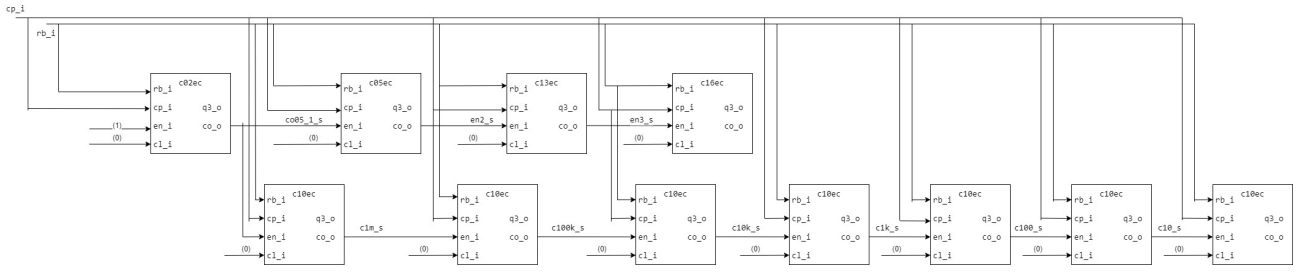

Figure 3: Baudrate Generator

In this component, counters have been used. These counters divide the clock frequency in such a way that the required frequency is obtained as the end result.

2.2 Debouncer

Debouncer is responsible for filtering the input signal from the sensor. This component waits for 15 ms after getting the sensor input in order to check whether the sensor signal is still available. If so, then it is a valid sensor signal. It avoids the possibility of getting glitches from the sensor.

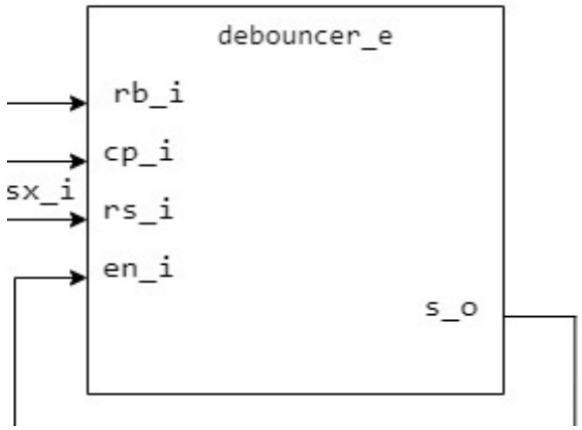

Figure 4: Baudrate Generator

It consists of rb_i and cp_i which are reset bit and clock respectively. rs_i is the raw signal from the sensor. en_i is obtained from the Baudrate generator which enables the component. s_o is the final sensor output which is going further to different blocks.

2.3 Track Timer

Track timer is responsible for generating the timing bits for the internal calculation. It is working just like Baudrate. It also consists of counters which further divide the frequency of the second pulse which is coming from the Baudrate.

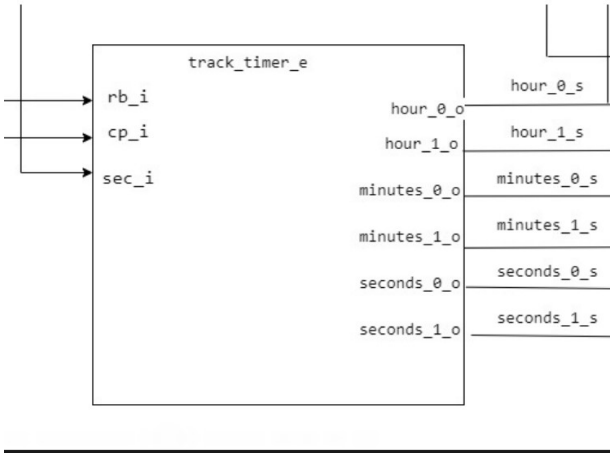

Figure 5: Track Timer

It consists of rb_i and cp_i which are reset bit and clock respectively.sec_i is the second pulse. hour_0_o and hour_1_o is the ones and tens digit respectively.Same goes for minutes and seconds.

2.4 Tea Bag Controller

Tea Bag Controller firstly selects which mode button has been pressed and passes this information to Acoustic Time Controller. It also takes the input time from the sensor and the current time at which the tea bag has been dipped.

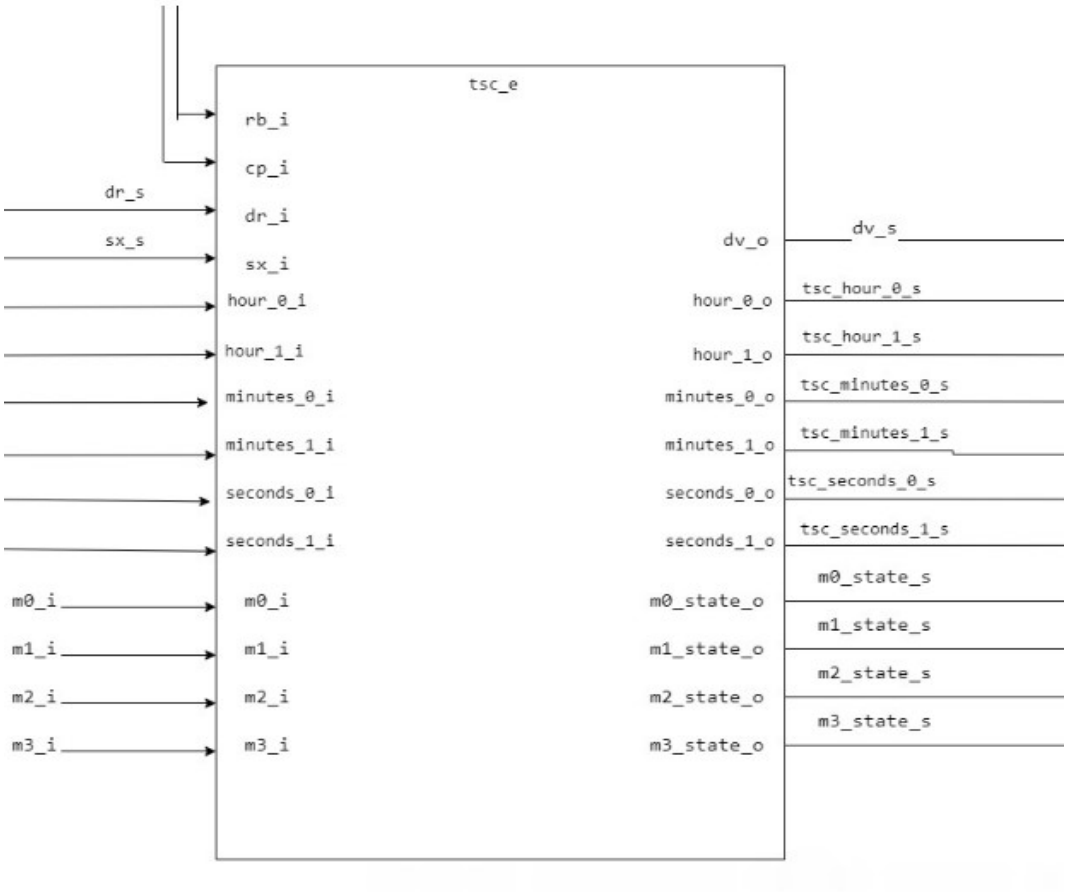

Figure 6: Tea Bag Controller

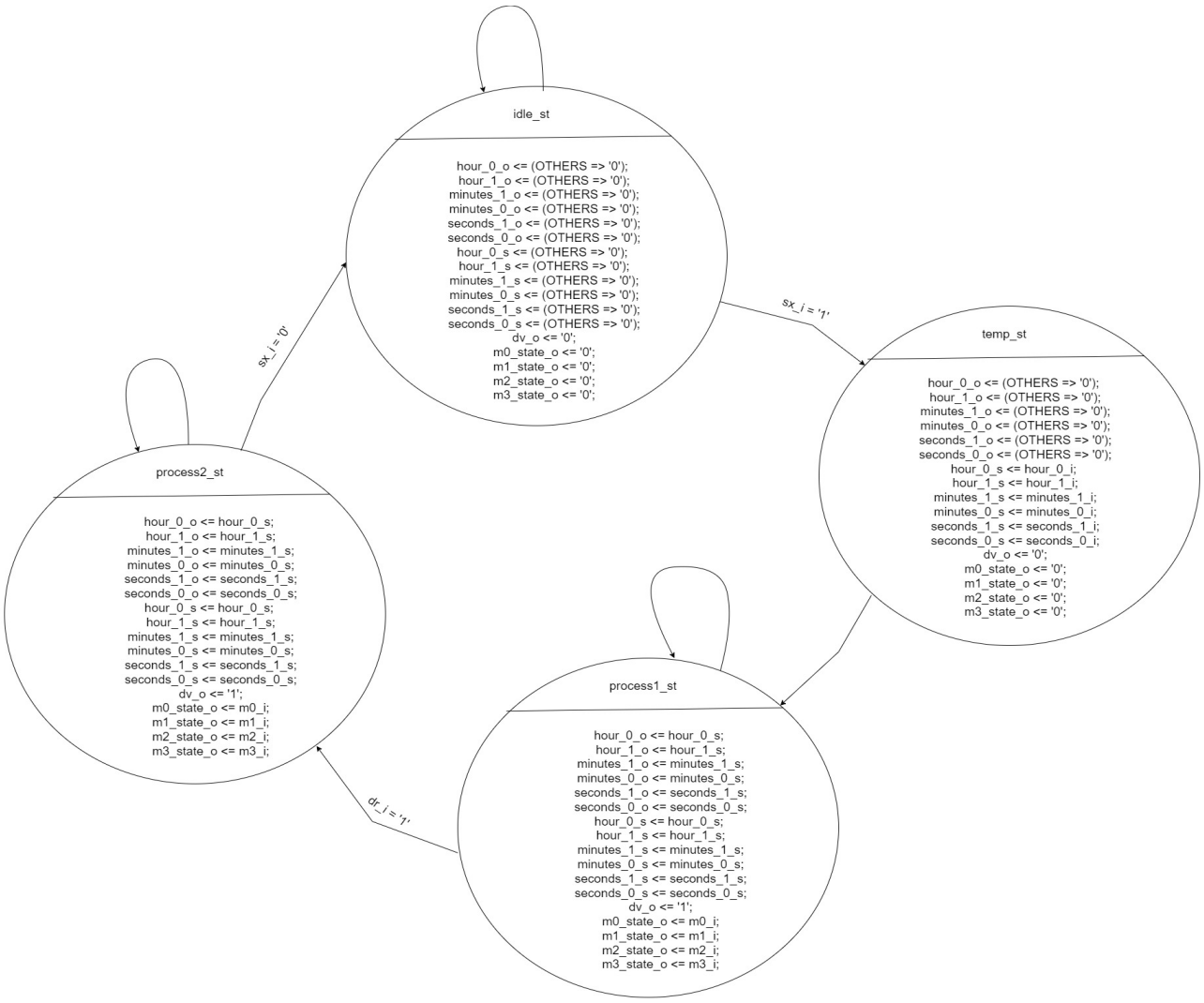

Figure 7: Tea Bag Controller

It consists of rb_i and cp_i which are reset bit and clock respectively.sx_i is the sensor signal coming from the debouncer. The current timing information is being driven to this block as well as the selection modes. The selection modes are responsible for setting up the time delay for the further process.hour_0_o, hour_1_o, minutes_0_o, minutes_1_o, seconds_0_o, seconds_1_o represent the current time at which the sensor has sensed the dipping of the tea bag.

2.5 Acoustic Timer Controller

Acoustic Timer Controller firstly receives the mode type and the current dipping time from TSC. As soon as it receives this data, it adds the respective delay (for eg. 2 mins if m0 and m1 are 0) to the dipped time. It also keeps track of the current time and compares it with the dipper time. When both of these times are equal, it sets the alarm on. This sound will be on till the off button is pressed. Also LED 8 will be lit to display that the brewing process is finished.

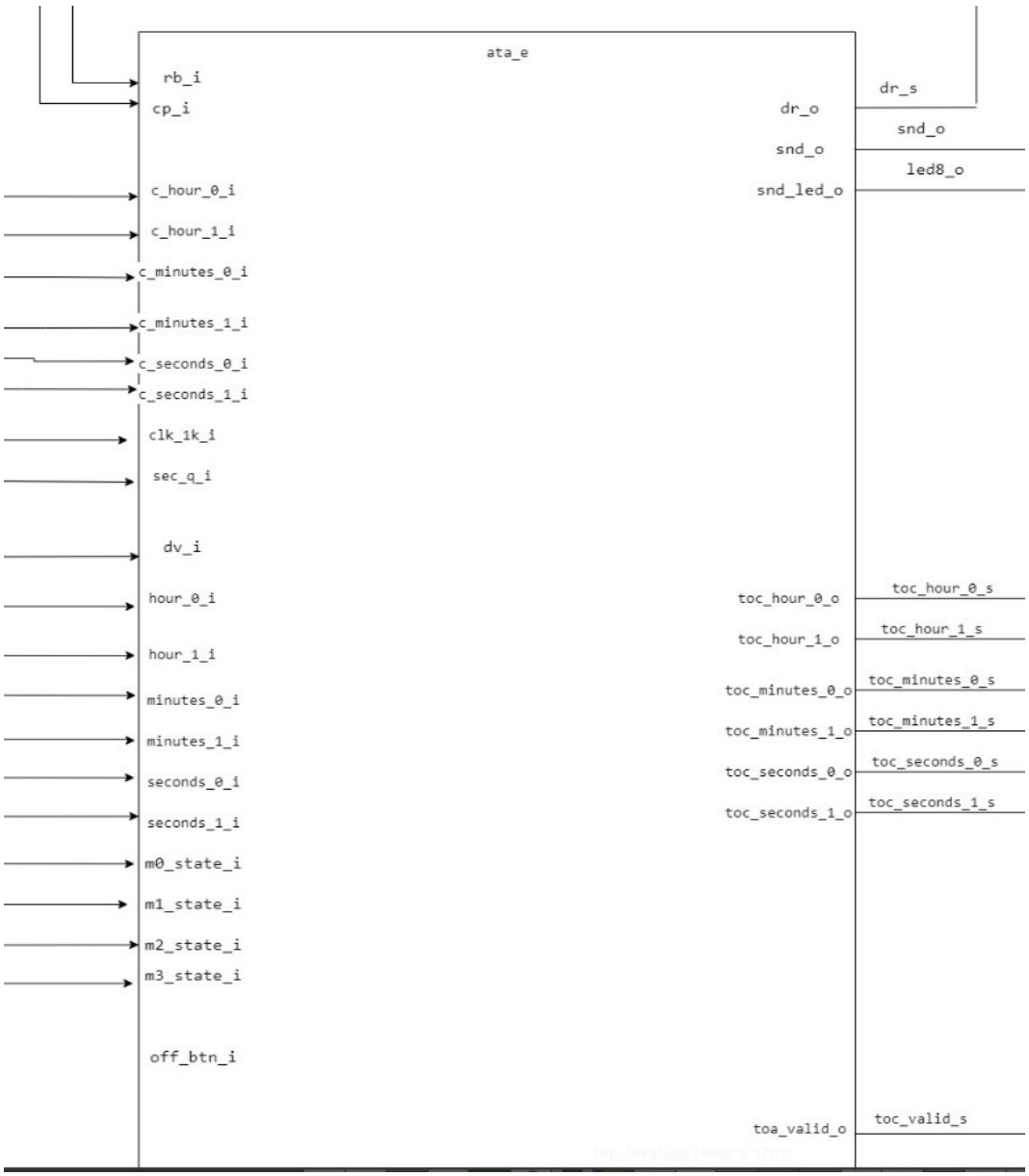

Figure 8: Acoustic Timer Controller

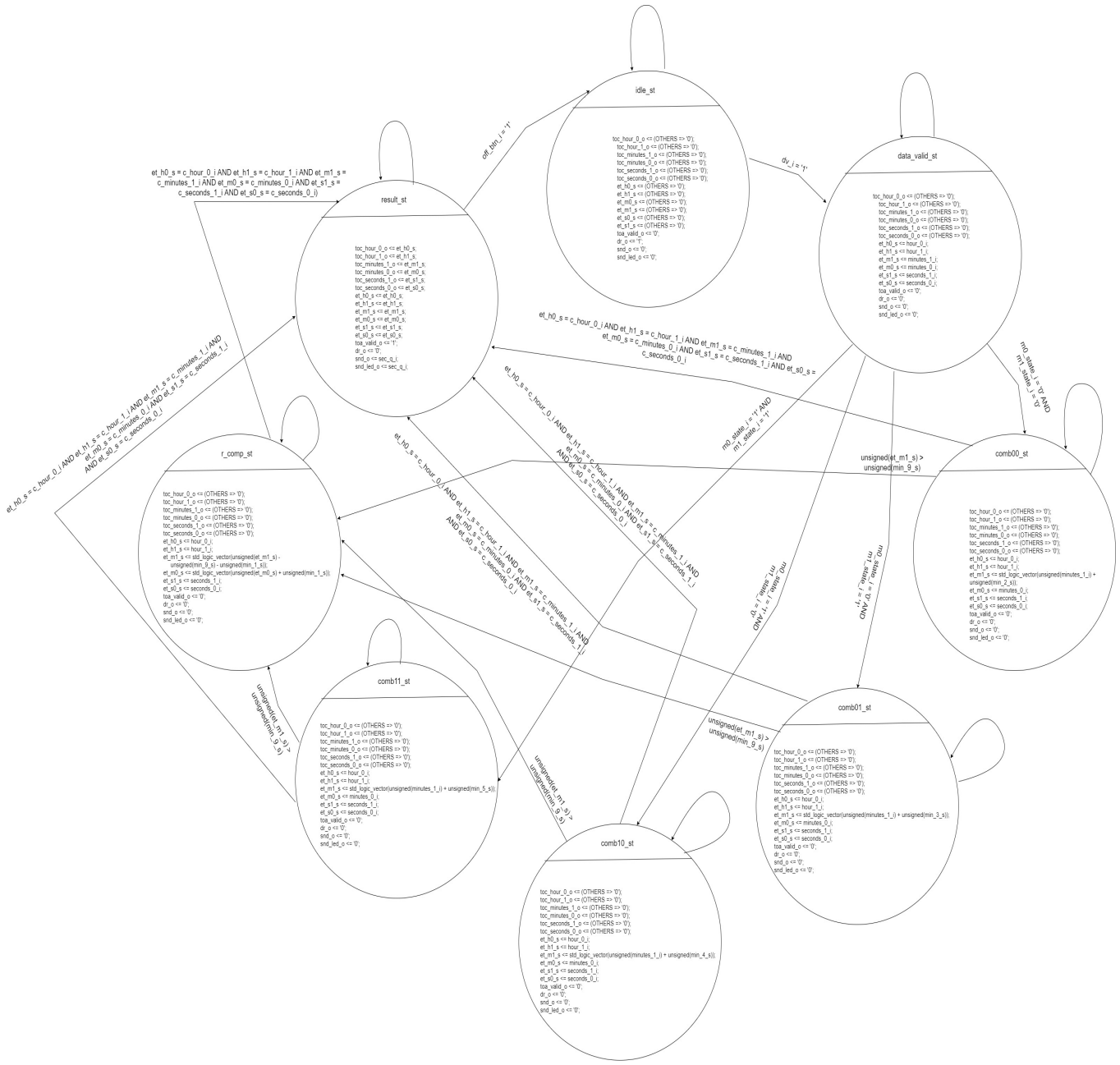

Figure 9: Acoustic Timer Controller

It consists of rb_i and cp_i which are reset bit and clock respectively.It transmits the time data at which the alarm sound begins to the Uart.

2.6 Transmission

The timing information from ATA is converted to ASCII and then sent to the Transmission block. Transmission block is responsible for transmitting the data to the real world via Uart RS232. This block consists of a few counters and multiplexers. These counters and multiplexers are handled by Uart FSM

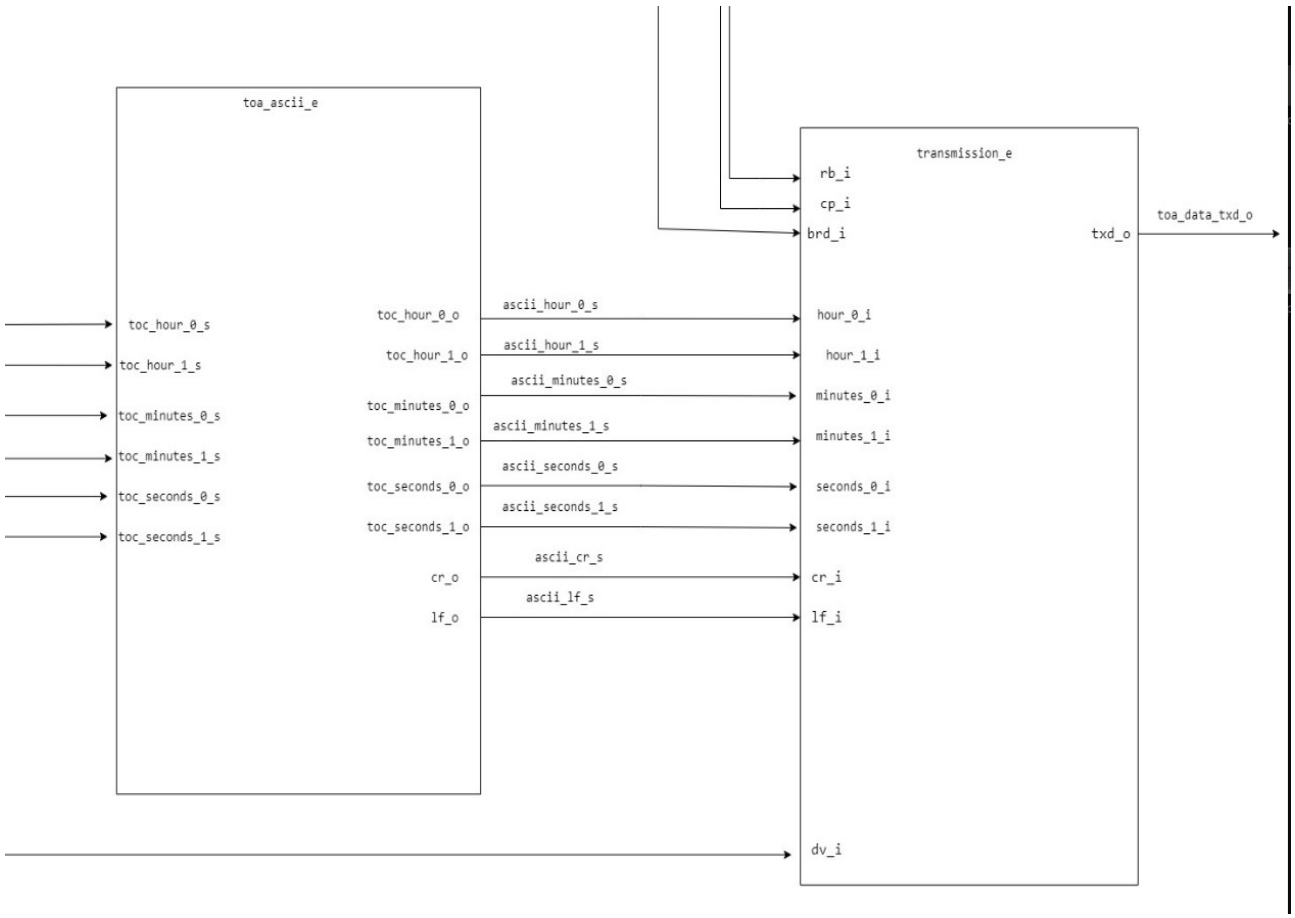

Figure 10: Transmission

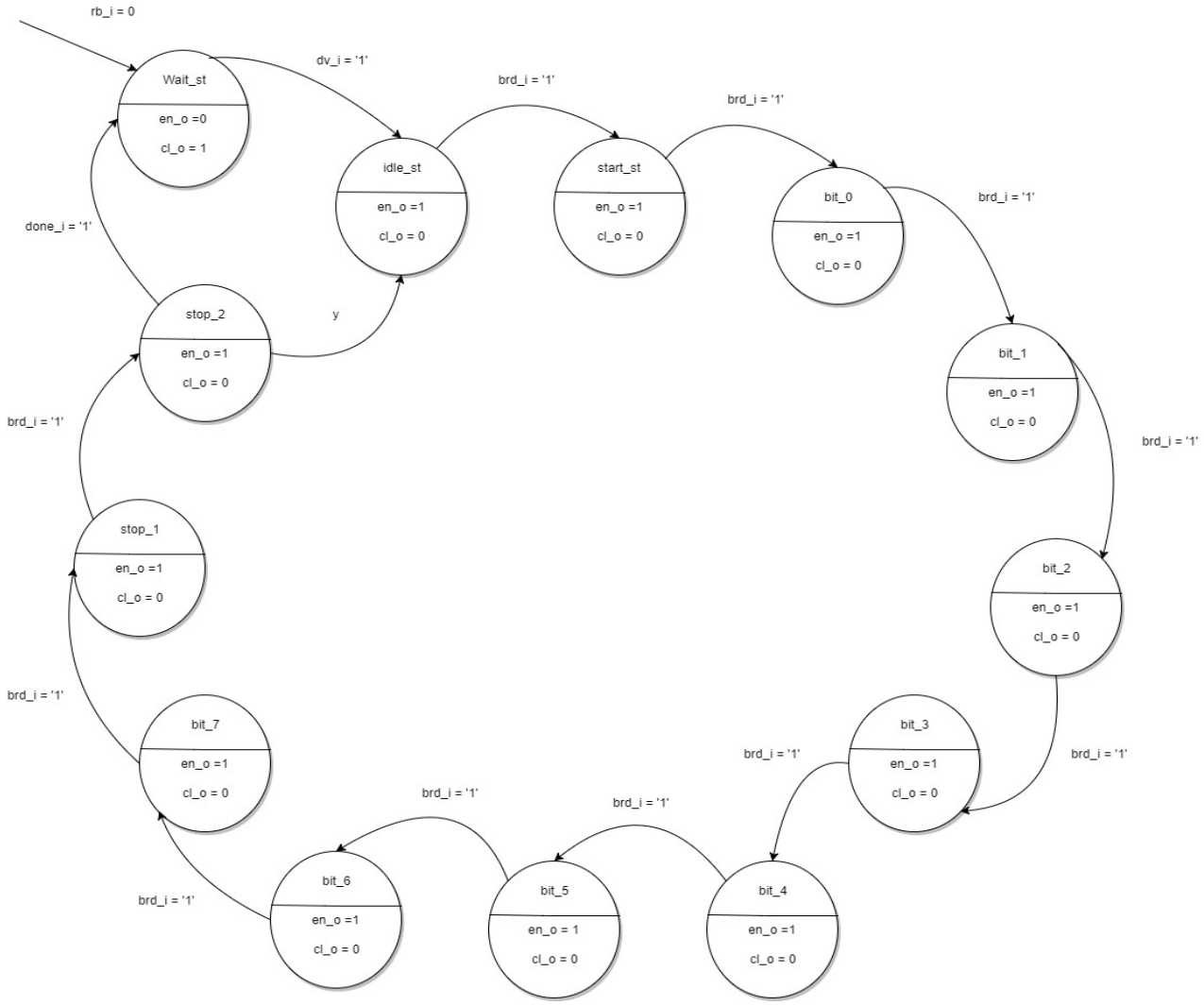

Figure 11: Transmission

It consists of rb_i and cp_i which are reset bit and clock respectively. cr_i and lfiare Carriage Return and Line Feed. txd_o is the output sent to the real world

3 Simulation

This chapter consists of the simulation of the individual components as well as the Top Level Design.

3.1 Baudrate Generator

The figure below represents the simulation of the Baudrate Generator.

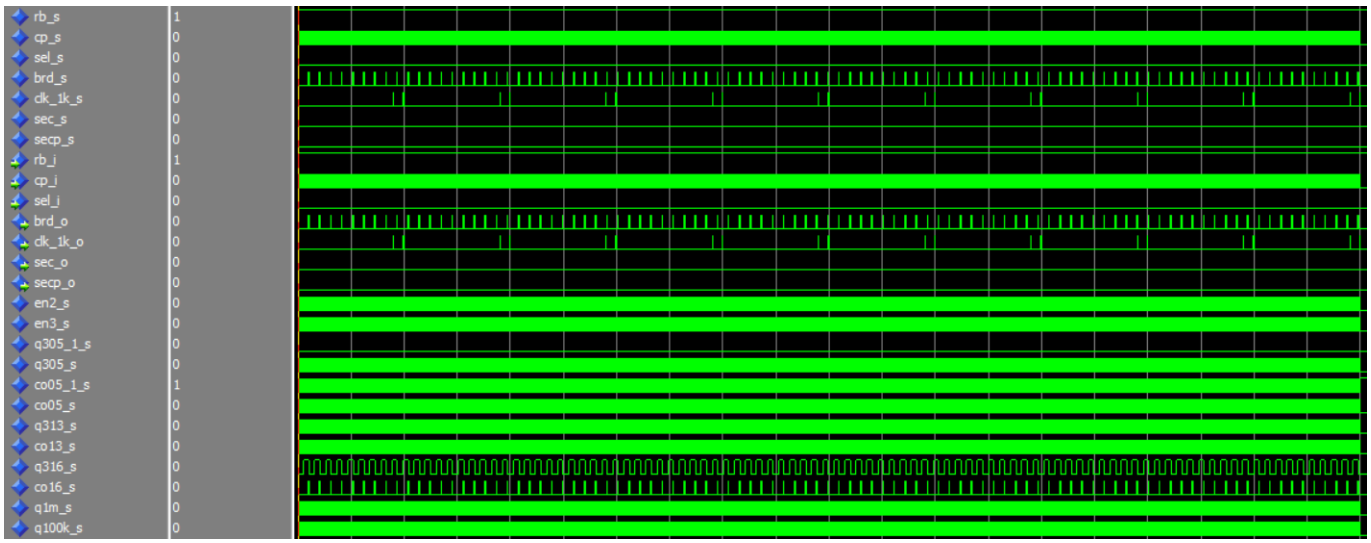

Figure 12: Baudrate Generator

3.2 Track Timer

The figure below represents the simulation of the Track Timer.

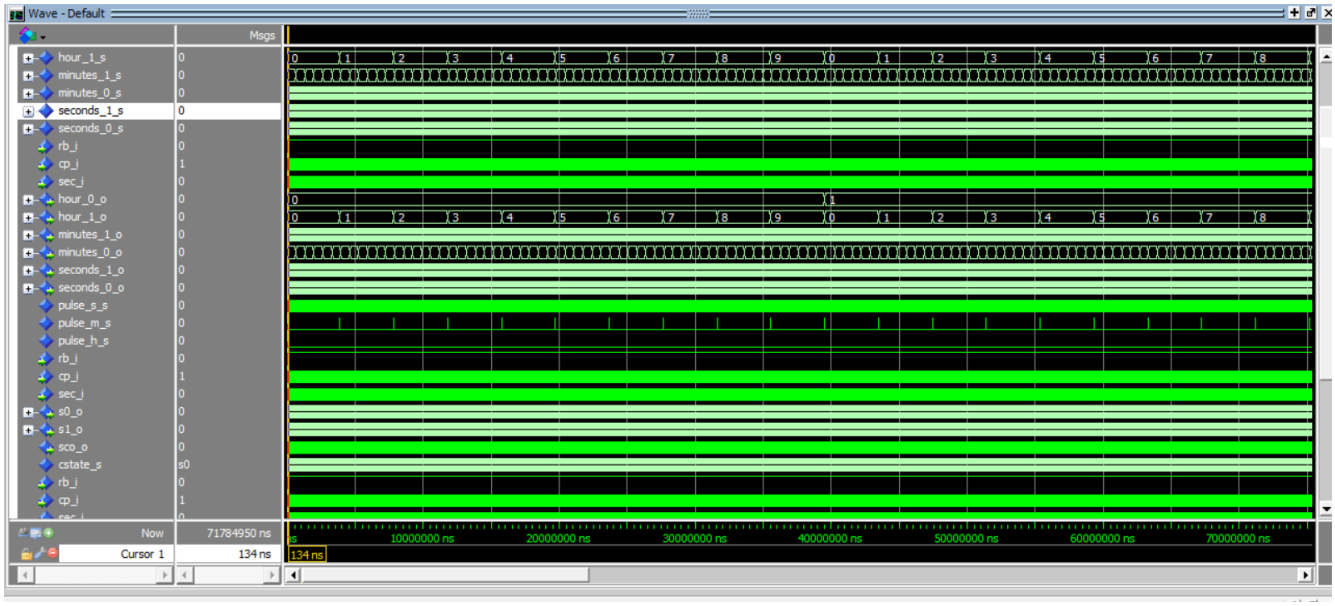

Figure 13: Track Timer

3.3 Tea Bag Controller

The figure below represents the simulation of the Tea Bag Controller.

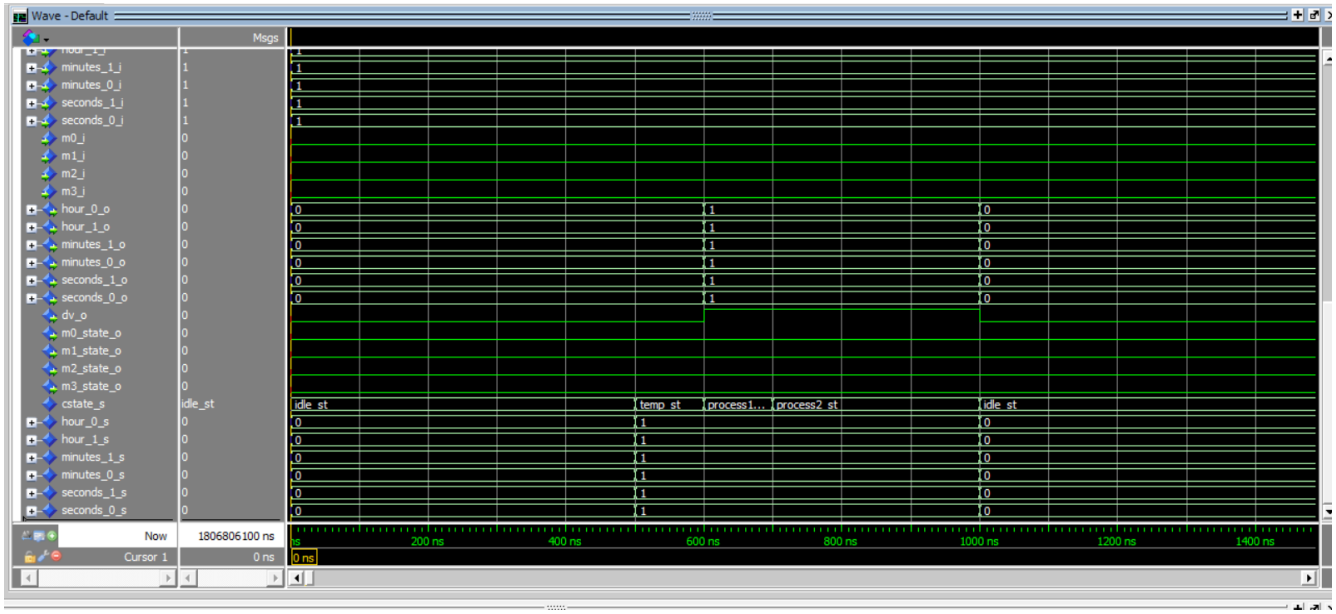

Figure 14: Tea Bag Controller

3.4 Acoustic Timer Controller

The figure below represents the simulation of the Acoustic Timer Controller.

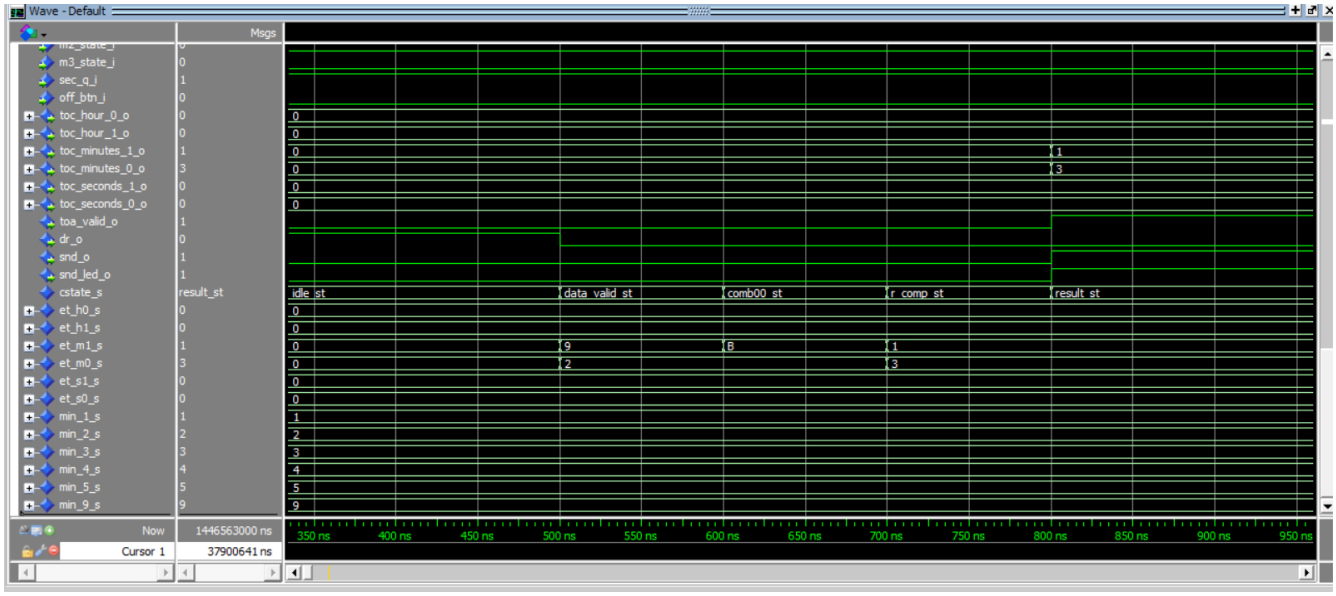

Figure 15: Acoustic Timer Controller

3.5 Transmission

The figure below represents the simulation of the Transmission.

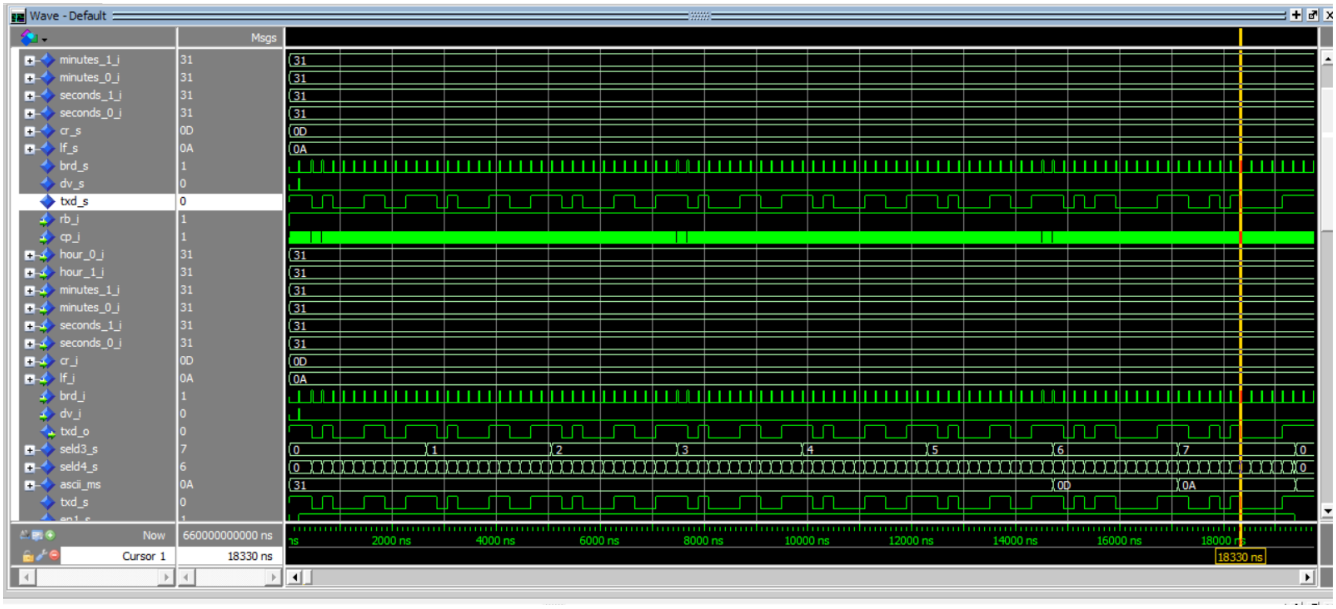

Figure 16: Transmission

3.6 Top Level

The figure below represents the simulation of the Top Level.

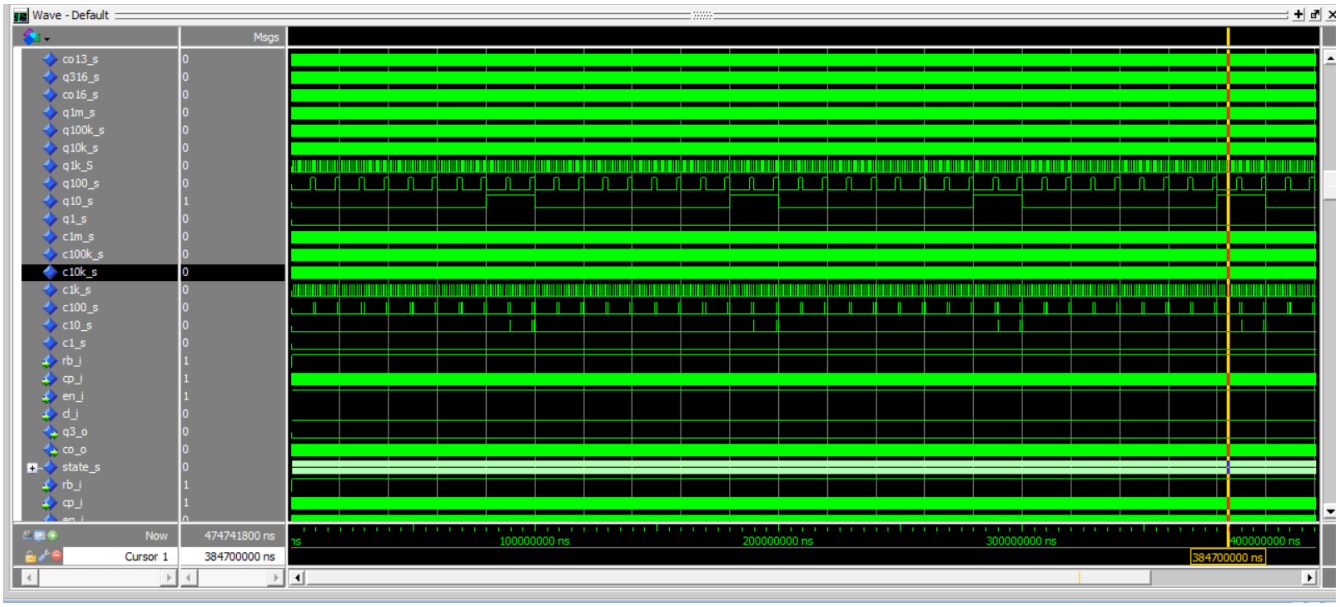

Figure 17: Top Level

4 Synthesis

This chapter consists of the synthesis of the Top Level design.

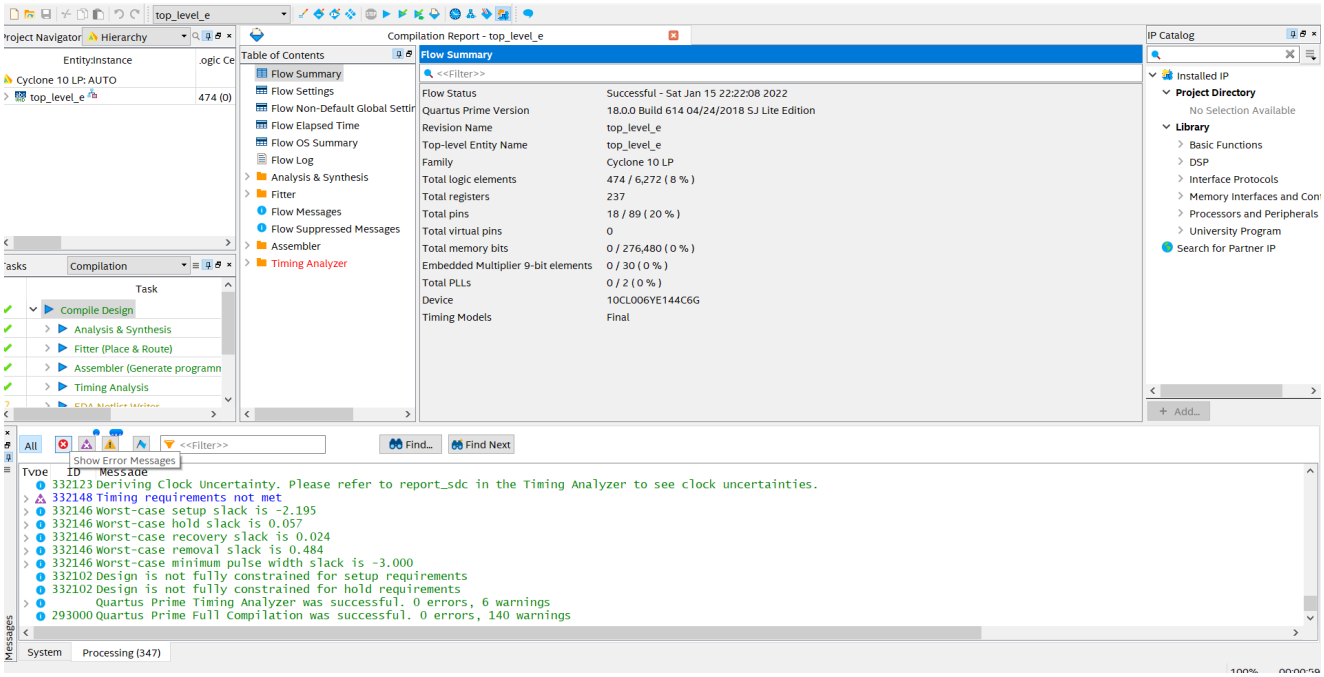

Figure 18: Top Level