Lecture Plan

Language

The language of the lecture/exercises will be German. The language of the texts is English.

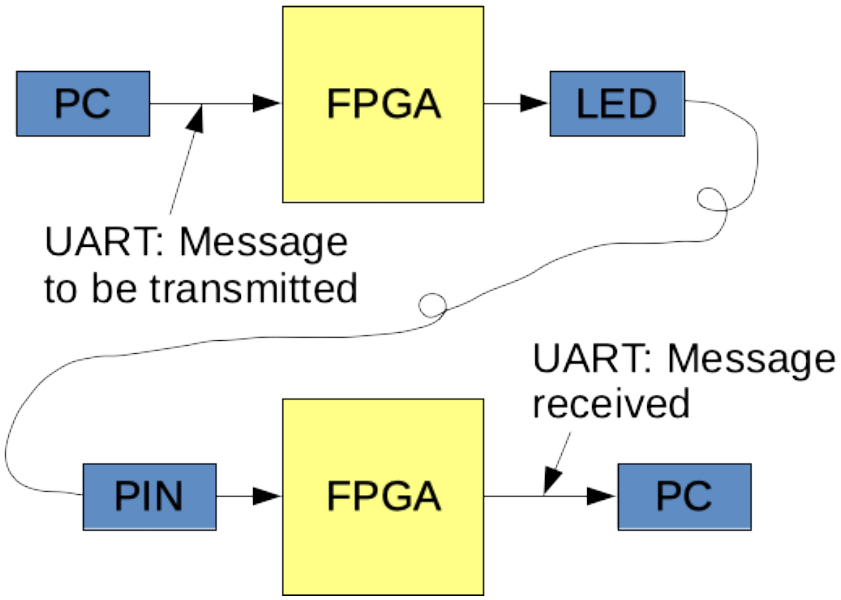
Handouts

- Design Guidelines
- Requirements explanation
- Various VHDL chapters
- Presentation
- Description of the project

The handouts will be available on Moodle.

VHDL Lecture and Exercises

The lecture gives a short theoretic introduction to the standard tool for the digital chip development, which is VHDL. The lecture will be completed by „hands-on" exercises with VHDL. The teacher explains VHDL and the student works on a given project which needs to be solved by means of VHDL. The teacher answers nearly all questions about VHDL will not solve the project.



The project is, the customer said: "I want to have an ASIC (FPGA), which ...
A circuit should be designed, which is able to receive a message from a PC (via a UART), the message should be translated to morsecode patterns, these patterns should drive a LED. Second, a circuit should be designed, where a photo diode receives the morsecode pattern, transmits it to the FPGA, the FPGA translates it to ASCII, the ASCII message should be transmitted to a PC. The needed FSMs must be three-block FSMs.
For all of those translations, time slots will be needed. Those time slots should be configured by means of 8 bit registers. The registers have an address and will be loaded via the UART.

So, the needed setup, configuration and working data should be stored in 8 bit registers. The registers must be loadable by an UART-RX (8N1, 9k6) and the content of the registers must be readable by an UART-TX (8N1, 9k6). The registers should be made addressable. All data should be made visible on a PC via this UART. The programming language is C++.
There are groups of two persons, one person designs the transmitter, the other the receiver.

The requirements and the specification, written in Latex, should contain: a history table (change management), the requirements, one chapter for each design-block, block diagram, FSM, I/O-tables for each block (with explanation), a table with used signals and processes, a table with registers (description of the bits, reset value, address if applicable), no tool description, no gossip.
By the way, I heard something about OSI layers, please explain your implementations with respect to the OSI layers (in the final specification). I want to understand, what those OSI layers are."

Deliverables

- After two weeks (05.04.22, 8:00): A requirements specification (functional requirements), by every single student. Written in Latex. It should be functional requirements which can be tested (VHDL assertions). It should be a table with all information needed.
- After one month (19.04.22, 8:00): A detailed block specification. Written in Latex.
- After 2,5 month (24.05.22, 18:00): A final simulation
- After 3 month (14.06.22, 18:00): A synthesized solution
- At the end: A finalized design specification (21.06.2022), written in Latex, the final product, an oral presentation (21.06.22 and 28.06.22) of your design.
- ~~All simulations and synthesis must be done on Linux PCs~~
- The simulation must run on MODELSIM (sign off)
- The synthesis must be done with ISE/Vivado/Quartus
- The design must strictly be according the design guideline
- Students must do the main work in the lab (H214)

Examination

- Requirements (10%), after ca. 2 weeks
- 1. Specification (10%), after ca. 1 month
- Simulation Sign-Off (10%), after ca. 2,5 months
- Synthesis Sign-Off (10%), after ca. 3 month
- Final Specification (40%), at the end
- Presentation & Questions (20%), at the end

Lectures and Labs

1. Presentation of the project and lab. organization
2. Presentation of the project
3. Team building
4. Project plan
5. Explanation of „requirements".
6. Explanation of „1. Block Specification".
7. ~~Set-up of the Design-Guidelines (together with the students).~~
8. Lecture
9. Explanation of the „Specification".