CAE

Vorläufig

VHDL-LAB-Tasks
The Semester-Project 2022SS22

Zusammenfassung

Morse-Code-Generator

Ein Mikrochip zur Erzeugung von Morsezeichen soll auf einem Field-Programmable-Gate-Array (FPGA) in zwei Architekturvarianten ($ar4$ und $ar3$) entwickelt werden.

Die Architekturen müssen folgende gemeinsame Eigenschaften haben:

- Morsezeichen (auch CW-Zeichen genannt) werden mit einer Geschwindigkeit von 15 Worten pro Minute (15 WpM) ausgegeben.

- Morsezeichen sind an einem Ausgang snd_o als akustische Signale ($1kHz$) z.B. mit einem Mini-Lautsprecher hörbar.

- Morsezeichen sollen am digitalen Ausgang cw_o eine Leuchtdiode ansteuern.

- Zur Kontrolle werden die Morsezeichen auch als serielles ASCII-Signal am Ausgang txd_o ausgegeben. txd_o ist mit einem PC oder Laptop verbunden.

- Hardware-Beschreibungssprache: VHDL.

A Microchip, which generates morsecode-patterns, is to be designed using a Field-Programmable-Gate-Array (FPGA). There will be two architecture-versions ($ar4$ und $ar3$).

The architectures must have the following properties in common:

- The Morsecode-Transmissions (also known as CW-Signals) must have a speed of 15 Words per Minute (same as 60 characters per minute)

- There must be an acoustic output ($1kHz$) at pin snd_o.
  snd_o could be connected to a small loudspeaker.

- There must be a digital output cw_o, e.g. connected to a light-emitting-diode (LED).

- There must be an output txd_o, which connects to a laptop or PC. txd_o produces the serial ASCII-version of the morse-code transmitted just now.

- Hardware-Description-Language: VHDL.

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1 Semester 4

1.1 Computer Aided Circuit Design, $ar4$

Die FPGA-Chip-Architektur $ar4$ realisiert zusätzlich:

- Die Dateneingabe erfolgt mit einer RS232-Schnittstelle. ASCII-Zeichen werden am Pin rxd_i empfangen und auf dem FPGA in Morsecode gewandelt.

Furthermore, the FPGA-Architecture $ar4$ has the following property:

- A RS232-Interface is used to enter data to the FPGA. ASCII-Data is applied to the FPGA-Pin rxd_i and converted to morse-code.

2 Semester 3

2.1 Circuit-Design-Lab, $ar3$, (VHDL-1911)

Die FPGA-Chip-Architektur $ar3$ realisiert ferner:

- Die Dateneingabe erfolgt mit einer Drei-Draht-Schnittstelle.

- ASCII-Zeichen-Texte (QTCs) werden durch Auswahlpins selektiert:

Furthermore, the FPGA-Architecture $ar3$ has the following property:

- A Three-Wire-Interface (TWI) is used to enter data to the FPGA.

- ASCII-Messages (QTCs) will be selected using some FPGA-Input-Pins:

QTC1: [ka] *hello world* [ar]
QTC2: [ka] *the quick brown fox jumps over the lazy dog* 1234567890 *times* [ar]
QTC3: Real-Time-Clock, e.g.: [ka] $QTR\ hhmmss$ [ar]

2.2 Mikrocontroller-Lab (uC-7077)

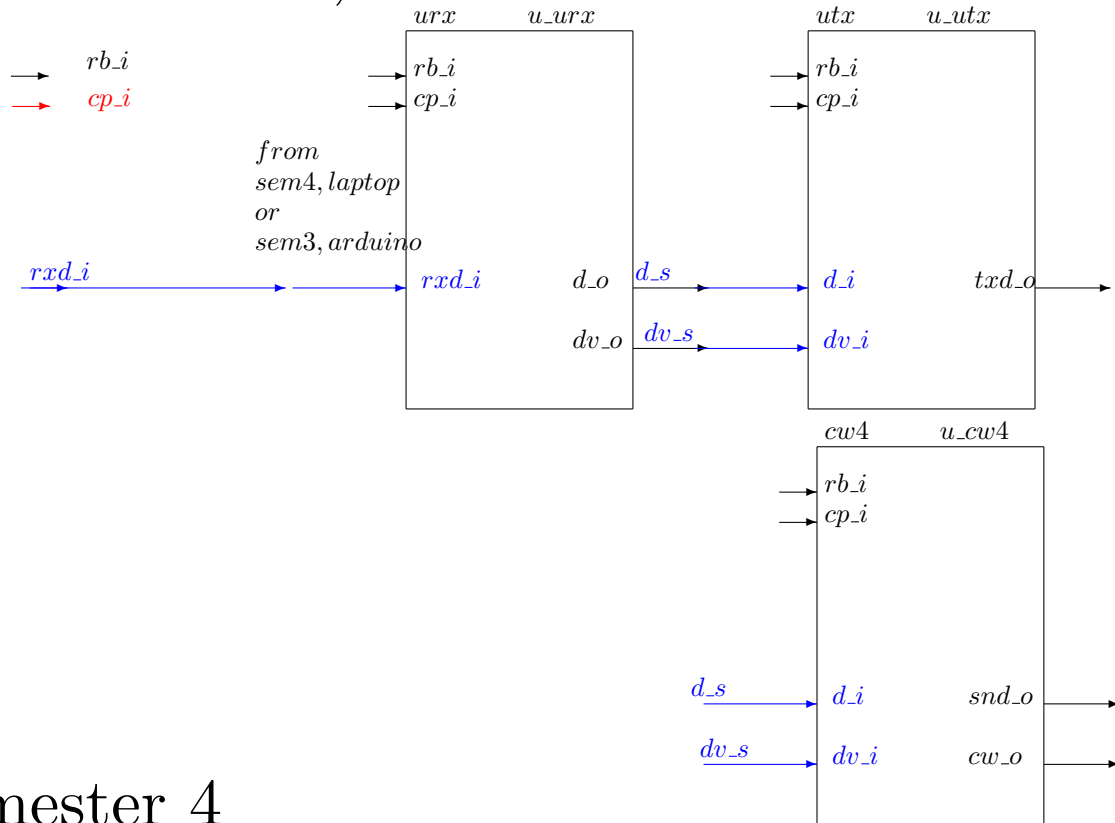Auf einem Arduino-Board wird ein Morsegenerator programmiert. Programmiersprache: C

- Dateneingabe:Arduino-USB,ASCII

- ASCII-Zeichen der Arduino-USB-Schnittstelle werden mit TWI zum FPGA übertragen.

- CW-Geschwindigkeit: 15 WpM.

- Ausgang cw_o: CW, digital
  Ausgang snd_o: CW, Ton, $1kHz$

- Optional:
  Erzeugung einiger Testmuster:
  Eingang PIN?2, Punktfolge . . . .
  Eingang PIN?3, Strichfolge _ _ _ _
  Eingang PIN?4: Sender aktiv
  Eingang PIN?5: QTC1
  Eingang PIN?6: QTC2
  Eingang PIN?7: QTC3

A Morse-Code-Generator must be implemented on an Arduino-Board. Programming-LanguageC

- Data Input:Arduino-USB,ASCII

- ASCII-Chars from Arduino-USB must be transferred to the FPGA via TWI.

- CW-speed: 15 WpM.

- Output cw_o: CW, digital
  Output snd_o: CW, sound, $1kHz$

- Optional:
  Generation of some Testpattern:
  Input PIN?2, dots only . . . .
  Input PIN?3, dashes only _ _ _ _
  Input PIN?4: on the air
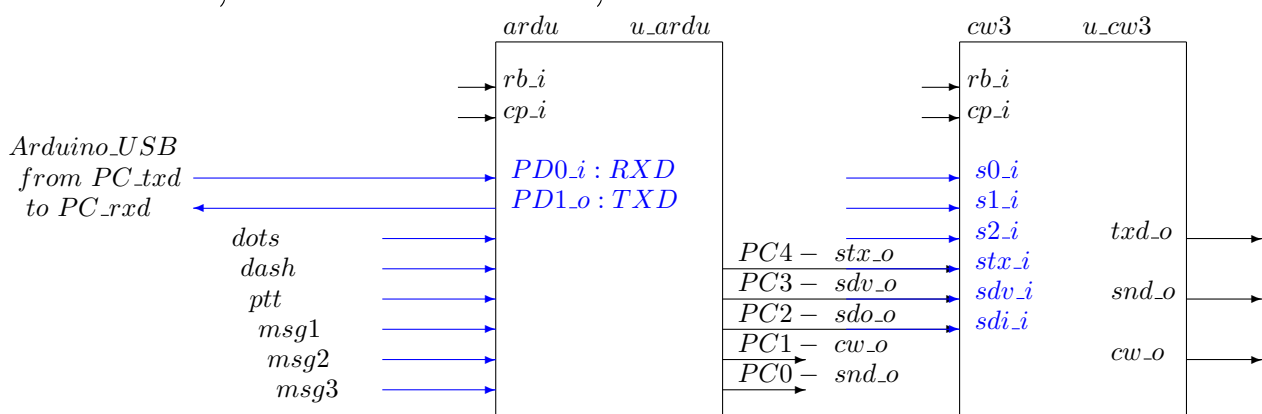 Input PIN?5: QTC1
  Input PIN?6: QTC2
  Input PIN?7: QTC3

https://www.qsl.net/dk5ke/morsezeichen.html
https://www.itu.int/dms_pubrec/itu-r/rec/m/R-REC-M.1677-1-200910-I!!PDF-E.pdf

3   Preliminary Block-Diagram

CW-Generator,VHDL

urx   *u_urx*

rb_i
cp_i

rb_i
cp_i

utx   *u_utx*

rb_i
cp_i

rb_i
cp_i

from
sem4, laptop
or
sem3, arduino

rxd_i

rxd_i   *d_o*   *d_s*   *d_i*

txd_o

dv_o   *dv_s*   *dv_i*

cw4   *u_cw4*

rb_i
cp_i

d_s   *d_i*   *snd_o*

dv_s   *dv_i*   *cw_o*

Semester 4

Arduino, CW-Generator,GCC

ardu   *u_ardu*

rb_i
cp_i

cw3   *u_cw3*

rb_i
cp_i

Arduino_USB
from PC_txd
to PC_rxd

PD0_i : RXD
PD1_o : TXD

s0_i
s1_i
s2_i

dots
dash
ptt
msg1
msg2
msg3

PC4 −   stx_o
PC3 −   sdv_o
PC2 −   sdo_o
PC1 −   cw_o
PC0 −   snd_o

stx_i
sdv_i
sdi_i

txd_o

snd_o

cw_o

Semester 3   CW-Generator,VHDL

```
-- ==========================================================================
-- THESE characters must be used in filenames and dirnames:
-- ==========================================================================
-- Alphabet, lower case:      abcdefghijklmnopqrstuvwxyz
--          upper case:       ABCDEFGHIJKLMNOPQRSTUVWXYZ
-- Numbers:                   01234567890
-- Special chars: <->,<_>,<.>  minus sign, underscore and dot
-- ========================================
-- !!!! All OTHER CHARACTERS ARE ILLEGAL !!!!
-- ========================================
-- FILEnames or DIRnames MUST NOT start with a special char!
-- A dot MUST BE used as a separator between a filename and its extension!
-- DIRnames must NOT have special chars exept the Underscore!
--
-- Examples:        Content of file is
-- mycirc_e.vhd      a VHDL-Entity called mycirc_e
-- mycirc_a1.vhd     a VHDL-Architecture mycirc, version a1
-- README.txt        some text

 -- ILLEGAL NAMES:    filename has ...
 -- .test.vhd  :        ... a dot at the beginning
 -- xx aa.vhd  :        ... an illegal char (blank or space)
-- ==========================================================================
-- Tree-structure:   xxxx is top-level of your project-directory-tree
--
-- xxxx---+---VHD----+---src  contains Entities and Architectures
--        |          +---tb   contains VHDL-Testbenches
--        |          +---sim  work-dir for simulation, not needed in TAR
--        |
--        +---DOC----+---pdf  contains PDF-Versions
--        |          +---tex  contains TEX-Sources
--        |
--        +---GCC----+---src-gcc  contains C-Sources
--                   +---src-ardu contains Sources for Arduino
-- ==========================================================================
-- HOW-TO archive a project:
-- ======================
-- 1) cd to your project directory, rm all rubbish and write the archive:
--    cd xxxx              # change to the project-directory
--    pwd                  # make sure, you are there
--    rm -R ./VHDL/sim     # delete any garbage produced during simulation
--    tar -cvf xxxx.TAR .  # write the tar-archive
--    ls  -all xxxx.TAR    # make sure you have the file
--
-- 2) Generate a md5-checksum of your archive:
--    openssl dgst -md5 xxxx.TAR > xxxx.TAR.md5  # write a md5-checksum
--
-- 3) Now you have two items to be taken anywhere as mail-attachments!
--    xxxx.TAR       : a TAR-file which contains your project
--    xxxx.TAR.md5   : a file containing the md5-chksum of xxxx.TAR
-- --------------------------------------------------------------------------
```

```
-- ------------------------------------------------------------------------
-- vhdl-2022SS22-0303-QATTR-P1.txt, FPGA is 10M16SAU169C8G
-- ------------------------------------------------------------------------
-- FPGApins:   ASSIGNMENT CAN BE CHANGED AT ANY TIME
-- POWER:      via USB, else VCC5V to J2,Pin 13 (has priority)
-- ------------------------------------------------------------------------
-- ATTRIBUTE chip_pin of PIN_E7 : SIGNAL IS  "E7"; -- SW1_RESET_aktiv_low
   ATTRIBUTE chip_pin          : string;
   ATTRIBUTE chip_pin of   rb_i : SIGNAL IS  "E6"; -- SW2_USR_BTN_akt_low;
   ATTRIBUTE chip_pin of   cp_i : SIGNAL IS  "H6"; -- CLK_12MHz
-- ATTRIBUTE chip_pin of   cp_i : SIGNAL IS  "G5"; -- CLK_EXT
-- ------------------------------------------------------------------------
-- J2-Side, below right, LEDs on QUARTUS BOARD, emits light when log1
-- ------------------------------------------------------------------------
   ATTRIBUTE chip_pin of  ld1_o : SIGNAL IS  "A8"; -- led1, ld1, e.g. rb_s
   ATTRIBUTE chip_pin of  ld2_o : SIGNAL IS  "A9"; -- led2, ld2, e.g.sec_s
   ATTRIBUTE chip_pin of  ld3_o : SIGNAL IS "A11"; -- led3, ld3, e.g.tx1_s
   ATTRIBUTE chip_pin of  ld4_o : SIGNAL IS "A10"; -- led4, ld4
   ATTRIBUTE chip_pin of  ld5_o : SIGNAL IS "B10"; -- led5, ld5
   ATTRIBUTE chip_pin of  ld6_o : SIGNAL IS  "C9"; -- led6, ld6
   ATTRIBUTE chip_pin of  ld7_o : SIGNAL IS "C10"; -- led7, ld7
   ATTRIBUTE chip_pin of  ld8_o : SIGNAL IS  "D8"; -- led8, ld8
-- ------------------------------------------------------------------------
-- ------------------------------------------------------------------------
--      12MHz:   H6           +------------------+
--      CLK_EXT: G5           +     --USB--       +  UBtn: E6......rb_i....
--                            +     --USB--     o +1 LED1: A8.....ld1_o <=  rb_s
--                            +     -------     o +2 LED2: A9.....ld2_o <= sec_s
--          J4 JTAG           +                 o +3 LED3: A11....ld3_o <= tx1_s
--          +1 GROUND         +                 o +4 LED4: A10....ld4_o....
--          +2 E5 JTAGEN +                      o +5 LED5: B10....ld5_o....
--          +3 G2 TCK    +                      o +6 LED6: C9.....ld6_o....
--          +4 F6 TDO    +                      o +7 LED7: C10....ld7_o....
--          +5 F5 TDI    + 10M16SAU169C8G o +8 LED8: D8.....ld8_o....
--          +6 G1 TMS    +                       +
--                   J1 + J3              J4  J2
--          D3 AREF  1+ +1 AIN   D2      +1  +14 +5V...................
--   ..........E1 AIN0  2+ +2            +2  +13 VIN-<-EXT,USER,VCCin..
--   ..........C2 AIN1  3+ +3 AIN7 B1    +3  +12 +3.3V.................
--   ..........C1 AIN2  4+                +4  +11 GND...................
--   ..........D1 AIN3  5+                +5  +10 RES   E7....DO.NOT.USE.
--   ..........E3 AIN4  6+                +6   +9 D14   G12.............
--   ..........F1 AIN5  7+                     +8 D13   H13.............
--   .QTC3_i...E4 AIN6  8+                     +7 D12   H10.............
--   .QTC2_i...H8 D0    9+      PMOD           +6 D11   J10.............
--   .QTC1_i..K10 D1   10+ VCC GND-PMOD        +5 D10   K12.............
--   ..........H5 D2   11+  : :  ....M1-RXD    +4 D9    K11.............
--   .sdi_i....H4 D3   12+  : : : ..M2-TXD     +3 D8    J13.............
--   .sdv_i....J1 D4   13+  : : :|: ..L3       +2 D7    J12...snd_o......
--   .stx_i....J2 D5   14+  : : : : : M3       +1 D6    L12....cw_o......
--                         6 5 4 3 2 1
--                         + + + + + +  J6 PIO_04...PIO_01
--                         + + + + + +     PIO_08...PIO_05
--                         1 1 1 9 8 7
--                         2 1 0 . . ...N3
--                   VCC...... . . ......N2
--                 GND-PMOD.... . .....K2-TXD at J6,Pin9
--                            .......K1-RXD at J6,Pin10
-- ------------------------------------------------------------------------
-- ------------------------------------------------------------------------
```

```
-- --------------------------------------------------------------------------
-- vhdl-2021WS22-0906-QATTR-P2.txt, prev: 2021-0829, FPGA is 10M16SAU169C8G
-- --------------------------------------------------------------------------
-- FPGApins:   ASSIGNMENT CAN BE CHANGED AT ANY TIME
-- POWER:      via USB, else VCC5V to J2,Pin 13 (has priority)
-- --------------------------------------------------------------------------
-- ATTRIBUTE chip_pin of PIN_E7 : SIGNAL IS  "E7"; -- SW1_RESET_aktiv_low
   ATTRIBUTE chip_pin         : string;
   ATTRIBUTE chip_pin of   rb_i : SIGNAL IS  "E6"; -- SW2_USR_BTN_akt_low;
   ATTRIBUTE chip_pin of   cp_i : SIGNAL IS  "H6"; -- CLK_12MHz
-- ATTRIBUTE chip_pin of   cp_i : SIGNAL IS  "G5"; -- CLK_EXT
-- --------------------------------------------------------------------------
-- J2-Side, below right, LEDs on QUARTUS BOARD, LEDx emits light when log1
-- --------------------------------------------------------------------------
   ATTRIBUTE chip_pin of  ld1_o : SIGNAL IS  "A8"; -- led1, ld1 <=  rb_s
   ATTRIBUTE chip_pin of  ld2_o : SIGNAL IS  "A9"; -- led2, ld2 <= sec_s
   ATTRIBUTE chip_pin of  ld3_o : SIGNAL IS "A11"; -- led3, ld3 <= tx1_s
   ATTRIBUTE chip_pin of  ld4_o : SIGNAL IS "A10"; -- led4, ld4
   ATTRIBUTE chip_pin of  ld5_o : SIGNAL IS "B10"; -- led5, ld5
   ATTRIBUTE chip_pin of  ld6_o : SIGNAL IS  "C9"; -- led6, ld6
   ATTRIBUTE chip_pin of  ld7_o : SIGNAL IS "C10"; -- led7, ld7
   ATTRIBUTE chip_pin of  ld8_o : SIGNAL IS  "D8"; -- led8, ld8
-- --------------------------------------------------------------------------
-- J1-Side, above left
-- --------------------------------------------------------------------------
-- AREF, D3, can not be used            AREF   D3                  (J1- 1)
   ATTRIBUTE chip_pin of  nn_i : SIGNAL IS  "E1"; -- ADC8 AIN0    (J1- 2)
   ATTRIBUTE chip_pin of  nn_i : SIGNAL IS  "C2"; -- ADC2/AIN1    (J1- 3)
   ATTRIBUTE chip_pin of  nn_i : SIGNAL IS  "C1"; -- ADC5/AIN2    (J1- 4)
   ATTRIBUTE chip_pin of  nn_i : SIGNAL IS  "D1"; -- ADC1/AIN3    (J1- 5)
-- ATTRIBUTE chip_pin of ..... : SIGNAL IS  "E3"; -- ADC3/AIN4    (J1- 6)
-- ATTRIBUTE chip_pin of ..... : SIGNAL IS  "F1"; -- ADC7/AIN5    (J1- 7)
-- ATTRIBUTE chip_pin of ..... : SIGNAL IS  "E4"; -- ADC4/AIN6    (J1- 8)
   ATTRIBUTE chip_pin of  nn_i : SIGNAL IS  "H8"; -- D0; Digital  (J1- 9)
   ATTRIBUTE chip_pin of .nn_i : SIGNAL IS "K10"; -- D1; Digital  (J1-10)
-- ATTRIBUTE chip_pin of ..... : SIGNAL IS  "H5"; -- D2; Digital  (J1-11)
-- ATTRIBUTE chip_pin of sdi_i : SIGNAL IS  "H4"; -- D3; Digital  (J1-12)
-- ATTRIBUTE chip_pin of sdv_i : SIGNAL IS  "J1"; -- D4; Digital  (J1-13)
-- ATTRIBUTE chip_pin of stx_i : SIGNAL IS  "J2"; -- D5; Digital  (J1-14)
-- --------------------------------------------------------------------------
-- J2-Side, above right, Pin1 to Pin14, AREF to D5
-- --------------------------------------------------------------------------
-- VCC, 5.0V-Power to the connector  5.0VCC                        (J2-14)
-- VCC, User Power into the MAX1000  3.3VCC                        (J2-13)
-- VCC, 3.3V-Power to the connector  3.3VCC                        (J2-12)
-- GND                               GND                           (J2-11)
-- RESET, "E7", not to be used       RESET  "E7"                   (J2-10)
-- ATTRIBUTE chip_pin of ..... : SIGNAL IS "G12"; -- D14; Digital  (J2- 9)
-- ATTRIBUTE chip_pin of ..... : SIGNAL IS "H13"; -- D13; Digital  (J2- 8)
-- ATTRIBUTE chip_pin of ..... : SIGNAL IS "H10"; -- D12; Digital  (J2- 7)
   ATTRIBUTE chip_pin of ..... : SIGNAL IS "J10"; -- D11; Digital  (J2- 6)
-- ATTRIBUTE chip_pin of ..... : SIGNAL IS "K12"; -- D10; Digital  (J2- 5)
-- ATTRIBUTE chip_pin of ..... : SIGNAL IS "K11"; --  D9; Digital  (J2- 4)
   ATTRIBUTE chip_pin of       : SIGNAL IS "J13"; --  D8; Digital  (J2- 3)
   ATTRIBUTE chip_pin of snd_o : SIGNAL IS "J12"; --  D7; Digital  (J2- 2)
   ATTRIBUTE chip_pin of cw_o  : SIGNAL IS "L12"; --  D6; Digital  (J2- 1)
-- --------------------------------------------------------------------------
-- PMOD-Side, Inputs and Outputs to RS232, using PMOD-Extension
-- --------------------------------------------------------------------------
   ATTRIBUTE chip_pin of tx1_o : SIGNAL IS  "K2"; -- D5; Digital (J6-PIN09)
   ATTRIBUTE chip_pin of rx1_o : SIGNAL IS  "K1"; -- D5; Digital (J6-PIN10)
-- --------------------------------------------------------------------------
```

```
-- -------------------------------------------------------------------------
-- vhdl-2022SS22-QGHDL.tex, FPGA is 10M16SAU169C8G
-- PIN-ASSIGNMENT CAN BE CHANGED ANY TIME
-- -------------------------------------------------------------------------
-- VCC/POWER via USB, ELSE external VCC/POWER via J2,Pin 13
-- -------------------------------------------------------------------------
-- GHDL-cmds:  ghdl -s xxx.vhd; ghdl -a xxx.vhd; ghdl -e xyz
--               syntax, assembly and elaboration (elab not for packages)
-- prep waveform: ghdl -r xxx_TB1 --wave=xxx_TB1_wave.ghw
-- show waveform: gtkwave xxx_TB1_wave.ghw
-- -------------------------------------------------------------------------
-- GHDL,QUARTUS: ATTRIBUTES in ARCHITECTURE;  XYLINX: ATTR in the ENTITY
-- -------------------------------------------------------------------------
-- ATTRIBUTE chip_pin         : string;
-- ATTRIBUTE chip_pin of  rb_i : SIGNAL IS  "E6"; -- SW2_USR_BTN_akt_low;
-- ATTRIBUTE chip_pin of  cp_i : SIGNAL IS  "H6"; -- CLK_12MHz
-- ATTRIBUTE chip_pin of ld1_o : SIGNAL IS  "A8"; -- led1, ld1,..see below
-- ATTRIBUTE chip_pin of ld2_o : SIGNAL IS  "A9"; -- led2, ld2,..see below
-- -------------------------------------------------------------------------
--   rb_i : at SW2_USR_BUTTON,E6 : global reset, active low
--   cp_i : at CLK_12MHz,H6      : local clock, XTAL at 12MHz
-- -------------------------------------------------------------------------
--        12MHz:   H6          +------------------+
--        CLK_EXT: G5          +    --USB--       +   UBtn: E6....rb_s<= rb_i
--                             +    --USB--     o +1  LED1: A8...ld1_o<= rb_s
--                             +    -------      o +2  LED2: A9...ld2_o<=sec_s
--             J4 JTAG         +                 o +3  LED3: A11..ld3_o<=tx1_s
--           +1 GROUND         +                 o +4  LED4: A10..ld4_o.......
--           +2 E5 JTAGEN +                      o +5  LED5: B10..ld5_o.......
--           +3 G2 TCK    +                      o +6  LED6: C9...ld6_o.......
--           +4 F6 TDO    +                      o +7  LED7: C10..ld7_o.......
--           +5 F5 TDI    + 10M16SAU169C8G       o +8  LED8: D8...ld8_o.......
--           +6 G1 TMS    +                        +
--                   J1 + J3            J4  J2
--           D3 AREF  1+ +1 AIN  D2    +1  +14 +5V...................
--  ..........E1 AIN0  2+ +2           +2  +13 VIN-<<<-EXT,USER-POWER
--  .........C2 AIN1  3+ +3 AIN7 B1    +3  +12 +3.3V................
--  .........C1 AIN2  4+                +4  +11 GND..................
--  .........D1 AIN3  5+                +5  +10 RES  E7....DO.NOT.USE.
--  .........E3 AIN4  6+                +6  +9 D14  G12..............
--  .........F1 AIN5  7+                    +8 D13  H13..............
--  .........E4 AIN6  8+                    +7 D12  H10..............
--  .........H8 D0    9+      PMOD          +6 D11  J10..............
--  .........K10 D1  10+ VCC GND-PMOD       +5 D10  K12..............
--  .........H5 D2   11+ : : ....M1-RXD     +4 D9   K11..............
--  .sdi_i....H4 D3  12+ : : : ..M2-TXD     +3 D8   J13..............
--  .sdv_i....J1 D4  13+ : : :|: ....L3     +2 D7   J12...snd_o......
--  .stx_i....J2 D5  14+ : : : : : ..M3     +1 D6   L12...cw_o.......
--                       6 5 4 3 2 1
--                       + + + + + +  J6 PIO_04....PIO_01
--                       + + + + + +     PIO_08....PIO_05
--                       1 1 1 9 8 7
--                       2 1 0 . . .N3
--                     VCC... . . . ...N2
--                 GND-PMOD..... . .....K2-TXD...at J6,Pin09, RS232-txd_o
--                               .......K1-RXD.....at J6,Pin10, RS232-rxd_i
-- -------------------------------------------------------------------------
-- Chk: Is "B11" hard-wired to J10 at J2-6? Check that!
-- Chk: Is "G13" hard-wired to H10 at J2-7? Check that!
-- Chk: ATTRIBUTE chip_pin of PIN_B11_R: SIGNAL IS "B11";B11_R;Pup IN(J2-6)
-- Chk: ATTRIBUTE chip_pin of PIN_G13_R: SIGNAL IS "G13";G13_R;Pup IN(J2-7)
-- -------------------------------------------------------------------------
```