Morse Code Generator Requirements

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Requirement	Importance	Verifiable	Description	Remarks
Top Level of FPGA	-	-	-	-
Reset Signal	High	Yes	System Reset	-
Clock Signal	High	Yes	System Clock	-
Rxd_i Signal	High	Yes	Serial Input as ASCII data	-
Snd_o Signal	Medium	Partially	1Khz Sound Output	-
cw_o Signal	Medium	Partially	Blinking Led as Morse Code	-
txd_o Signal	High	Yes	ASCII format of Morse Code	Sends to PC
utx Component	**High**	**Yes**	**Data Transmission via UART**	-
Reset Signal	High	Yes	System Reset	-
Clock Signal	High	Yes	System Clock	-
d_s Signal	High	Yes	UART data receive	-
dv_s Signal	High	Yes	Validate UART data	-
txd_o Signal	High	Yes	ASCII format of Morse Code	Sends to PC
urx Component	**High**	**Yes**	**Data Reception via UART**	-
Reset Signal	High	Yes	System Reset	-
Clock Signal	High	Yes	System Clock	-
Rxd_i Signal	High	Partially	Serial Input as ASCII data	-
d_s Signal	High	Yes	UART data receive	-
dv_s Signal	High	Yes	Validate UART data	-

Table 1: Requirements

Requirement	Importance	Verifiable	Description	Remarks
cw4 Component	**High**	**Yes**	**Morse Code Generation**	-
Reset Signal	High	Yes	System Reset	-
Clock Signal	High	Yes	System Clock	-
d_s Signal	High	Yes	UART data receive	-
dv_s Signal	High	Yes	Validate UART data	-
Snd_o Signal	Medium	Partially	1Khz Sound Output	-
cw_o Signal	Medium	Partially	Blinking Led as Morse Code	-

Table 2: Requirements