Prithvish Vijaykumar Nembhani

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Academic Qualifications

Delft University of Technology — **Delft, Netherlands**
Master of Science in Computer Engineering GPA: 7/10 — *September 2020 - February 2023*

VIT University, Chennai Campus — **Chennai, India**
Bachelors in Electronics and Communication Engineering GPA: 8.51/10 — *July 2013 - June 2017*

Work Experience

Barcelona Supercomputing Center — **Barcelona - Spain**
Research Engineer 3 (Senior Research Engineer) — *September, 2023 - January 2024*

- Worked on designing a software hardware (PS-PL) framework with Zynq ultra-scale MPSoC and accelerated algorithms for a microsatellite.
- Reviewed papers for the DATE conference 2024 on computer architecture and EDA tools. Gave appropriate feedback to improve on these papers.
- Worked on pipelining kernels of the algorithm with no data dependency with Dynamic function exchange and Partial dynamic reconfiguration features offered by the Zynq Ultrascale+.
- Resolved bugs on the kernel, rootfs, drivers, device tree, deployed and tested openmp, fpga manager and utils on petalinux builds.
- Setup the MPSoC available across VPN by setting it up on the existing networking infrastructure at BSC enabling remote deployment, orchestration, build over tftp and debugging (over ethernet and Serial connections).
- Xilinx UltraScale MPSOC, Vitis & Vivado Development, PetaLinux, SDSoC & SDAccel Xilinx development, device tree configuration, Arm Cortex A53, Arm cortex R5, Kernel & rootfs build

Arista Networks — **Bangalore - India**
Technical Solution Engineer — *July 2017 - Aug 2020*

- Expanding upon the basics of routing and switching, got a chance to work on a variety of advanced technologies such as EVPN, Vxlan, GRE, IPSEC, MPLS, ISIS, PTP, Docker Products, VMware Products, etc as a Network Engineer.
- Provided solutions to various multi-vendor problems to a variety of customers ranging from cloud giants such as Facebook, and Microsoft; Trading firms like Tower research, NYSE, etc to ISPs where Arista devices are in place from the APAC and EMEA regions.
- Adapting to an organization's knowledge-sharing culture, inculcated and developed qualities such as teamwork, communicating tactically, presenting, and addressing wider audiences as a whole.
- Gained insight into several merchant silicon chips manufactured by Intel, Broadcom, etc., and proprietary architecture design of the Arista switches.

Internships

Interuniversity Microelectronics Center — **Eindhoven, Netherlands**
Master Thesis Intern — *Dec 2021 – Nov 2022*

- Worked on designing a tool for efficient mapping of spiking neural networks on a neuromorphic chip. (SENeCA).
- Compared the tool with the existing solution and improved the time to solution for the tool from 30 days to 3 hours for large-scale SNNs being mapped onto to neuromorphic chip with architectural parameters of a flexible chip in the synthesis loop.
- Compared several meta-heuristic, optimization algorithms for single and multi-objective optimization on use case, time to solution and convergence parameters.
- Fixed bugs and compared the existing simulator SENSIM (for SENeCA) with other software simulators and tools by academia and industry and published papers which were accepted at the HiPEAC conference Europe (NeuroEdge) January 2024 and IJCNN (IEEE WCCI) Japan 2024.
- In parallel, gained knowledge and skills in hardware modeling, event-based simulator design, mapper design, spiking neural networks, quantization, neuromorphic hardware, asynchronous system design, benchmarking, software architecture design, single and multi-objective optimization, and algorithms, neuromorphic architectures such as Loihi1/2, Truenorth, SpiNNaker1/2, Brainchip Akida, software tools like the Lava framework, BlindsNET, NEURON, etc.
- The work is in collaboration with the neuromorphic team at IMEC (Eindhoven) for the European projects TEMPO and ANDANTE.

Delft University of Technology — **Delft, Netherlands**
Mentor — *Aug 2021 – Jan 2022*

- Mentored the computer engineering and embedded systems batch 2021-2023 with the selection of courses in computer engineering, machine learning, systems and control, networking and robotics.
- Hosted Barbeques and beer parties to make sure all the 2021 batch would mingle with each other apart from courses.

Philips — **Eindhoven, BEST, Netherlands**
Intern — *July 2021 – Oct 2021*

- The aspects of the internship covered the modeling of hardware from the X-RAY back-end systems using machine learning.
- The project/internship was supported by the Vivaldy EU project

Arista Networks **Bangalore - India**

Technical Solutions Engineer Intern *Jan 2017 – Jul 2017*

- The Internship covered the basics of the PHY layer, the L2 protocols (STP, PVSTP, RSTP, LACP, LLDP) etc; L3 protocols such as (BGP, OSPF) and other networking protocols and technologies such as NAT, BFD, TAP-Agg, QoS, etc.
- Other aspects involved basic network design and troubleshooting and a final Industrial Project-Dynamic Detection of DDoS in a distributed data center.

LNMIIT Summer Research Internship **Jaipur - India**

Research Intern *May 2016 – July 2016*

- Incorporated game theory along with various positioning strategies of wireless stations, followed by analyzing and evaluating the models in terms of signal-to-noise ratio using MATLAB with the aim of devising a novel optimal design.
- In addition to game theory approaches, various geometric models were analyzed in depth and simulated in MATLAB to obtain the best possible antenna that places the model in a region. In the study, parameters such as antenna patterns and 3-dimensional surface were assumed to be constant

Phynart Technologies **Pune - India**

Development Intern *Dec 2015 – Jan 2016*

- Developed a module to automate the process of connecting the UFO hub to the home network in its initial setup, which involved primarily dealing with USB-based Realtek and Mediatek Wireless adapters and its drivers.
- Other aspects involved interfacing with BBB, RTC modules code debugging, cross-compilation, etc.

Edubotix Innovation Lab **Ahmedabad - India**

Trainee *Jun 2014 – Jul 2014*

- Worked with ATMEL microcontroller and AVR- embedded C, followed by interface and calibration of various sensory modules such as IR, ultrasonic GSM, GPS, RF, and Bluetooth etc.
- Contributed to ongoing industrial projects like programming a small Bi-ped robot and GPS module on multi-terrain robots.

Publication

An IoT-Based Smart Shopping Cart Using the Contemporary Barcode Scanner, Intelligent embedded systems, Volume II - Springer LNEE, Published on 17th February 2018, Authors: Prithvish V. N., Shraddha Agrawal, Prof. John Sahaya Rani Alex

SENSIM: An Event-driven Parallel Simulator for Multi-core Neuromorphic Systems HiPEAC Neuroedge, IEEE CIS World conference, Japan, 2024 (accepted, yet to present) VLink

Efficient Mapping of Large Scale Spiking Neural Networks and Rate based DNN on a neuromorphic chip TU Delft Repository, Prithvish V. N.

Optimizing Event-Based Neural Networks on Digital Neuromorphic Architecture: A Comprehensive Design Space Exploration Frontiers of neuroscience, IMEC-NL team

Technical skills

- **Operating Systems** Linux (ubuntu, Debian, fedora, Redhat, petalinux, yocto), RTOS (FreeRTOS), Windows, Mac-OS
- **Programming** C, C++ , python, MATLAB, Shell, tcl, VHDL, systemC
- **Tools** LTspice, NI-Labview, and Signal express, Wireshark, scapy, Cadence-virtuoso, Xilinx-Vivado, Xilinx-Vitis, Xilinx-SDSoC, Xilinx-SDAccel, Eagle,
- **Hardware Boards** BeagleBone Black, Xilinx ZYNQ boards, Arduino series, MSP430, TIVA C series, NI DAQ, NI myRIO, Arista (switches and routers)
- **Data center Networking Protocols** EVPN, VxLAN, MPLS, MP-BGP, OSPF, LDP, ISIS, SR, PTP, STP, RSVP, DHCP, IPSEC, BGP, OSPF, TCP/IP stack, UDP, MLAG, VARP, STP.
- **Hardware communication protocols/standards** UART, RS232, AXI4, SPI, I2C, CAN (in theory), PCIe (in theory), Ethernet (in theory).
- **Hardware Technologies** Analog/digital mixed signal circuit design (Digital FIR, IIR filters, Class A-D amplifier / invertor designs), OpenMP, OpenCl, AVX, CUDA, GPUs, TPUs, NPUs,Amdals law, Roofline model, hardware verification, DFT (BoundryScan, JTAG, PUFs, hardware attacks (Rawhammer etc, power trace analysis)), Device tree configuration, Kernel configuration, Rootfs configuration, BIOS configurations, petalinux
- **RTOS and embedded** scheduling , mutex, semaphores, mutex, queueing theory, petrinets, markov chains, jitter analysis, feasibility analysis etc
- **Artificial intelligence and algorithmics** pytorch, tensorflow, keras, scikit, Machine learning (linear regression, logistic regression, SVM, Decision Tree, Random forest, clustering, PCM, feature reduction, Bayes algorithm,), Deep learning (CNN, RNN, DNN, Autoencoder, GNN, GANs, Advarserial machine learning, transfer learning, SNN, LSTM, GRUs, Transformer models, federated learning), graph theory (Kernighan–Lin, clique partitioning algorithm)
- **Optimization** Linear Programming, Quadratic Programming, convex optimization, non-linear optimization, constraint, meta-heuristics, evolutionary algorithms, Genetic Algorithm, Biased Random Key Genetic Algorithm, Non-Dominant Sorting genetic

algorithm, Adaptive geometry estimated based MOEA, No free lunch theorem, Stochastic Ranking Evolutionary Strategy etc.
- **Software defined networking** Docker, Kubernetes, cloud-platforms (GCP, ,AWS), Graphana, telemetry, ansible, VMware (NSX, hypervisors, Vsphere), OpenStack, P4 programming,
- **miscellaneous** Research, Git, LaTex, troubleshooting, debugging, leadership, planning, skills,

Awards and Achievements

- Springer Best Paper Presentation Award for an IoT-Based Smart Shopping Cart Using the Contemporary Barcode Scanner. (Cash prize - 150 euros) Plink
- MindSwitch was recognized among the top 10 academic projects nationwide in NIYANTRA-2016 VLink Vlink
- DMD4DMD got well recognized by RESNA for a project in the category of emerging technologies Link
- Was a part of Team Technocrats which stood 23^{rd} in ABU Robocon-2015 Link

Current Projects

REEaLity: REELS to Reality

- In a world where endless scrolling through reels has become a new addiction for many, I want to reignite a passion for reading old school books. PS: I dont want my kids to grow in a generation which does not read.
- The goal of the project is to spark curiosity about books and papers, encouraging people to rediscover the joy and depth of reading by means of reels and reduce the social media usage. Something like the Ted-Ed
- Some Links MobileLLM • text-2-video Huggingface • vision-transformers

BED-MED

- Insomnia can affect anyone. While screen time did not originally cause insomnia, increased stress and anxiety levels, lifestyle factors, and even rare occurrences in children can contribute to it.
- Although methods like melatonin consumption are available to treat insomnia, this project aims to generate audio (with soothing sounds and waves tuned to a frequency that promotes sleep, adapting to your activities during bed time) as a natural remedy.
- While tools like Audacity and KukuFM exist, this solution will offer a superior experience tailored specifically for sleep improvement.

Masters Projects

Optimizing the Ethereal Engine - Ethereal Matter Inc.

- This project focused on improving the robotic armatures of a novel fitness platform that combines virtual reality (VR) with physical exercise. The goal was to enhance the user's experience by addressing limitations in the existing prototype.
- My primary focus in the interdisciplinary team was to optimize the power by choosing better motor driving technology and improve upon motion capture technology to create a more immersive and engaging VR fitness experience

Flight control software for a Quadrupel

- The project developed flight control software for a Quadrupel (QR) drone, from manual joystick control to automatic stabilization using cascaded P control.
- The software was rigorously tested and optimized for hardware discrepancies, achieving control goals, with potential for improved robustness in future iterations.

High-Performance Low power Binary Neural Networks for MNIST Classification: From Software to ASIC

- The project designed a Binary Neural Network (BNN) for image classification on the MNIST dataset, highlighting its efficiency for edge computing.
- The BNN hardware implementation, simulated using GENUS, achieved a 358 MHz operating frequency, significantly outperforming GPU software inference.

Low Power MIPS Processor

- This project aims to enhance the performance metrics of a MIPS architecture processor, focusing on reducing energy consumption while maintaining performance. Modifications include optimizing the cache hierarchy, implementing a radix-4 multiplier, and incorporating a prefix adder.
- Design space exploration led to a configuration saving 3.2 Joules and reducing cycles by 2.8 million, resulting in a final processor capable of running benchmarks in 4948 million cycles with only 7.59 Joules.

Deep Orchards - Reproducibility Project

- This project aims to reproduce a research paper by integrating the Deep Orchards dataset with the Faster RCNN network, enhancing understanding and practical skills in deep learning.
- The project provides insights into applying deep learning techniques, highlighting steps for integrating datasets and implementing complex neural network architectures like Faster RCNN.

Real-time Execution of a Multiprocessing System - A Survey

- This survey examines RTEMS, an open-source RTOS, highlighting its support for 18 processor architectures, various scheduling frameworks, and numerous APIs.
- RTEMS's versatility and comprehensive feature set make it suitable for space flight, medical, networking, and other embedded applications.

Optimization and Overhead Analysis of Real-Time Systems Using Earliest Deadline First Scheduling

- The project explores the impact of system overhead in real-time systems using the EDF scheduling algorithm, analyzing the effects of task parameters on overhead.
- Findings show that shorter periods increase overhead, with plots demonstrating the correlation between task frequency and system performance.

Comparative Analysis of Real-Time Scheduling Policies: FIFO, RR, and DEADLINE

- This analysis compares the performance of FIFO, RR, and DEADLINE scheduling policies, focusing on periodic tasks with varying priorities.
- The study reveals the strengths and limitations of each policy, providing insights into their impact on system overhead and real-time performance.

Optimized Scheduling and Resource Binding for Digital Filters

- The project evaluates various scheduling algorithms, such as ALAP and Force Directed Scheduling, in digital system design, using MATLAB simulations.
- It emphasizes trade-offs in clock period minimization and resource utilization, validating findings through VHDL testbenches and ModelSim simulations.

Comparing Caching Methodologies for Multiprocessor Systems - A Survey

- This survey compares three caching methodologies—Cooperative Caching (CC), Distributed Cooperative Caching (DCC), and Adaptive Set-Granular Cooperative Caching (ASCC)—for Chip Multiprocessors (CMPs).
- The study evaluates each methodology's performance using SPEC benchmarks, focusing on off-chip misses, network latency, and overall performance improvement.

Optimizating of scientific benchmarks on VLIW/VEX Architectures on a simulating platform & FPGA

- This project analyzes matrix multiplication and 7x7 convolution benchmarks in scientific domains, focusing on optimizing performance while considering resource utilization.
- The report details the process of finding optimal VEX architecture configurations on an FPGA, presenting results across low-power embedded systems, high-performance scientific applications, and balanced solutions for performance, energy efficiency, and area utilization.

Accelerating algorithms with SSE/AVX/AVX2, OpenMP, OpenCL, CUDA

- This project focuses on accelerating and optimizing single-precision and double-precision matrix multiplication, image processing algorithms (histogram, ripple effect, contrast enhancement, gaussian bluring), CNN using Intel SSE/AVX/AVX2, OpenMP, OpenCL, CUDA on multi-core processor systems.
- Observations and benchmarks compare performance against native baseline, profiling, arithmetic intensity estimation, bottleneck estimation, developing custom kernels analyzing the effectiveness of each computational technique etc.

Discrete Time State Space Model Optimization for a Traffic Network - Nonlinear Optimization

- The project optimizes an urban traffic network using nonlinear programming, focusing on discrete-time state-space models and optimizing green time lengths for traffic signals.
- Key findings include the identification of output link capacity constraints and consistent total time spent in the system (TTS) across different scenarios, demonstrating effective optimization of traffic flow.

Optimization of a Cooling System - Linear and Quadratic Programming

- This project optimizes air conditioning units using linear and quadratic programming techniques, aiming to maximize power under budget and space constraints while ensuring thermal comfort and energy efficiency.
- The project covers parameter identification, discrete model formulation, and quadratic cost function minimization using MATLAB, highlighting practical applications in engineering scenarios.

Starliner Mission Model in mCRL2

- This project focuses on modeling the launch segment of the Starliner Mission using mCRL2, with four independent controllers—Flight Controller (FC), Booster Module Controller (BMC), Launch Module Controller (LMC), and Orbital Module Controller (OMC).
- The model simulates events from ground launch to detachment of the Service and Crew Modules (SCM) from the Orbital Module (OM), validating system behavior and interactions between controllers.

Undergrad Projects

MindSwitch

- Mindswitch came out as an EEG based wearable device for controlling various electronic appliances in the surrounding using visually evoked EEG signals acquired from the occipital lobe with the purpose was to help to ease day-to-day life for the differently-abled.
- Initial research work was carried out with tools using NI LabView, NI signal express, MATLAB, followed by deploying the wearable tool on myRIO. The process involved implementing various Machine learning models on NI-myRIO.

DMD4DMD

- A Prototype of an IoT based wearable medical device that aims at making a global repository of DMD patients' data to accelerate the research for its cure as well as to assist the patient for its physiotherapy treatment.
- Explored Machine learning and various feature extraction techniques, analysed EMG signals via NI DAQ, developed customized signal conditioning circuits, used Beagle bone black ADC to collect data and sent it to the Parse cloud.

Badminton playing Robots

- A pair of Robots made specifically for the ABU Robocon 2016 guided by the rules and problem statement and design specifications provided by ABU Robocon in the year 2015 by a collective group of Robotics enthusiasts named Technocrats.
- As a member of Technocrats, worked in an interdisciplinary environment along with fellow enthusiasts from the mechanical and computer science department, majorly contributing to the electronics and electrical division.
- Tasks involved motor calculations and acquisition, sensor development, calibration or acquisition, simulations on MATLAB and interfacing, wireless Bluetooth modules with Arduino Mega.

Multimodal person identification system- Bachelor Thesis

- The project consisted of the identification of an individual through the combination of three biometrics - face, voice, and fingerprint.
- The initial stages involved evaluating the pros and cons of all the available approaches in the field, selecting the most optimum approach followed by custom dataset creation and development of a final model diffusing the scores from each biometric based on its reliability.
- Worked on algorithms such as MFCC, HMM, ORB descriptors, Harris corner detector etc.

Finger gesture Locking system

- A door lock system that unlocks with a series of finger gestures by means of a Laser-LDR sensory grid.
- The circuitry for the magnetized door lock & laser-LDR grid was integrated with BeagleBone black which also hosted a wireless network by means of a Wireless adapter giving the users to connect by means of a custom android app as a fail-safe mechanism.

Voice conversion

- A research initiative taken to primarily understand speech signals, and analyze and apply different voice conversion techniques to convert one individual's voice into another (implemented in MATLAB) while focussing on reducing the computational complexity and improving the naturalness of the converted voice.
- Explored several techniques and features used in the past for the same like Quefrency and Cepstrum analysis.

Channel encoding and decoding

- A Project implementing convolutional encoding and Viterbi decoding on MATLAB as well as on FPGA and also evaluating its efficiency by introducing different bit errors.
- While pursuing the project got a chance to work on FPGA programming languages like VHDL for programming the Xilinx FPGAs.

Dynamic modeling and simulating a PLL system in MATLAB and Simulink

- This project focused on understanding different blocks of a PLL system and designing a PLL system in MATLAB using the different transfer functions for each block.
- Further, the simulation was done on Simulink understanding different parameters of a PLL block.
- In the process, got the chance to explore several toolboxes in matlab like Partial differential toolbox toolbox and simulating several control system concepts in matlab by writing custom codes.

Secret sharing of an image

- Implemented the partially modified Adi-Shamir secret number sharing algorithm to encrypt images using MATLAB.
- In the process, got a chance to learn various algorithms in the field of applied numerical mathematics

Inverter for the Google Little Box Challenge

- The purpose was to design an inverter with more than 90 percent efficiency to fit in the specifications of Google Little Box Challenge.
- The idea was to design a sine wave inverter that works on tri-level PWM and class D amplifier.
- In the process, got a chance to learn class A, B, AB, C,D amplifier design and applications of operational amplifiers

Audio spectrum analyzer

- An operational amplifiers based circuitry which divides the audio spectrum in 3 bands and displays it on a scaling metric made of LEDs. The same was then extended to display patterns on an LED cube with music.
- Working on the project got a chance to explore applications of operational amplifiers and various parameters one needs to take care of when designing analog circuits like slew rate, gain bw and op-amp constants for different IC's

Horn Antenna Design

- This project simulates a pyramidal horn antenna for communication purposes at 10 GHz using HFSS software.
- Analysis includes 3D radiation pattern, impedance, gain vs. frequency, directivity, and key antenna parameters.

Band-Pass Filter Design for Microwave Frequency

- This project designs a compact microwave band-pass filter (BPF) using a parallel edge coupled line structure with HFSS with a center frequency of 2.48 GHz, 10% fractional bandwidth, and a Chebyshev response.
- It utilizes four parallel coupled line pairs on an FR4 substrate and optimizes dimensions for desired performance.

Copy Cat Robot

- A pair of robots made where one was supposed to follow a line the other was supposed to imitate the same.
- Worked on TI's MSP430 and Wireless booster pack.

Electromagnetic Scrap Separator

- The objective was to separate heavy iron objects with the lighter ones. The implementation consisted of an electromagnet (made by rotating wire on an iron screw) interfaced with Arduino along with Darlington transistor (for current amplification).
- The process got a chance to understand various laws in electromagnets practically like Ampere's law; producing a magnetic field when current flows.

Automated shed for Segway

- A prototype of an automated shed that folds and unfolds on seasonal changes like rainfall, scorching sun etc.
- The project being one of my early ECE projects understood various applications of passive components like capacitor resistor basic IC's, reading Data-sheets and dealing with problems while integrating various circuits like the common ground problem.

Scrabble

- A multiplayer LAN game made in C which emulates the famous board game scrable primarily taken as a project to explore GUI and socket programming libraries in C.

Hobbies & Extracurricular activities

- Was a part of Dance and drama stage shows at Arista Fiesta, in 2018 & 2019
- An avid reader (SciFi, Bipics, Research Papers, Tech blogs, Reddit), a decent Swimmer, an ice/skater, a moderately skilled dancer - bhangra, salsa, bachata, kizomba, an incredible host and party igniter, a bathroom singer (not even close to singers in my family)
- Ardent Passion for Music (Classical Indian, Indi blues, Bollywood, pop, rock, EDM) and traveling
- A home-grown part-time Indian chef known for his butter chicken, coconut chicken, shahi paneer, chats, and grilled chicken in Europe.
- Occasionally would play badminton and football.

Master's Coursework

Courses	Description
Advanced Computing Systems	○ Basics of Compute System design and software paradigms associated with it. ○ Accelerators, interconnect, memory subsystem, compute subsystem, GPU, CPU, FPGA, CUDA, OpenCL, OpenMP, AVX. ○ Roofline model, Amdahls Law, Bottlenecks, back of the envelope calculations, arithmetic intensity estimation, sparse, dense matrix compute estimation, GPU architectures (Kepler, Ampere, volta, turing), Multicore, multiprocessor, shared memory and resource handling, Simultaneous multithreading, Base core equivalent estimation for heterogeneous systems, Dark silicon and Amdhals law for multi-core era, synchronisation, contention & coherency,
System Validation	○ Validating complex embedded systems with Labelled transition system mythology, process algebra, abstract data types, model checking with the modal mu-calculus, and model-based testing. ○ Programming and validation in mCRL2. As an academic project programmed the stages of a Starliner mission such as lift-off, Booster Separation, stage separation, payload fairing jettison & Payload Deployment in mCRL2.
Methods and Algorithm for System Design	○ Algorithms for optimal digital system designs. ○ Improved and optimized the design for several filters like the IIR, FIR, elliptical filter and extracted in the form of a Directed Acyclic graph. ○ Retiming, VHDL code generation, Dot language domain specific langauge, graphviz, pareto optimality, scheduling, resource binding, clique partitioning, ALAP, force directed graph, graph theory.
Modern Computer Architecture	○ Familiar with the design process for modern computing systems and architecture. ○ Instruction set architectures, pipelining and pipelining consequences, multiple-issue (superscalar and VLIW) processors, multimedia SIMD extensions, out-of-order execution, branch prediction, speculative execution, advanced memory hierarchies, pre-fetching, multithreaded processors and multiprocessors, energy consumption, and reliability. ○ Modeling, profiling, caching scheme, associativity, design of experiments, pipelining, benchmarking, Hazards (RAW, WAR etc), Distributed memory hierarchy.
Re-configurable computing	○ Understood the working of FPGA in detail as emulation and accelerating devices. ○ Vivado HLS, Vitis HLS, HLx, IP generation. ○ Accelerated a Canny edge algorithm on the FPGA, verified with MATLAB and python execution and estimated the speed up. ○ Estimated the amount of digital resources used on the FPGA, BRAM, FF, LUT, DSP. ○ Improved the design further with CORDIC algorithm and quantization techniques to reduce the utilization of DSP.

Hardware dependability	○ Verification, validation and secure design of digital electronics. ○ Verification of clocked circuits in an optimized manner, static timing analysis. ○ Designing optimal test patterns (test pattern generation) for verification of clocked circuits. ○ Boundary scans, JTAG, Physical Unclonable device, hardware attacks, Analysing power traces & data analytics, hardware attacks, fault injection & mitigation, block ciphers HW implementation.
Systems engineering & Profile and orientation	○ Designing larger complex digital systems and validation, meeting requirements, etc. ○ Problem Formulation, Requirements specification, Use case model, Functional Decomposition, Means and Morphological Analysis, Decision Making, Simulation and modeling, Risk Analysis, Testing ○ Scientific writing, oral paper presentations, paper reviews.
Hardware Architectures for AI	○ Worked on upcoming new architectures for Artificial design (TPU, GPU, NPU, etc.). ○ Designing a Binarized neural network ASIC and measuring power, timing area verification of ASICs. Tools used TensorflowRT, Xilinx Vivado ○ Benchmarking algorithms on a GPU, TPU, CPU. ○ Spike Time Dependent Plasticity training algorithms, Spiking Neural Networks, Crossbars, Memristers, Phase change memories, SpiNNaker1/2, Lohi1/2, Truenorth, Akida, Neuogrid
Processor Design Project	○ Improved the design of a MIPS processor by improving the design of the adder, multiplier and caching design policy for a low-power MIPS processor. ○ ISA manipulation, compiler manipulation, benchmarking, clocking in processors, hybrid Brunt kung, dadda and wallace. ○ VHDL, data analytics, design of experiments, MIPS cross-compiler, MiBench suites, GMP-bench suits.
Real-time systems	○ Worked on the kernel for real-time systems, schedulers, feasibility analysis, jitter analysis, Rate monotonic, Multiple tasks/jobs handling, preemptive, non-preemptive kernel concepts. ○ Jackson, horn, Rate-Monotonic, Earliest deadline first w/o constraints, deadline monotonic, ○ Server concepts(Background Scheduling, Polling Server, Deferrable Server, Priority Exchange, Sporadic Server, Slack Stealing). ○ Dynamic Priority Servers (Exchange Server, Sporadic Server, Total Bandwidth Server, Earliest Deadline Late Server, Improved Priority Exchange Server, Improved TBS, Constant Bandwidth Server (CBS), ○ Resource Access Protocols, Non-Preemptive Protocol, Highest Locker Priority Protocol, Priority Inheritance Protocol, Priority Ceiling Protocol, Stack Resource Policy
Joint interdisciplinary project Ethereal matter	○ Worked on redesigning the full-body motion capture for the ethereal engine. ○ Worked on optimizing the power consumption of motors used in the ethereal engine. ○ Unity, inverse kinematics, UX design, Human-Robot Interaction, Presentation skills. ○ Teamwork, partying in Netherlands, planning trips in Europe, learned how to cook Italian food (carbonara). Taught everyone the culinary skills to master butter chicken, stayed with an Italian family.
Embedded-Systems Design	○ Designed embedded software for hard real-time systems (drones) under significant constraints. ○ Control theory, filtering, Kalman filters, queuing theory, bare metal programming, Petri nets, design of experiments, Markov chains, etc.

Deep Learning

- Designing Deep learning algorithms, convolutional neural networks, deep neural networks.
- LSTMs, GRUs, GANs, Autoencoders, Recurrent neural networks, Self-organizing maps, network compression, regularization, Transformer models, Transfer learning, Federated learning,
- Worked on reproducing results for 2 papers in pytorch keras.

Machine learning

- Supervised, unsupervised, reinforcement learning, identifying data and the problem type, early data analytics.
- Regression methods (Linear and Logistic), least squares fitting, Overfitting, cross-validation, regularization, labeling data, outliers, High-dimensional data, data augmentation, Hyper-parameter optimization (grid search vs random search)
- Parametric vs Non-parametric classifiers, KNN , Classification, gradient descent and optimization, Support vector machines, Principle component analysis, feature reduction techniques, Local linear embeddings, Random forest and ensemble methods, Gaussian mixture model.
- Python Numpy, pandas, matplotlib, Scikit, PyTorch, Keras, sklearn

Computer Arithmetic

- Learned how optimized mathematical operations are designed in a computing system.
- Radix change operations, number theory, dada & wallace tree, burt kung, carry-lookahead adders, array and tree multipliers, square rooting, division, PD plots, estimating every design in terms of area, power, and timing, Cordic algorithm.

Audit courses Digital IC Design 1 • Optimisation for System and control • Embedded Software • System design with HDL • Quantum Architectures • Fundamentals of quantum information • Quantu Hardware 1 • Introduction to quantum coputing • Quantum Algorithms