VLSI Lab Report Assignment 1

BCSE 4th Year 2nd Semester

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*Submission Date : **13th March 2021***

1. Description

Write VHDL code for two binary inputs ***a*** and ***b*** which outputs a bus of an 8-bit, ***c*** where each bit represents the following:

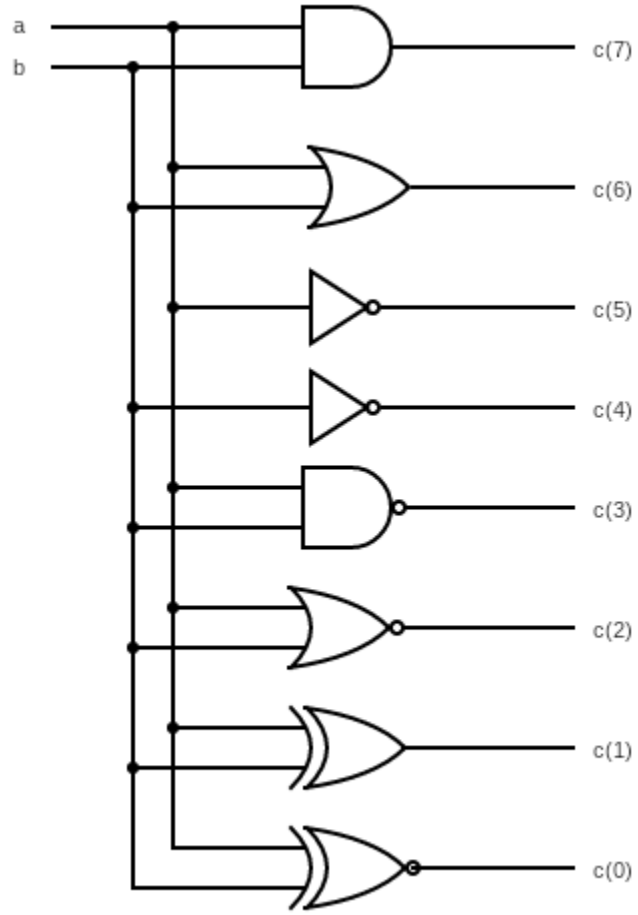
Bit	Represents
7	c(7) => a **AND** b
6	c(6) => a **OR** b
5	c(5) => **NOT** a
4	c(4) => **NOT** b
3	c(3) => a **NAND** b
2	c(2) => a **NOR** b
1	c(1) => a **XOR** b
0	c(0) => a **XNOR** b

Also, verify the result by using testbench and plot the timing diagram.

2. Entity

Inputs: a, b
Output: c

3. Logic Gate



4. Truth Table

Input		*Output*								
a	**b**	**c**								**c[7:0]**
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
0	0	0	0	1	1	1	1	0	1	00111101
0	1	0	1	1	0	1	0	1	0	01101010
1	0	0	1	0	1	1	0	1	0	01011010
1	1	1	1	0	0	0	0	0	1	11000001

5. Architecture

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    18:20:17 03/10/2021
-- Design Name:
-- Module Name:    Logic_Gates - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Logic_Gates is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC_VECTOR (7 downto 0));
end Logic_Gates;

architecture Behavioral of Logic_Gates is

begin
        c(7) <= a and b;
        c(6) <= a or b;
        c(5) <= not a;
        c(4) <= not b;
        c(3) <= a nand b;
        c(2) <= a nor b;
        c(1) <= a xor b;
        c(0) <= a xnor b;
end Behavioral;
```

6. Test Bench

```
--------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:   18:33:44 03/10/2021
-- Design Name:
-- Module Name:   /mnt/e/JU/8/VLSI/Lab/Code/Assignment1/Logic_Gates_Test_Bench.vhd
-- Project Name:  Assignment1
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: Logic_Gates
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test.  Xilinx recommends
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
--------------------------------------------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY Logic_Gates_Test_Bench IS
END Logic_Gates_Test_Bench;

ARCHITECTURE behavior OF Logic_Gates_Test_Bench IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT Logic_Gates
    PORT(
         a : IN  std_logic;
         b : IN  std_logic;
         c : OUT  std_logic_vector(7 downto 0)
        );
    END COMPONENT;
```

```
    --Inputs
    signal aa : std_logic := '0';
    signal bb : std_logic := '0';

         --Outputs
    signal cc : std_logic_vector(7 downto 0);
    -- No clocks detected in port list. Replace <clock> below with
    -- appropriate port name

BEGIN

         -- Instantiate the Unit Under Test (UUT)
    uut: Logic_Gates PORT MAP (
           a => aa,
           b => bb,
           c => cc
         );

    -- Stimulus process
    stim_proc: process
    begin
                  aa <= '0';
                  bb <= '0';
                  wait for 1 ps;

                  aa <= '0';
                  bb <= '1';
                  wait for 1 ps;

                  aa <= '1';
                  bb <= '0';
                  wait for 1 ps;

                  aa <= '1';
                  bb <= '1';
                  wait for 1 ps;
    end process;

END;
```

7. Timing Diagram