VLSI Lab Report
Assignment 3 Annexure 1

BCSE 4th Year 2nd Semester

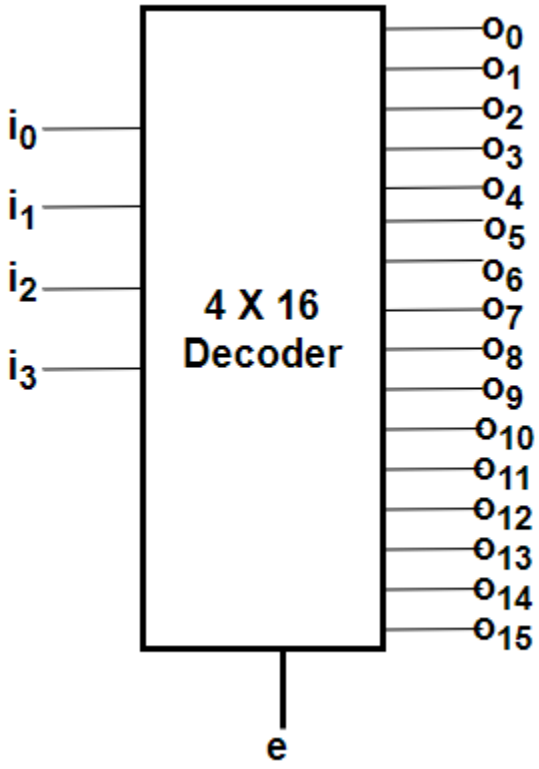
Name: ***Priti Shaw***
Roll No. : ***001710501076***
Batch: ***A3***

1. Description

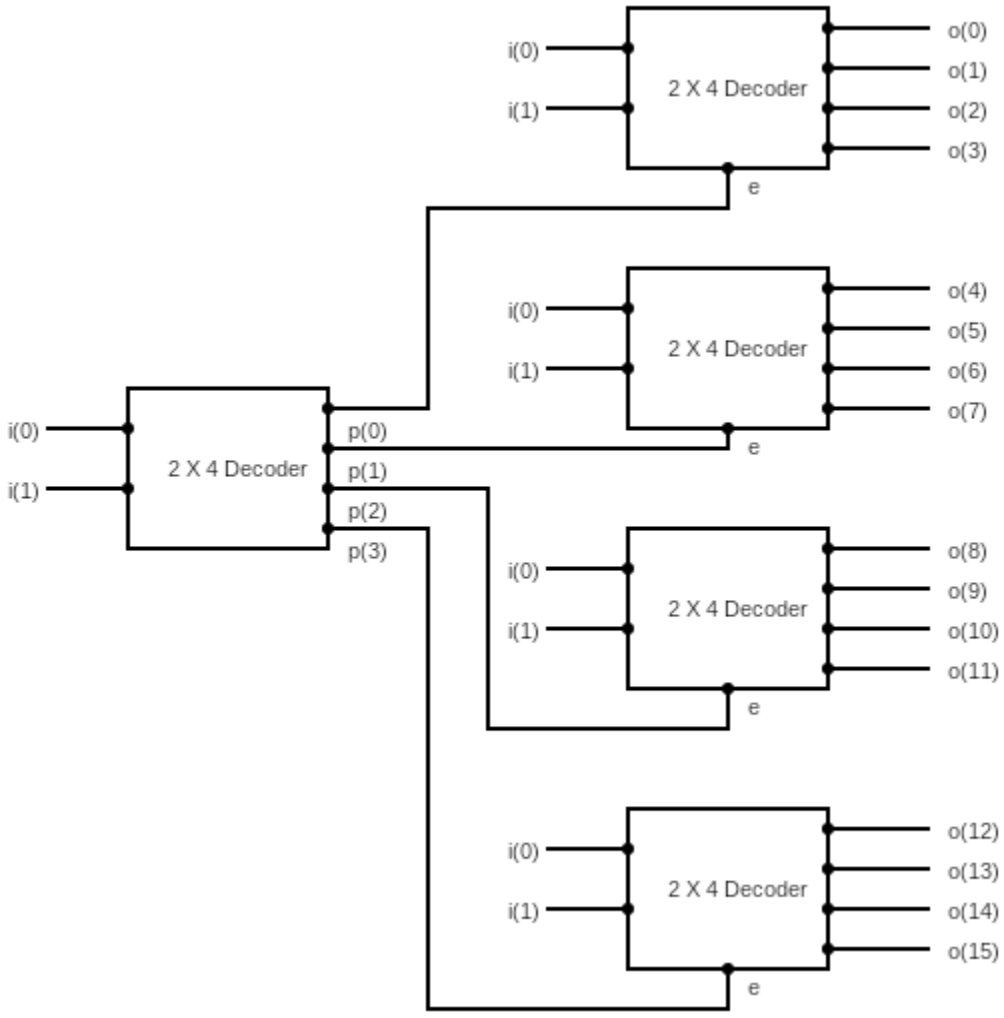
Design 4 X 16 decoder using 2 X 4 decoders using generate statement. Write a test bench using a behavioral statement.

A decoder is a combinational circuit that has N input lines and a maximum of 2^N output lines. One of these outputs will be active high based on the combination of inputs present when the decoder is enabled. That means the decoder detects a particular code. A 4 to 16 decoder has 4 input lines and 16 output lines. An enable input is provided to switch the decoder on and off.

2. Block Diagram



3. Circuit Diagram



4. Entity

```
entity Annexure1 is
    Port ( enable : in  STD_LOGIC;
           input : in  STD_LOGIC_VECTOR (3 downto 0);
           output : out  STD_LOGIC_VECTOR (15 downto 0));
end Annexure1;
```

5. Truth Table

Input					Output															
e	**i_3**	**i_2**	**i_1**	**i_0**	**o_{15}**	**o_{14}**	**o_{13}**	**o_{12}**	**o_{11}**	**o_{10}**	**o_9**	**o_8**	**o_7**	**o_6**	**o_5**	**o_4**	**o_3**	**o_2**	**o_1**	**o_0**
0	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6. Architecture

```
architecture Behavioral of Annexure1 is

component QuestionTwo_PartB_one is
    Port ( ee : in  STD_LOGIC;
           ii : in  STD_LOGIC_VECTOR (1 downto 0);
           oo : out  STD_LOGIC_VECTOR (3 downto 0));
end component;

signal p: STD_LOGIC_VECTOR(3 downto 0);

begin
c4: QuestionTwo_PartB_one port map(enable, input(3 downto 2), p);
gen1: for k in 0 to 3 generate
      cc: QuestionTwo_PartB_one port map(p(k), input(1 downto 0),
output(((4*k)+3) downto (4*k)));
end generate;
end Behavioral;
```

7. TestBench

```
ENTITY Annexure1_TestBench IS
END Annexure1_TestBench;

ARCHITECTURE behavior OF Annexure1_TestBench IS

    -- Component Declaration for the Unit Under Test (UUT)
    COMPONENT Annexure1
    PORT(
         enable : IN  std_logic;
         input : IN  std_logic_vector(3 downto 0);
         output : OUT  std_logic_vector(15 downto 0)
        );
    END COMPONENT;

   --Inputs
   signal enable : std_logic := '0';
   signal input : std_logic_vector(3 downto 0) := (others => '0');

   --Outputs
   signal output : std_logic_vector(15 downto 0);
```

```
   BEGIN
      -- Instantiate the Unit Under Test (UUT)
   uut: Annexure1 PORT MAP (
          enable => enable,
          input => input,
          output => output
        );
   -- Stimulus process
   stim_proc: process
      variable k,j,a:integer;
   begin
            if enable='0' then
                  enable<='1';
            elsif enable='1' then
                  enable<='0';
            end if;
            for k in 0 to 15 loop
                  j:=k;
                  a:=0;
                  while a<4 loop
                        if (j rem 2)=0 then
                              input(a)<='0';
                        elsif (j rem 2)=1 then
                              input(a)<='1';
                        end if;
                        j:=j/2;
                        a:=a+1;
                  end loop;
            wait for 1 ps;
            end loop;
   end process;
END;
```

8. Timing Diagram