University of Central Florida

Department of Computer Science

CDA 5106: Fall 2020

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

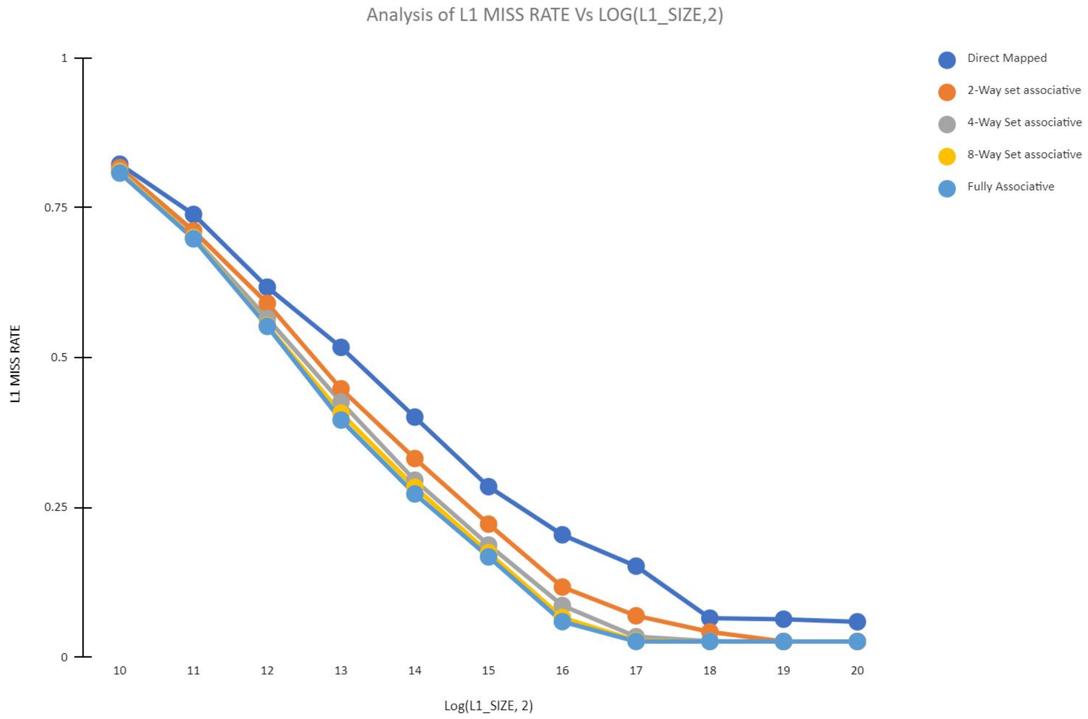
Priya Sudharsanan

Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student’s electronic signature: ______________Priya Sudharsanan________________
(sign by typing your name)

8.1. L1 cache exploration: SIZE and ASSOC

Graph 1-



1.
    - L1 miss rate decreases whenever the size of L1 Cache increases.
    - Smaller cache size, with increasing associativity reduces L1 miss rate.
    - For larger L1 cache size, we can see that the L1 miss rate remains constant for all associativities.This means that after increasing the cache size beyond a certain size, L1 miss rate remains the size which is the compulsory miss rate.

2. Compulsory miss rate occurs when the blocks are brought into the cache for the first time. From the graph, L1 miss rate value stays constant for larger cache size Compulsory miss rate obtained from the graph is 0.2582.

3. **Conflict** misses are caused when several addresses map to the same set and evict blocks that are still needed.In other words, it occurs when the associativity is too small or insufficient.

   From the graph, conflict miss rate for-

   i)Directly mapped-0.0789

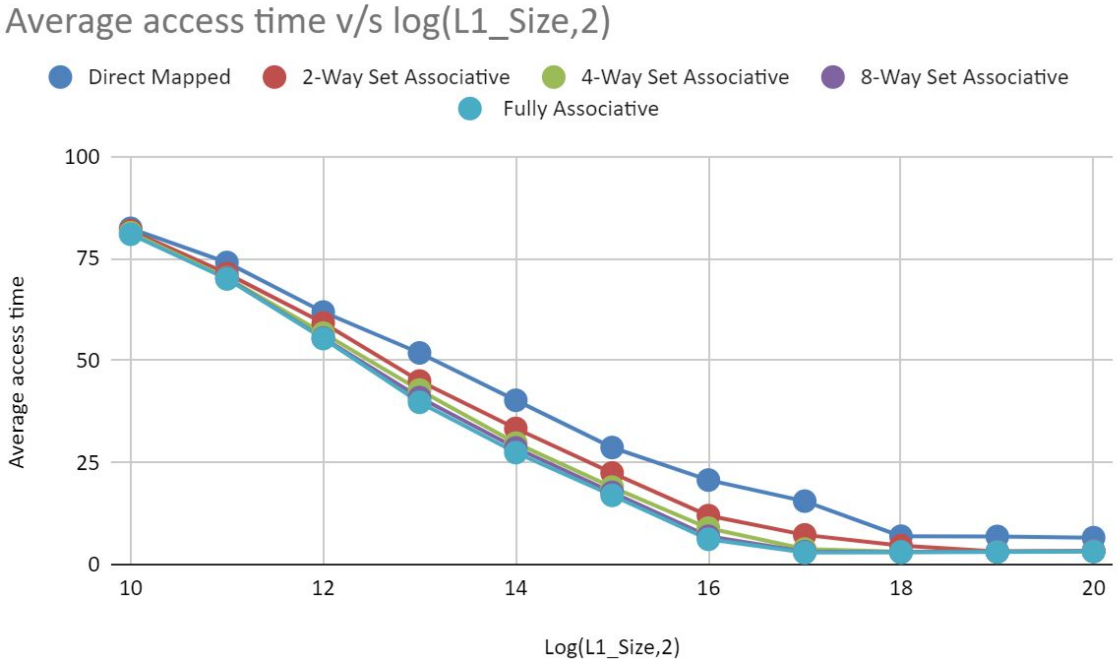
   ii)2-way associativity-0.03126

   iii)4-way associativity-0.01169

   iv)8-way associativity-0.00393

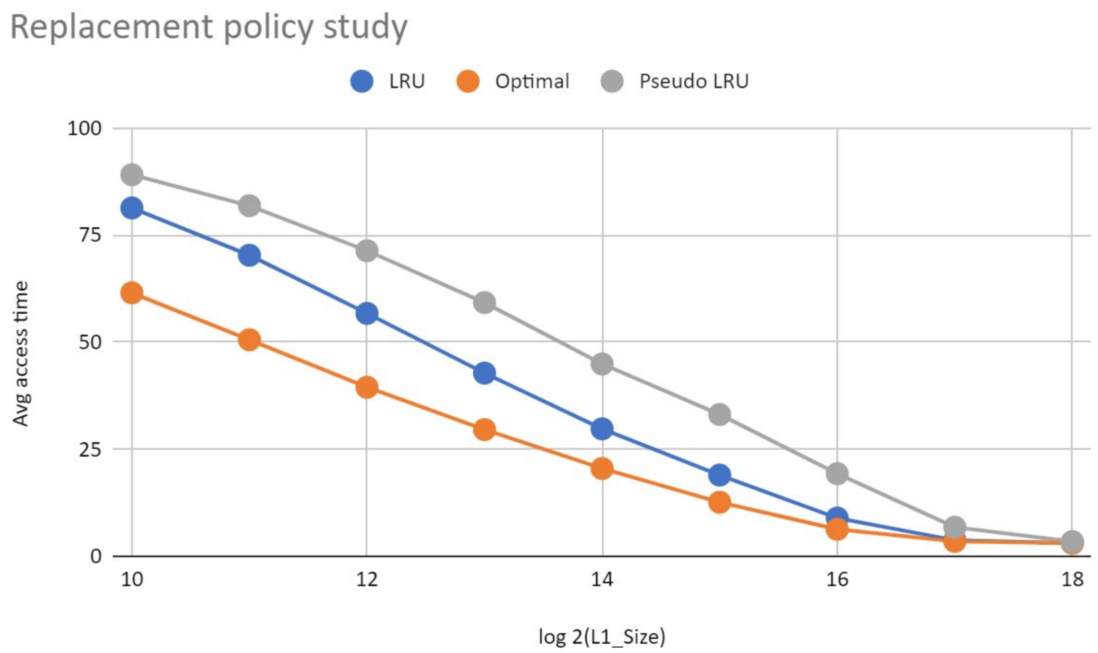
   v)Fully Associative-0

Graph 2-



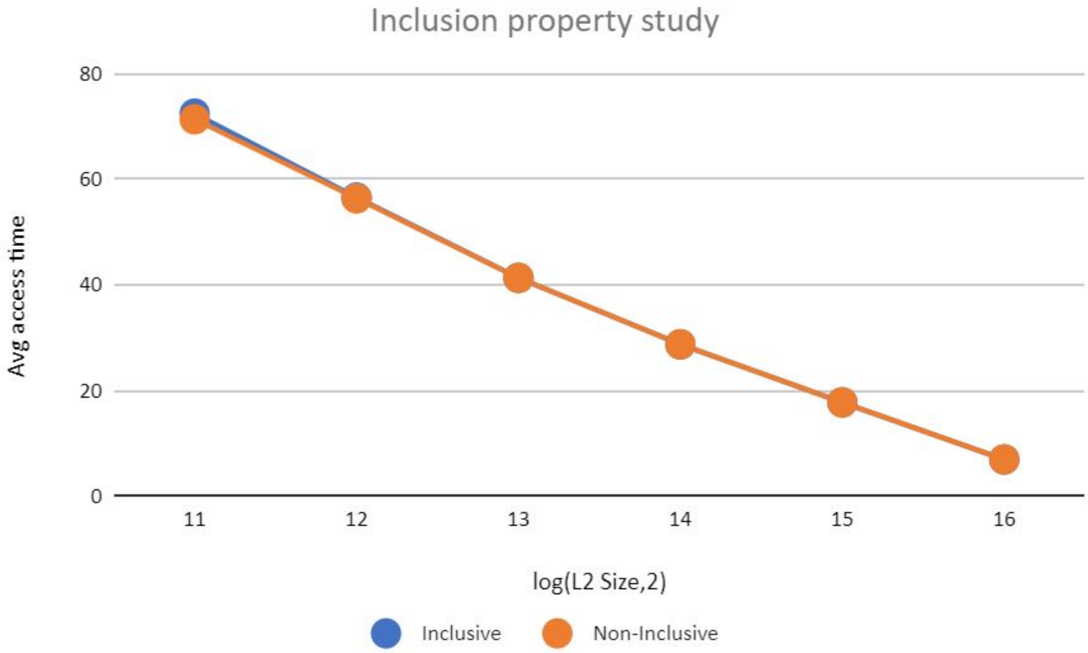
- Average access time (AAT) decreases for smaller cache size with increasing associativity. For log2 size of 10 with associativity of maximum (fully associative),gives the minimum AAT.
- Once the log2(cache size) has reached 18, AAT remains the same for any associativity.Associativity doesn't make any changes to AAT in this case.

Graph 3-



- We can see from the graph that cache size is indirectly proportional to AAT until some point. As the size of cache increases, the AAT decreases.
- Optimal policy has the least AAT,followed by LRU and then by pseudo LRU for log2(cache size) of 10 to 17.
- For Log(size)>18, it can be observed that the AAT remains the same for LRU, Pseudo LRU and Optimal policies.
- Thus caches having smaller size functions better with optimal replacement policy, but for the optimal replacement, we need to have knowledge of future trace,which isn’t possible to implement.

Graph 4-



- From the graph, we can see that the non-inclusive property yields slightly less AAT compared to inclusive cache. For log(size)>=12, AAT remains constant for inclusive and non inclusive.
- Non-inclusive property can be slightly better for smaller size cache.