1. Write detailed description of 8 bit Carry Look-Ahead Adder and its working with the proper circuit diagram in a PDF file. Then write the Verilog code module to implement Carry Look-Ahead Adder. Now, add a test bench to test the Carry Look-Ahead Adder. Make sure to display your inputs, sum, and carry out. Your test bench must have fifteen different inputs. Put five-time unit delay between consecutive inputs.
2. Write detailed description of 8-bit Johnson Counter and its working with the proper circuit diagram and truth table in a PDF file. Then write the Verilog code module to implement 8-bit Johnson Counter. Now, add a test bench to test all the states of the 8-bit Johnson Counter.

Instruction:

Submit your code, PDF file for the writeup and other files inside in a zip file named clearly as

described below.

G<Group No.>R_<Roll no.> A<Assignment No.>.zip

Example. G1R_200410_200411_200412.zip

Any information/assumption about implementation should be described

clearly in a separate text file.

Submit your iverilog/verilog files named clearly as described below.

A<Assignment No.>Q<Question No.>_<top module name>.v

Example. A2Q2_look_ahead_adder.v