Introduction

This project focuses on the design and implementation of a high-precision low-dropout (LDO) voltage reference capable of delivering a stable output under demanding conditions. Implemented in the SG13G2 130 nm BiCMOS process and simulated in LTSpice, the design integrates a curvature-compensated Brokaw bandgap reference with post-fabrication trimming support via an I²C-compatible Verilog HDL interface, achieving an initial accuracy of 0.1% and a temperature coefficient of 40 ppm/°C (Monte Carlo run). A folded cascode amplifier with a flipped voltage follower buffer stage was developed to support load currents up to 100 mA, while careful loop stabilization using Miller compensation ensured robust transient performance. Extensive simulations were conducted to characterize and quantify load regulation, line regulation, and quiescent current, making the design suitable for precision analog and mixed-signal systems requiring reliable low-noise power references.

SG13G2 BiCMOS Technology

The **SG13G2 technology node** is a 130 nm **SiGe:C BiCMOS process** developed by IHP Microelectronics, designed specifically for high-performance analog, RF, and mixed-signal integrated circuit design. It combines the advantages of **advanced CMOS transistors** for logic and low-power digital functions with **high-speed SiGe heterojunction bipolar transistors (HBTs)** for analog precision and RF front-ends, making it ideal for applications that demand both integration and performance. The availability of precision resistors, high-quality capacitors, and multiple metal layers enables compact, reliable, and scalable implementations of complex analog and mixed-signal circuits.

A key feature of SG13G2 is its **SiGe:C HBT devices** with an f_T (cutoff frequency) of up to **250 GHz** and f_{max} of around **340 GHz**, which provide excellent gain and speed characteristics while maintaining low noise performance. These HBTs are crucial for circuits such as bandgap references, low-dropout regulators (LDOs), operational amplifiers, and RF blocks, where precision and high-frequency operation are essential. The technology also supports robust **1.2 V CMOS devices** and extended-voltage devices for analog front-end design, enabling designers to implement mixed-signal systems that combine RF, analog, and digital functionality on the same die.

From a design perspective, SG13G2 offers a **comprehensive Process Design Kit (PDK)** that integrates with popular EDA tools such as Cadence and LTSpice, allowing access to accurate device models, parasitic extraction, and corner/Monte Carlo simulations for yield and variability analysis. Passive components such as high-resistivity polysilicon resistors, metal-insulator-metal (MIM) capacitors, and thick top metals provide reliable support for precision analog circuits and power delivery networks. In addition, the process includes **back-end-of-line (BEOL)** options with multiple metal layers, enabling flexible routing and power distribution.

Overall, SG13G2 is widely adopted in academic and industrial research for **analog/mixed-signal IC design, RF front-ends, voltage regulators, frequency synthesizers, and sensor interfaces**. Its combination of high-speed HBTs, low-leakage CMOS, and robust passive devices makes it a versatile and reliable choice for projects

requiring both high performance and integration density. In the context of this work, SG13G2 enables the design of a curvature-compensated Brokaw bandgap reference and an LDO regulator that meet stringent requirements of accuracy, stability, and load-driving capability.

The overall circuit diagram of the system is shown in figure 1-

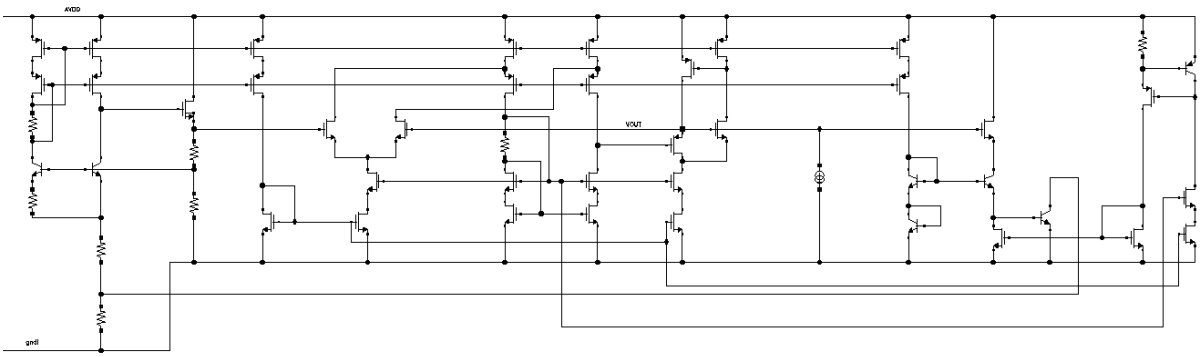


Fig 1 : Complete circuit diagram

Brokaw Bandgap

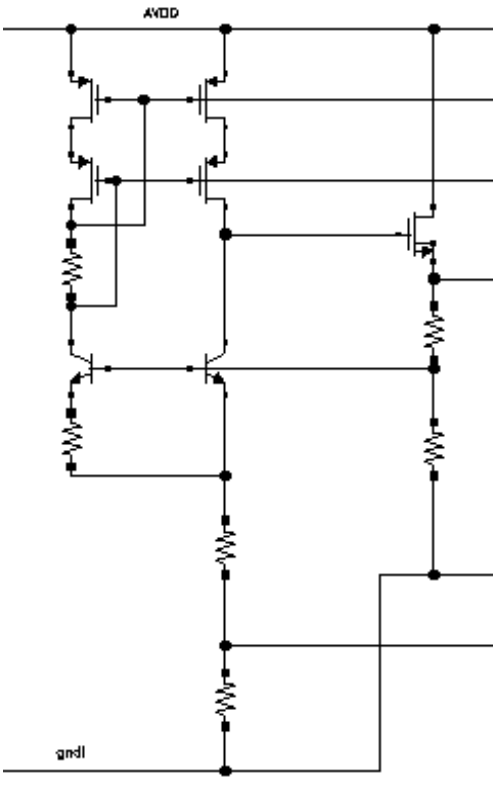


Fig 2: Brokaw Bandgap

The Brokaw bandgap reference combines:

- A **CTAT voltage** (Complementary-To-Absolute-Temperature) → the **base-emitter voltage V_{BE}** of a BJT decreases with temperature (≈ –2 mV/°C).

- A **PTAT voltage** (Proportional-To-Absolute-Temperature) → generated from the difference of base-emitter voltages of two BJTs operating at different current densities.
- By summing CTAT + PTAT in proper proportion, the temperature dependence cancels out, yielding ~1.2 V reference, nearly independent of temperature.

Current Mirror and Motorola Biasing

- The left-top transistors (a pair of stacked PMOS/NMOS) form a **current mirror** that ensures proper biasing.
- Mo

Bipolar Core

- Two BJTs (or diode-connected BJTs) are present with **different emitter areas**

$$\Delta V_{BE} = V_T \ln\left(\frac{A_2}{A_1}\right)$$

Resistor Network

- Resistors scale ΔVBE into a current:

$$I_{PTAT} = \frac{\Delta V_{BE}}{R}$$

  This current is mirrored and forced through another resistor to generate a **PTAT voltage drop**.

Summing Node (Core Bandgap Equation)

- At the reference output, you add:
  - The **CTAT term**: V_{BE} of one BJT.
  - The **scaled PTAT term**: $m \cdot \Delta V_{BE}$, with value of m determined by resistor ratio.
- The final bandgap output:

$$V_{ref} = V_{BE} + m \cdot \Delta V_{BE}$$

Choosing mmm for Zero Temp Coefficient

- V_{BE} slope ≈ –2 mV/°C.

- ΔV_{BE} slope ≈ +0.086 mV/°C × ln(A2/A1)\ln(A_2/A_1)ln(A2/A1).
- By picking proper R ratios (thus setting m), these cancel at a “zero temperature coefficient” point.
- This yields: $V_{ref} \approx 1.205\,\mathrm{V}$

Scaling resistors

Resistors on the right side are used to scale the bandgap voltage from 1.2V to 3.3V

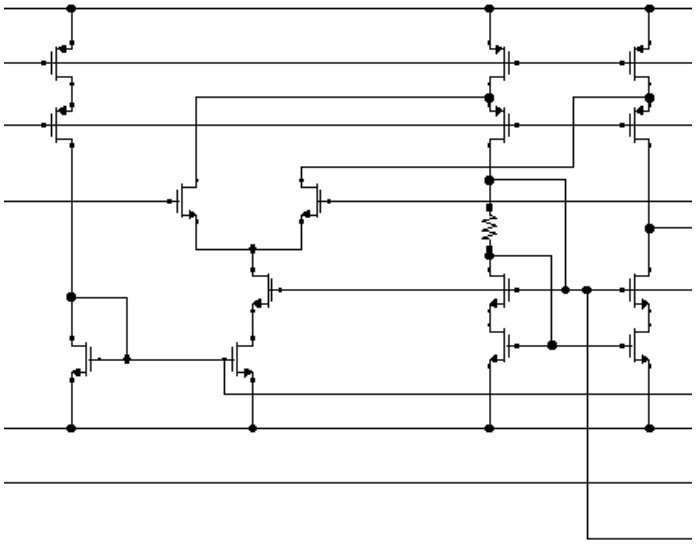


Fig 3: Scaling Resistors

The folded cascode amplifier is a high-performance operational amplifier (op-amp) topology commonly used in analog integrated circuit design. It combines a differential input stage with a cascode output stage, but with a "folded" configuration that allows for improved headroom, higher gain, and better frequency response compared to simpler telescopic cascode designs. The folding refers to routing the differential signal current through parallel paths (one for bias and one for signal), which enables the use of cascode transistors without stacking them directly on top of the input pair, thus reducing the required supply voltage headroom.

This topology is particularly useful in low-voltage applications, high-speed circuits, or where high output swing and gain are needed (e.g., in data converters, filters, or sensor interfaces). The circuit you described (and depicted in the schematic) appears to be a single-ended folded cascode amplifier with an NMOS differential input pair, biased using current mirrors. I'll break it down step by step, referencing the key elements you mentioned: the left branch for bias current, the NMOS input pair, the NMOS mirror with Motorola (likely referring to Monticelli/Motorola) biasing, and the PMOS current mirror. I'll assume the schematic shows

a typical implementation with transistors arranged in branches, where the left side generates bias voltages/currents, the center is the input stage, and the right is the output cascode stage.

1. Overall Circuit Structure and Operation

- **Basic Functionality**:
  The amplifier converts a differential input voltage (applied to the gates of the NMOS input pair) into a single-ended output current or voltage with high gain. The differential signal is amplified by the transconductance (gm) of the input pair, and the cascode stage boosts the output impedance for higher voltage gain (Av ≈ gm * Rout, where Rout is very high due to cascoding).
- **Key Advantages**:

- High DC gain (typically 60-100 dB) due to the cascode's high output resistance.
  Good output swing (close to rail-to-rail in some designs) because the folding avoids excessive transistor stacking.
  Improved power supply rejection and bandwidth compared to basic differential amplifiers.
  In this NMOS-input version, it's suited for low common-mode input voltages (near ground), making it ideal for grounded sensors or low-voltage rails.

- **Disadvantages**:
  Slightly higher power consumption due to the folding currents, and potential stability issues in feedback loops (requires compensation, e.g., via Miller capacitor, though not shown here).
- **Biasing Overview**:
  The circuit operates in the saturation region for all transistors to ensure linear amplification. Bias currents set the operating points, and mirrors replicate these currents across branches for symmetry.

2. Bias Current Generation

- **Description**:
  This is the reference branch that establishes the bias currents and voltages for the entire amplifier. It typically consists of a bias current source (e.g., an external reference current I_{bias}, often generated off-chip or via a bandgap reference) feeding into a stack of transistors or mirrors.
- **Components**:
  A current source at the top (from VDD) or bottom (to GND), setting a reference current (e.g., 10-100 µA depending on the process/technology).
  Possibly diode-connected transistors (NMOS or PMOS) to generate gate-source voltages (Vgs) for mirroring.
- **Role**:
  It provides stable bias points to the gates of current mirrors elsewhere in the circuit. This ensures matched currents in the input and cascode stages, minimizing offset and distortion.
- **How It Works**:
  The bias current flows through the branch, creating voltage drops across transistors. These voltages are "mirrored" to other branches via gate connections. In low-voltage designs, this branch might include level-shifting to accommodate the Monticelli biasing (detailed below).

3. NMOS Input Pair

- **Description**:
  This is the transconductance stage (the "front end" of the amplifier). It consists of two matched NMOS transistors (let's call them M1 and M2) configured as a differential pair.
  - Gates: Connected to the differential inputs (V_{in}^+ and V_{in}^-).
  - Sources: Tied together and connected to a tail current source (often an NMOS transistor biased from the left branch, sinking current to GND).
  - Drains: Connected to the folding points (typically to PMOS transistors from VDD).
- **Biasing**: The tail current (I_{tail}, e.g., 2 * I_{bias}) is mirrored from the left branch. Each half of the pair carries $I_{tail}/2$ in quiescence (no input signal).
- **Operation**:
  1. DC (Bias) Mode: With $V_{in}^+ = V_{in}^-$, the currents in M1 and M2 are equal ($I_{tail}/2$ each). The common-mode input sets the gate-source voltage (V_{gs}) for proper saturation.
  2. AC (Signal) Mode: A small differential input ($\Delta V_{in} = V_{in}^+ - V_{in}^-$) steers current between M1 and M2. The transconductance gm ($\approx \sqrt{(2 * \mu_n * C_{ox} * (W/L) * I_{drain})}$) converts ΔV_{in} to differential drain currents ($\Delta I = gm * \Delta Vin / 2$).
  3. In the folded configuration, these drain currents are subtracted from fixed bias currents provided by PMOS transistors above (from the PMOS mirror), creating signal currents that "fold" into the cascode branch.
- **Why NMOS?**:
  NMOS transistors have higher mobility (faster) than PMOS, making this suitable for high-speed applications. However, it requires the input common-mode voltage to be at least $V_{gs} + V_{dsat}$ above ground.

4. NMOS Mirror with Motorola Biasing

- **Description**: This is likely the bottom current mirror (sinking currents to GND) used for the folding bias currents. It's an NMOS current mirror enhanced with "Motorola" (Monticelli) biasing to enable low-voltage operation.
  - Standard Current Mirror: Diode-connected NMOS (reference) with gates tied to mirrored NMOS transistors.
  - But here, it's a cascode mirror (stacked NMOS for higher output impedance) with special biasing.
- **What is Motorola/Monticelli Biasing?**: This refers to a low-voltage cascode current mirror technique developed by Daniele Monticelli at Motorola in the 1980s. In a standard cascode mirror:
  - Two NMOS stacked per branch (bottom for mirroring, top for cascoding).
  - Minimum output voltage (headroom) is 2 * V_{dsat} + V_{th} (where V_{dsat} is saturation voltage, V_{th} is threshold), which can be high (~1-2V).
  - The Monticelli version reduces this to ~2 * V_{dsat} by using a biasing network (often a resistor or additional transistor) to set the cascode gate voltage optimally. This shifts the gate bias of the cascode transistors so they operate with minimal Vds on the bottom transistors.
  - Configuration: The reference branch has a diode-connected NMOS, but the cascode gate is biased via a voltage drop (e.g., from a PMOS or resistor) tied back from the left bias branch.

- **Role in the Circuit**: This NMOS mirror provides the bias currents for the folding points (e.g., $I_b > I_{tail}/2$ per side). It sinks the excess current from the PMOS above the input pair, allowing the signal current to fold into the cascode.
  - In the schematic, this might appear as the bottom transistors with zigzag connections (for biasing resistor if used).
- **Operation**:
  - Mirrors the left-branch bias current to multiple outputs.
  - The cascode increases the mirror's output resistance ($Rout_{mirror} \approx gm_{cas} * ro^2$, where ro is intrinsic resistance), reducing channel-length modulation and improving accuracy.
  Motorola biasing ensures the mirror works down to lower supply voltages (e.g., 1.5-2V total headroom), crucial for modern CMOS processes.
- **Why Here?**: In folded cascode, the bottom mirror handles the folding currents, and high impedance helps maintain high gain.

5. PMOS Current Mirror

- **Description**: This is the top current mirror (sourcing currents from VDD), often used as the active load for the cascode stage.
  - Typically, two or more PMOS transistors: one diode-connected (reference), others mirroring.
  - It might also be cascoded for higher impedance, biased from the left branch.
- **Role**: Provides bias currents to the folding nodes (above the NMOS input pair drains) and acts as the load for the output cascode.
  - In the folded structure, PMOS sources current I_b to each side of the input pair. The input pair drains pull $I_{tail}/2$ + signal, so the excess ($I_b - I_{tail}/2$ - signal) folds to the NMOS cascode transistors.
- **Operation**:
  - Mirrors bias from the left branch.
  - At the output node, the PMOS cascode load increases Rout, boosting gain.
  - Signal-wise, it converts the folded current back to voltage at the output.
- **Why PMOS?**: PMOS complements NMOS for push-pull-like behavior, and in the top position, it handles sourcing from VDD efficiently.

6. How the Signal Flows (Small-Signal Analysis)

- Input $\Delta V_{in} \rightarrow$ NMOS pair generates differential currents ΔI.
- At folding nodes: PMOS mirror sources fixed I_b, NMOS pair drains vary by $\pm\Delta I/2$, so folded current to cascode is $(I_b - I_{tail}/2) \pm \Delta I/2$.
- The cascode NMOS (common-gate) amplifies this current with high impedance, passing it to the PMOS mirror load.
- Output voltage: $Vout = - (gm_{input} * \Delta Vin) * Rout_{cascode}$.
- Gain: High due to $Rout \approx (gm_{cas} * ro_{cas} * ro_{load})$.
- Frequency Response: Pole at output node limits bandwidth; folding adds a zero for better phase margin.

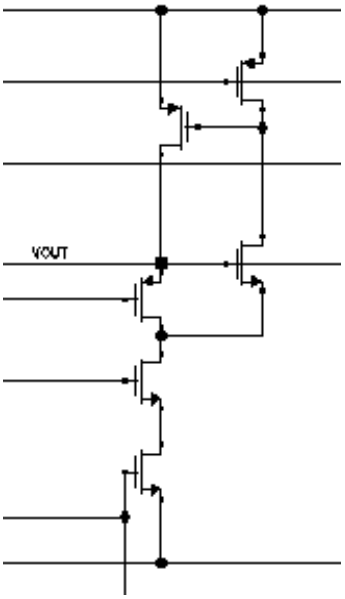


Fig 4 : Signal flow

Overall Circuit Structure and Functionality

- **Basic Purpose**: The FVF acts as a voltage buffer or regulator that makes V_{OUT} closely track an input reference voltage (V_{in} or V_{ref}) with minimal dropout ($V_{DO} \approx V_{dsat}$, typically 50-200mV). It provides unity gain ($V_{OUT} \approx V_{in}$), low output impedance (20-100Ω), and high current capability (sourcing/sinking >10x bias current). The fast loop enhances bandwidth and transient response, allowing recovery from load steps (e.g., 1mA to 100mA) in nanoseconds to microseconds.
- **Key Advantages**:
    - Low-voltage compatibility: Minimum $V_{DD} \approx V_{th} + 2*V_{dsat}$ (e.g., ~0.9-1V in 0.18µm CMOS).
    - Capacitorless operation: No off-chip capacitor needed for stability, reducing area and cost.
    - Fast transients: Undershoot/overshoot <100mV, settling time <1µs via the fast loop.
    - High power supply rejection ratio (PSRR >60dB) and low quiescent current (Iq <50µA).

In this circuit the top left pie mass acts as a pass device to carry the hundred milliamps of current as load. The input of the flipped voltage follower is given at the gate of the p mass which is below the pass device. The feedback loop is closed through the NMOS cascode which is biased using without and a current source on top to have a proper operating point there is a current source at the bottom of the whole structure to ensure that the pass device always has some bias current even at the no load condition.

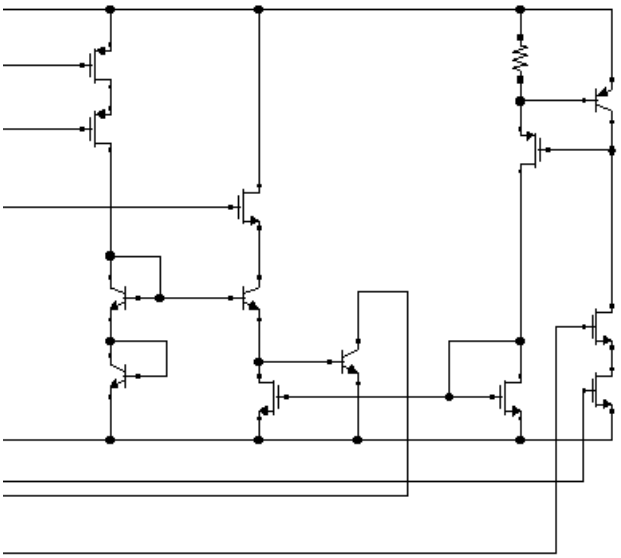


Fig 5 : Bias with CTET current

This circuit is used to correct the curvature in the band gap the left branch has the is biased with PTET current which has a positive temperature coefficient it is passed through two BJT is and hence to bbe voltage is generated the next branch is bias with a CTET current which is generated on the right hand side of the circuit using V_{BA} / r. This branch BJT drops one of the babies from the last two babies and its faith to the next BJP the current through which is IP tat square divided by ictet which has a curvature which is used to correct for the correct the curvature generated by the vve or the CTET component of the band gap.

Further improvements

- A current limit a circuit is to be added to restrict the output current in case of short circuit
- Miller compensated second stage is being added in the folded cascoded amplifier to increase the gain even further and have lower offset

Staility

Stability of the whole loop is ensured using a dominant pole compensation done at the output of the folded cascode amplifier where 10 pF of capacitance is added to make this a dominant pole . As output capacitance increases, the system is expected to become unstable at very high values of output capacitors.

The peter generator loop is inherently stable because it is a positive feedback loop with gain less than 1

Results

Below are the results from the simulations done on the circuit:

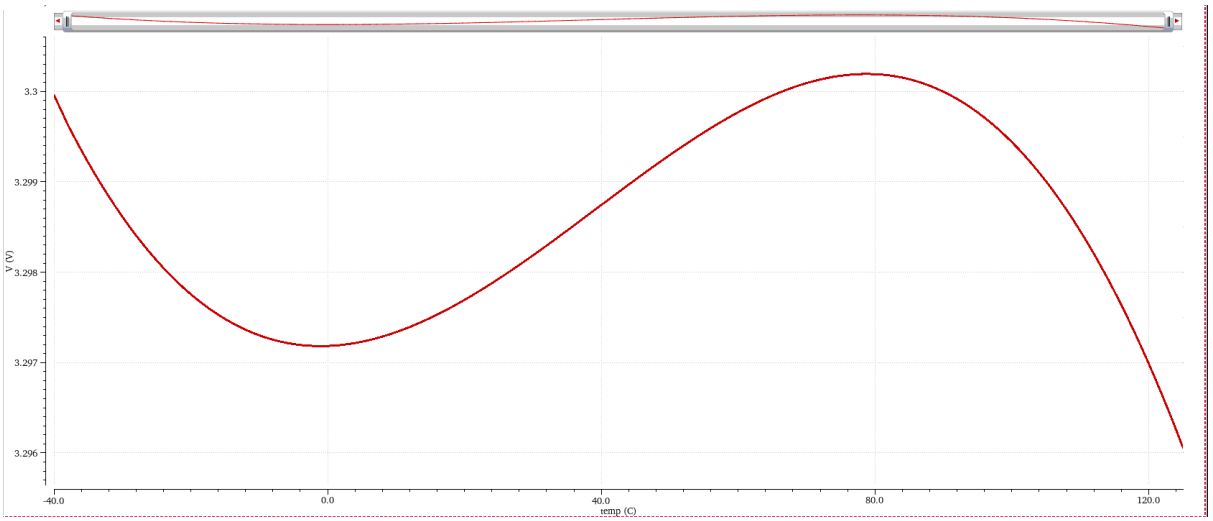


Fig 6 : Nominal behaviour across temperature of V out at no load

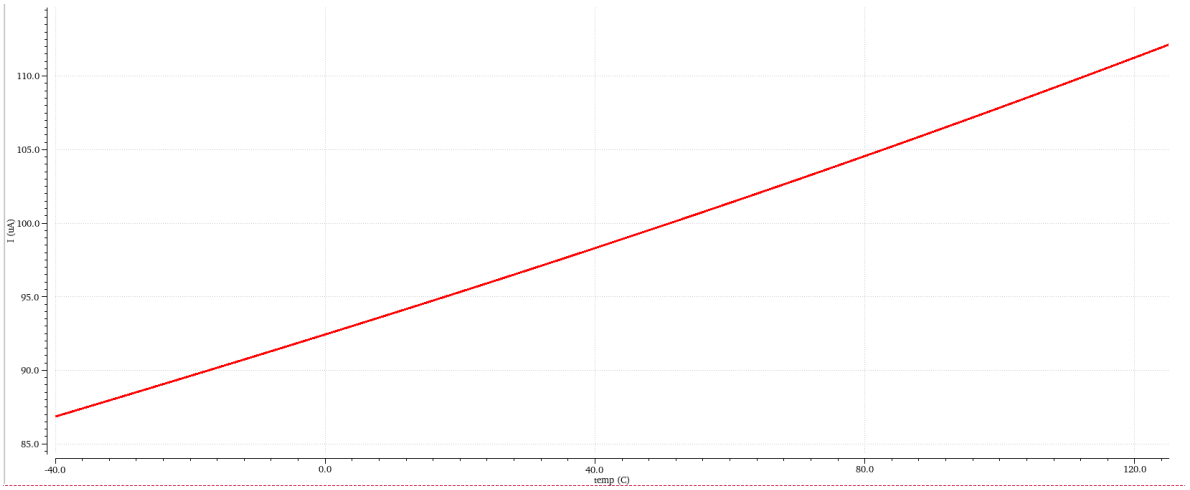


Fig 7 : The crescent current or the IQ of the device across temperature nominally

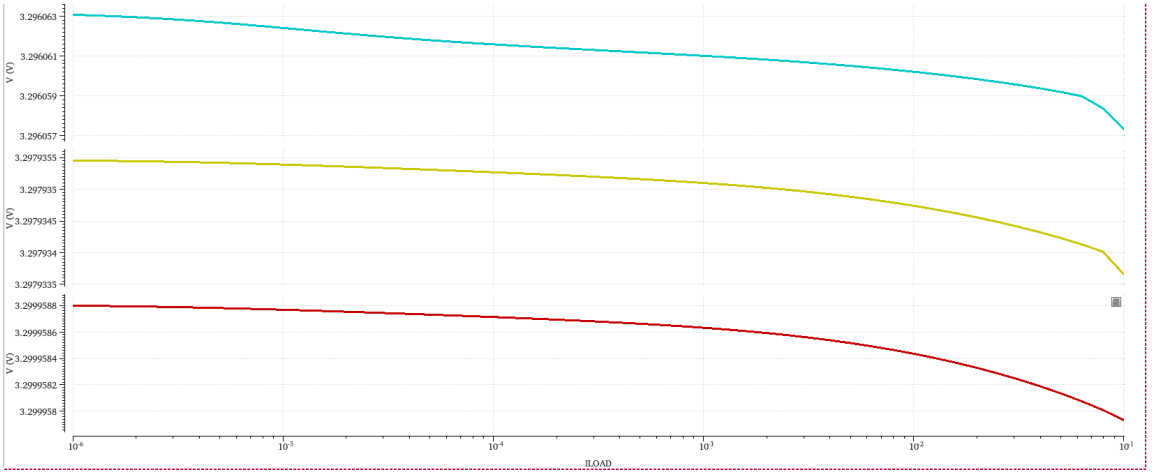


Fig 8 : The load regulation of the ldo at 5 volt supply across temperature the top graph is at 125c the middle one at 25c and the bottom one at minus 40c

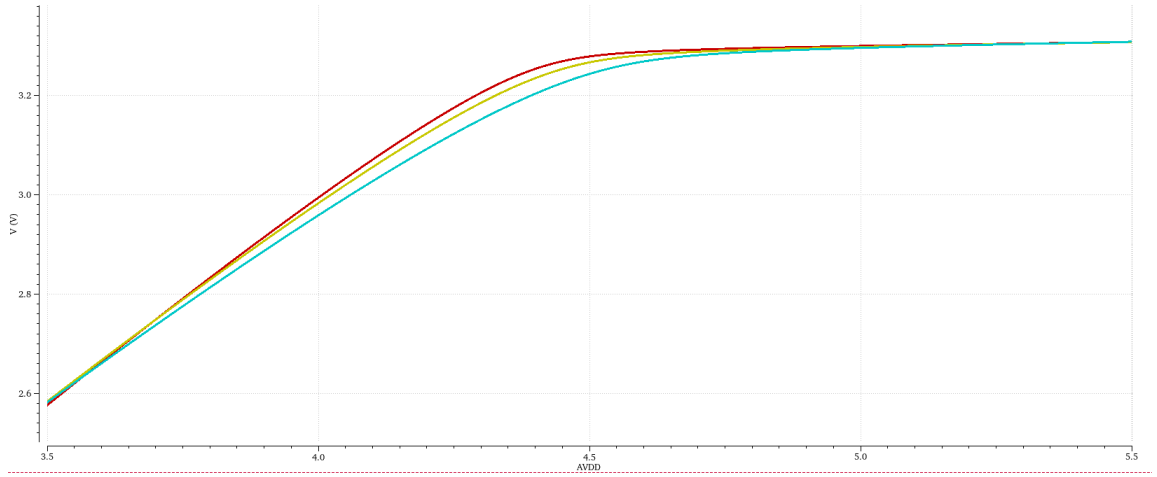
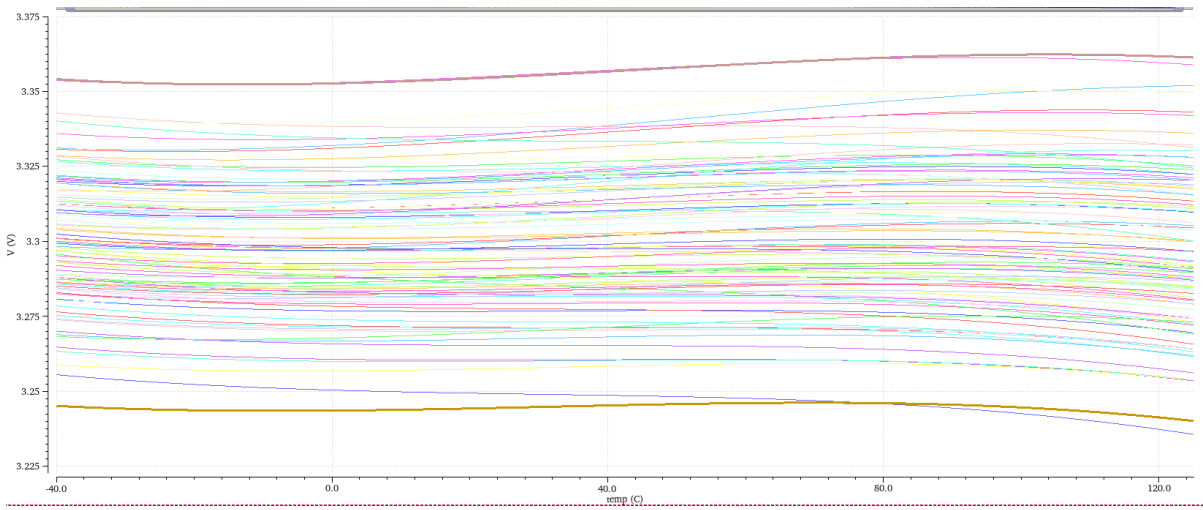


Fig 9 : The line regulation of the ldo from 3.5 volt supply to 5.5 volt supply across temperature



Output	Min	Max	Mean	Median	Std Dev
tempco	6.157	49.07	16.52	14.14	8.554

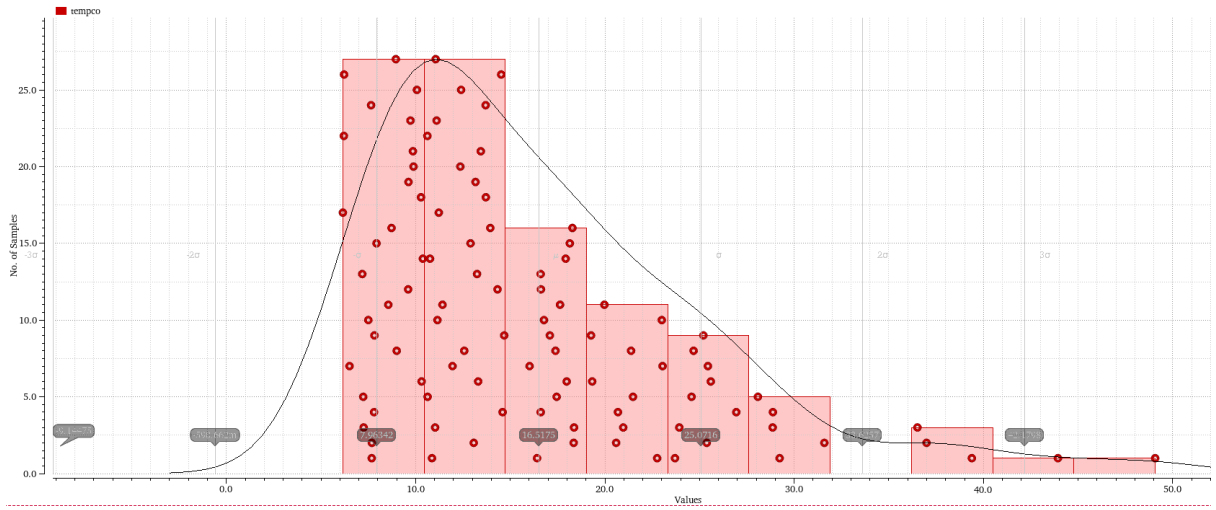


Fig 10 : MC 100 point run results before trim

References

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