Priyanjana Pal

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Google Scholar Profile

Experience

GlobalFoundries **Bangalore, India**
Senior Device-Circuit Co-Design and Enablement Engineer *Jan 2020–Nov 2022*

- **ESD Compact Modeling:** Measured and modeled the DC-IV, CV, TLP (HBM, CDM) characteristics of LV, MV, and HV ESD devices (e.g., LDMOS, VPNPs, BiSCR, Switch FETs) for nodes including 130nm, 45SPCLO, 28nm BCDlite, and 22FDX using SPECTRE and SPICE.
- **RF ESD Device and Circuit Design (with DE and US team):** Designed RF-compatible ESD designs for mmWave applications and optimized device performance using EMX tools.
- **Model Automation and QA(with DE and US team):** Developed QA scripts (R and Python) for validating compact models, hardware correlation, and processing data across multiple technologies.
- **Layout Design and Tape-out:** Designed and taped out DC and RF test structures for compact modeling, including LVS/PEX extraction for BEOL resistance and capacitance using EMX and RF (S-parameter) modeling.
- **Collaboration and Training:** Trained peers in compact modeling workflows, including spectre simulations, layout design, and EMX/PEX extraction.

Education

Karlsruhe Institute of Technology (KIT) **Karlsruhe, Germany**
PhD in "Reliable Analog Computing" at CDNC, ITEC - Department of Computer Science *Dec 2022–Present*
Research in analog circuit design, reliability testing, and ML-trained neuromorphic circuits with **Prof. Mehdi Tahoori**, IEEE Fellow

Indian Institute of Technology (IIT) Gandhinagar **Gujarat, India**
M.Tech in Microelectronics and VLSI *2018–2020*
CGPA: 7.79/10. Thesis: Design and optimization of high voltage (HV) De-FinFETs for analog SoC using 3D-TCAD.

National Institute of Technology (NIT) Agartala **Agartala, India**
B.Tech in Electronics and Communication Engineering *2014–2018*
CGPA: 8.98/10

Research Interests

Analog and mixed-signal circuit co-design, neuromorphic computing, energy-efficient reliable circuit design, and machine learning integration in hardware.

Technical Skills

CAD Tools: Cadence Virtuoso, Synopsys DC, Sentaurus 3D TCAD, EMX, Calibre, QRC/XRC, PEX

Programming: Verilog, Verilog-A, Tcl, Linux scripting, R, Python

Languages: English (Fluent), Hindi (Fluent), Bengali (Native), German (A1 Level)

Conference and Journal Publications

ICCAD 2025: SpikeSynth: Energy-Efficient Adaptive Analog Printed Spiking Neural Networks

ESWEEK 2025: PRINT-SAFE: PRINTed ultra-low-cost electronic X-Design with Scalable Adaptive Fault Endurance

DAC 2025: Power-Constrained Printed Neuromorphic Hardware Training

ICCAD 2024: Neural Architecture Search for Highly Bespoke Robust Printed Neuromorphic Circuits.

DATE 2024: Analog Printed Spiking Neuromorphic Circuit; On-Sensor Printed Machine Learning Classification via Bespoke ADC and Decision Tree Co-Design.

ETS 2024: Fault Sensitivity Analysis of Printed Bespoke Multilayer Perceptron Classifiers.

IEEE TCAD 2024: Neural Evolutionary Architecture Search for Compact Printed Analog Neuromorphic Circuits.

ICCAD 2023: Power-Aware Training for Energy-Efficient Printed Neuromorphic Circuits.

ASPDAC 2024: A Dynamic Testing Scheme for Resistive-Based Computation-In-Memory Architectures.

Technical Projects

Low Dropout Regulator (LDO): Designed an LDO regulator in SCL 180nm technology for digital applications with the following specifications:

- Input Voltage: 2V to 1.8V (200mV dropout voltage), Settling Time: 200ns, Quiescent Current: 10μA, Power Supply Rejection Ratio (PSRR): -40dB at 1MHz

Bandgap Reference Circuit (BGR): Designed a BGR circuit in SCL 180nm technology for low-power linear regulators with the following specifications:

- Supply Voltage: 1.8V (with variation from 1.8V to 2.5V), Temperature Range: -40°C to 125°C, Power Dissipation: 50μW

Charge Pump: Designed a high-efficiency charge pump in SCL 180nm technology for flash memory applications:

- Addressed threshold voltage degradation due to the body effect, achieved improved power efficiency with minimal performance loss.

Two-Stage Operational Amplifier (OP-AMP): Designed a two-stage fully differential OP-AMP for use in low-power LDO regulators:

- Gain: 70 V/V, Output Swing: 1V, Unity-Gain Bandwidth (UGB): 10MHz, Phase Margin: 72°, Power Dissipation: 35μW

Achievements

Awards: Received multiple appreciation and spotlight awards at GlobalFoundries for ESD compact model development.

Scholarships: National Visual Arts Painting Scholarship by CCRT, India, North-Eastern-Council (NEC) Scholarship in Bachelor's, Early Admit MTech with MHRD, India, GATE'2018.

Hobbies

Activities: Painting, Swimming, Chess, Cooking