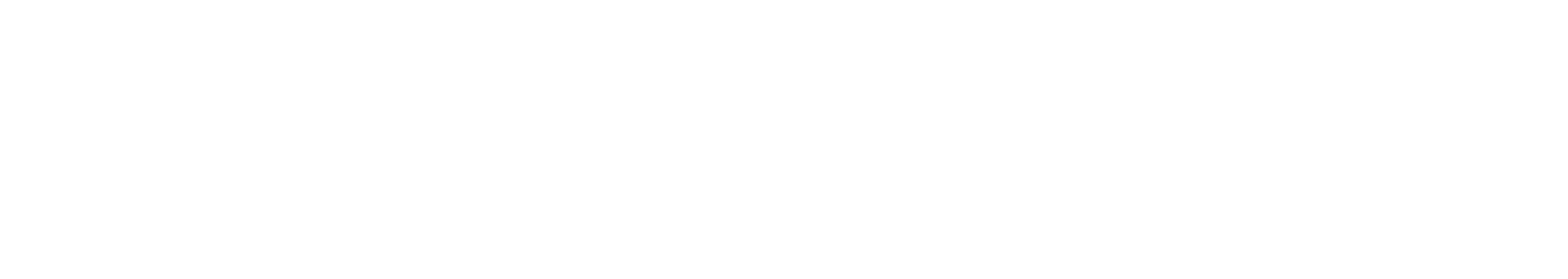
**[2-bit Subtractor using NAND gates]**



**Submitted by**

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**External**

**Project Report**

**on**

**Digital Logic Design**

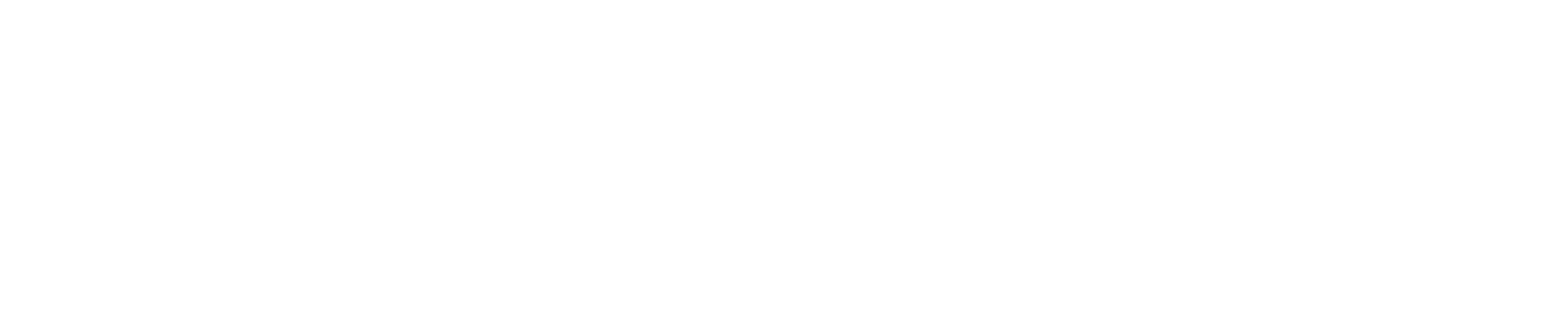
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**B**.**Tech. CSE 3rd Semester (Section - 41)**

# Declaration

We, the undersigned students of B. Tech. of **(CSE)** Department hereby declare that we own the full responsibility for the information, results etc. provided in this PROJECT titled “**(2-bit SUBTRACTOR)**” submitted to **Siksha ‘O’ Anusandhan Deemed to be University, Bhubaneswar** for the partial fulfillment of the subject **Digital** **Logic Design (EET 1211)**. We have taken care in all respect to honor the intellectual property right and have acknowledged the contribution of others for using them in academic purpose and further declare that in case of any violation of intellectual property right or copyright we, as the candidate(s), will be fully responsible for the same.

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**PLACE: ITER, BHUBANESWAR**

**Abstract**

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**1. Introduction**

In digital electronics, a **subtractor** is a combinational logic circuit that performs the subtraction of two binary numbers. However, the subtraction of binary number can be performed using adder circuits by taking 1’s or 2’s compliments. But, we may also realize a dedicate circuit to perform the subtraction of two binary numbers.

In the subtraction of two binary numbers, each subtrahend bit of the number is subtracted from its corresponding significant minuend bit to form a difference bit. During the subtraction, if the minuend bit is smaller than the subtrahend bit, then a 1 is borrowed from the next position. Depending upon the number of bits taken as input, there are two types of subtractors namely, **Half Subtractor** and **Full Subtractor**.

### Advantages of using NAND and NOR gates to implement Half Subtractor:

1. Universality: NAND and NOR gates are considered universal gates because they can be used to implement any logical function, including binary arithmetic functions such as addition and subtraction.
2. Cost-effectiveness: NAND and NOR gates are relatively simple and inexpensive to manufacture compared to other types of gates.
3. Reduced power consumption: NAND and NOR gates consume less power compared to other types of gates, making them suitable for low-power applications.

### Disadvantages of using NAND and NOR gates to implement Half Subtractor:

1. Propagation delay: The propagation delay of NAND and NOR gates can be higher compared to other types of gates, which can affect the overall performance of the system.
2. Noise susceptibility: NAND and NOR gates can be susceptible to noise and other types of interference, which can cause incorrect operation of the circuit

## 2. **Problem Statement** :-

* 1. Explanation of problem and identification of input and output variables.

ii. Highlighting the constraints.

* Half subtractors do not take into account “Borrow-in” from the previous circuit.
* This is a major drawback of half subtractors.
* This is because real time scenarios involve subtracting the multiple number of bits which can not be accomplished using half subtractors.

Identify the input and output variables-

* Input variables = A, B (either 0 or 1)
* Output variables = d, b where d = Difference and b = borrow

## 3. **Methodology** :-

1. Generating the solution to the problem by the use of Truth table/excitation table, K- map and (or) Boolean algebra.
2. Finding out the different digital ICs to be used in the optimized design.

|  |  |  |  |
| --- | --- | --- | --- |
| **Inputs** | | **Outputs** | |
| **A** | **B** | **d (Difference)** | **b (Borrow)** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
|  |  |  |  |

## K-Map for Difference(d)

|  |  |
| --- | --- |
|  |  |
|  |  |

## K-Map for Borrow(b)

|  |  |
| --- | --- |
|  |  |
|  |  |

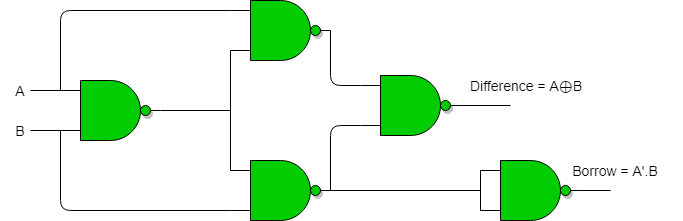
## **IC Used**

For **Half Subtracter Using NAND Gates**:

| **IC Number** | **IC Name** |
| --- | --- |
| 74LS00 | Quad 2-input NAND Gates |

## **4.Implementation :-**

1. Drawing the logic diagram using Nand logic gates.

**Implementation of 2-bit Subtractor using NAND gates :** Total 5 NAND gates are required to implement half subtractor.

From this logic circuit diagram, we can see that 9 NAND gates are required for realization of the half subtractor.

The output equations of the half subtractor in NAND logic are as follows −

**Difference Bit (d)**

Difference, d = ((A.(AB)’)’.(B.(AB)’)’)’ =A⊕B

**Borrow Bit (b)**

Borrow, b= ((B.(AB)’)’)’ = A’B

## **5.Results & Interpretation** :-

Verification of the output for different inputs that satisfies the problem statement by the use of truth table.

|  |  |  |  |
| --- | --- | --- | --- |
| **Inputs** | | **Outputs** | |
| **A** | **B** | **d (Difference)** | **b (Borrow)** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
|  |  |  |  |

Using this truth table, we can determine the output equation of the half subtractor. The following are the equations of difference bit (d) and borrow bit (b) −

**Different Bit (d) −**

Difference, d=A′B+AB′=A⊕B

**Borrow Bit (b) −**

Borrow, b=A′B

**6. Conclusion**

For the above experiment (2-bit subtractor) we have used 7400 quad-2 input NAND gate ic’s and verified . We observed that it is working for all the inputs.

**7.References**

* **Fundamentals of Logic Design- by Charles H .Roth , Jr Larry L Kinney**
* <https://www.geeksforgeeks.org/full-subtractor-in-digital-logic/>
* <https://www.theengineeringprojects.com/2021/02/2-bit-full-subtractor-in-proteus-isis.html#:~:text=2%20bit%20Full%20Subtractor%20is,2nd%20value%20will%20be%20Subtracted>.

# **8.Appendices**

Justification of the architecture / digital ICs used for implementation.

(Attach datasheets of the devices/ ICs that you have used)