

ECE (302) Lab #2

Transistor Amplifier

Lab section: (D41) Bench #:-- Date:12/10/2022

Abstract

In this lab, we designed and prototyped an audio-band amplifier with a midband voltage gain of $11 \text{ V/V} \pm 5\%$ at a design frequency of 2 kHz. Additionally, we ensured that the input impedance was greater than $10 \text{ k}\Omega$ and that the minimum output voltage swing was 10V_{PP} . The design was divided into three stages which were tackled over three different lab sessions. The first stage(lab 2a) involved designing and prototyping a common emitter amplifier, the second stage required us to build a common collector amplifier, and in the final stage we tested our entire lab 2 circuit in tandem with our DC power supply rails from lab 1. Overall experimental gain was found to be 10.5, which has a four percent difference from the theoretical value, with an input impedance of 13 kOhms. All 3 of the stages were first simulated with the aid of LTSpice prior to being implemented on SK-10 breadboard with the provided 302 lab components. The prototype results were measured using the Agilent InfiniiVision 2000 X-Series oscilloscope. This report entails our design process, results, and our discussion regarding the experiment.

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Our signatures certify that we are submitting our own, original work only, and do so in accordance with the University Code of Student Behaviour and APEGGA's Code of Ethics.

2.1 Objectives

The objective of the lab is to design and prototype an audio-band amplifier with a midband voltage gain of $11 \text{ V/V} \pm 5\%$ at a design frequency of 2 kHz. Additionally the input impedance is to be greater than $10 \text{ k}\Omega$ and the minimum output voltage swing must be 10VPP. The design should be divided into three individual testing stages-Stage 1 amplifier, Stage 2 amplifier and a final testing stage where all the stages are combined . The final circuit is to be supplied using the regulated DC power supply from Lab 1. The amplifier load will consist of a $1200:8 \text{ }\Omega$ impedance transformer driving an 8Ω speaker.

2.2 Design

As mentioned earlier, the design is divided and tested as three different stages which work in tandem to provide the desired output. Dividing the project into multiple stages made it easier to narrow down and identify any problems with the design. We want an amplifier which gives us a high gain and has a high input impedance. Common Emitter configuration provides us a high gain and Common Collector configuration will let us have a high input impedance, thus combining the two will help us achieve the desired output. We have thus divided the lab in the following three stages:

- 1) Stage 2a: This stage requires the selection and subsequent designing/prototyping of an appropriate amplifier such that the voltage gain is greater than 11 V/V . Thus we use a Common Emitter amplifier.
- 2) Stage 2b: The second stage required us to make design choices so that we can have high input impedance in our amplifier and thus we chose the common collector amplifier.
- 3) Stage 3c: In this stage we test the coupled amplifier and check the overall gain.

2.2.1 Lab 2a-Stage 1 amplifier testing

This part of the lab required the selection and subsequent designing/prototyping of an appropriate amplifier such that the voltage gain is greater than 11V/V . After careful examination of the properties of different types of amplifiers, we concluded that the common emitter amplifier was the ideal candidate for this stage.

Having decided on the appropriate amplifier, we had to first determine the resistor values that we would use. To ensure maximum power transfer, we had to assume $R_C = R_L$. Given an R_L value of $1.2 \text{ k}\Omega$, we could determine $R_C=1.2 \text{ k}\Omega$. In order to perform further calculations, some more assumptions had to be made. The assumptions are as follows,

$$1. V_E = 0V, \quad I_B = 0A$$

$$2. r_e = \frac{25}{V_E}$$

$$3. \beta = 100$$

With these assumptions in mind, we could determine the remaining impedance values using the following equations,

1.Voltage gain,

$$A_V = \frac{R_C \parallel R_L}{r_e + R_E} \quad (eqtn.2.1)$$

2.Input Impedance,

$$R_{in} = R_1 \parallel R_2 \parallel [\beta(r_e + R_E)] \quad (eqtn.2.2)$$

3.Output Impedance,

$$R_{out} = R_C \quad (eqtn.2.3)$$

In addition to the previously mentioned resistor values, the resistors used in our final design are as follows,

- $R_1 = 22.68 \text{ k}\Omega$
- $R_2 = 1380 \Omega$
- $R_E = 51 \Omega$
- $R_S = 51 \Omega$ (Supply resistor)

After calculating the required resistor values, we first ran a simulation on LTSpice to get an idea of the voltage values to be expected from the prototype. We then built the prototype and measured the DC bias voltages along with the input and output voltages, all of which are provided in section 2.4

2.2.2 Lab 2b-Stage 2 amplifier testing

Similar to lab 2a, this part required us to first pick an amplifier with a configuration such that it provided high input impedance and unity gain. For this purpose, we used a common collector amplifier. Again, we had to pick appropriate resistances to build this stage of the amplifier. Taking the same assumptions from 2a into consideration, the required impedances could be calculated using the following formulae,

1.Voltage gain,

$$A_V = \frac{R_E \parallel R_L}{r_e + R_E \parallel R_L} \quad (eqtn.2.4)$$

2.Input Impedance,

$$R_{in} = R_1 \parallel R_2 \parallel (\beta + 1)(r_e + R_E \parallel R_L) \quad (eqtn.2.5)$$

3.Output Impedance,

$$R_{out} = R_E \parallel \left[r_e + \frac{R_1 \parallel R_2 \parallel R_{source}}{\beta + 1} \right] \quad (eqtn.2.6)$$

The resistances for the CC stage were calculated to be as follows,

- $R_1=22 \text{ k}\Omega$
- $R_2=26 \text{ k}\Omega$
- $R_E=2.4 \text{ k}\Omega$

In order to determine the values of the input and output impedances, we had to make use of a variable resistor. Having the variable resistor connected between the wave generator and the i/p port of the amplifier, we gradually increased the resistance(starting with short circuit) till we achieved even voltage division. This gave us the input impedance. To find the output impedance, we reconnected the variable resistor to the amplifier output port and started with an open circuit, gradually decreasing the impedance till even voltage division was achieved.

After implementing the amplifiers in each stage, we measured the values of V_E , V_B , V_C and the input/output resistances. All the calculations are provided in the results section. It is to be noted that for the actual prototype, we had to make some approximations and use resistance values that were close but not exact to the calculated values.

2.2.3 Lab 2c-Entire circuit testing

In this final stage of testing, we coupled the two amplifier stages using a 10uF capacitor supplied the entire circuit with the DC power supply that we designed in lab 1. The input we used was the signal generator and the output was a speaker coupled to the amplifier through an impedance transformer.

2.3 Simulation Results



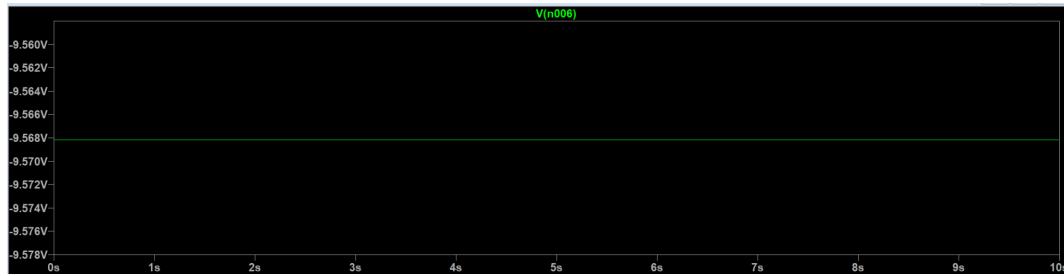


Fig 2.1:-DC bias Voltages for CE; $V_c=0.006V$, $V_b=-8.88V$, $V_e=-9.57V$ in order

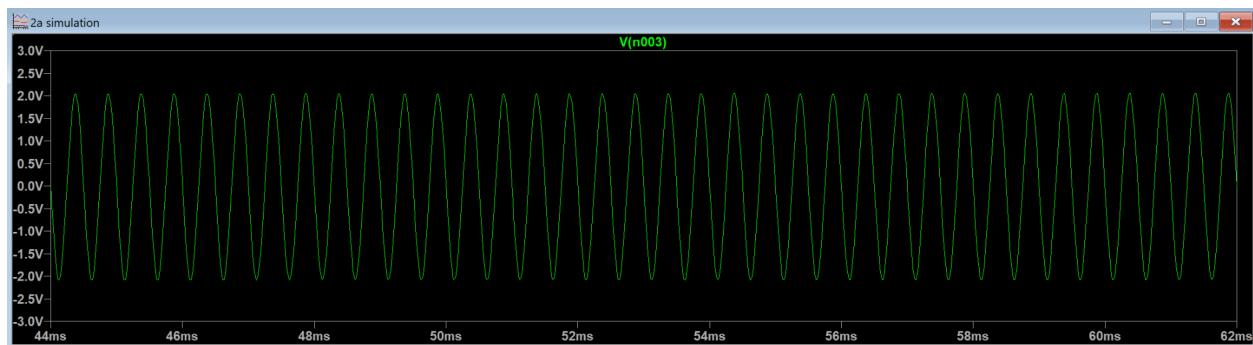


Fig 2.2:-Output Voltage for CE ; $V_{out} = 2.02V$

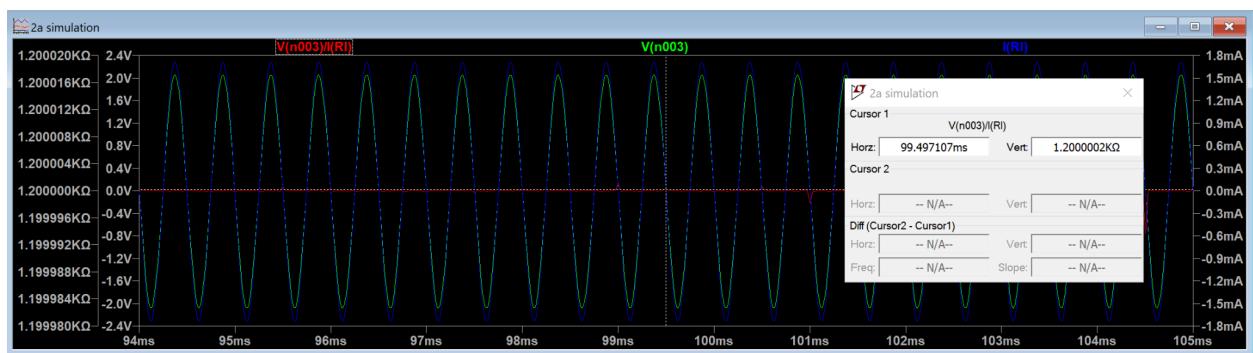


Fig 2.3:- Input Impedance for CE, $R_{in} = 1.2k\text{Ohms}$

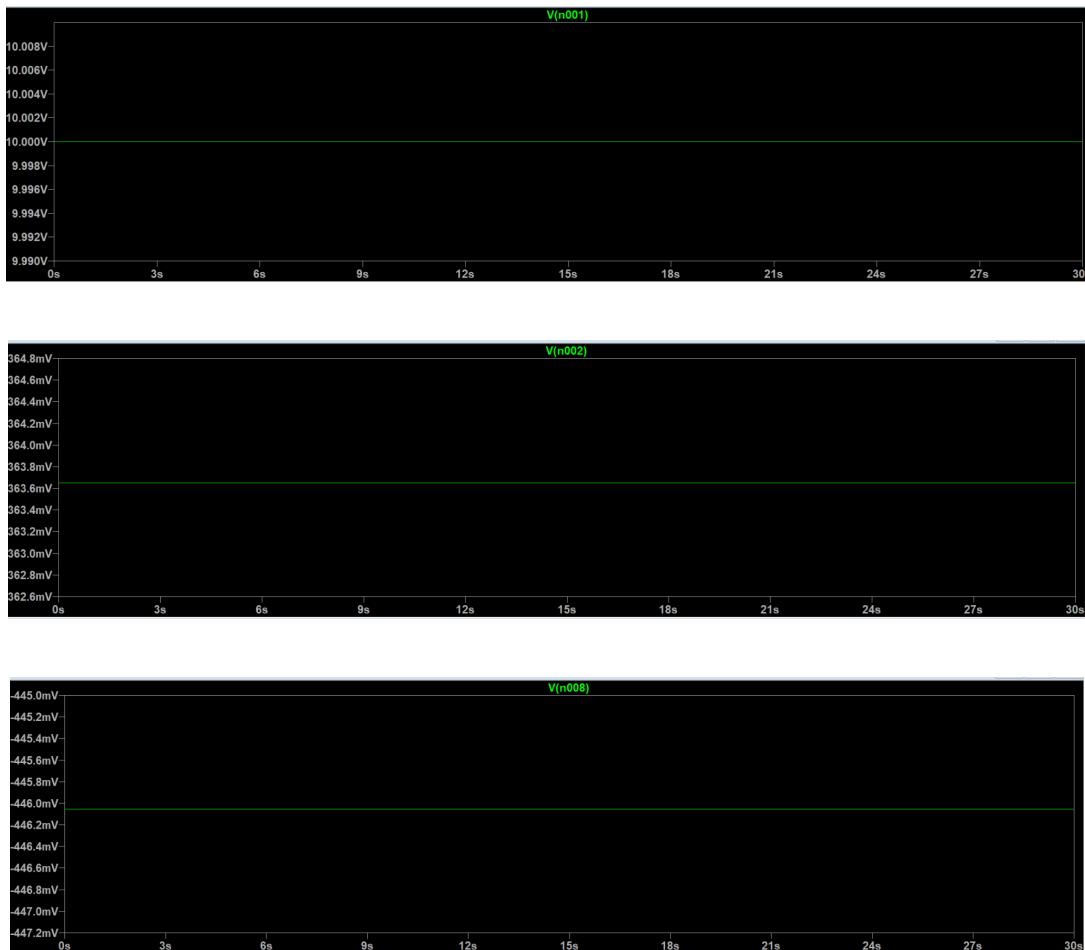


Fig 2.4:- DC bias Voltages for CC; $V_c=10$ V, $V_b=0.363$ mV, $V_e=-0.446$ mV in order

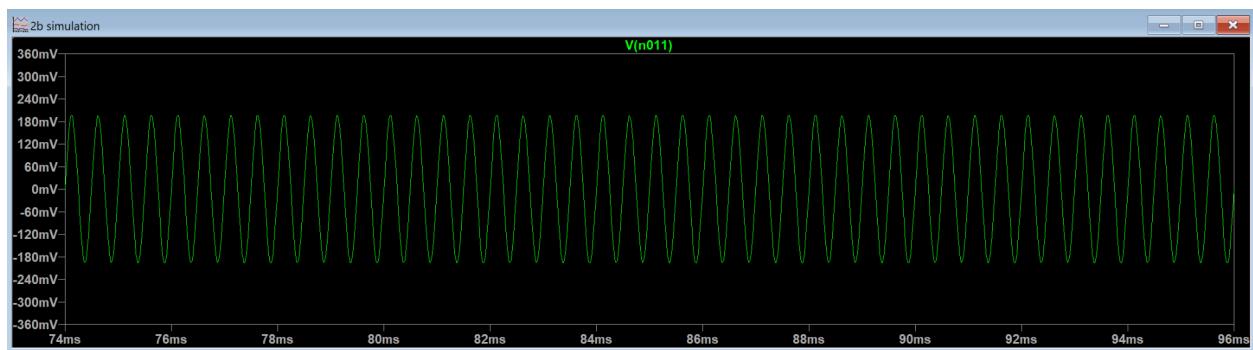


Fig 2.5:- Output Voltage for CC, $V_{out} = 0.197$ mV

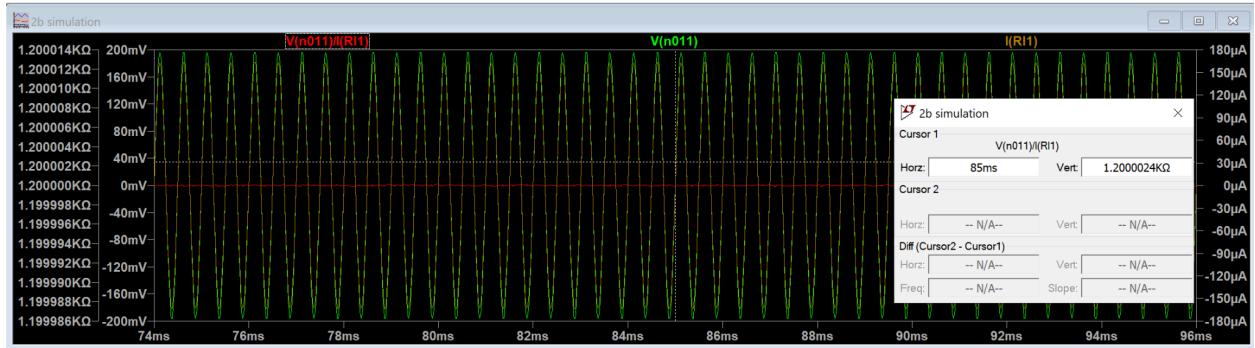


Fig 2.6:- Input Impedance for CC, Rin = 1.2kOhms

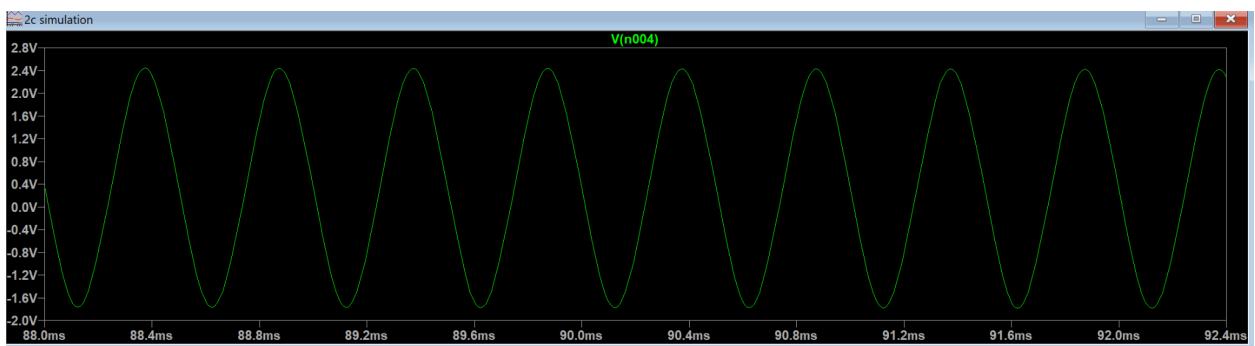


Fig 2.7:- Output Voltage of the coupled stage; Vout (pk-pk)=2.428V

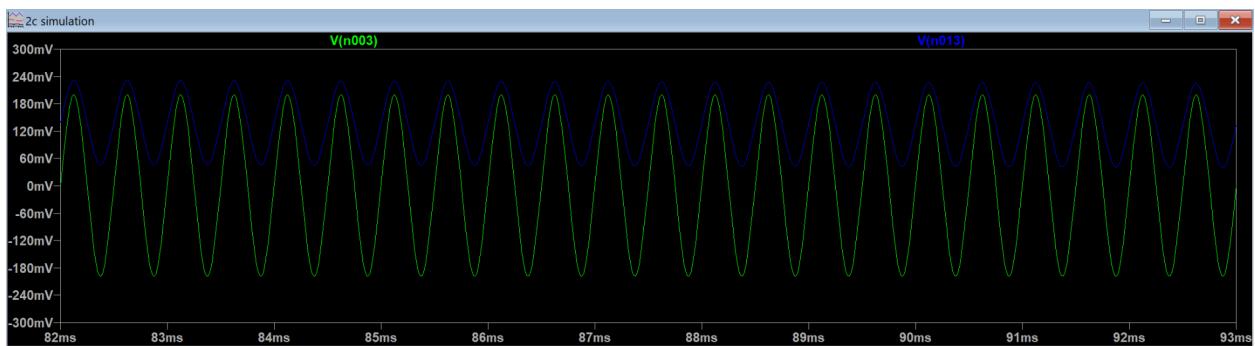


Fig 2.8:- Input Impedance of the coupled stage; Rin= 1.2kOhms

2.4. Calculations & Results

*Calculation included in the appendix section

Results

| Parameters | Theoretical Results | Simulated Results | Experimental Results |
|---|---------------------|-------------------|----------------------|
| V _{in} | 0.200 V | 0.200 V | 0.200 V |
| Lab 2a: Common Emitter Amplifier | | | |
| V _C | 0 V | 0.00632 V | 0.0200 V |
| V _B | -8.87 V | -8.65 V | -8.80 V |
| V _E | -9.57 V | -9.57 V | -9.6 V |
| V _{out} | - | 2.02 V | 2.09 V |
| A _{v,ce} (gain) | 11 | 10.1 | 10.45 |
| Lab 2b: Common Collector Amplifier | | | |
| V _C | 10 V | 10.0 V | 9.80 V |
| V _B | 0.7 V | 0.364 V | 0.300 V |
| V _E | 0 V | -0.446 V | 0.100 V |
| V _{out} | - | 0.197 V | 0.215 V |
| A _{v,cc} | 1 | 0.985 V | 1.075 V |
| Lab 2c: Coupled CE and CC amplifiers | | | |
| V _{out} | - | 2.40 V | 2.11 V |
| A _v (Coupled Voltage Gain) | 11 | 12 | 10.5 |
| R _{in} (Input Impedance) | > 10.0 kOhms | 12 kOhms | 13.0 kOhms |

Table 1. DC Bias and Voltage gain parameters

| Amplifier | % Error in Av (Voltage Gain) (Theoretical vs Experimental) | % Error in Av (Voltage Gain) (Theoretical vs Simulated) |
|-------------------------|---|--|
| Common Emitter | 5 % | 8 % |
| Common Collector | 7.5 % | 1.5 % |
| Coupled Stage | 4 % | 9 % |

Table 2. % Error difference in voltage gain

2.5 Discussion:

It is important to note that the order of the amplifiers matters because, of the design requirements of a high input impedance which means that the Common Collector (CC) amplifier needs to be on the input side and high voltage gain which meant that the load resistance was to be connected after the Common Emitter (CE) stage. This means there is only one possible order of the amplifiers, which is CC followed by CE.

The next important thing was to ensure the stability of the amplifier. Before calculating the gain for each stage, it was important to obtain the right terminal voltages matching with the theoretically obtained values. For Lab 2a CE stage, obtaining the correct collector terminal voltage ($V_c = 0V$) was the challenging part. By varying the values of R_1 and R_2 , we were eventually able to obtain the right V_c . It was observed that on increasing the value of R_1 , the value of V_c decreased. For Lab 2b CC stage, we were able to obtain the expected voltage gain using the calculated. Based on observations, the amplifier was stable and the overall gain observed was in the reasonable range of error which can be verified from the experimental results.

The stability of the circuit also depends on the stability of each of the circuit components. The design requirement states that we need a high impedance amplifier, this is to ensure that very little current is drawn (a circuit drawing high amounts of current is dangerous to work with and can also damage the circuit components for which the current limits will be exceeded), which in turn results in minimal heat loss.

After designing the coupled amplifier, it was important to be able to transfer the voltage to the load safely. An impedance transformer was used to safely transfer the output voltage from the amplifier to the load (speaker), without having to connect it directly to the source of power. It is necessary for impedance matching, where on one side the input impedance is the output impedance of the amplifier and on the output side of the transformer, is the load impedance.

Lastly, it was a fair assumption that the input and output impedance were purely resistive. This is because we were working with only one frequency. The issue with this assumption is that most real world devices have a frequency dependent impedance, which means they have capacitance and inductance apart from resistance as well. In our case, we were using capacitors which have a low impedance at high frequencies, thus having a negligible non-resistive impedance. Another potential issue is that varying the frequency could cause a variance in impedance, which will not be accounted for if we assume the impedance to be purely resistive.

The major difficulty faced was to get the % error between the theoretical and experimental gain below 5%. In the common collector stage, the % error was 7.5% between the theoretical and experimental gain whereas it was 1.5% between the theoretical and simulated gain. The simulated version used the calculated resistance values of R1 and R2, whereas experimentally, even though the same R1 and R2 values were used in the circuit, the gain was different. This was because there were deviations in the values of the DC bias voltage VE found experimentally. Theoretically, VE(CC stage) is 0V, but experimentally, we have a value of 0.1V. Also, there were fluctuations in the DC power supply to the circuit, which was in turn due to fluctuations generated by the transformer.

2.6 Conclusion:

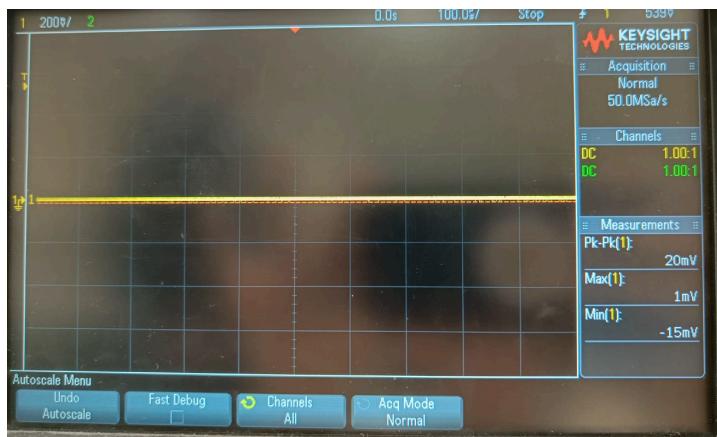
The goal of this project was to build an amplifier with a high input impedance ($>10k$ Ohms) and high voltage gain (11V) using bipolar junction transistors (BJT). We used two types of BJT configurations, common emitter for high voltage gain and common collector for high input impedance. On coupling the amplifiers, the expected output was to get an overall gain of 11 V with 5% margin of error, and our design gave a gain of 10.5 which has a 4% difference from the expected results, thus being within the tolerance limits. Experimentally, our input impedance was found to be 13.0 kOhms, which matches the expectations of having an input voltage $>10k$ Ohms theoretically. Finally, we checked the voltage swing of Vout from the coupled stage and it was found to be 10V peak to peak without clipping at an input voltage of 989 mV peak to peak. All the design requirements were met successfully.

2.7 Tables and Figures

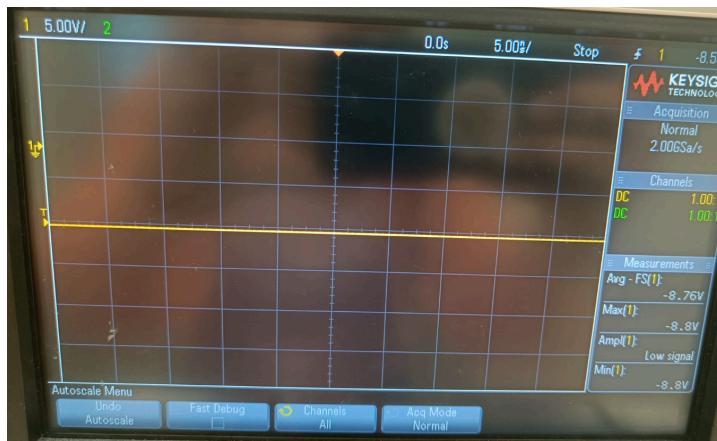
2.7.1 Experimental Observations Images

Lab 2a

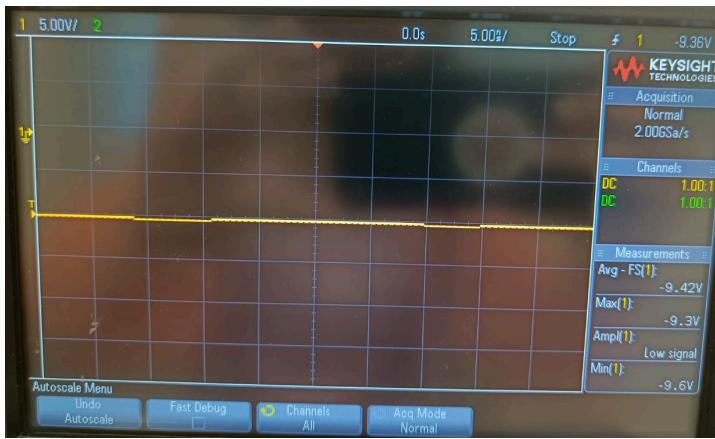
VC



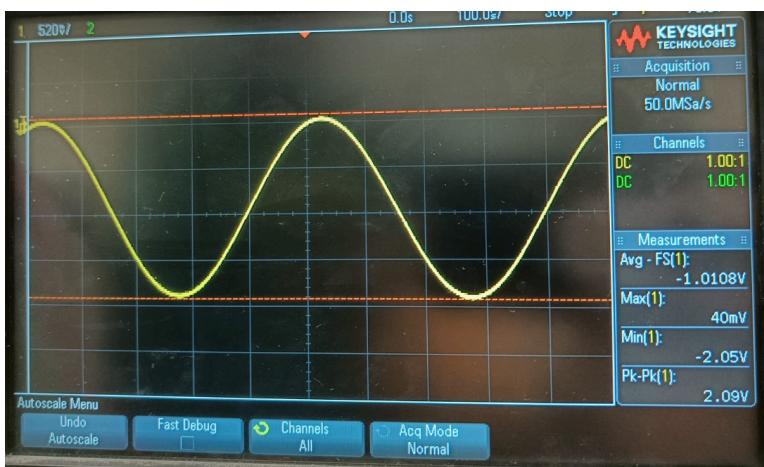
VB



VE

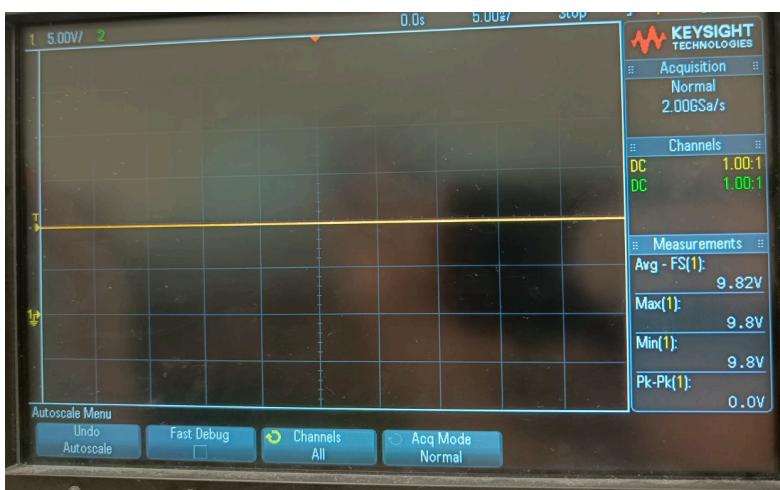


Vout



Lab 2b

VC



VB



VE

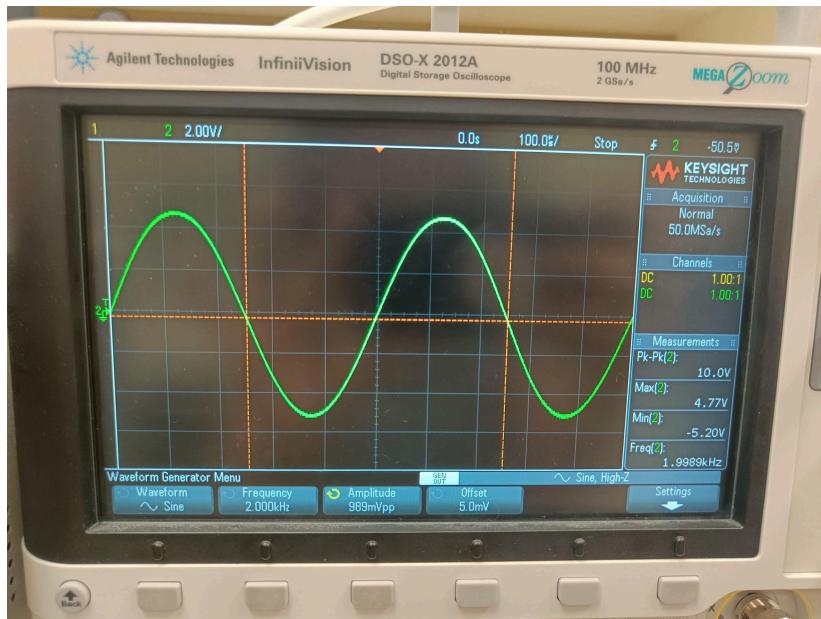


Vout

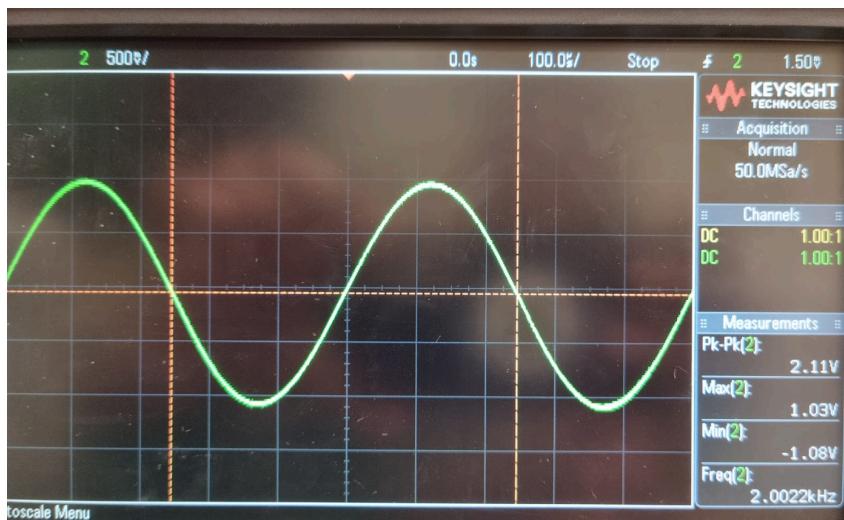


Lab(2c)

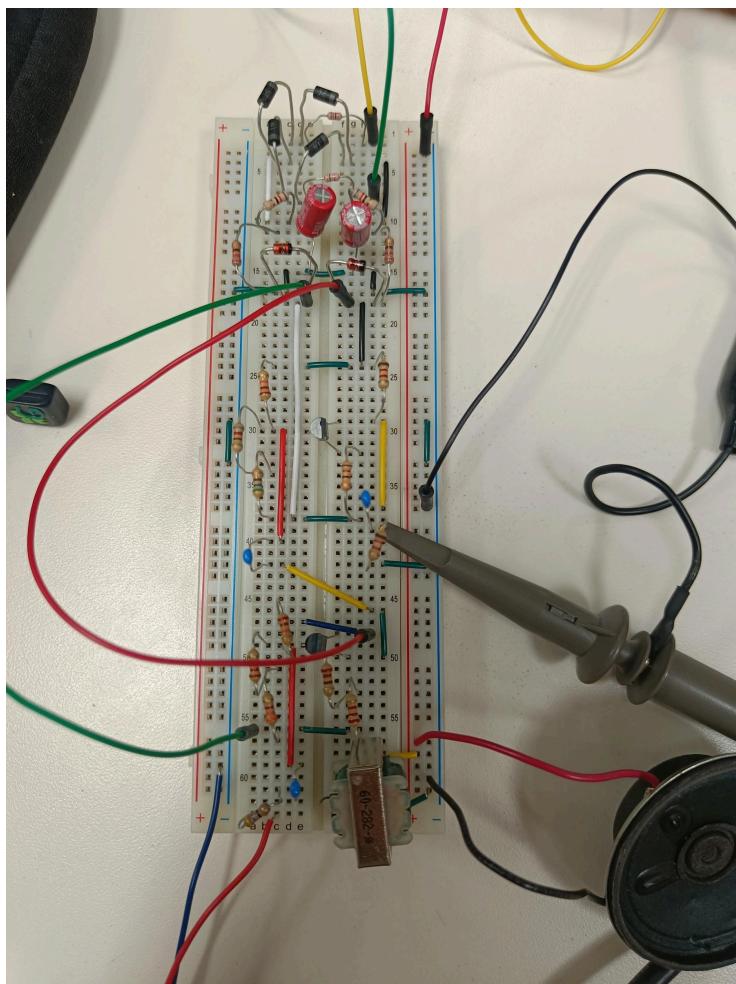
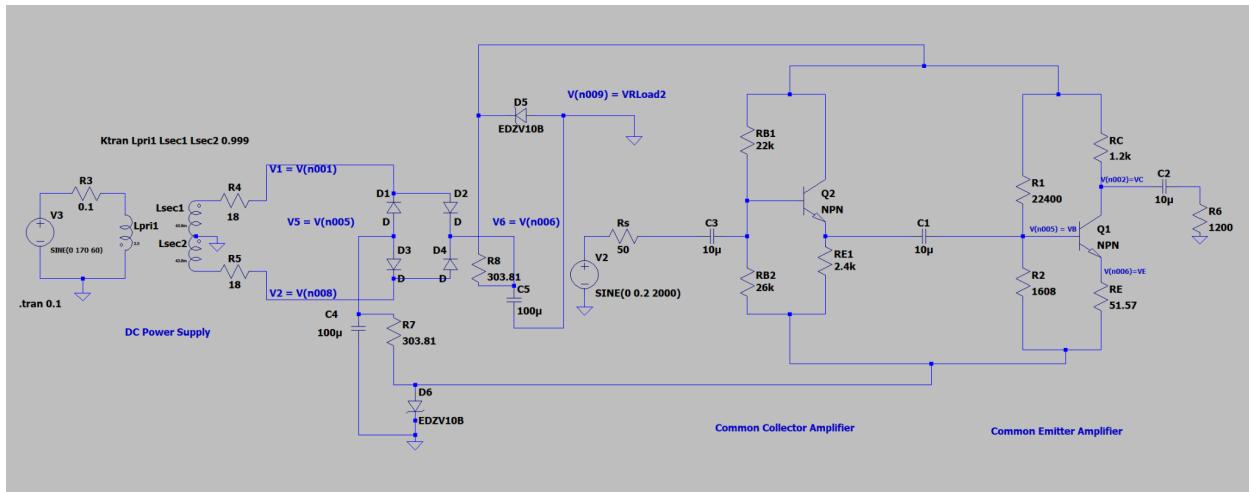
10v pk-pk without clipping



Vout



2.8 Appendix



2.8.1 Calculations:

For CE:

As mentioned earlier in the section 2.2.1, we aimed to ensure maximum power transfer,

$$R_C = R_L = 1.2k\Omega$$

Since we are making the assumption that $I_B=0$, $I_E=I_B+I_C \Rightarrow I_E=I_C$,

$$I_C = I_E = \frac{V-0}{R_C} = \frac{10}{1200} = 8.3mA \quad (\text{eqtn.2.7})$$

$$I_{Bias} = \frac{I_C}{10} = \frac{8.3mA}{10} = 0.83mA \quad (\text{eqtn.2.8})$$

$$r_e = \frac{25mV}{I_E} = \frac{25mV}{8.3mA} = 2.97\Omega \quad (\text{eqtn.2.9})$$

From eqtn 2.1,

$$A_V = \frac{1.2k\Omega || 1.2k\Omega}{2.97\Omega + R_E} = 11$$

$$\Rightarrow R_E = 51.57\Omega$$

$$V_E = I_E \cdot R_E - V = (8.3mA) (51.57\Omega) - 10V \quad (\text{eqtn.2.10})$$

$$\Rightarrow V_E = -9.566V$$

$$V_B = 0.7 + V_E = -8.866V \quad (\text{eqtn.2.11})$$

$$R_1 = \frac{V-V_B}{I_{Bias}} = \frac{10-(-8.866)}{0.833mA} = 22648.3\Omega \quad (\text{eqtn.2.12})$$

$$R_2 = 24k\Omega - R_1 = 1361.34\Omega \quad (\text{eqtn.2.13})$$

Using eqtn 2.2,

$$R_{in,CE} = (22k\Omega || 1.38k\Omega) || [(100 + 1)(2.97 + 68)] = 1298.55\Omega || 7167.97\Omega$$

$$R_{in,CE} = 1099.38\Omega \approx 1k\Omega$$

For CC:-

$$I_{C,\max} = 25mA - I_{C,\max(CE)} = 8.34mA \quad (\text{eqtn.2.14})$$

For max AC swing,

$$I_{C,DC(CC)} = \frac{8.34mA}{2} = 4.17mA \quad (\text{eqtn.2.15})$$

Since $I_B=0$,

$$I_E = I_C = 4.17mA$$

Using eqtn 2.8,

$$I_{Bias} = \frac{I_C}{10} = 0.417mA$$

$$R_E = \frac{0V - (-10)V}{I_E} = \frac{10V}{4.17mA} = 2.39808k\Omega \approx 2.4k\Omega \quad (\text{eqtn.2.16})$$

$$V_{BE} = V_B - V_E$$

Since V_E is assumed to be 0 and $V_{BE}=0.7$,

$$\Rightarrow V_B = 0.7V$$

$$R_2 = \frac{V_B+10}{I_{Bias}} = \frac{10.7V}{0.417mA} = 25.6595k\Omega \approx 26k\Omega \quad (\text{eqtn.2.17})$$

$$I_{Bias}(R_1 + R_2) = V - (-V)$$

$$\Rightarrow R_1 = \frac{2V}{I_{Bias}} - R_2 \quad (\text{eqtn.2.18})$$

$$\Rightarrow R_1 = \frac{20V}{0.417mA} - \frac{10.7V}{0.417mA}$$

$$\Rightarrow R_1 = 22.302k\Omega \approx 22k\Omega$$

Using eqtn 2.5,

$$\Rightarrow R_{in} = (22k\Omega || 26k\Omega) \parallel [(100 + 1)(6\Omega + 2.4k\Omega || 1k\Omega)] = 11916.67\Omega || 71346.4\Omega$$

$$\Rightarrow R_{in} = 10.21k\Omega$$

$$R_{Out,CC} = R_{in,CE} \approx 1k\Omega$$

$$R_{in,CC} = 10.21k\Omega$$

Voltage Gain Calculations

CE gain

$$A_V = \frac{V_{out}}{V_{in}} \quad (\text{eqtn.2.19})$$

$$\%Error = \left| \frac{\text{observed}-\text{actual}}{\text{actual}} \right| \cdot 100 \quad (\text{eqtn.2.20})$$

Using equation 2.19,

$$A_V (\text{experimental}) = \frac{2.09V}{0.200V} = 10.45$$

$$A_V (\text{simulated}) = \frac{2.02V}{0.200V} = 10.1$$

$$A_V (\text{theory}) = 11$$

Using equation 2.20,

Experimental Error:

$$\%Error = \left| \frac{10.45-11}{11} \right| \cdot 100 = 5\%$$

Simulation Error:

$$\%Error = \left| \frac{10.1-11}{11} \right| \cdot 100 = 8\%$$

CC gain

Using equation 2.19,

$$A_V (\text{experimental}) = \frac{0.215V}{0.200V} = 1.075$$

$$A_V (\text{simulated}) = \frac{0.197V}{0.200V} = 0.985$$

$$A_V (\text{theory}) = 1$$

Using equation 2.20,

Experimental Error:

$$\%Error = \left| \frac{1.075-1}{1} \right| \cdot 100 = 7.5\%$$

Simulation Error:

$$\%Error = \left| \frac{0.985-1}{1} \right| \cdot 100 = 1.5\%$$

Coupled gain

Using equation 2.19,

$$A_V (\text{experimental}) = \frac{0.211V}{0.200V} = 10.55$$

$$A_V (\text{simulated}) = \frac{0.240V}{0.200V} = 12$$

$$A_V (\text{theory}) = 11$$

Using equation 2.20,

Experimental Error:

$$\%Error = \left| \frac{10.55 - 11}{11} \right| \cdot 100 = 4\%$$

Simulation Error:

$$\%Error = \left| \frac{12 - 11}{11} \right| \cdot 100 = 9\%$$