ECE 304 Lab 1: Inverter Design
Section: D51
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Abstract:
The purpose of this lab was to design and simulate an inverter in the Cadence environment, while also gaining familiarity with the software itself. Our specific objectives were to determine the propagation time of the inverter signal, as well as the ideal PMOS width for even pull up and pull down strength. Our propagation time, T_{prop}, was 0.16658ns. We used a parametric simulation of 7 steps to find the ideal PMOS width was 150nm. The final inverter design can be used in any future schematic that requires an inverter.

Discussion:

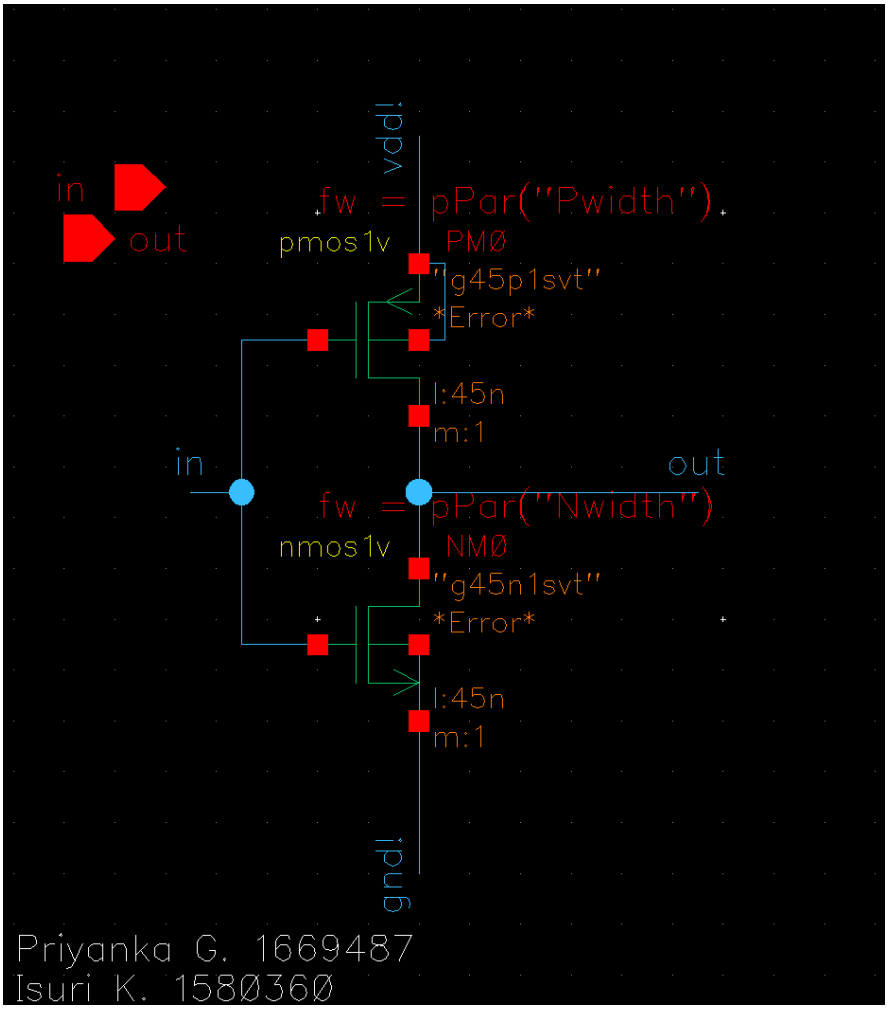

Figure 1: Inverter Schematic

This is the schematic of the designed inverter. The pull up network consists of one PMOS and the pull down network consists of one NMOS, both of type gpdk045. Both have the same input; at once one one of the networks is active. These MOSFETS have different widths Pwidth and

Nwidth to make their pull strengths equal. Source of the PMOS is connected to Vdd, source of NMOS is connected to GND.

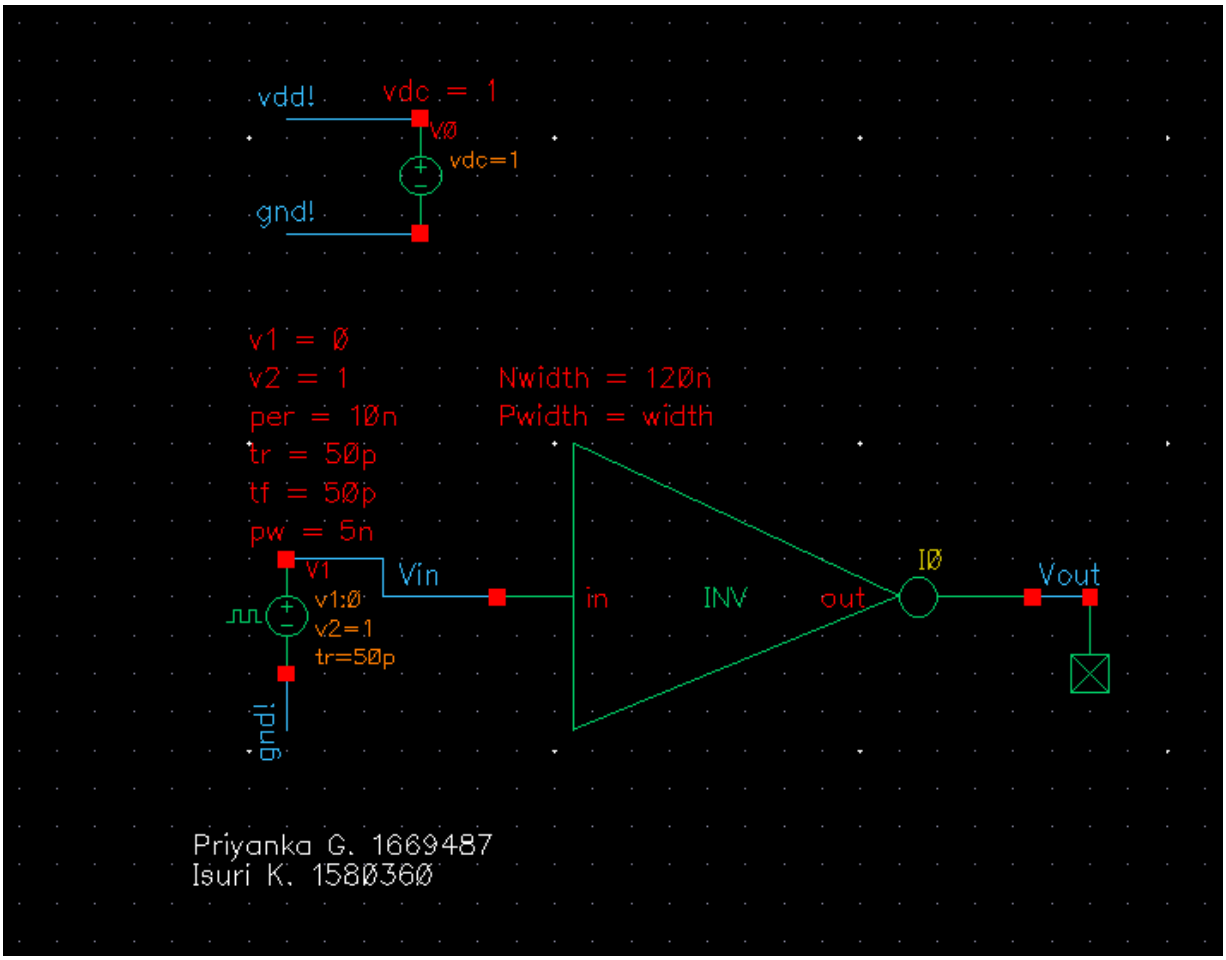

Figure 2: Inverter Test Bench Schematic

The above schematic shows the setup of the inverter before we test it with different parameters. It is attached to a DC power supply of 1V. The input signal is a transient pulse signal which cycles from 0V to 1V, with rise and fall time of 50ps. The pulse width is 5ns and the the period is 10ns.

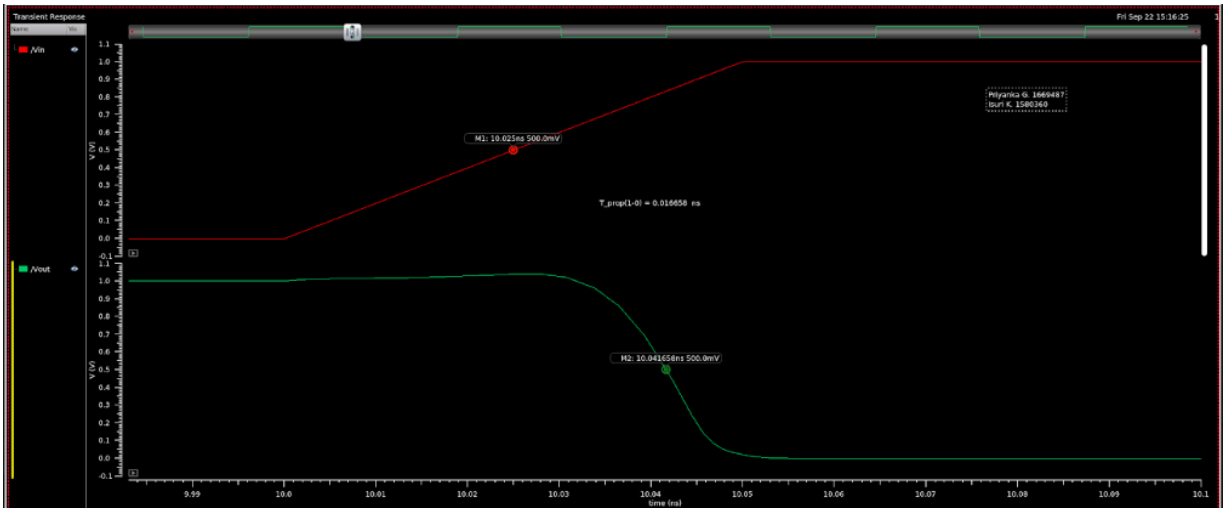

Figure 3: Inverter Transient Response Plot, zoomed in on edges with a Tprop marker

This is a transient analysis plot which was generated with an aim to calcute the propagation delay of MOSFETs. We have plotted Vout and Vin vs Time. As this is an inverter, Vout wave is the inverted version of your Vin wave. Our point of interest is Vdd/2 because this is where Vin crosses Vout. The difference between the time coordinates at Vdd/2 for the Vout and Vin signals gives us the propogation delay. T prop(1 − 0) is the propagation time of the inverter, which is the time taken by the signal to be received.Since this is Voltage vs Time plot, M2x - M1x is the propagation time of the signal (These are the x-coordinates of when the input and output signals are both 5V). Our graph tells us that Tprop(1-0) ~ 0.016 ms.

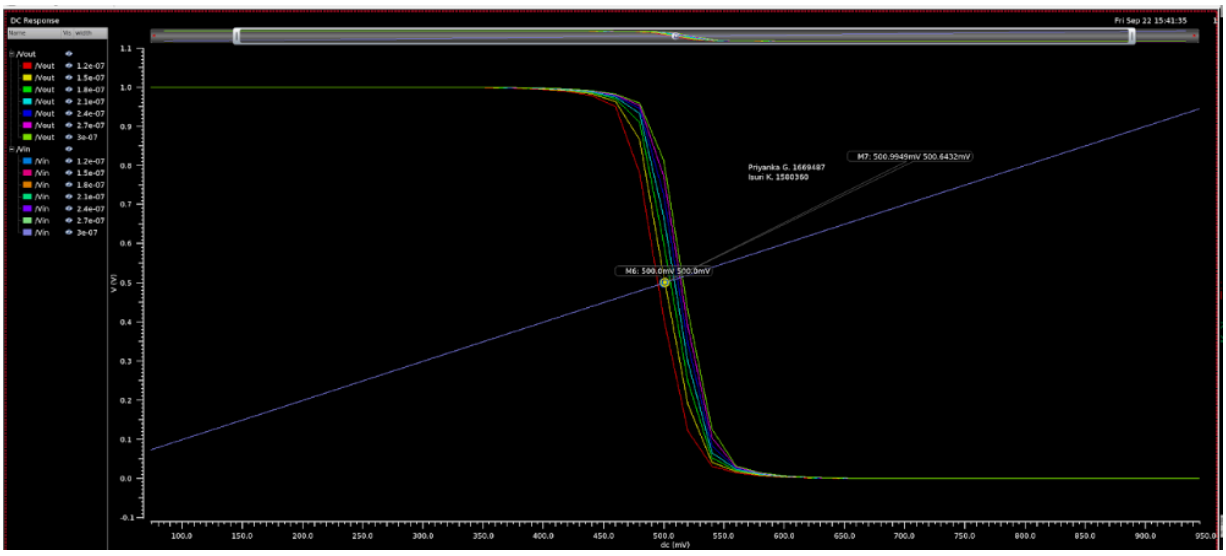

Figure 4: Simulation Results of Varying PMOS widths applied to the inverter

The above screenshot shows the simulation results when 7 different PMOS widths are simulated in our inverter; this is a parametric simulation. We are interested in finding the PMOS width for

which Vout crosses over the Vin line at ~0.5V. The plot tells us that the yellow line, with PMOS width 150nm is the desired width. We used a marker to mark this width that gave the best PMOS to NMOS ratio that achieves even pull up and pull down strength. We observe that PMOS should have a width of 150nm which is 1.25 times the width of the NMOS.

Questions:

1. What are two reasons to use Wire Labels?
   The first reason to use wire labels is so we know which signals are connected to which wires. Another reason is for ease of wire identification; if a wire is accurately labeled we can find it quickly if given a warning for it.

2. Where do you always connect the bulk terminals for digital transistors?
   For NMOS transistors, the bulk terminal should be connected to ground. For PMOS transistors, the bulk terminal should be connected to the highest voltage available, typically V_{DD}.

3. Why are instance names important?
   Instance names help us in assigning unique identifiers to each instance. They are necessary to distinguish instances of the same type. They also make documentation easy, make designs easier to understand and make designs reusable.

4. What is a netlist?
   A netlist is a description of all the connections in the circuit diagram, listing all the components and the nodes they are connected to. It is a textual representation of the circuit.