Design and implementation of a SD Host Controller

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1 Overview

The SD(Secure Digital) Card is a flash memory card that is specifically designed to meet the security, capacity, performance, and environment requirements inherent in newly emerging audio and video consumer electronic devices.This paper discusses about the design of the SD Host Controller that compatible with SDSC/SDHC/SDXC cards. The processor associated with the design will be the AJIT (a 32-bit general purpose processor designed in IIT-Bombay).

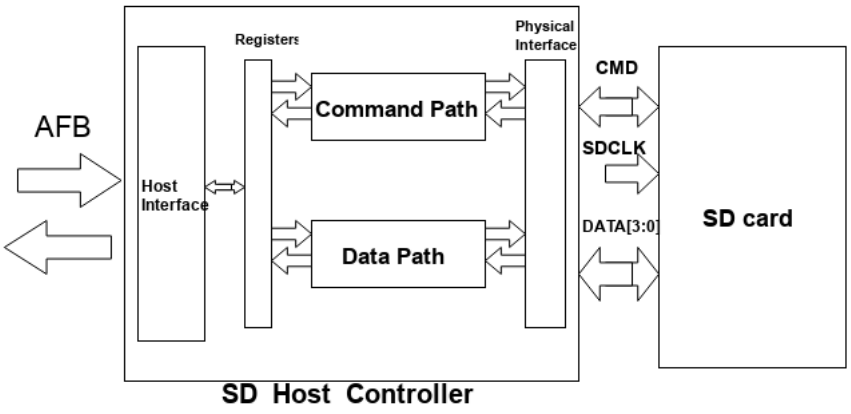

Figure 1: Block Diagram of Host Controller

2 Internals of the SD card

2.1 SD Card Registers

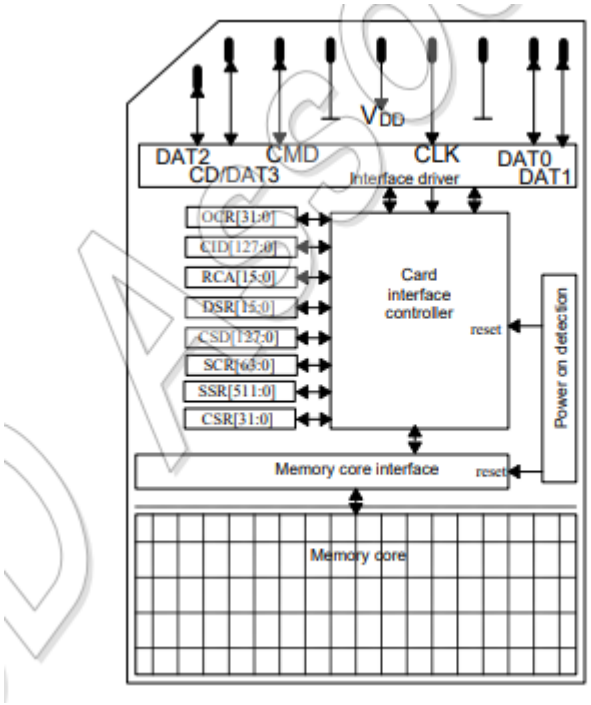

Figure 2: SD Memory Card Architecture.

Name	Width	Description
CID	128	Card Identification; card individual number for identification.
RCA	16	Relative card address;. local system address of a card, dynamically suggested by the card and approved by the host during initialization.
CSD	128	Card Specific Data; information about the SD Memory Card's Special Features capabilities.
SCR	64	SD Configuration Register; information about the SD Memory Card's Special Features capabilities.
OCR	32	Operation condition register.
SSR	512	SD Status; information about the card proprietary features.
CSR	32	Card Status; information about the card status.

2.1.1 CID register

The Card Identification(CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual READ/WRITE(RW) card shall have a unique identification number.

2.1.2 RCA register

The writable 16-relative card address register carries card the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after card identification procedure.The default value of RCA register is 0x0000.

2.1.3 CSD register

The Card-Specific Data register provides information regarding access to the card contents. The CSD defines the data format, error correction type, maximum data access time, etc.The programmable part of the register can be changed by the CMD27.

2.1.4 SCR register

SCR register provides information on the SD Memory Card's special features that were configured into the given card. The size of SCR register is 64 bits. This register shall be set in the factory by the SD Memory Card manufacture.

2.1.5 OCR register

The 32-bit operation conditions register stores the VDD voltage profile of the card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit.

2.1.6 SSR register

The 512 bit register gives information about the card proprietary features.

2.1.7 CSR register

This 32-bit register gives information about the current status of the card.

3 Basic read/write operation

CMD17, CMD18 : Single and multiple block read command.
CMD24, CMD25 : Single and multiple block write command.
Note that the below figure shows only one data line but it can also work in 4bit bus mode. More detailed description of commands and responses are in their respective sections.

4 Interface Description

4.1 Clock, Reset Interfaces

- A single clock signal Clk comes as input. The controller is a positive edge-triggered.
- A single active-high synchronous reset signal as input.

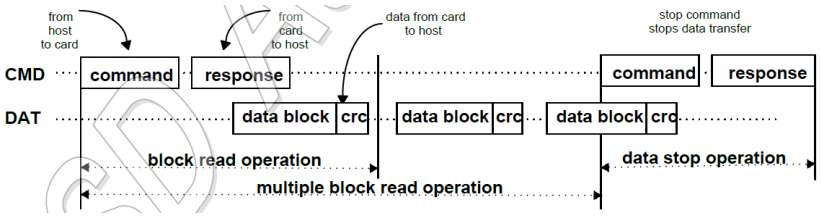

Figure 3: Block Read

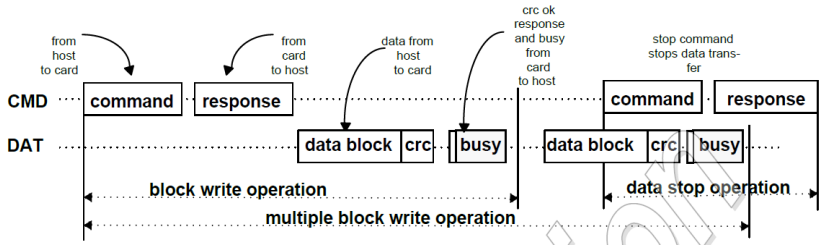

Figure 4: Block Write

4.2 Processor Side Interface

On the processor side, there is AJIT 32-bit FIFO Bus Interface. It has a request FIFO interface and a response FIFO interface.

4.2.1 Request FIFO Interface

GENERIC_CORE_AFB_REQUEST_pipe_write_data:**IN (73: 0)**;
GENERIC_CORE_AFB_REQUEST_pipe_write_req: **IN(0:0)**;
GENERIC_CORE_AFB_REQUEST_pipe_write_ack : **OUT(0:0)** ;

The AFB_REQUEST_pipe_write_data has the following bit-fields:
Bit 73: lock bit
Bit 72: read/write-bar
Bits 71-68: Byte-mask
A 4-bit byte-mask indicating which bits from the data field to be written. The most significant bit corresponds to the most significant byte.
Bits 67-32: Physical address
Bits 31-00: Write-data

The AFB_REQUEST_pipe_write_req is asserted by AJIT core if it has data to present.

The AFB_REQUEST_pipe_write_ack is asserted when the controller is able to accept data.

4.2.2 AFB Response

GENERIC_CORE_AFB_RESPONSE_pipe_read_data: **OUT (32:0)**;
GENERIC_CORE_AFB_RESPONSE_pipe_read_req : **IN(0:0)**;

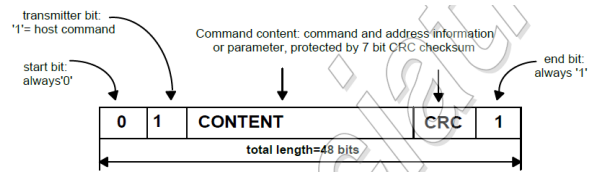

Figure 5: Command format

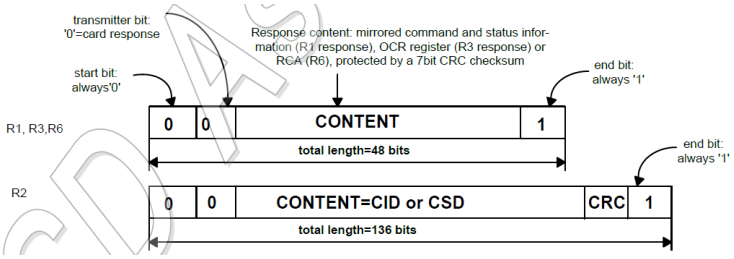

Figure 6: Response format

GENERIC_CORE_AFB_RESPONSE_pipe_read_ack : **OUT(0:0)**;

The AFB_RESPONSE_pipe_read_data has the following bit-fields:
Bits 32: Error-bit
Bits 31-00: Read-Data

The AFB_RESPONSE_pipe_read_req is asserted by AJIT Core when it is ready to accept data.

The AFB_RESPONSE_pipe_read_ack is asserted by the host controller when it is ready to send data.

4.3 SD Card Bus Interface

SD_CLK: **OUT (0:0)**;
Provides clock to the SD card.
CMD: **INOUT(0:0)**;
A **bidirectional** wire that is used to send commands serially to the card and receive their corresponding responses from the addressed card to the host.The CMD signal operates in push-pull mode.
DAT : **INOUT(3:0)**;
A **bidirectional** bus used to transmit data from the host to the card and vice versa. The DAT signal operates in push-pull mode. The 4th bit in transfer mode register indicates the direction of data transfers
1 : read (card to host)
0 : write (host to card)

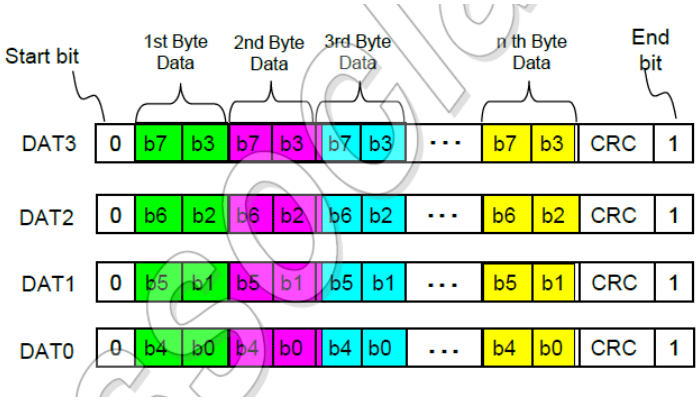

Figure 7: Four bit bus

5 SD Host Standard Registers

Following are the registers of the SD device.These registers can be accessed by the SD Host for all operations.

5.1 Register Attributes

- **RO** : Read-only register, register bits cannot be altered by software or any reset operation. Writes are ignored.
- **ROC** : Read only status, these bits are initialized to zero. Writes are ignored.
- **RW** : Read Write register, it could be set or cleared by software or any reset signal.
- **RW1C** : Read-only status, Write-1-to-clear status: Register bits indicate status when read, a set bit indicating a status event may be cleared by writing a 1. Writing a 0 to RW1C bits has no effect.
- **RWAC** : Read-Write, automatic clear register: The Host Driver requests a Host Controller operation by setting the bit. The Host Controllers shall clear the bit automatically when the operation is complete. Writing a 0 to RWAC bits has no effect.
- **HwInit** : Hardware Initialized: Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial EEPROM. Bits are read-only after initialization, and writes to these bits are ignored.
- **Rsvd** : Reserved. These bits are initialized to zero, and writes to them are ignored.
- **WO** : Write-only register. It is not physically implemented register. Rather, it is an address at which registers can be written.

Note that the Host Controller shall set all registers to their initial values at power-on reset. Initial values of the register are defined as follows.

Sl. No	Registers	Width	Address Offset
1	Argument 2 register	32	0x0
2	Block Size Register	16	0x4
3	Block Count Register	16	0x6
4	Argument Register	32	0x8
5	Transfer Mode Register	16	0xC
6	Command Register	16	0xE
7	Response0 Register	32	0x10
8	Response2 Register	32	0x14
9	Response4 Register	32	0x18
10	Response6 Register	32	0x1c
11	Buffer Data Port Register	32	0x20
12	Present State Register	32	0x24
13	Host Control Register	8	0x28
14	Power Control Register	8	0x29
15	Block Gap Control Register	8	0x2A
16	Wakeup Control Register	8	0x2B
17	Clock Control Register	16	0X2C
18	Timeout Control Register	8	0X2E
19	Software Reset Register	8	0X2F
20	Normal Interrupt Status Register	16	0x30
21	Error Interrupt Status Register	16	0x32
22	Normal Interrupt Status Enable Register	16	0x34
23	Error Interrupt Status Enable Register	16	0x36
24	Normal Interrupt Signal Enable Register	16	0x38
25	Error Interrupt Signal Enable Register	16	0x3A
26	Auto CMD error status Register	16	0x3C
27	Host Control 2 Register	16	0x3E
28	Capabilities Register	32	0X40
29	Host Controller Version Register	16	0XFE

- All registers default value shall be set to zero.
- Values of the Capabilities register and Maximum Current Capabilities register depends on the Host Controller.
- Value of the Host Controller Version register depends on the Host Controller.
- The reserved bits of the registers are kept for future use, as of now they can be set to '0'.

5.2 Argument 2 register

Location	Attribute	Function
Offset + (31-00)	RW	**Argument 2** This register is used with Auto CMD23 field in transfer mode register to set a 32-bit block count value to the argument of CMD23.

5.3 Block Size Register (Offset 004h)

This register is used to configure the number of bytes in a data block.

Location	Attribute	Function
Offset + 15	Rsvd	RESERVED
Offset + (14-12)	RW	Used for SDMA (not required)
Offset + (11-0)	RW	**Transfer Block Size** : This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. For SD memory cards, it shall be set up to 512 bytes(0x200). It can be accessed only if no transaction is executing.

5.4 Block Count Register (Offset 006h)

This register is used to configure the number of data blocks.

Location	Attribute	Function
Offset + (15-00)	RW	**Blocks Count For Current Transfer** : This register is enabled when Block Count Enable in the *Transfer Mode register* is set to 1 and is valid only for multiple block transfers The **Host Driver** shall set this register to a value between 1 and the maximum block count. This register should be accessed only when no transaction is executing

5.5 Argument Register (Offset 008h)

Location	Attribute	Function
Offset + (31-00)	RW	Command Argument The SD Command Argument is specified as bit39-8 of Command-Format in the Physical Layer Specification.

5.6 Transfer Mode Register (Offset 00Ch)

This register is used to control the operation of data transfers. The Host Driver shall set this register before issuing a command which transfers data, or before issuing a Resume command.

Location	Attribute	Register Field Explanation
Offset + (15-06)	Rsvd	**Reserved**
Offset + 05	RW	**Multi/Single Block Select** this bit is set when issuing multiple-block transfer commands using DAT line.
Offset + 04	RW	**Data Transfer Direction Select** This bit defines the direction of DAT line data transfer. 1 : read (card to host)
Offset + (03-02)	Rsvd	**Auto CMD Enable** This field determines the use of auto command functions. (1)01 : Auto CMD12 Enable (2)10 : Auto CMD23 Enable (3)00 : Auto command disabled (4)11 : reserved These two are the methods to stop multiblock transfers
Offset + 01	RW	**Block Count Enable**
Offset + 00	RW	**DMA Enable** (Not used) DMA is not supported, this bit shall always read 0.

The below table shows the summary of how register settings determine types of data transfer.

Multi/Single Block Select	**Block Count Enable**	**Block Count**	**Function**
0	Don't care	Don't care	Single Transfer
1	0	Don't care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

5.7 Command Register (Offset 00Eh)

The Host Driver shall check the **Command Inhibit (DAT)** bit and **Command Inhibit (CMD)** bit in the Present State register before writing to this register. Writing to the upper byte of this register triggers SD command generation. The Host Driver has the responsibility to write this register because the Host Controller does not protect for writing when **Command Inhibit (CMD)** is set.

Location	Attribute	Register Field Explanation
Offset + (15-14)	Rsvd	**Reserved**
Offset + (13-08)	RW	**Command Index** This is a 6-bit binary value corresponds to one of the 64 commands available (CMD,ACMD).
Offset + (07-06)	RW	**Command Type** There are three special commands available 11 : Abort(CMD12) 10 : Resume(CMD52) 01 : Suspend(CMD52) 00 : For all other normal commands
Offset + 05	RW	**Data Present select** High value indicates that data is present and shall be transferred using DAT line.
Offset + 04	RW	**Command Index Check Enable** High value indicates that the host controller shall check the command index in response and compare it to the command index of command also.
Offset + 03	RW	**Command CRC Check Enable** High value indicates that the host controller shall check the crc bits in response and compare it to the crc bits of command also.
Offset + 02	Rsvd	**Reserved**
Offset + (01-00)	RW	**Response Type Select** 00 : no response 01 : Response length 136 10 : Response length 48 11 : Response length 48 check busy after response

Response Type	Index Check Enable	CRC Check Enable	Name of Response Type
00	0	0	No Response
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R5, R6, R7
11	1	1	R1b, R5b

Figure 8: Caption

5.8 Response Register(Offset 010h)

This register is used to store response from SD cards.

Location	Attribute	Register Field Explanation
Offset + (127-00)	ROC	**Command Response**

Kind of Response	Meaning of Response	Field	Register
R1,R1b(normal response)	Card Status	R[39:8]	REP[31:0]
R1b (Auto CMD12 response)	Card Status for Auto CMD12	R[39:8]	REP[127:96]
R1 (Auto CMD23 response)	Card Status for Auto CMD23	R[39:8]	REP[127:96]
R2 (CID, CSD register)	CID or CSD reg. incl.	R[217:8]	REP[119:0]
R3 (OCR register)	OCR register for memory	R [39:8]	REP [31:0]
R4 (OCR register)	OCR register for I/O etc	R [39:8]	REP [31:0]
R5,R5b	SDIO response	R [39:8]	REP [31:0]
R6 (Published RCA response)	New published RCA[31:16] etc	R [39:8]	REP [31:0]

5.9 Buffer Data Port Register(Offfset 020h)

32 bit data port register to access internal buffer.

Location	Attributes	Register Field Explanation
Offset + (31-00)	RW	The Host Controller Buffer can be accessed through this register.

5.10 Present State Register (Offset 024h)

The Host Driver can get status of the Host Controller from this 32-bit read only register.

Location	Attributes	Register Field Explanation
Offset + (31-25)	Rsvd	**Reserved**
Offset + 24	RO	**CMD Line Signal Level** Used for checking CMD line levels to recover from errors
Offset + (23-20)	RO	**DAT[3:0] Line Signal Level** Used to recover from error and also for detecting busy signal
Offset + 19	RO	**Write Protect Switch Pin Level** 1 indicates it is write protected. It reflects the SDWP pin
Offset + 18	RO	**Card Detect Pin Level** 1 indicates that the card is present.
Offset + 17	RO	**Card State Stable** 0 indicates that **Card detect pin level** is not stable.
Offset + 16	RO	**Card Inserted** 1 indicates that card is inserted
Offset + (15-12)	Rsvd	**Reserved**
Offset + 11	ROC	**Buffer Read Enable** If this bit is 1 readable data exists inside the buffer. 1 to 0 transition occurs if all data has been read. 1:Read enable
Offset + 10	ROC	**Buffer Write Enable** If this bit is 1 data can be written to the buffer. 1 to 0 transition occurs if all the data has been written into the buffer. 1:Write enable
Offset + 9	ROC	**Read transfer Active** This status is used for dectecting completion of read . transfer. This bit is set to 1 for either of the following conditions: (1) After the end bit of the read command. (2) When read operation is restarted by writing a 1 to **Continue Request** in the Block gap control register.
Offset + 8	ROC	**Write Transfer Active** This status is used for dectecting completion of write transfer. This bit is set to 1 for either of the following conditions: (1) After the end bit of the write command. (2) When read operation is restarted by writing a 1 to **Continue Request** in the Block gap control register.
Offset + (7-4)	Rsvd	**Reserved**
Offset + 3	ROC	**Re-Tuning Request** 1:Sampling clock needs re-tuning
Offset +2	ROC	**DAT line Active** While reading, Changing this value from 1 to 0 generates a **Block Gap Event interrupt** in the Normal Interrupt Status register as the result of the **Stop At Block Gap Request** being set. While reading, Changing this value from 1 to 0 generate a **Transfer Complete** interrupt in the Normal Interrupt Status register.
Offset + 1	ROC	**Command Inhibit (DAT)** This status bit is generated if either the **DAT Line Active** or the **Read Transfer Active** is set to 1. If this bit is 0, it indicates the Host Controller can issue the next SD Command.
Offset + 0	ROC	12 **Command Inhibit (CMD)** If this bit is 0, it indicates the **CMD** line is not in use and the Host Controller can issue a SD Command using the **CMD** line.

5.11 Host Control Register (Offset 028h)

Location	Attributes	Register Field Explanation
Offset + 7	RW	**Card Detect Signal Selection** Card insertion can be detected in two ways 1 : Card detect test level(for testing purpose) 0 : SDCD pin(for normal use)
Offset + 6	RW	**Card Detect Test Level** 1 : card inserted 0 : no card
Offset + 5	RW	**Extended Data Transfer Width** 1 : 8-bit bus width 0 : Bus width decided by **Data transfer width**
Offset + (4-3)	RW	**DMA Select**
Offset + 2	RW	**High Speed Enable** 1 : High speed mode 0 : Default mode In high speed mode HC can supply CMD and DAT at rising edge up to 50Mhz. In default mode the HC supplies CMD and DAT up to 25MHZ on falling edge
Offset + 1	RW	**Data Transfer Width** 1 : 4-bit mode 0 : 1-bit mode
Offset + 0	RW	**LED Control** 1 : LED ON, indicates that the card should not be removed

5.12 Power Control Register (Offset 029h)

Location	Attributes	Register Field Explanation
Offset + (07-04)	Rsvd	**Reserved**
Offset + (03-01)	RW	**SD Bus Volatge Select** 111 : 3.3V 110 : 3V 101 : 1.8V others : reserved
Offset + 00	RW	**SD Bus Power** 1 indicates bus is ON.

5.13 Block Gap Control Register (Offset 02Ah)

Location	Attributes	Register Field Explanation
Offset + (07-04)	Rsvd	**Reserved**
Offset + 03	RW	**Interrupt At Block Gap** (Not required) This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle.
Offset + 02	RW	**Read Wait Control**(Not required) The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using the **DAT**[2] line.
Offset + 01	RWAC	**Continue Request** This bit is used to restart a transaction, which was stopped using the **Stop At Block Gap Request.**
Offset + 00	RW	**Stop At Block Gap Request** This bit is used to stop executing read and write transaction at the next block gap for all transfers

5.14 Wakeup Control Register

Location	Attribute	Function
Offset + (7-3)	Rsvd	Reserved
Offset + (2)	RW	**Wakeup event enable of SD card removal** This bit enables wakeup event via Card Removal assertion in the Normal Interrupt.
Offset + (1)	RW	**Wakeup event enable on SD card insertion** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status Register
Offset + (0)	RW	**Wakeup event enable on card interrupt** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt status register.

5.15 Clock Control Register (Offset 02Ch)

At the initialization of the Host Controller, the Host Driver shall set the SDCLK Frequency Select according to the Capabilities register.

Location	Attributes	Register Field Explanation
Offset + (15-08)	RW	**SD Clock Frequency Set** **10-bit Divided Clock Mode** 3FFh 1/2046 Divided Clock .... N 1/2N Divided Clock (Duty 50%) .... 002h 1/4 Divided Clock 001h 1/2 Divided Clock 000h Base Clock (10MHz-255MHz)
Offset + (07-06)	RW	**Upper Bits of SDCLK Frequency Select** these bits to expand SDCLK Frequency Select to 10-bit. Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select.
Offset + (05-03)	RO	**Reserved**
Offset + 02	RW	**SD Clock Enable** The Host Controller shall stop SDCLK when writing this bit to 0. SDCLK Frequency Select can be changed when this bit is 0. Then, the Host Controller shall maintain the same clock frequency until SDCLK is stopped (Stop at SDCLK=0). If the Card Inserted in the Present State register is cleared, this bit shall be cleared. 1-Enable 0-Disable
Offset + 01	ROC	**Internal Clock Stable** This bit is set to 1 when SD Clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1. 1 – Ready 0 – Not Ready
Offset + 00	RW	**Internal Clock Enable** This bit is set to 0 when the Host Driver is not using the Host Controller or the Host Controller awaits a wakeup interrupt. The Host Controller should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the Host Controller shall set Internal Clock Stable in this register to 1. This bit shall not affect card detection. 1-Oscillate 0-Stop

5.16 Timeout Control Register (Offset 02Eh)

At the initialization of the Host Controller, the Host Driver shall set the Data Timeout Counter Value according to the Capabilities register.

Location	Attributes	Register Field Explanation
Offset + (07-04)	Rsvd	**Reserved**
Offset + (03-00)	RW	**Data Timeout Counter Value** This value determines the interval by which DAT line timeouts are detected. For more information about timeout generation, refer to the Data Timeout Error in the Error Interrupt Status register. Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register) 0000b- TMCLK X 2^{13} 0001b- TMCLK X 2^{14} 0010b- TMCLK X 2^{15} . . . . 1110b- TMCLK X 2^{27} 1111b- Reserved

5.17 Software Reset Register (Offset 02Fh)

A reset pulse is generated when writing 1 to each bit of this register. After completing the reset, the Host Controller shall clear each bit. Because it takes some time to complete software reset, the SD Host Driver shall confirm that these bits are 0.

Location	Attributes	Register Field Explanation
Offset + (07-03)	Rsvd	**Reserved**
Offset + 02	RW	**Software Reset for DAT Line** The following registers and bits are cleared by this bit: *Buffer Data Port register* Buffer is cleared and initialized. *Present State register* **Buffer Read Enable** **Buffer Write Enable** **Read Transfer Active** **Write Transfer Active** **DAT Line Active** **Command Inhibit (DAT)** *Block Gap Control register* **Continue Request** **Stop At Block Gap Request** *Normal Interrupt Status register* **Buffer Read Ready** **Buffer Write Ready** **Block Gap Event** **Transfer Complete** 1 Reset 0 Work
Offset + 01	RW	**Software Reset for CMD Line** Only part of command circuit is reset. The following registers and bits are cleared by this bit: *Present State register* **Command Inhibit (CMD)** *Normal Interrupt Status register* **Command Complete** 1 Reset 0 Work
Offset + 00	RWAC	**Software Reset for all** This reset affects the entire Host Controller except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the Host Driver shall set this bit to 1 to reset the Host Controller. The Host Controller shall reset this bit to 0 when Capabilities registers are valid and the Host Driver can read them. Additional use of Software Reset For All may not affect the value of If this bit is set to 1, the host driver should issue reset command and reinitialize the SD card. 1-Reset 0-Work

5.18 Normal Interrupt Status Register(Offset 030h)

Location	Attributes	Register Field Explanation
Offset + 15	ROC	**Error Interrupt**
Offset + (14-13)	Rsvd	**Reserved**
Offset + 12	ROC	**Re-Tuning Event Status Enable**
Offset + 11	ROC	**INT-C Status Enable**
Offset + 10	ROC	**INT-B Status Enable**
Offset + 9	ROC	**INT-A Status Enable**
Offset + 8	ROC	**Card Interrupt Status Enable**
Offset + 7	RW1C	**Card Removal Status Enable**
Offset + 6	RW1C	**Card Insertion Status Enable**
Offset + 5	RW1C	**Buffer Read Ready Status Enable**
Offset + 4	RW1C	**Buffer Write Ready Status Enable**
Offset + 3	RW1C	**DMA Interrupt Status Enable**(Not required)
Offset + 2	RW1C	**Block Gap Event Status Enable**
Offset + 1	RW1C	**Transfer Complete Status Enable**
Offset + 0	RW1C	**Command Complete Status Enable**

5.19 Error Interrupt Status Enable Register(Offset 032h)

Location	Attributes	Register Field Explanation
Offset + (15-12)	RW	**Vendor Specific Error Status Enable**
Offset + 11	Rsvd	**Reserved**
Offset + 10	RW	**Tuning Error Status Enable**
Offset + 9	RW	**ADMA Error Status Enable**(Not required)
Offset + 8	RW	**Auto CMD Error Status Enable**
Offset + 7	RW	**Current Limit Error Status Enable**
Offset + 6	RW	**Data End Bit Error Status Enable**
Offset + 5	RW	**Data CRC Error Status Enable**
Offset + 4	RW	**Data Timeout Error Status Enable**
Offset + 3	RW	**Command Index Error Status Enable**
Offset + 2	RW	**Command End Bit Error Status Enable**
Offset + 1	RW	**Command CRC Error Status Enable**
Offset + 0	RW	**Command Timeout Error Status Enable**

5.20 Normal Interrupt Status Enable Register (Offset 034h)

Setting corresponding bits to 1 enables Interrupt Status. A '0' corresponds to the following bit masked.

Location	Attributes	Register Field Explanation
Offset + (15-13)	RO	Reserved.
Offset + 12	RW	Re-tuning Event Status Enable
Offset + (11-09)	RO	Reserved.
Offset + 08	RW	Card Interrupt Enable.
Offset + 07	RW	Card Removal Status Enable.
Offset + 06	RW	Card Insertion Status Enable.
Offset + 05	RW	Buffer Read Ready Status Enable.
Offset + 04	RW	Buffer Write Ready Status Enable.
Offset + 03	RW	DMA Interrupt Status Enable.
Offset + 02	RW	Block Gap Event Status Enable.
Offset + 01	RW	Transfer Complete Status Enable.
Offset + 00	RW	Command Complete Status Enable.

5.21 Error Interrupt Status Enable Register (Offset 036h)

Setting corresponding bits to 1 enables Interrupt Status. A '0' corresponds to the following bit masked.

Location	Attributes	Register Field Explanation
Offset + (15-11)	RO	Reserved.
Offset + 10	RW	Tuning Error Status Enable.
Offset + 09	RW	ADMA Error Status Enable.
Offset + (08-07)	R0	Reserved.
Offset + 06	RW	Data End Bit Error Status Enable.
Offset + 05	RW	Data CRC Error Status Enable.
Offset + 04	RW	Data Timeout Error Status Enable.
Offset + 03	RW	Command Index Error Status Enable.
Offset + 02	RW	Command End Bit Error Status Enable.
Offset + 01	RW	Command CRC Error Status Enable.
Offset + 00	RW	Command Timeout Error Status Enable.

5.22 Normal Interrupt Signal Enable Register (Offset 038h)

This register is used to select which interrupt status is indicated to the Host System as the interrupt. These status bits all share the same1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Location	Attributes	Register Field Explanation
Offset + (15-13)	RO	Reserved.
Offset + 12	RW	Re-tuning Event Signal Enable
Offset + (11-09)	RO	Reserved.
Offset + 08	RW	Card Interrupt Signal Enable.
Offset + 07	RW	Card Removal Signal Enable.
Offset + 06	RW	Card Insertion Signal Enable.
Offset + 05	RW	Buffer Read Ready Signal Enable.
Offset + 04	RW	Buffer Write Ready Signal Enable.
Offset + 03	RW	DMA Interrupt Signal Enable.
Offset + 02	RW	Block Gap Event Signal Enable.
Offset + 01	RW	Transfer Complete Signal Enable.
Offset + 00	RW	Command Complete Signal Enable.

5.23 Error Interrupt Signal Enable Register (Offset 03Ah)

This register is used to select which interrupt status is notified to the Host System as the interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1 enables interrupt generation.

Location	Attributes	Register Field Explanation
Offset + (15-11)	RO	Reserved.
Offset + 10	RW	Tuning Error Signal Enable.
Offset + 09	RW	ADMA Error Signal Enable.
Offset + (08-07)	R0	Reserved.
Offset + 06	RW	Data End Bit Error Signal Enable.
Offset + 05	RW	Data CRC Error Signal Enable.
Offset + 04	RW	Data Timeout Error Signal Enable.
Offset + 03	RW	Command Index Error Signal Enable.
Offset + 02	RW	Command End Bit Error Signal Enable.
Offset + 01	RW	Command CRC Error Signal Enable.
Offset + 00	RW	Command Timeout Error Signal Enable.

5.24 Host Control 2 Register (Offset 03Eh)

Location	Attributes	Register Field Explanation
Offset + 15	RW	**Preset Value Enable** If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver.
Offset + 14	RW	**Asynchronous Interrupt Enable** This bit can be set to 1 if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register.
Offset + (13-08)	Rsvd	**Reserved**
Offset + 7	RW	**Sampling Clock Select** Tuned clock is used to sample data then this bit is 1.
Offset + 6	RWAC	**Execute Tuning** 1 : Execute clock tuning
Offset + (5-4)	RW	**Driver Strength Select** 00 : Driver type B (default) 01 : Driver type A 01 : Driver type C 01 : Driver type D
Offset + 3	RW	**1.8V Signaling Enable**
Offset + (2-0)	RW	**UHS Mode Select** 000 : SDR12 001 : SDR25 010 : SDR50 011 : SDR104

5.25 Auto CMD error status Register

Location	Attributes	Function
Offset + (15-08)	RSVD	Reserved
Offset + (07)	ROC	**Command not issued by Auto CMD** 1:Not issued, 0:No error
Offset + (06-05)	RSVD	Reserved
Offset + (04)	ROC	**Auto CMD index error** 1:Command index error, 0 : no error
Offset + (03)	ROC	**Auto CMD end bit error** 1:End bit error
Offset + (02)	ROC	**Auto CMD CRC error** 1:CRC error
Offset + (01)	ROC	**Auto CMD timeout error** This bit is set if no response is returned within 64 SDCLK cycles from the end bit of command.
Offset + (00)	ROC	**Auto CMD not executed** If multiple block transfer is not executing, we don't need auto CMD so this bit is set to 1

5.26 Capabilities Register (Offset 040h)

Location	Attributes	Register Field Explanation
Offset + (63-48)	Rsvd	**Reserved**
Offset +(47-46)	HwInit	**Re-Tuning Modes**
Offset + 45	HwInit	Use Tuning for SDR50
Offset + (44-35)	Rsvd	Reserved
Offset + 34	Hwinit	DDR50 Support
Offset + 33	HwInit	SDR104 Support
Offset + 32	HwInit	SDR50 Support
Offset + (31-27)	Rsvd	Reserved
Offset + 26	RO	Voltage Support 1.8V
Offset + 25	RO	Voltage Support 3.0V
Offset + 24	RO	Voltage Support 3.3V
Offset + 23	RO	Suspend/Resume Support
Offset + 22	RO	SDMA Support
Offset + 21	RO	High Speed Support
Offset + 20	Rsvd.	Reserved
Offset + 19	RO	ADMA2 Support
Offset + 18	Rsvd.	Reserved
Offset + (17-16)	RO	Max Block Length
Offset + (15-14)	Rsvd	Reserved
Offset + (13-8)	RO	Base Clock Frequency for SD clock
Offset + 7	RO	Timeout Clock Unit
Offset + 6	Rsvd	Reserved
Offset + (5-0)	RO	Timeout Clock Frequency

5.27 Host Controller Version Register (Offset 0FEh)

Location	Attributes	Register Field Explanation
Offset + (15-08)	HwInit	**Vendor Verfication Number** This status is reserved for Vendor Verification Number. The Host Driver should not use this status.
Offset + (07-00)	HwInit	**Specification Version Number** This status indicates the Host Controller Specification Number.The upper and lower 4-bits indicate the version. 00h- SD Host Specification V1.0 01h- SD Host Specification V2.0 02h- SD Host Specification V3.0 others- Reserved

6 SD Card Host Controller Commands

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	x	x	x	'1'
Description	Start bit	Transmission bit	Command index	Argument	CRC7	End bit

Figure 9: Command Format

CMD INDEX	ARGUMENT	ABBREVIATION	Command Description
CMD0	[31:0] stuff bits	GO_IDLE_STATE	Reset all cards to idle state
CMD2	[31:0] stuff bits	ALL_SEND_CID	Ask any card to send the CID numbers on the CMD line
CMD3	[31:0] stuff bits	SEND_RELATIVE_ ADDR	Ask the card to publish a new relative address(RCA)
CMD4	[31:16] DSR [15:0] stuff bits	SET_DSR	Programs the DSR of all cards
CMD7	[31:16] RCA [15:0] stuff bits	SELECT/DESELEC T_CARD	Command toggles a card between the stand-by and transfer states or between the programming and disconnect states.
CMD8	[31:12]reserved [11:8]supply voltage [7:0]check pattern	SEND_IF_COND	Send SD Memory Card Interface condition, which includes host supply voltage information and ask the card whether the card supports voltage.
CMD9	[31:16] RCA [15:0] stuff bits	SEND_CSD	Addressed card send its card specific data (CSD) on the CMD line
CMD10	[31:16] RCA [15:0] stuff bits	SEND_CID	Addressed card its card identification (CID) on the CMD line
CMD11	[31:0] reserved bits(all 0)	VOLTAGE_SWITCH	Switch to 1.8V bus signaling level
CMD12	[31:0] stuff bits	STOP_TRANSMISS	Forces the card to stop transmission

		ION	
CMD13	[31:16]RCA [15] Send Task Status Register [14:0] stuff bits	SEND_STATUS/SEND_TASK_STATUS	CQ not enabled: [15] = '0' or '1'. Addressed card sends its status register. CQ enabled: [15] = '0'. Addressed card sends its status register. [15] = '1', Addressed card sends task status register.
CMD15	[31:16] RCA [15:0] reserved bits	GO_INACTIVE_STATE	Sends an addressed card into the inactive state. This commands is used when the host explicitly wants to deactivate a card. Reserved bits shall be set to '0'.
CMD18	[31:0] data address	READ_MULTIPLE_BLOCK	Continuously transfer data blocks from card to host until interrupted by a STOP_TRANSMISSION command.
CMD19	[31:0] reserved bits (all set 0)	SEND_TUNING_BLOCK	64 bytes tuning pattern is sent for SDR50 and SDR104
CMD20	[31:28] Speed Class Control [27:0] See command description	SPEED_CLASS_CONTROL	Speed class control command. [27:0] Speed Class

CMD23	[31:0]Block Count	SET_BLOCK_COUNT	Specified block count for CMD18 and CMD25
CMD25	[31:0] data address	WRITE_MULTIPLE	Continuously writes blocks of data transmission until a STOP_TRANSMISSION follows
CMD27	[31:0] stuff bits	PROGRAM_CSD	Programming of the programmable bits of the CSD.
CMD32	[31:0] data	ERASE_WR_BLK_	Sets the address of the first write block to be

	address	START	erased.
CMD33	[31:0] data address	ERASE_WR_BLK_END	Sets the address of the last write block of the continuous range to be erased
CMD38	[31:0] Erase Function	ERASE	Erase function 00000001h = Discard 00000002h = FULE others= Erase
CMD42	[31:0] Reserved bits (set all 0)	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the card. The size of the data block is set by SET_BLOCK_LENGTH command. Reserved bits in the argument and in Lock card data Structure shall be set to 0.
CMD55	[31:16] RCA [15:0] stuff bits	APP_CMD	Indicates to the card that the next command is application specific command than a standard command
CMD56	[31:1] stuff bits [0] : RD/WR	GEN_CMD	Used either a data block to the card or to get data block from the card general purpose/application specific commands. The host sets RD/WR=1 for reading data and sets to 0 for writing data to the card.
ACMD6	[31:2] stuff bits [1:0] bus width	SET_BUS_WIDTH	Defines the data bus width('00' = 1 bit or '01'=4 bit bus) to be used for the data transfer. The allowed data bus widths are given in the SCR register.
ACMD13	[31:0] stuff bits	SD_STATUS	Send the SD Status.
ACMD22	[31:0] stuff bits	SEND_NUM_RE_BLOCKS	Send the number of the written write block. Responds with 32bits+CRC data block. If WRITE_BL_PARTIAL ='0', the unit of ACMD22 is a block length which was used when the write command was executed
ACMD23	[31:23]stuff bits [22:0] Number of blocks	SET_WR_BLK_ERASE_COUNT	Set the number of write blocks to be pre-erased before writing (to be used for faster Multiple Block WR command)
ACMD41	[31:1] stuff bits [0] set_cd	SET_CLR_CARD_DETECT	Connect[1]/disconnect[0] the 50 kOHM pull up resistor on CD?DAT3(pin 1) of the card

ACMD51	[31:0] stuff bits	SEND_SCR	Reads the SD Configuration Register(SCR)

7 Responses

There are five responses defined for SD memory card

7.1 R1

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	x	x	x	'1'
Description	start bit	transmission bit	command index	card status	CRC7	end bit

Figure 10: R1

7.2 R1b

R1b is identical to R1 with an optional busy signal transmitted at the data line. The card may become busy after receiving this command based on its state prior to command reception.

7.3 R2

Bit position	135	134	[133:128]	[127:1]	0
Width (bits)	1	1	6	127	1
Value	'0'	'0'	'111111'	x	'1'
Description	start bit	transmission bit	reserved	CID or CSD register incl. internal CRC7	end bit

Figure 11: R2

7.4 R3

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'111111'	x	'1111111'	'1'
Description	start bit	transmission bit	reserved	OCR register	reserved	end bit

Figure 12: R3

7.5 R6

Bit position	47	46	[45:40]	[39:8] Argument field		[7:1]	0
Width (bits)	1	1	6	16	16	7	1
Value	'0'	'0'	x	x	x	x	'1'
Description	start bit	transmission bit	command index ('000011')	New published RCA [31:16] of the card	[15:0] card status bits: 23,22,19,12:0 (see Table 4-42)	CRC7	end bit

Figure 13: R6

7.6 R7(card interface condition)

Bit position	47	46	[45:40]	[39:22]	21	20	[19:16]	[15:8]	[7:1]	0
Width (bits)	1	1	6	18	1	1	4	8	7	1
Value	'0'	'0'	'001000'	'00000h'	x	x	x	x	x	'1'
Description	Start bit	Transmission bit	Command index	Reserved bits	PCIe 1.2V Support 1)	PCIe Response 2)	Voltage accepted	Echo-back of check pattern	CRC 7	End bit

Figure 14: R7

8 Functional Description

CARD STATE	OPERATION MODES
Inactive State	Inactive Mode
Idle State	Card Identification Modes
Ready State	
Identification State	
Standby State	Data Transfer Modes
Transfer State	
Sending-data State	
Receiving-data State	
Programming State	
Disconnect State	

CATEGORISE THE COMMANDS DEPENDING ON THE STATES, DRAW STATE DIAGRAMS AND STRICTLY FOLLOW UHS-1 MODE CONFIGURATION FOR THIS DESCRIPTION.

8.1 Card Identification Modes

Operations performed in this mode are:

- Resets Card.
- Validates operation voltage range.
- Identifies type of card.
- Publish Relative Card Address(RCA) of the card.

8.1.1 Card Reset

The command CMD0(GO_IDLE_STATE) is the software reset command and sets the card into Idle State regardless of the current card state.Cards in Iactive State are not affected by this command.

After CMD0, all cards CMD lines are in input mode, waiting for start-bit of the next command.The cards are initialised by a default RCA(0x0000h) and with a default driver strength with 400Khz clock frequency.For 1.8V signalling, default driver strength is specified by type B driver.

8.1.2 Operating Voltage Validation

Once the reset command(CMD0) has been issued by the host with a specified voltage assuming it is supported by the card, the voltage is verified by the CMD8(SEND_IF_COND) command.The card checks the validity of operating condition by analysing the arguments of CMD8 and host checks by analysing the response of CMD8.

If the card can operate on the supply voltage, the response echoes back the supplied voltage and CRC pattern.If the card cannot operate on the supplied voltage, it returns no response and stays in IDLE STATE.

Post CMD8, ACMD41(SD_SEND_OP_CMD) is used to initialise SDHC or SDXC cards. ACMD41 is designed to provide SD Host with a mechanism to identify and reject cards which do not match the required VDD range. Cards which cannot perform data transfer in the specified range discards themselves from further bus operations and goes into Inactive State. As ACMD41 is an application specific command it should be preceded by CMD55(APP_CMD). RCA to be used for the command is the default RCA(0x0000).

8.1.3 Card Initialisation and Identification Process

After ACMD41 activates the bus the host starts initialisation and identification.The initialisation process starts with ACMD41 by setting its operational conditions and HCS(Host Capacity Support) bit. A '1' indicates host supporting SDHC or SDXC cards, '0' indicating support of none. If HCS is set to '0', the cards never return a ready status(keep busy bit to 0).The busy bit in OCR is used by the card to inform the host whether initialisation of ACMD41 is completed.Setting busy bits to '1' indicates completion of initialisation.The host repeatedly issues ACMD41 for atleast 1 second or until the busy bit is set to '1'. The card checks the operational conditions and the HCS bit in the OCR only at the first ACMD41.Whlle repeating ACMD41, the host shall not issue another command except CMD0.

If the card responds to CMD8, the response of ACMD41 includes the CCS(Card Capacity Status) information. CCS is valid when card returns ready(busy bit set to 1).CCS=0 means the card is SDSC.

The host then issues CMD2(SEND_CID) to the card to get its unique CID number.card that is unidentified(i.e. which is in Ready State) sends its CID number as the response(on the CMD line).After CID is sent by the card it goes into Identification State.Thereafter, the host issues CMD3(SEND_REL_ADDR) which asks the card to publish a new relative card address, which is shorter than CID and is used to address the card in future data transfer mode.Once RCA is received, the card changes to a Stand-by State. At this point, if the host wants

to assign another RCA number, it can ask the card to publish a new number by sending another CMD3 command to the card. The last published RCA is the actual number of the card

8.2 Data Transfer Mode

In data transfer mode the host issues SEND_CSD (CMD9) to obtain the Card Specific Data (CSD register), e.g. block length, card storage capacity, etc. CMD7 is used to select the card and put it into the *Transfer State*.The card de-selection is done if the card gets CMD7 with un-matched RCA.

All data communication in the Data Transfer Mode is point-to point between the host and the selected card (using addressed commands). All addressed commands get acknowledged by a response on the CMD line.

The relationship between the various data transfer modes is summarized below.

- All data read commands can be aborted any time by the stop command (CMD12). The data transfer will terminate and the card will return to the *Transfer State*. The read commands are: block read (CMD17), multiple block read (CMD18), and general command in read mode (CMD56).
- All data write commands can be aborted any time by the stop command (CMD12). The write commands shall be stopped prior to deselecting the card by CMD7. The write commands are: block write (CMD24 and CMD25), program CSD (CMD27), and general command in write mode (CMD56).
- As soon as the data transfer is completed, the card will exit the data write state and move either to the *Programming State* (transfer is successful) or *Transfer State* (transfer failed).
- If a block write operation is stopped and the block length and CRC of the last block are valid, the data will be programmed.
- The card may provide buffering for block write. This means that the next block can be sent to the card while the previous is being programmed. If all write buffers are full, and as long as the card is in *Programming State*, the DAT0 line will be kept low (BUSY).
- There is no buffering option for writing to CSD and erase.
- Parameter set commands are not allowed while card is in *programming state*. Parameter set commands are: set block length (CMD16), erase block start (CMD32) and erase block end (CMD33).
- Read commands are not allowed while card is in *programming state*.
- A card can be reselected while in the *Disconnect State*, using CMD7. In this case the card will move to the *Programming State* and reactivate the busy indication.

8.2.1 Wide Bus Selection/Deselection

Wide Bus (4 bit bus width) operation mode may be selected/deselected using ACMD6. The default bus width after power up or GO_IDLE (CMD0) is 1 bit bus width.

8.2.2 Data Read

The DAT bus line level is high by the pull-up when no data is transmitted. A transmitted data block consists of start bits (1 or 4 bits LOW), followed by a continuous data stream. The data stream contains the payload data (and error correction bits). The data stream ends with end bits (1 or 4 bits HIGH). The data transmission is synchronous to the clock signal.

Read command is rejected if BLOCK_LEN_ERROR or ADDRESS_ERROR occurred and no data transfer is performed.

- **Block Read**
  - The basic unit of data transfer is a block whose maximum size is always **512 bytes**.Smaller blocks whose starting and ending address are entirely contained within 512 bytes boundary may be transmitted in SDSC only, it is not allowed in SDHC and SDXC.
  - Block Length set by CMD16 can be set up to 512 bytes.
  - A CRC is appended to the end of each block ensuring data transfer integrity.
  - CMD17 (READ_SINGLE_BLOCK) initiates a block read and after completing the transfer, the card returns to the *Transfer State*.
  - CMD18 (READ_MULTIPLE_BLOCK) starts a transfer of several consecutive blocks. Blocks will be continuously transferred until a STOP_TRAN SMISSION command (CMD12) is issued. The stop command has an execution delay due to the serial command transmission. The data transfer stops after the end bit of the stop command.
  - When the last block of user area is read using CMD18, the host should ignore OUT_OF_RANGE error that may occur even the sequence is correct.

8.2.3 Data Write

For block oriented write data transfer, the CRC check bits are added to each data block. The card performs 1 or 4 bits CRC parity check for each received data block prior to the write operation. By this mechanism, writing of erroneously transferred data can be prevented.

Write command is rejected if BLOCK_LEN_ERROR or ADDRESS_ERROR occurred and no data transfer is performed.

- **Block Write**
  - During block write (CMD24 - 27, 42, 56 (w)) one or more blocks of data are transferred from the host to the card with 1 or 4 bits CRC appended to the end of each block by the host.

- A card supporting block write shall be required that Block Length set by CMD16 shall be 512 bytes.
- If WRITE_BL_PARTIAL is allowed (=1) then smaller blocks, up to resolution of one byte, can be used as well.
- If the CRC fails, the card shall indicate the failure on the DAT line, the transferred data will be discarded and not be written, and all further transmitted blocks (in multiple block write mode) will be ignored.
- Multiple block write command shall be used rather than continuous single write command to make faster write operation.
- Programming of the CSD register does not require a previous block length setting.
- After receiving a block of data and completing the CRC check, the card will begin writing and hold the DAT0 line low if its write buffer is full and unable to accept new data from a new WRITE_BLOCK command.
- The host may poll the status of the card with a SEND_STATUS command (CMD13) at any time, and the card will respond with its status. The status bit READY_FOR_DATA indicates whether the card can accept new data or whether the write process is still in progress.
- The host may deselect the card by issuing CMD7 (to select a different card) which will displace the card into the Disconnect State and release the DAT line without interrupting the write operation.

- **Pre-erased Setting prior to a Multiple Block Write Operation**
  Setting a number of write blocks to be pre-erased (ACMD23) will make a following Multiple Block Write operation faster compared to the same operation without preceding ACMD23. The host will use this command to define how many number of write blocks are going to be send in the next write operation. It is recommended using this command preceding CMD25, some of the cards will be faster for Multiple Write Blocks operation.

8.2.4 Erase

It is desirable to erase many write blocks simultaneously in order to enhance the data throughput. Identification of these write blocks is accomplished with the ERASE_WR_BLK_START (CMD32), ERASE_WR_BLK_END (CMD33) commands.
The host should adhere to the following command sequence: ERASE_WR_BLK _START, ERASE_WR_BLK_END and ERASE (CMD38).
If an erase (CMD38) or address setting (CMD32, 33) command is received out of sequence, the card shall set the ERASE_SEQ_ERROR bit in the status register and reset the whole sequence.
As described above for block write, the card will indicate that an erase is in progress by holding DAT0 low.

9 Verification and Validation

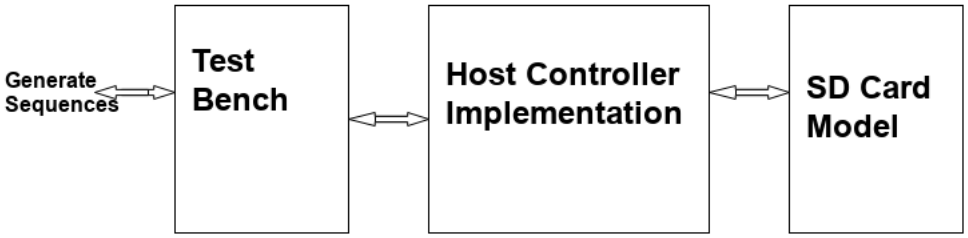

Figure 15: Verification Plan

9.1 Front end Verification

- Implement a behavioural model of the SD card(In VHDL).
- Host Controller to be implemented compliant to version 3.0.
- Communicate with the SD card model using the controller by generating sequence of commands using testbenches. The sequnce of commands is available in **Functional Description**.

9.2 Validation

This process will be implementedhttps://www.overleaf.com/project/5f1e6159e3ce7b000187974d on a FPGA platform.

- Load the binary file of the implemented host controller on the FPGA card.
- Connect the desired SD card to the board for verification.
- Via SDK, generate commands in the controller to perform the required operations.

10 Performance Goals

With this controller, the SD card is expected to operate at a maximum speed of **104MBps** for SDXC cards(Capacity:32GB-2TB), **50MBps** for cards other than SDXC (Capacity ¡ 32GB), and a minimum speed of **12.5MBps** (applicable to all cards).